4:1, DIFFERENTIAL-TO-3.3V OR 2.5V LVPECL/ECL CLOCK MULTIPLEXER

ICS853054

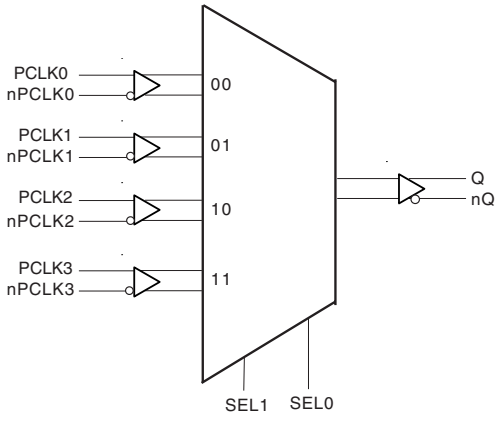
General Description

The ICS853054 is an 4:1 Differential-to-3.3V or 2.5V LVPECL/ECL Clock Multiplexer which can operate up to 2.5GHz and is a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS853054 has 4 selectable differential clock inputs. The PCLKx, nPCLKx input pairs can accept LVPECL, LVDS, CML or SSTL levels. The fully differential architecture and low propagation delay make it ideal for use in clock distribution circuits. The select pins have internal pulldown resistors. The SEL1 pin is the most significant bit and the binary number applied to the select pins will select the same numbered data input (i.e., 00 selects PCLK0, nPCLK0).

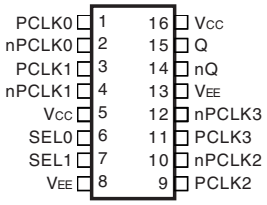
Features

- High speed 4:1 differential multiplexer
- One differential 3.3V or 2.5V LVPECL output
- Four selectable differential PCLK, nPCLK inputs
- PCLKx, nPCLKx pairs can accept the following differential input levels: LVPECL, LVDS, CML, SSTL
- Maximum output frequency: 3.2GHz
- Translates any single ended input signal to LVPECL levels with resistor bias on nPCLKx input
- Part-to-part skew: TBD
- Propagation delay: 465ps (typical)
- Additive phase jitter, RMS: 0.238ps (typical)
- LVPECL mode operating voltage supply range: V_{CC} = 2.375V to 3.465V, V_{EE} = 0V
- ECL mode operating voltage supply range: V_{CC} = 0V, V_{EE} = -3.465V to -2.375V
- -40°C to 85°C ambient operating temperature
- Available in both standard and lead-free RoHS-compliant packages

Block Diagram



Pin Assignment



ICS853054
16-Lead TSSOP
4.4mm x 5.0mm x 0.92mm package body
G Package
Top View

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	PCLK0	Input	Pulldown	Non-inverting differential LVPECL clock input.
2	nPCLK0	Input	Pullup/Pulldown	Inverting differential LVPECL clock input. $V_{CC}/2$ default when left floating.
3	PCLK1	Input	Pulldown	Non-inverting differential LVPECL clock input.
4	nPCLK1	Input	Pullup/Pulldown	Inverting differential LVPECL clock input. $V_{CC}/2$ default when left floating.
5, 16	V_{CC}	Power		Positive supply pins.
6, 7	SEL0, SEL1	Input	Pulldown	Clock select input pins. LVCMOS/LVTTL interface levels.
8, 13	V_{EE}	Power		Negative supply pin.
9	PCLK2	Input	Pulldown	Non-inverting differential LVPECL clock input.
10	nPCLK2	Input	Pullup/Pulldown	Inverting differential LVPECL clock input. $V_{CC}/2$ default when left floating.
11	PCLK3	Input	Pulldown	Non-inverting differential LVPECL clock input.
12	nPCLK3	Input	Pullup/Pulldown	Inverting differential LVPECL clock input. $V_{CC}/2$ default when left floating.
14, 15	nQ, Q	Output		Differential output pair. LVPECL interface levels.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$R_{PULLDOWN}$	Input Pulldown Resistor			75		kΩ
$R_{VDD/2}$	Pullup/Pulldown Resistosr			50		kΩ

TABLE 3. CLOCK INPUT FUNCTION TABLE

Inputs		Outputs
SEL1	SEL0	Q/nQ
0	0	PCLK0/nPCLK0
0	1	PCLK1/nPCLK1
1	0	PCLK2/nPCLK2
1	1	PCLK3/nPCLK3

Absolute Maximum Ratings

Supply Voltage, V_{CC}	4.6V (LVPECL mode, V_{EE} = 0)
Negative Supply Voltage, V_{EE}	-4.6V (ECL mode, V_{CC} = 0)
Inputs, V_I (LVPECL mode)	-0.5V to V_{CC} + 0.5V
Inputs, V_I (ECL mode)	0.5V to V_{EE} - 0.5V
Outputs, I_O	
Continuous Current	50mA
Surge Current	100mA
Operating Temperature Range, TA	-40°C to +85°C
Storage Temperature, T_{STG}	-65°C to 150°C
Package Thermal Impedance, θ_{JA} (Junction-to-Ambient)	89°C/W (0 lfpm)

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, V_{CC} = 2.375 to 3.465V; V_{EE} = 0V

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Positive Supply Voltage		2.375	3.3	3.465	V
I_{CC}	Power Supply Current			61		mA

Table 4B. LVCMOS/LVTTL DC Characteristics, V_{CC} = 2.375 to 3.465V; V_{EE} = 0V

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{CC} = 3.3V	2		V_{CC} + 0.3	V
			V_{CC} = 2.5V	1.7		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage		V_{CC} = 3.3V	-0.3		0.8	V
			V_{CC} = 2.5V	-0.3		0.7	V
I_{IH}	Input High Current	SEL0, SEL1	$V_{CC} = V_{IN}$ = 3.465V, $V_{CC} = V_{IN}$ = 2.625V			150	µA
I_{IL}	Input Low Current	SEL0, SEL1	V_{CC} = 3.465V, V_{IN} = 0V, V_{CC} = 2.625V, V_{IN} = 0V	-150			µA

Table 4C. LVPECL DC Characteristics, V_{CC} = 2.375 to 3.465V; V_{EE} = 0V

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	PCLK0:PCLK3 nPCLK0:nPCLK3	$V_{CC} = V_{IN}$ = 3.465V			150	µA
I_{IL}	Input Low Current	PCLK0:PCLK3	V_{CC} = 3.465V, V_{IN} = 0V	-10			µA
		nPCLK0:nPCLK3	V_{CC} = 3.465V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Input Voltage			0.15			V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			1.2		3.3	V
V_{OH}	Output High Voltage Voltage; NOTE 3				V_{CC} - 1.005		V
V_{OL}	Output Low Voltage; NOTE 3				V_{CC} - 1.78		V
V_{SWING}	Peak-to-Peak Output Voltage Swing				0.8		V

NOTE 1: Common mode voltage is defined as V_{IH}.
NOTE 2: For single ended applications, the maximum input voltage for PCLKx, nPCLKx is V_{CC} + 0.3V.
NOTE 3: Outputs terminated with 50Ω to V_{CC} - 2V.

TABLE 4D. ECL DC CHARACTERISTICS, V_{CC} = 0V; V_{EE} = -3.465V TO -2.375V

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1				-1.005		V
V_{OL}	Output Low Voltage; NOTE 1				-1.78		V
V_{IH}	Input High Voltage			-1.225		-0.94	V
V_{IL}	Input Low Voltage			-1.87		-1.535	V
V_{PP}	Peak-to-Peak Input Voltage				800		mV
V_{CMR}	Input High Voltage Common Mode Range; NOTE 2, 3			V_{EE} + 1.2		0	V
I_{IH}	Input High Current	PCLK0:PCLK3 nPCLK0:nPCLK3				150	µA
I_{IL}	Input Low Current	PCLK0:PCLK3		-10			µA
		nPCLK0:nPCLK3		-150			µA

NOTE 1: Outputs terminated with 50Ω to V_{CC} - 2V.
NOTE 2: Common mode voltage is defined as V_{IH}.
NOTE 3: For single-ended applications, the maximum input voltage for PCLKx, nPCLKx is V_{CC} + 0.3V.

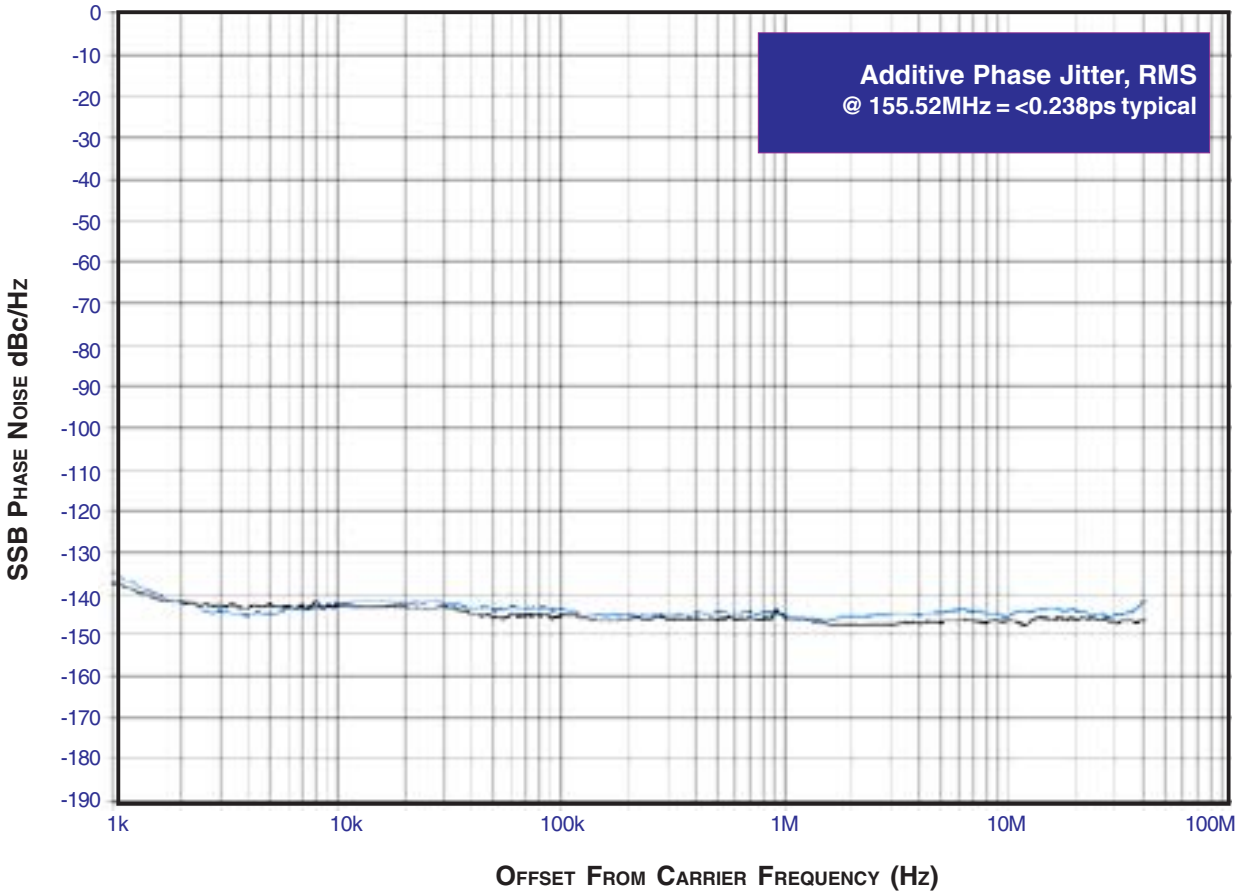
TABLE 5. AC CHARACTERISTICS, V_{CC} = 0V; V_{EE} = -3.465V TO -2.375V OR V_{CC} = 2.375 TO 3.465V; V_{EE} = 0V

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				3.2	GHz
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	155.52MHz, 12kHz - 20MHz		0.238		ps
t_{PD}	Propagation Delay; NOTE 1			465		ps
*t*sk(pp)	Part-to-Part Skew; NOTE 2, 3			TBD		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		200		ps
$MUX_{ISOLATION}$	MUX Isolation	V_{IN} 1.6V to 2.4V, 155.52MHz		-55		dB

All parameters measured up to 1.3GHz unless noted otherwise.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 3: This parameter is defined according with JEDEC Standard 65.

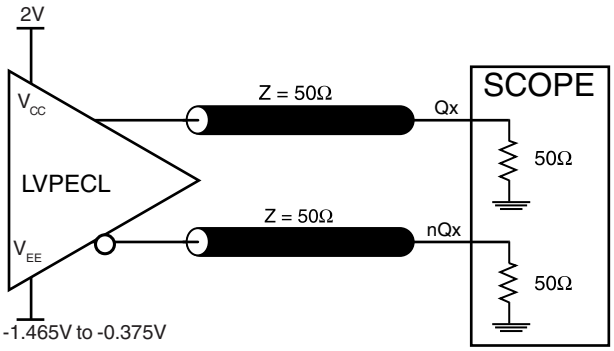
Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

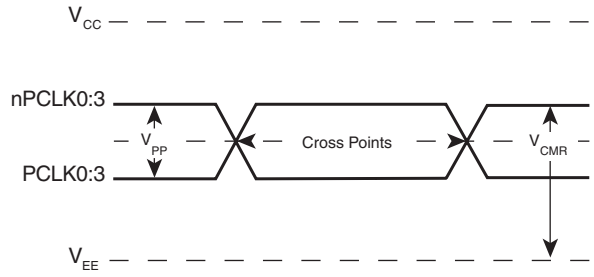


As with most timing specifications, phase noise measurements have issues. The primary issue relates to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependant on the input source and measurement equipment.

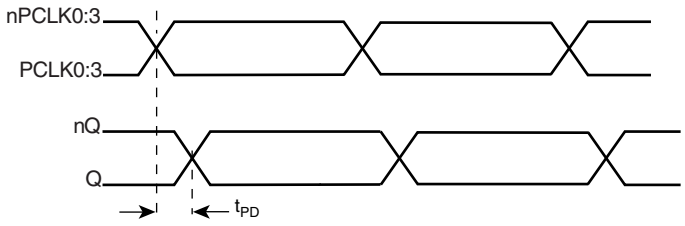
PARAMETER MEASUREMENT INFORMATION



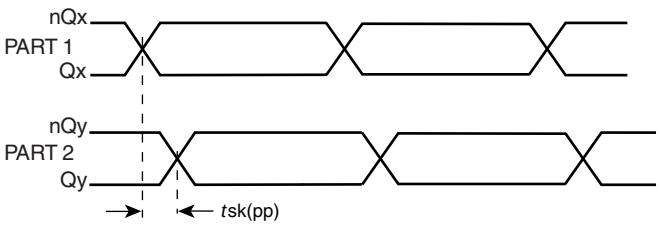
OUTPUT LOAD AC TEST CIRCUIT



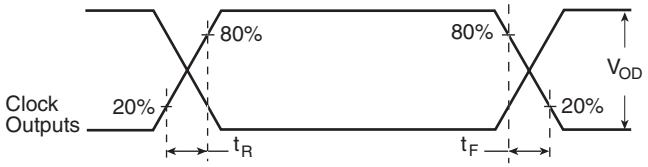
DIFFERENTIAL INPUT LEVEL



PROPAGATION DELAY



PART-TO-PART SKEW



OUTPUT RISE/FALL TIME

APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{CC}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{CC}= 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

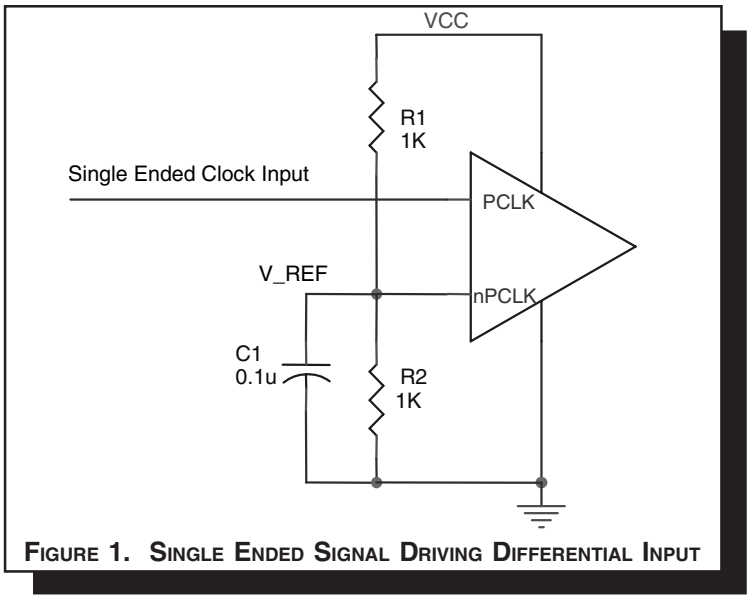


FIGURE 1. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

RECOMMENDATIONS FOR UNUSED INPUT PINS

INPUTS:

PCLK/nPCLK INPUT:
For applications not requiring the use of a differential input, both the PCLK and nPCLK pins can be left floating. Though not required, but for additional protection, a 1kΩ resister can be tied from PCLK to ground.

SELECT PINS:
All select pins have internal pull-ups and pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resister can be used.

LVPECL Clock Input Interface

The PCLK /nPCLK accepts LVPECL, CML, SSTL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 2A to 2E* show interface examples for the HiPerClockS PCLK/nPCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

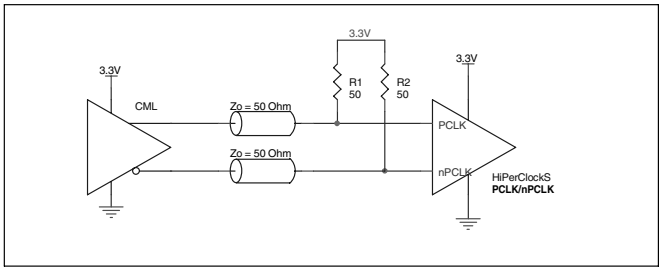


Figure 2A. HiPerClockS PCLK/nPCLK Input Driven by a CML Driver

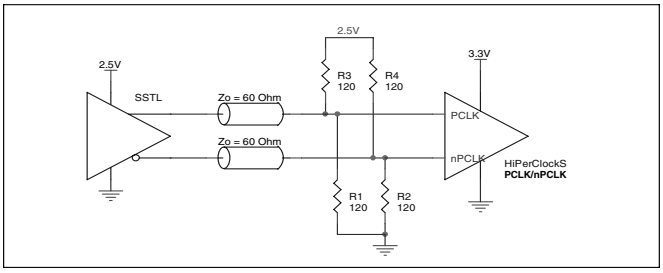


Figure 2B. HiPerClockS PCLK/nPCLK Input Driven by an SSTL in Driver

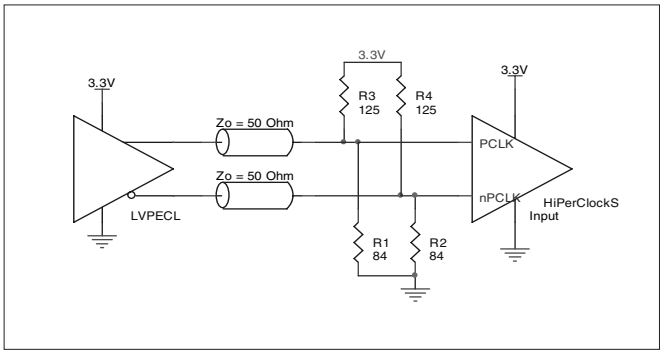


Figure 2C. HiPerClockS PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver

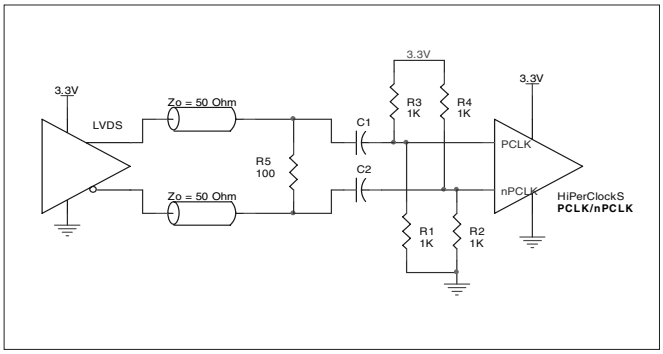


Figure 2D. HiPerClockS PCLK/nPCLK Input Driven by a 3.3V LVDS Driver

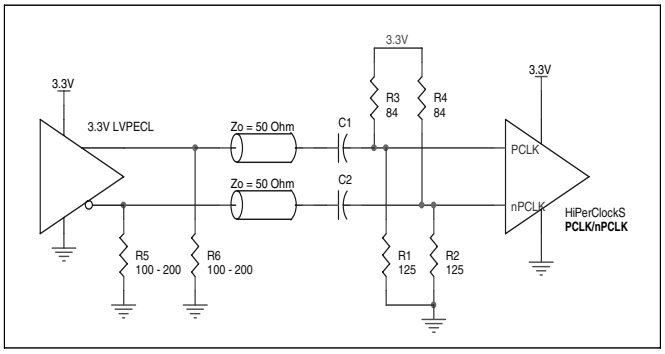


Figure 2E. HiPerClockS PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver with AC Couple

TERMINATION FOR 3.3V LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 3A and 3B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

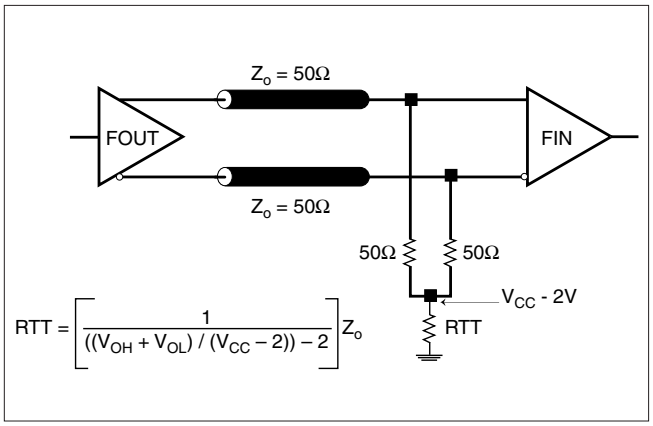


FIGURE 3A. LVPECL OUTPUT TERMINATION

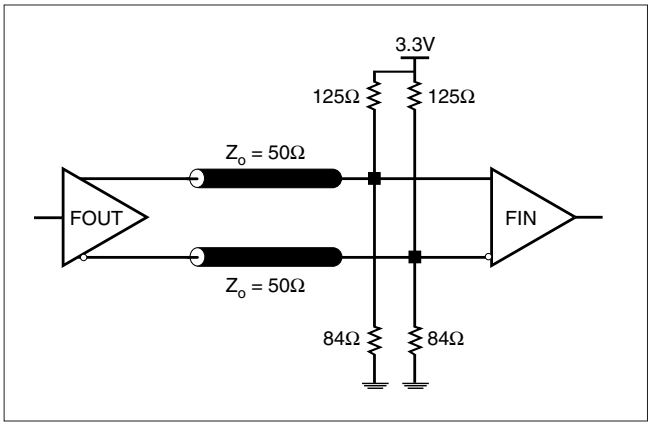


FIGURE 3B. LVPECL OUTPUT TERMINATION

TERMINATION FOR 2.5V LVPECL OUTPUT

Figure 4A and *Figure 4B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} - 2V. For V_{CC} = 2.5V, the V_{CC} - 2V is very close to ground level. The R3 in Figure 4B can be eliminated and the termination is shown in *Figure 4C.*

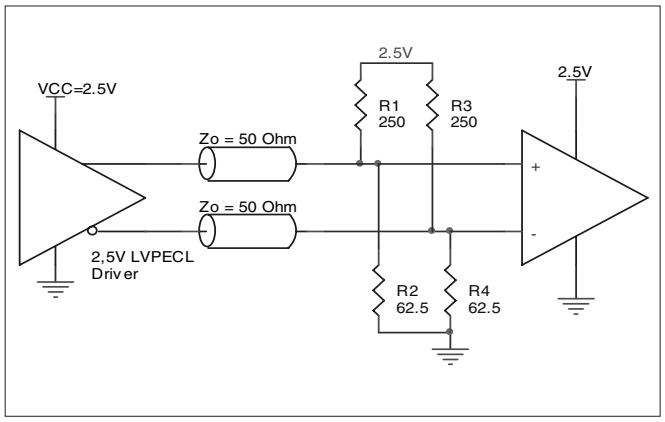


FIGURE 4A. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

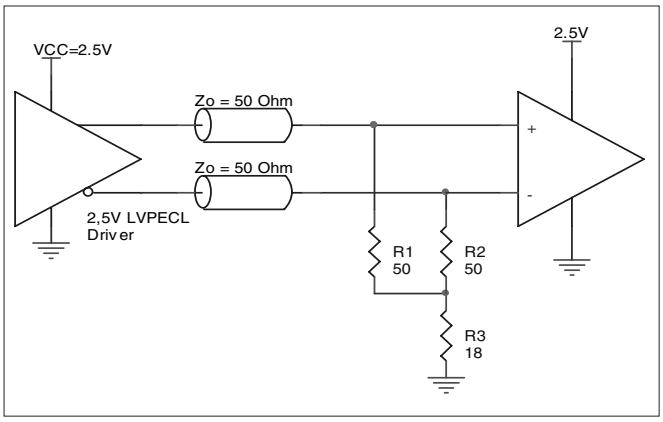


FIGURE 4B. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

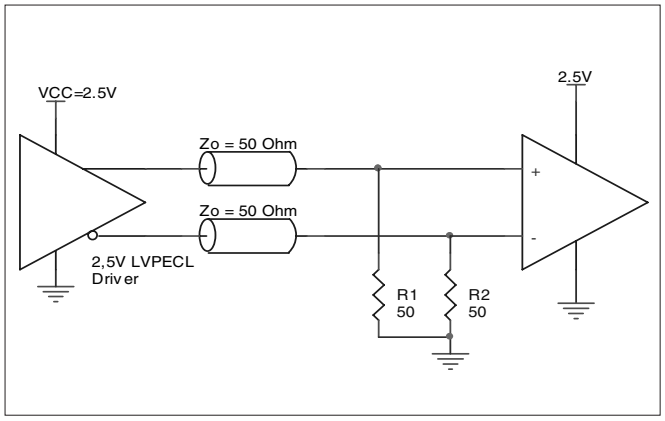


FIGURE 4C. 2.5V LVPECL TERMINATION EXAMPLE

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS853054.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the ICS853054 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.3V ± 5% = 3.465V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{CC_MAX} * I_{EE_MAX} = 3.465V * 61mA = **211.37mW**
- Power (outputs)$_{MAX}$ = **27.83mW/Loaded Output pair**

Total Power$_{_MAX}$ (3.465V, with all outputs switching) = 211.37mW + 27.83mW = **239.2mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 meters per second and a multi-layer board, the appropriate value is 81.8°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:
85°C + 0.239W * 81.8°C/W = 104.6°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 6. THERMAL RESISTANCE θ_{JA} FOR 16-PIN TSSOP FORCED CONVECTION

θ_{JA} by Velocity (Meters per Second)	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	137.1°C/W	118.2°C/W	106.8°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	89.0°C/W	81.8°C/W	78.1°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 5.*

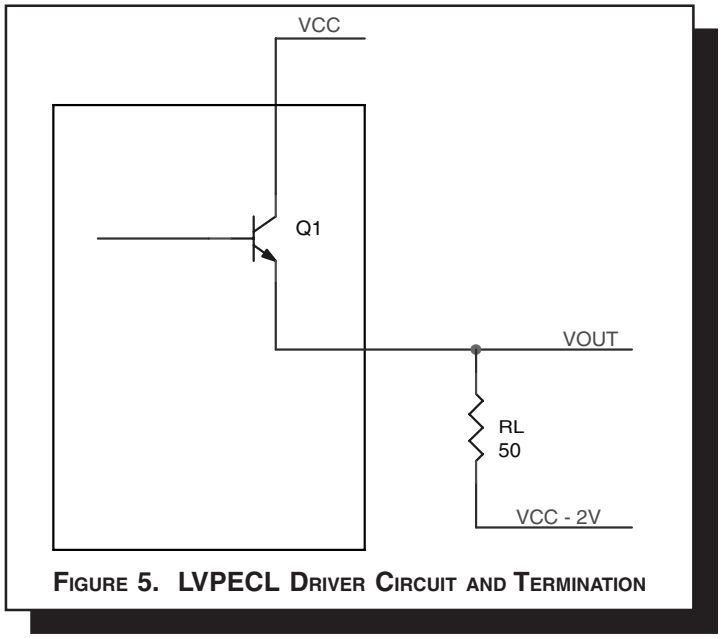


FIGURE 5. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CC} - 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CC\_MAX} - 1.005V}$

  $(V_{CC\_MAX} - V_{OH\_MAX}) = \mathbf{1.005}$

- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CC\_MAX} - 1.78V}$

  $(V_{CC\_MAX} - V_{OL\_MAX}) = \mathbf{1.78V}$

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) =$
$[(2V - 1.005V)/50Ω] * 1.005V =$ **20mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.78V)/50Ω] * 1.78V =$ **7.83mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **27.83mW**

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for 16 Lead TSSOP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	137.1°C/W	118.2°C/W	106.8°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	89.0°C/W	81.8°C/W	78.1°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

Transistor Count

The transistor count for ICS853054 is: 326

Package Outline - G Suffix for 16 Lead TSSOP

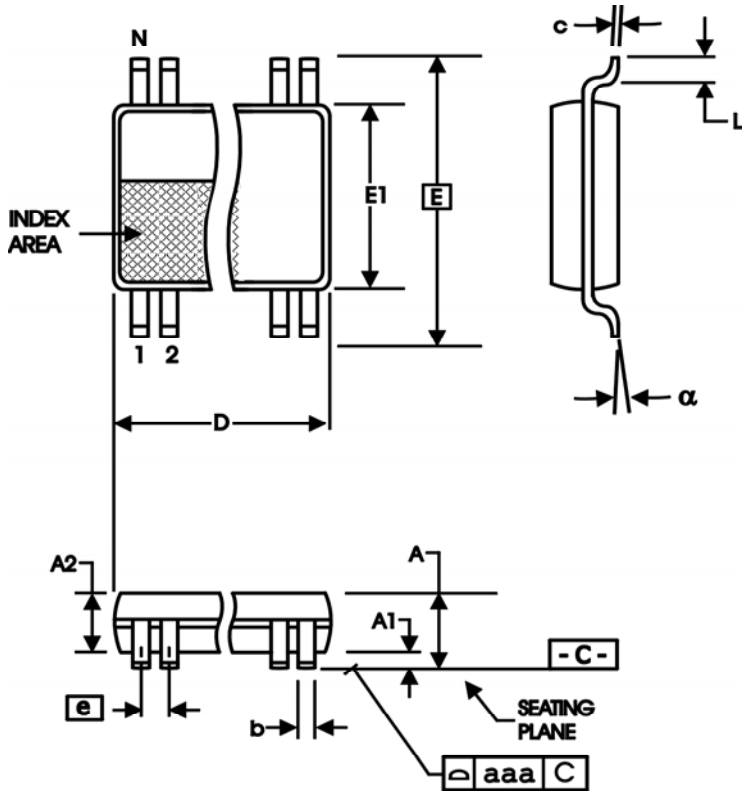


Table 8. Package Dimensions

SYMBOL	Millimeters	
	Minimum	Maximum
N	16	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS853054AG	853054AG	16 Lead TSSOP	tube	-40°C to 85°C
ICS853054AGT	853054AG	16 Lead TSSOP	2500 tape & reel	-40°C to 85°C
ICS853054AGLF	853054AL	16 Lead "Lead-Free" TSSOP	tube	-40°C to 85°C
ICS853054AGLFT	853054AL	16 Lead "Lead-Free" TSSOP	2500 tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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