DIFFERENTIAL-TO-LVCMOS FANOUT BUFFER W/ DIVIDER AND GLITCHLESS SWITCH

ICS870S208

General Description

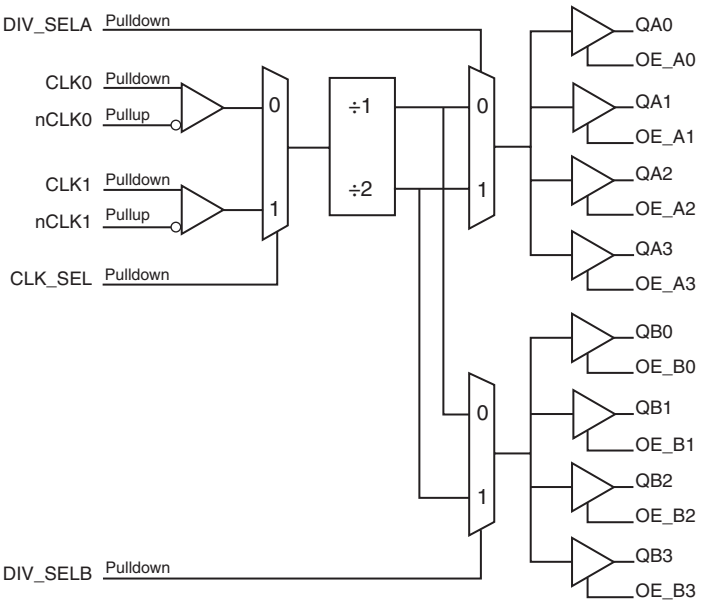
The ICS870S208 is a low skew, 8 output LVCMOS / LVTTL Fanout Buffer with selectable divider and a member of the HiPerClockS™ family of High Performance Clock Solutions from IDT. The ICS870S208 has 2 selectable inputs that accept a variety of differential input types. The device provides the capability to suppress any glitch at the outputs of the device during an input clock switch to enhance clock redundancy in fault tolerant applications. The low impedance LVCMOS outputs are designed to drive 50Ω series or parallel terminated transmission lines. The effective fanout can be increased from 8 to 16 by utilizing the ability of the outputs to drive two series terminated lines. The divide select inputs, DIV_SELA and DIV_SELB, control the output frequency of each bank. The output banks can be independently selected for ÷1 or ÷2 operation. The output enable pins assigned to each output, support enabling and disabling of each output individually.

The ICS870S208 is characterized at full 3.3V and 2.5V, and mixed 3.3V/2.5V output operating supply modes. Guaranteed output and part-to-part skew characteristics make the ICS870S208 ideal for high performance, single ended applications.

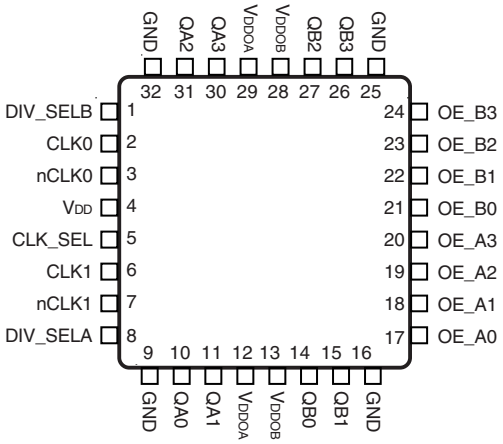
Features

- Eight LVCMOS/LVTTL outputs (2 banks of 4 outputs)
  Each output has individual synchronous output enable
- Two selectable differential CLKx/nCLKx clock inputs
- Dual differential input pairs can accept the following differential input levels: LVPECL, LVDS, LVHSTL, SSTL, HCSL
- Maximum output frequency: 250MHz
- Independent bank control for ÷1 or ÷2 operation
- Glitchless output behavior during input switch
- Output skew: 50ps (typical) @ 3.3V
- Bank skew: 30ps (typical) @ 3.3V
- Supply modes:
  Core/Output
  3.3V/3.3V
  2.5V/2.5V
  3.3V/2.5V
- 0°C to 70°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

Block Diagram



Pin Assignment



ICS870S208
32-Lead VFQFN
5mm x 5mm x 0.925mm
package body
K Package
Top View

The Preliminary Information presented herein represents a product in pre-production. The noted characteristics are based on initial product characterization and/or qualification. Integrated Device Technology, Incorporated (IDT) reserves the right to change any circuitry or specifications without notice.

FUNTIONAL DESCRIPTION

TWO VALID CLOCKS

The ICS87S0208 has a glitch free input mux that is controlled by the CLK_SEL pin. It is designed to switch between 2 input clocks whether running or not. In the case where both clocks are running, when CLK_SEL changes, the output clocks go low after one cycle of the output clock (nominally). The outputs then stay low for one cycle of the new input clock (nominally) and then begin to follow the new input clock. This is shown in *Figure 1A.*

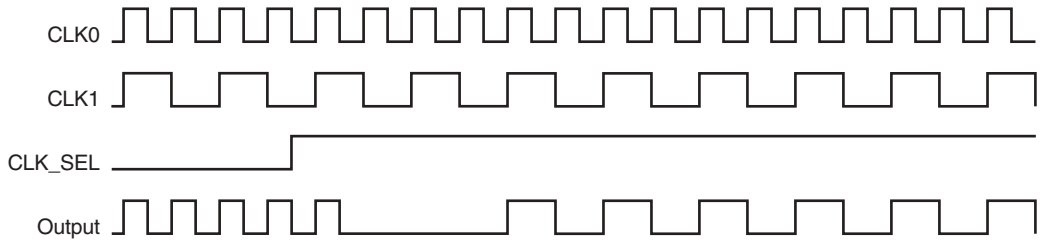


FIGURE 1A. CLK_SEL TIMING DIAGRAM

When DIV_SEL changes, the part waits for the output to complete the cycle of the selected divider then changes seamlessly to the new divider.

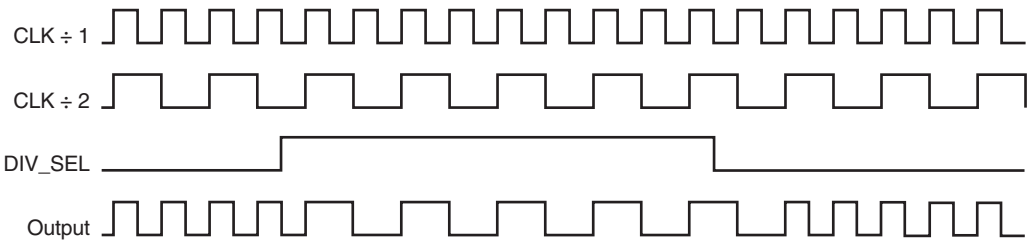


FIGURE 1B. DIV_SELx TIMING DIAGRAM

When an Output Enable pin is pulled low, the part waits for the output to complete its period, then transitions to a Hi-Z state. When Output Enable is asserted, the output transitions from the Hi-Z to a low state to ensure a clean rising edge of the first output clock.

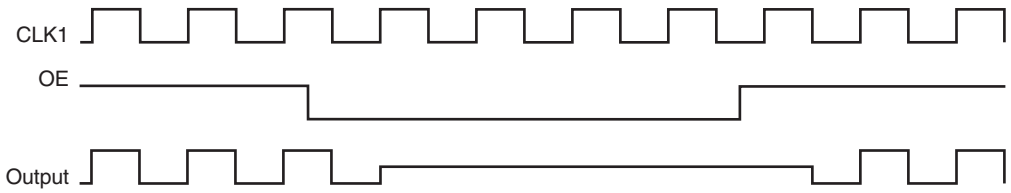


FIGURE 1C. OEx TIMING DIAGRAM

Bad Input Clock

An internal timer monitors the state of both input clocks. If a clock is stopped (stuck high or low for over approximately 200ns), its internal input bad flag is set and the part will perform as depicted in the following diagrams. If the clock is restored, the internal input bad detector waits for 4 full clock periods before clearing the input bad flag and returning to normal operation.

If the selected input clock goes bad (stuck high or low for over approximately 200ns), an internal input bad flag is set. When the input bad flag is set, the output goes low until the next valid clock event. If the selected clock is restored, the input bad detector waits 4 full clock periods before clearing the flag and returning to normal operation. If CLK_SEL is changed to select a valid input clock, the output will stay low for one full peiod of the new input clock, then return to normal operation.

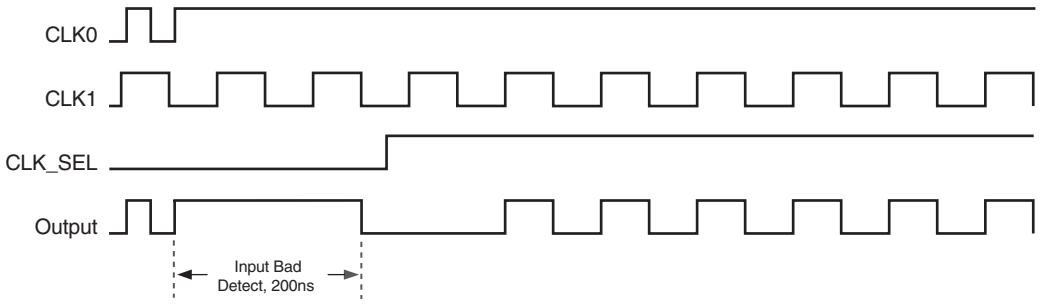


Figure 1D. CLK_SEL with Bad Input Timing Diagram

If the selected input clock goes bad (stuck high or low for over approximately 200ns), an internal input bad flag is set. When the input bad flag is set, the output goes low until the next valid clock event. If DIV_SEL is changed, the output will transition from the low state following the selected divide when a valid input clock is restored.

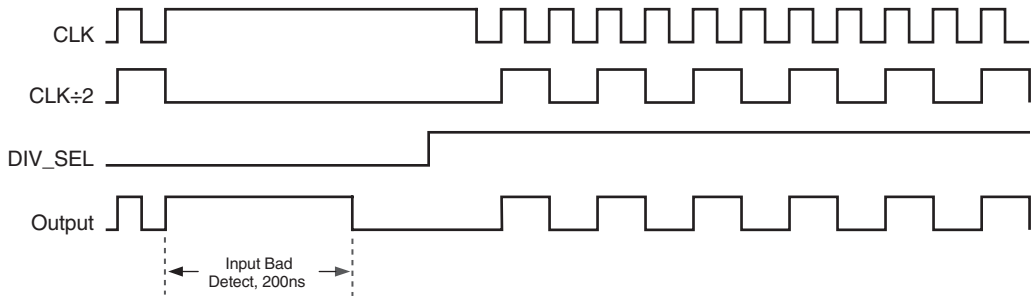


Figure 1E. DIV_SELx with Bad Input Timing Diagram

If the input bad flag has been set (The input has been stuck high or low for over approximately 200ns), and OEx is pulled low, the output will immediately go to a HighZ state. If the clock is restored while the OEx is low, the output will transition from the HighZ to a low state to ensure a clean rising edge of the first output clock when the Oex is pulled high again.

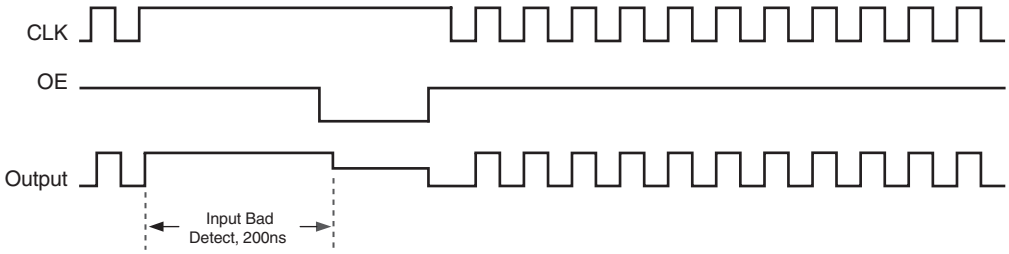


Figure 1F. OEx with Bad Input Timing Diagram

Switch During an Input Bad Detect

If a CLK_SEL, DIV_SEL, or OE event happens after a clock has stopped , but before the input bad flag has been set (during the ~200ns detect period) the SELECT change will not take effect until the internal bad flag has been set. The output will go low after the input bad flag is set and follow the second period of the new clock input. Although no glitches will occur, due to the unknown state of the failing clock, a transition may take up to 1us to execute.

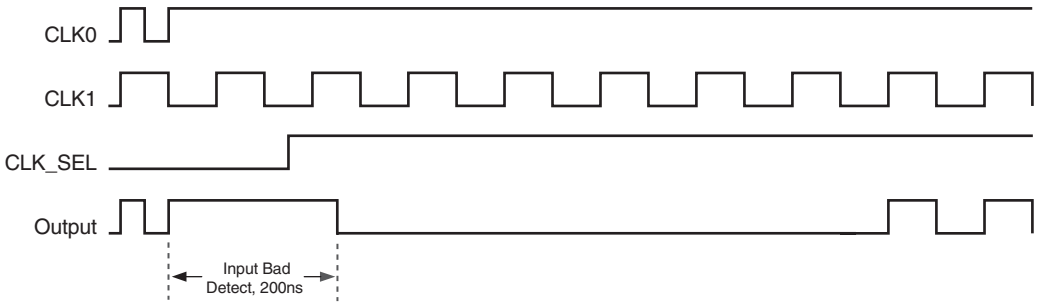


Figure 1G. CLK_SEL with Bad Input Timing Diagram

Table 1. Pin Descriptions

Number	Name	Type		Description
1	DIV_SELB	Input	Pulldown	Controls frequency division for Bank B outputs. LVCMOS / LVTTL interface levels.
2	CLK0	Input	Pulldown	Non-inverting differential clock input.
3	nCLK0	Input	Pullup	Inverting differential clock input. V_{DD}/2 default when left floating.
4	V_{DD}	Power		Positive supply pin.
5	CLK_SEL	Input	Pulldown	Clock select input. When HIGH, selects CLK1, nCLK1 inputs. When LOW, selects CLK0, nCLK0 inputs. LVCMOS / LVTTL interface levels.
6	CLK1	Input	Pulldown	Non-inverting differential clock input.
7	nCLK1	Input	Pullup	Inverting differential clock input. V_{DD}/2 default when left floating.
8	DIV_SELA	Input	Pulldown	Controls frequency division for Bank A outputs. LVCMOS / LVTTL interface levels.
9, 16, 25, 32	GND	Power		Supply ground.
10, 11, 30, 31	QA0, QA1, QA3, QA2	Output		Bank A outputs. LVCMOS / LVTTL interface levels.
12, 29	V_{DDOA}	Power		Output Bank A supply pins.
13, 28	V_{DDOB}	Power		Output Bank B supply pins.
14, 15, 26, 27	QB0, QB1, QB3, QB2	Output		Bank B outputs. LVCMOS / LVTTL interface levels.
17	OE_A0	Input	Pullup	Output enable for QA0 output. Active HIGH. If OE pin is LOW, outputs will drive Hi-Z. LVCMOS / LVTTL interface levels. See Table 3.
18	OE_A1	Input	Pullup	Output enable for QA1 output. Active HIGH. If OE pin is LOW, outputs will drive Hi-Z. LVCMOS / LVTTL interface levels. See Table 3.
19	OE_A2	Input	Pullup	Output enable for QA2 output. Active HIGH. If OE pin is LOW, outputs will drive Hi-Z. LVCMOS / LVTTL interface levels. See Table 3.
20	OE_A3	Input	Pullup	Output enable for QA3 output. Active HIGH. If OE pin is LOW, outputs will drive Hi-Z. LVCMOS / LVTTL interface levels. See Table 3.
21	OE_B0	Input	Pullup	Output enable for QB0 output. Active HIGH. If OE pin is LOW, outputs will drive Hi-Z. LVCMOS / LVTTL interface levels. See Table 3.
22	OE_B1	Input	Pullup	Output enable for QB1 output. Active HIGH. If OE pin is LOW, outputs will drive Hi-Z. LVCMOS / LVTTL interface levels. See Table 3.
23	OE_B2	Input	Pullup	Output enable for QB2 output. Active HIGH. If OE pin is LOW, outputs will drive Hi-Z. LVCMOS / LVTTL interface levels. See Table 3.
24	OE_B3	Input	Pullup	Output enable for QB3 output. Active HIGH. If OE pin is LOW, outputs will drive Hi-Z. LVCMOS / LVTTL interface levels. See Table 3.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
C_{PD}	Power Dissipation Capacitance (per output)	V_{DD}, V_{DDOA}, V_{DDOB} = 3.465V		11		pF
		V_{DD}, V_{DDOA}, V_{DDOB} = 2.625V		TBD		pF
		V_{DD} = 3.465, V_{DDOA}, V_{DDOB} = 2.625V		TBD		pF
R_{OUT}	Output Impedance			15		Ω

TABLE 3. OE FUNCTION TABLE

Inputs	Outputs
OEx	**QAx, QBx**
0	Hi-Z
1	Active

Absolute Maximum Ratings

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	49.5°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDOA} = V_{DDOB} = 3.3V±5\%$, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{DDOA}, V_{DDOB}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current			60		mA
I_{DDOA}, I_{DDOB}	Output Supply Current	No Load		0		mA

Table 4B. Power Supply DC Characteristics, $V_{DD} = V_{DDOA} = V_{DDOB} = 2.5V±5\%$, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		2.375	2.5	2.625	V
V_{DDOA}, V_{DDOB}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current			60		mA
I_{DDOA}, I_{DDOB}	Output Supply Current	No Load		0		mA

Table 4C. Power Supply DC Characteristics, $V_{DD} = 3.3V±5\%$, $V_{DDOA} = V_{DDOB} = 2.5V±5\%$, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{DDOA}, V_{DDOB}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current			60		mA
I_{DDOA}, I_{DDOB}	Output Supply Current	No Load		0		mA

TABLE 4D. LVCMOS DC CHARACTERISTICS, T_A = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{DD} = 3.3V ± 5%	2		V_{DD} + 0.3	V
			V_{DD} = 2.5V ± 5%	1.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		V_{DD} = 3.3V ± 5%	-0.3		0.8	V
			V_{DD} = 2.5V ± 5%	-0.3		0.7	V
I_{IH}	Input High Current	CLK_SEL, DIV_SELA, DIV_SELB	V_{DD} = 3.3V ± 5%			150	µA
			V_{DD} = 2.5V ± 5%			150	µA
		OE_A0:OE_A3, OE_B0:OE_B3	V_{DD} = 3.3V ± 5%			5	µA
			V_{DD} = 2.5V ± 5%			5	µA
I_{IL}	Input Low Current	CLK_SEL, DIV_SELA, DIV_SELB	V_{DD} = 3.3V ± 5%	-5			µA
			V_{DD} = 2.5V ± 5%	-5			µA
		OE_A0:OE_A3, OE_B0:OE_B3	V_{DD} = 3.3V ± 5%	-150			µA
			V_{DD} = 2.5V ± 5%	-150			µA
V_{OH}	Output High Voltage		$V_{DDOA, B}$ = 3.3V ± 5%; NOTE 1	2.6			V
			$V_{DDOA, B}$ = 2.5V ± 5%; NOTE 1	1.8			V
V_{OL}	Output Low Voltage		$V_{DDOA, B}$ = 3.3V ± 5%; NOTE 1			0.5	V
			$V_{DDOA, B}$ = 2.5V ± 5%; NOTE 1			0.5	V

NOTE 1: Outputs terminated with 50Ω to $V_{DDOA, B}$/2. See Parameter Measurement section, "Load Test Circuit" diagrams.

TABLE 4E. DIFFERENTIAL DC CHARACTERISTICS, V_{DD} = 3.3V±5% OR 2.5V±5%, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	nCLK0, nCLK1	V_{IN} = V_{DD} = 3.465V, V_{IN} = V_{DD} = 2.625V			5	µA
		CLK0, CLK1	V_{IN} = V_{DD} = 3.465V, V_{IN} = V_{DD} = 2.625V			150	µA
I_{IL}	Input Low Current	nCLK0, nCLK1	V_{IN} = 0V, V_{DD} = 3.465V, V_{IN} = 0V, V_{DD} = 2.625V	-150			µA
		CLK0, CLK1	V_{IN} = 0V, V_{DD} = 3.465V, V_{IN} = 0V, V_{DD} = 2.625V	-5			µA
V_{PP}	Peak-to-Peak Input Voltage			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 0.5		V_{DD} - 0.85	V

NOTE 1: For single ended applications, the maximum input voltage for CLKx, nCLKx is V_{DD} + 0.3V.
NOTE 2: Common mode voltage is defined as V_{IH}.

TABLE 5A. AC CHARACTERISTICS, $V_{DD} = V_{DDOA} = V_{DDOB} = 3.3V \pm 5\%$, $T_A = 0°C$ TO $70°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency					250	MHz
t_{PD}	Propagation Delay; NOTE 1				3		ns
*t*sk(b)	Bank Skew; NOTE 2, 6	QA[0:3]/nQA[0:3]			30		ps
		QB[0:3]/nQB[0:3]			50		ps
*t*sk(o)	Output Skew; NOTE 3, 6				50		ps
*t*sk(pp)	Part-to-Part Skew; NOTE 4, 6				TBD		ps
t_R / t_F	Output Rise/Fall Time		20% to 80%		350		ps
odc	Output Duty Cycle				50		%
t_{EN}	Output Enable Time; NOTE 5					10	ns
t_{DIS}	Output Disable Time; NOTE 5					10	ns

NOTE 1: Measured from the differential input crossing point to $V_{DDOA, B}/2$ of the output.
NOTE 2: Defined as skew within a bank with equal load conditions.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDOA, B}/2$.
NOTE 4: Defined as skew between outputs on different devices operating a the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at $V_{DDOA, B}/2$.
NOTE 5: These parameters are guaranteed by characterization. Not tested in production.
NOTE 6: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 5B. AC CHARACTERISTICS, $V_{DD} = V_{DDOA} = V_{DDOB} = 2.5V \pm 5\%$, $T_A = 0°C$ TO $70°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency					250	MHz
t_{PD}	Propagation Delay; NOTE 1				3.2		ns
*t*sk(b)	Bank Skew; NOTE 2, 6	QA[0:3]/nQA[0:3]			35		ps
		QB[0:3]/nQB[0:3]			50		ps
*t*sk(o)	Output Skew; NOTE 3, 6				50		ps
*t*sk(pp)	Part-to-Part Skew; NOTE 4, 6				TBD		ps
t_R / t_F	Output Rise/Fall Time		20% to 80%		360		ps
odc	Output Duty Cycle				50		%
t_{EN}	Output Enable Time; NOTE 5					10	ns
t_{DIS}	Output Disable Time; NOTE 5					10	ns

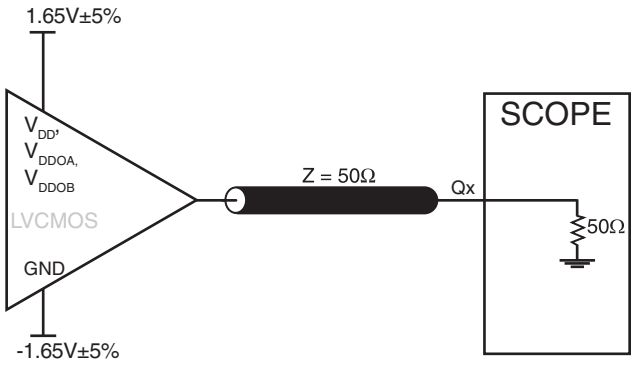
NOTE 1: Measured from the differential input crossing point to $V_{DDOA, B}/2$ of the output.
NOTE 2: Defined as skew within a bank with equal load conditions.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDOA, B}/2$.
NOTE 4: Defined as skew between outputs on different devices operating a the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at $V_{DDOA, B}/2$.
NOTE 5: These parameters are guaranteed by characterization. Not tested in production.
NOTE 6: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 5C. AC CHARACTERISTICS, V_{DD} = 3.3V±5%, V_{DDOA} = V_{DDOB} = 2.5V±5%, T_A = 0°C TO 70°C

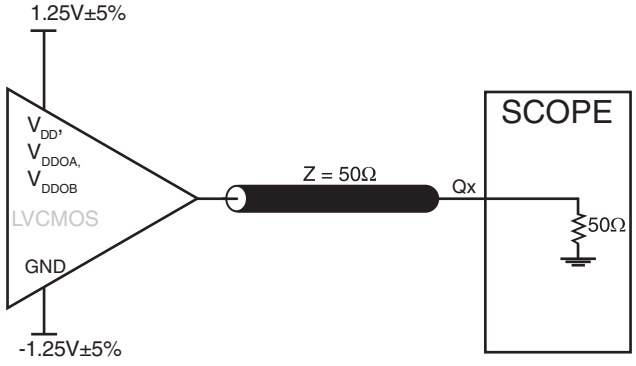
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency					250	MHz
t_{PD}	Propagation Delay; NOTE 1				3.3		ns
*t*sk(b)	Bank Skew; NOTE 2, 6	QA[0:3]/nQA[0:3]			35		ps
		QB[0:3]/nQB[0:3]			55		ps
*t*sk(o)	Output Skew; NOTE 3, 6				60		ps
*t*sk(pp)	Part-to-Part Skew; NOTE 4, 6				TBD		ps
t_R / t_F	Output Rise/Fall Time		20% to 80%		360		ps
odc	Output Duty Cycle				50		%
t_{EN}	Output Enable Time; NOTE 5					10	ns
t_{DIS}	Output Disable Time; NOTE 5					10	ns

NOTE 1: Measured from the differential input crossing point to $V_{DDOA, B}$/2 of the output.
NOTE 2: Defined as skew within a bank with equal load conditions.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDOA, B}$/2.
NOTE 4: Defined as skew between outputs on different devices operating a the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at $V_{DDOA, B}$/2.
NOTE 5: These parameters are guaranteed by characterization. Not tested in production.
NOTE 6: This parameter is defined in accordance with JEDEC Standard 65.

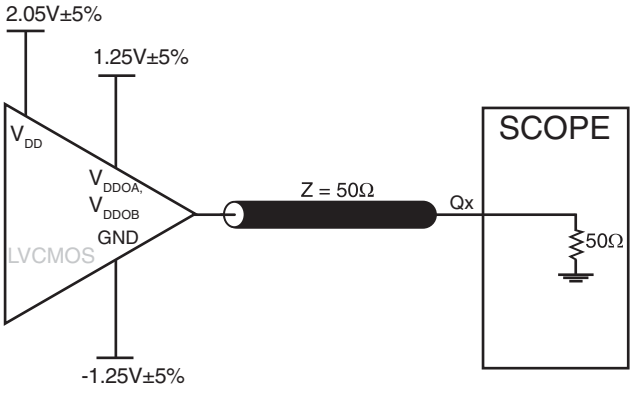
PARAMETER MEASUREMENT INFORMATION



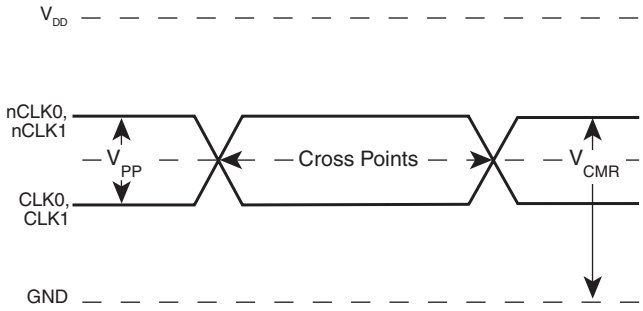
3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT



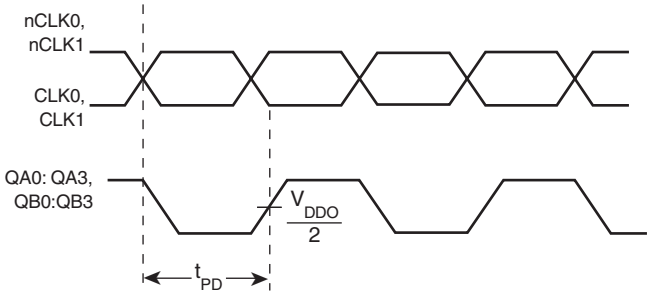
2.5V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT



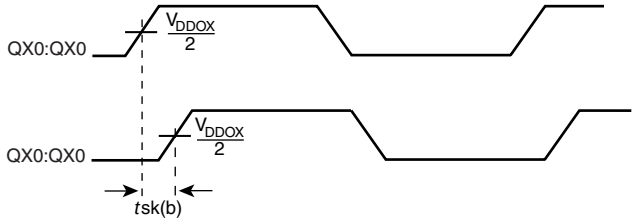
3.3V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT



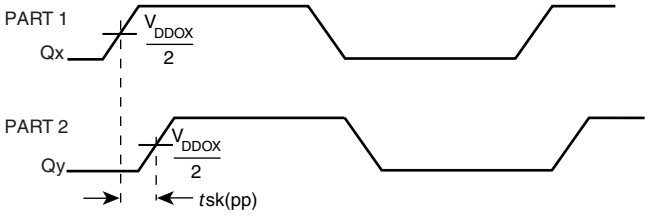
DIFFERENTIAL INPUT LEVEL



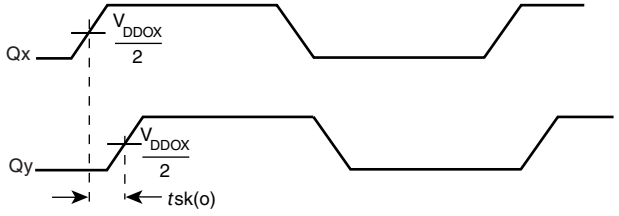
PROPAGATION DELAY



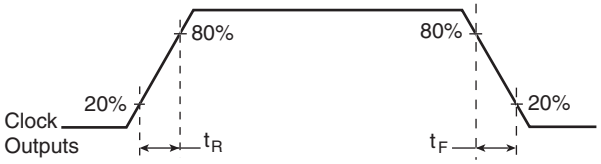
BANK SKEW (where X denotes outputs in the same bank)



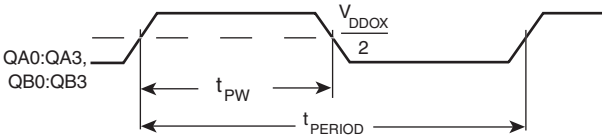
PART-TO-PART SKEW



OUTPUT SKEW



OUTPUT RISE/FALL TIME



$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 2 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

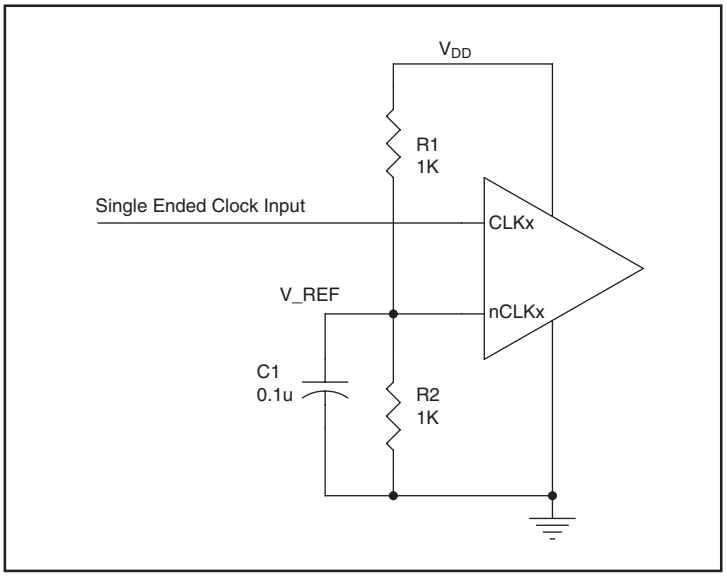


FIGURE 2. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

CLK/nCLK INPUTS

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

LVCMOS CONTROL PINS

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

OUTPUTS:

LVCMOS OUTPUTS

All unused LVCMOS output can be left floating. There should be no trace attached.

Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. Figures 3A to 3F show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 3A,* the input termination applies for IDT HiPerClockS open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

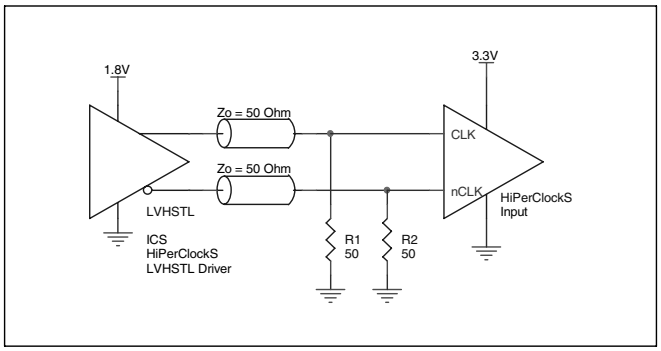


Figure 3A. HiPerClockS CLK/nCLK Input Driven by an IDT Open Emitter HiPerClockS LVHSTL Driver

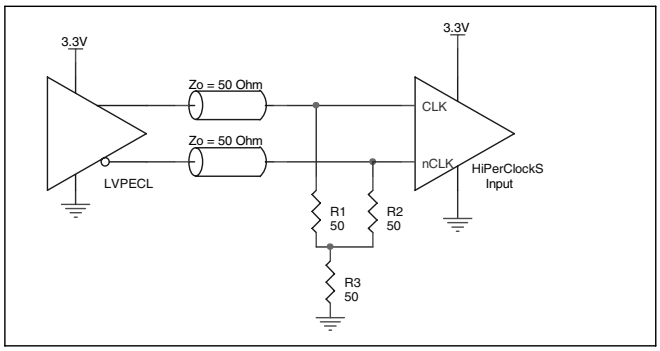


Figure 3B. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVPECL Driver

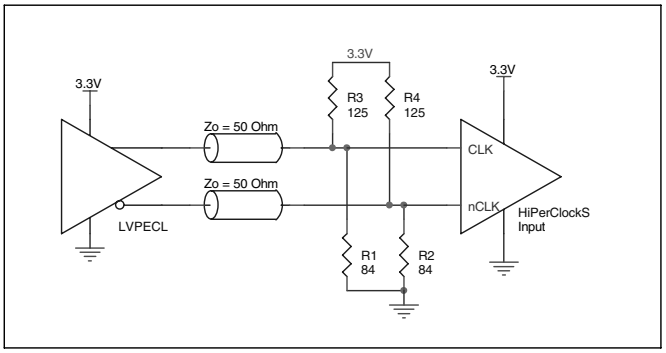


Figure 3C. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVPECL Driver

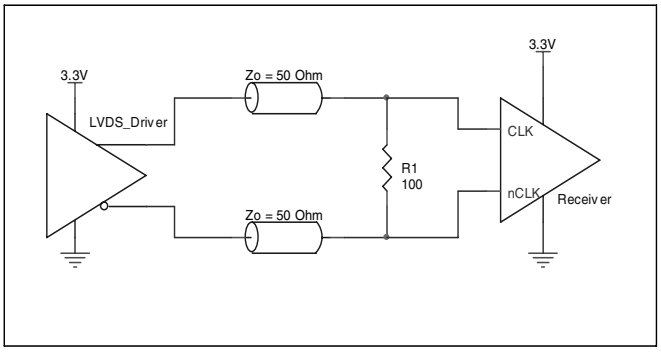


Figure 3D. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVDS Driver

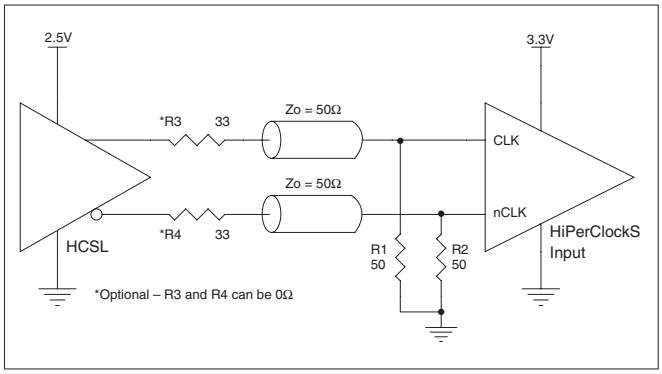


Figure 3E. HiPerClockS CLK/nCLK Input Driven by a 3.3V HCSL Driver

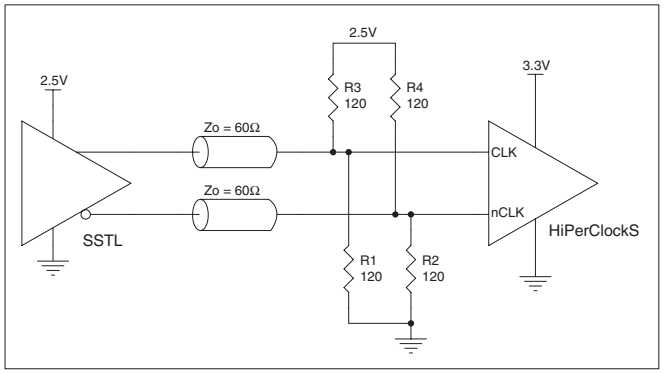


Figure 3F. HiPerClockS CLK/nCLK Input Driven by a 2.5V SSTL Driver

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 4.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as "heat pipes". The number of vias (i.e. "heat pipes") are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, refer to the Application Note on the *Surface Mount Assembly* of Amkor's Thermally/Electrically Enhance Leadfame Base Package, Amkor Technology.

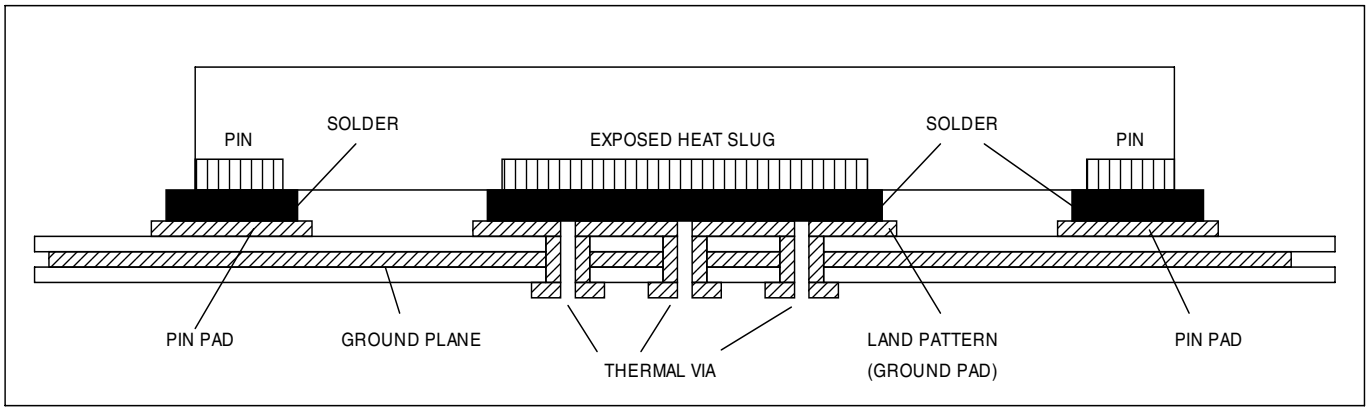


Figure 4. P.C.Assembly for Exposed Pad Thermal Release Path –Side View (Drawing not to Scale)

RELIABILITY INFORMATION

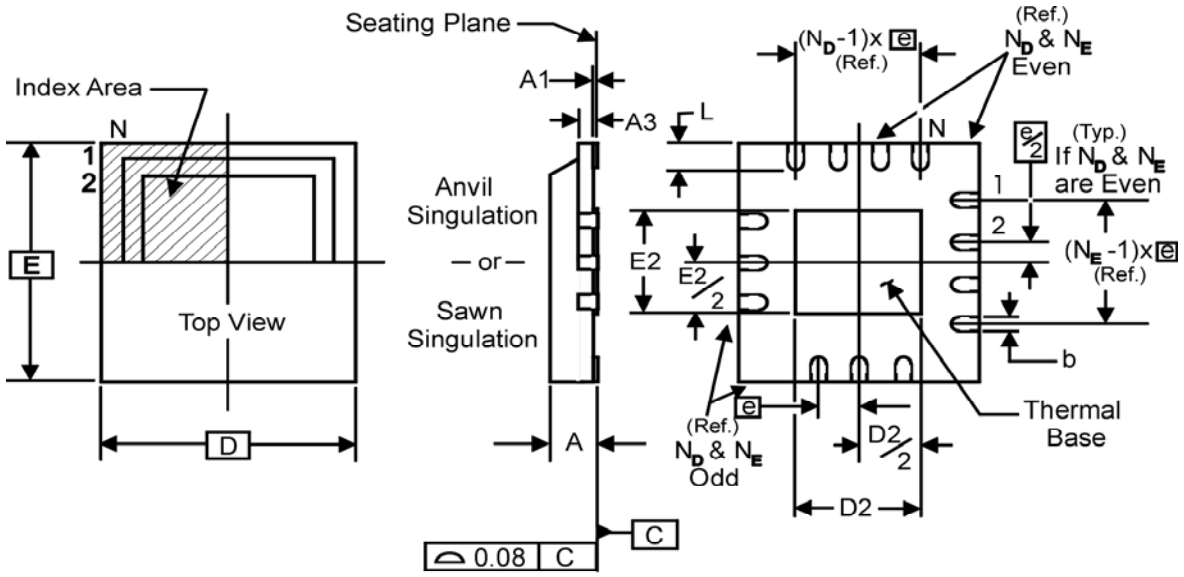
TABLE 6. θ_{JA} VS. AIR FLOW TABLE FOR A 32 LEAD VFQFN

θ_{JA} vs. Air Flow (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	49.5°C/W	43.3°C/W	38.8°C/W

TRANSISTOR COUNT

The transistor count for ICS870S208 is: 2788

PACKAGE OUTLINE - K SUFFIX FOR 32 LEAD VFQFN



NOTE: The following package mechanical drawing is a generic drawing that applies to any pin count VFQFN package. This drawing is not intended to convey the actual pin count or pin layout of this device. The pin count and pinout are shown on the front page. The package dimensions are in Table 8 below.

TABLE 7. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS		
SYMBOL	**Minimum**	**Maximum**
N	32	
A	0.80	1.0
A1	0	0.05
A3	0.25 Reference	
b	0.18	0.30
e	0.50 BASIC	
N_D	8	
N_E	8	
D, E	5.0	
D2, E2	3.0	3.3
L	0.30	0.50

Reference Document: JEDEC Publication 95, MO-220

TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS870S208BK	ICS870S208B	32 Lead VFQFN	tray	0°C to 70°C
ICS870S208BKT	ICS870S208B	32 Lead VFQFN	2500 tape & reel	0°C to 70°C
ICS870S208BKLF	ICS70S208BL	32 Lead "Lead-Free" VFQFN	tray	0°C to 70°C
ICS870S208BKLFT	ICS70S208BL	32 Lead "Lead-Free" VFQFN	2500 tape & reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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