

### GENERAL DESCRIPTION

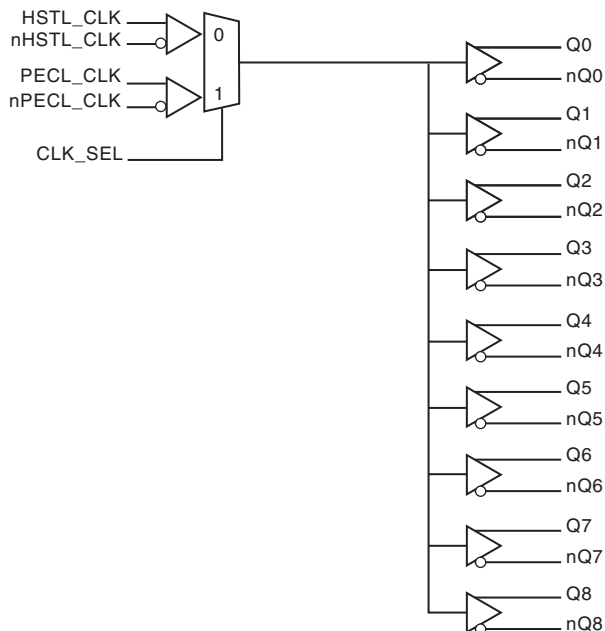
The ICS852911I is a low skew, 1-to-9 Differential-to-HSTL Fanout Buffer. The ICS852911I has two selectable clock inputs which can accept most differential input levels.

Guaranteed output skew, part-to-part skew and crossover voltage characteristics make the ICS852911I ideal for today's most advanced applications, such as IA64 and static RAMs.

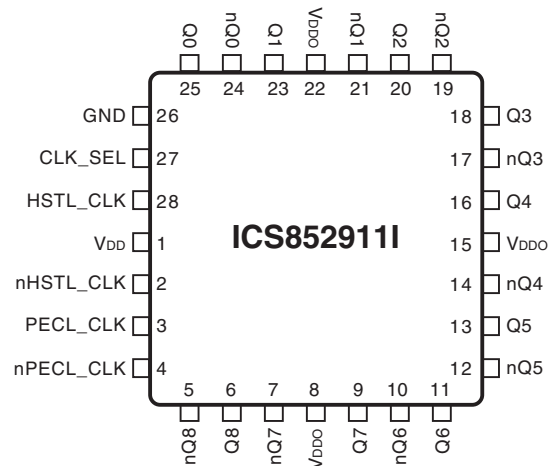
### FEATURES

- 9 HSTL outputs
- Selectable differential CLK, nCLK or LVPECL clock inputs
- HSTL\_CLK, nHSTL\_CLK pair can accept the following differential input levels: LVPECL, LVDS, HSTL, SSTL, HCSL
- PECL\_CLK, nPECL\_CLK supports the following input types: LVPECL, CML, SSTL
- Maximum output frequency: 500MHz
- Output skew: 100ps (maximum)
- Part-to-part skew: 300ps (maximum)
- Propagation delay: 1.7ns (maximum)
- $V_{OH} = 1.4V$  (maximum)
- 3.3V core, 1.6V to 3.6V output supply range
- -40°C to 85°C ambient operating temperature

### BLOCK DIAGRAM



### PIN ASSIGNMENT



**28-Lead PLCC**  
11.6mm x 11.4mm x 4.1mm package body  
**V Package**  
Top View



**TABLE 1. PIN DESCRIPTIONS**

Number	Name	Type		Description
1	V <sub>DD</sub>	Power		Core supply pin.
2	nHSTL_CLK	Input	Pullup/ Pulldown	Inverting differential clock input. V <sub>CC</sub> /2 default when left floating.
3	PECL_CLK	Input	Pulldown	Non-inverting differential LVPECL clock input.
4	nPECL_CLK	Input	Pullup/ Pulldown	Inverting differential clock input. V <sub>CC</sub> /2 default when left floating.
5, 6	nQ8, Q8	Output		Differential output pair. HSTL interface level.
7, 9	nQ7, Q7	Output		Differential output pair. HSTL interface level.
8, 15, 22	V <sub>DDO</sub>	Power		Output supply pins.
10, 11	nQ6, Q6	Output		Differential output pair. HSTL interface level.
12, 13	nQ5, Q5	Output		Differential output pair. HSTL interface level.
14, 16	nQ4, Q4	Output		Differential output pair. HSTL interface level.
17, 18	nQ3, Q3	Output		Differential output pair. HSTL interface level.
19, 20	nQ2, Q2	Output		Differential output pair. HSTL interface level.
21, 23	nQ1, Q1	Output		Differential output pair. HSTL interface level.
24, 25	nQ0, Q0	Output		Differential output pair. HSTL interface level.
26	GND	Power		Power supply ground.
27	CLK_SEL	Input	Pulldown	Clock select input. When HIGH, selects PECL_CLK, nPECL_CLK inputs. When LOW, selects HSTL_CLK, nHSTL_CLK. LVTTTL / LVCMOS interface levels.
28	HSTL_CLK	Input	Pulldown	Non-inverting differential clock input.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

**TABLE 2. PIN CHARACTERISTICS**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C <sub>IN</sub>	Input Capacitance			4		pF
R <sub>PULLUP</sub>	Input Pullup Resistor			51		kΩ
R <sub>PULLDOWN</sub>	Input Pulldown Resistor			51		kΩ

**TABLE 3. CONTROL INPUT FUNCTION TABLE**

Inputs	
CLK_SEL	Selected Sourced
0	HSTL_CLK, nHSTL_CLK
1	PECL_CLK, nPECL_CLK



# ICS852911I

## LOW SKEW, 1-TO-9 DIFFERENTIAL-TO-HSTL FANOUT BUFFER

### ABSOLUTE MAXIMUM RATINGS

Supply Voltage, $V_{CC}$	4.6V
Inputs, $V_i$	-0.5V to $V_{DD} + 0.5V$
Outputs, $I_o$	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, $\theta_{JA}$	37.8°C/W (0 lfpm)
Storage Temperature, $T_{STG}$	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 4A. POWER SUPPLY DC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 0.3V$ ,  $V_{DDO} = 1.6V$  TO  $3.6V$ ,  $T_A = -40^\circ C$  TO  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Core Supply Voltage		3.0	3.3	3.6	V
$V_{DDO}$	Output Supply Voltage		1.6	3.3	3.6	V
$I_{DD}$	Power Supply Current				95	mA

**TABLE 4B. LVCMOS/LVTTL DC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 0.3V$ ,  $V_{DDO} = 1.6V$  TO  $3.6V$ ,  $T_A = -40^\circ C$  TO  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	CLK_SEL		2		$V_{DD} + 0.3$	V
$V_{IL}$	CLK_SEL		-0.3		0.8	V
$I_{IH}$	Input High Current	CLK_SEL $V_{IN} = V_{DD} = 3.6V$			150	$\mu A$
$I_{IL}$	Input Low Current	CLK_SEL $V_{IN} = 0V, V_{DD} = 3.6V$	-5			$\mu A$

**TABLE 4C. LVPECL DC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 0.3V$ ,  $V_{DDO} = 1.6V$  TO  $3.6V$ ,  $T_A = -40^\circ C$  TO  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$I_{IH}$	Input High Current	PECL_CLK	$V_{DD} = V_{IN} = 3.6V$		150	$\mu A$
		nPECL_CLK	$V_{DD} = V_{IN} = 3.6V$		150	$\mu A$
$I_{IL}$	Input Low Current	PECL_CLK	$V_{DD} = 3.6V, V_{IN} = 0V$	-5		$\mu A$
		nPECL_CLK	$V_{DD} = 3.6V, V_{IN} = 0V$	-150		$\mu A$
$V_{PP}$	Peak-to-Peak Input Voltage		0.3		1	V
$V_{CMR}$	Common Mode Input Voltage; NOTE 1, 2		1.5		$V_{DD}$	V

NOTE 1: Common mode voltage is defined as  $V_{IH}$ .

NOTE 2: For single ended applications, the maximum input voltage for PECL\_CLK and nPECL\_CLK is  $V_{DD} + 0.3V$ .



# ICS8529111

## LOW SKEW, 1-TO-9 DIFFERENTIAL-TO-HSTL FANOUT BUFFER

**TABLE 4D. HSTL DC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 0.3V$ ,  $V_{DDO} = 1.6V$  TO  $3.6V$ ,  $T_A = -40^\circ C$  TO  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$I_{IH}$	Input High Current	HSTL_CLK	$V_{IN} = V_{DD} = 3.6V$		150	$\mu A$
		nHSTL_CLK	$V_{IN} = V_{DD} = 3.6V$		150	$\mu A$
$I_{IL}$	Input Low Current	HSTL_CLK	$V_{IN} = 0V, V_{DD} = 3.6V$	-5		$\mu A$
		nHSTL_CLK	$V_{IN} = 0V, V_{DD} = 3.6V$	-150		$\mu A$
$V_{PP}$	Peak-to-Peak Input Voltage		0.15		1.3	V
$V_{CMR}$	Common Mode Input Voltage; NOTE 1, 2		0.5		$V_{DD} - 0.85$	V
$V_{OH}$	Output High Voltage; NOTE 3		1.0		1.4	V
$V_{OL}$	Output Low Voltage; NOTE 3		0		0.4	V
$V_{OX}$	Output Crossover Voltage; NOTE 4		40		60	%
$V_{SWING}$	Peak-to-Peak Output Voltage Swing		0.6		1.1	V

NOTE 1: For single ended applications, the maximum input voltage for HSTL\_CLK and nHSTL\_CLK is  $V_{DD} + 0.3V$ .

NOTE 2: Common mode voltage is defined as  $V_{IH}$ .

NOTE 3: Outputs terminated with  $50\Omega$  to ground.

NOTE 4: Defined with respect to output voltage swing at a given condition.

**TABLE 5. AC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 0.3V$ ,  $V_{DDO} = 1.6V$  TO  $3.6V$ ,  $T_A = -40^\circ C$  TO  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{MAX}$	Output Frequency				500	MHz
$t_{PD}$	Propagation Delay; NOTE 1		1.3	1.5	1.7	ns
$t_{sk(o)}$	Output Skew; NOTE 2, 4				100	ps
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 3, 4				300	ps
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	200		600	ps
odc	Output Duty Cycle		47		53	%

All parameters measured at  $f_{MAX}$  unless noted otherwise.

NOTE 1: Measured from the differential input crossing point to the differential output crossing point.

Measured from  $V_{DD}/2$  to the output differential crossing point for single ended input levels.

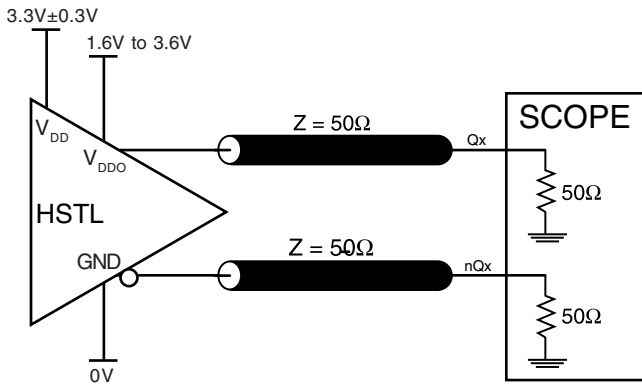
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.

Measured at the output differential cross points.

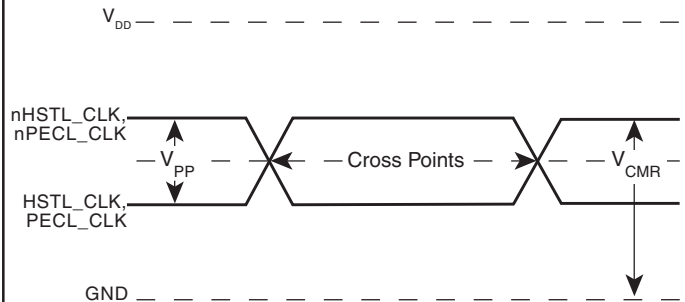
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

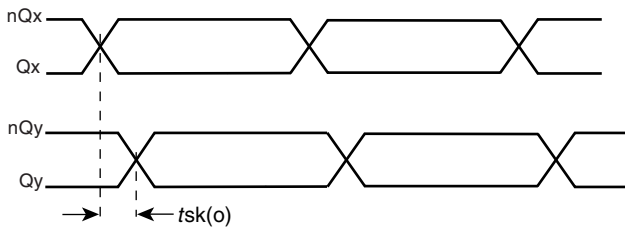
## PARAMETER MEASUREMENT INFORMATION



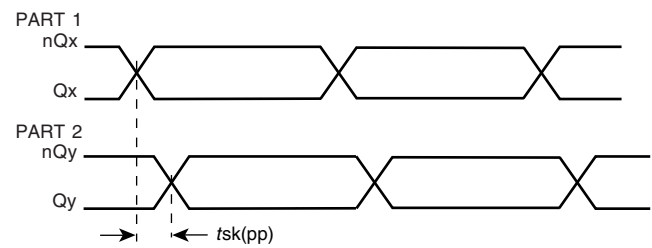
**3.3V CORE/1.6V TO 3.6V OUTPUT LOAD AC TEST CIRCUIT**



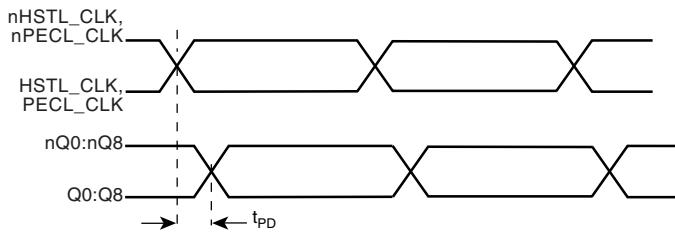
**DIFFERENTIAL INPUT LEVEL**



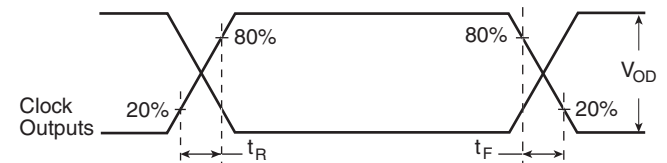
**OUTPUT SKEW**



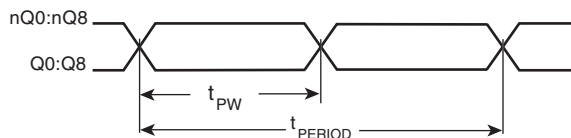
**PART-TO-PART SKEW**



**PROPAGATION DELAY**



**OUTPUT RISE/FALL TIME**



$$\text{odc} = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

**OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD**

## APPLICATION INFORMATION

### WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage  $V_{REF} = V_{DD}/2$  is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio

of R1 and R2 might need to be adjusted to position the  $V_{REF}$  in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and  $V_{DD} = 3.3V$ ,  $V_{REF}$  should be 1.25V and  $R2/R1 = 0.609$ .

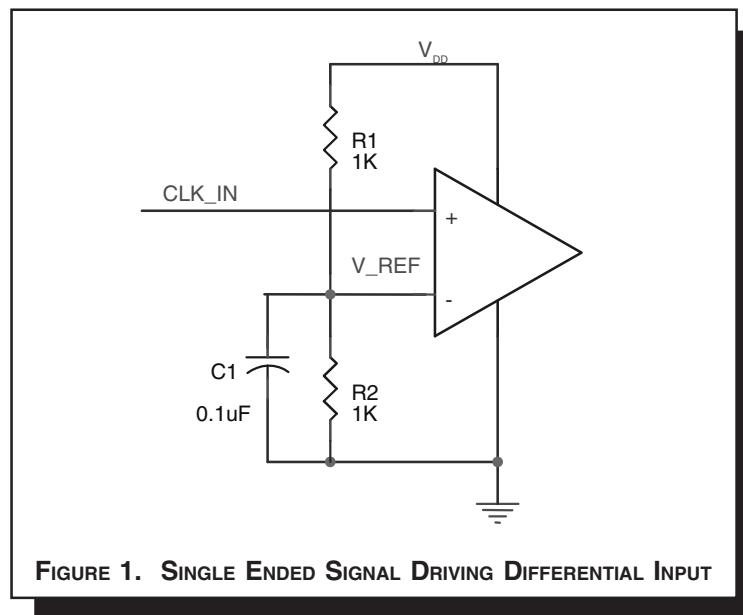
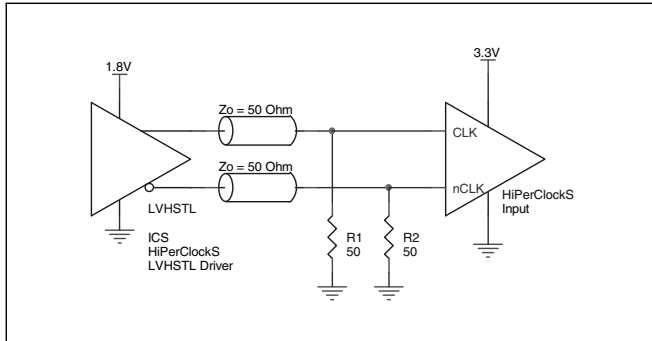


FIGURE 1. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

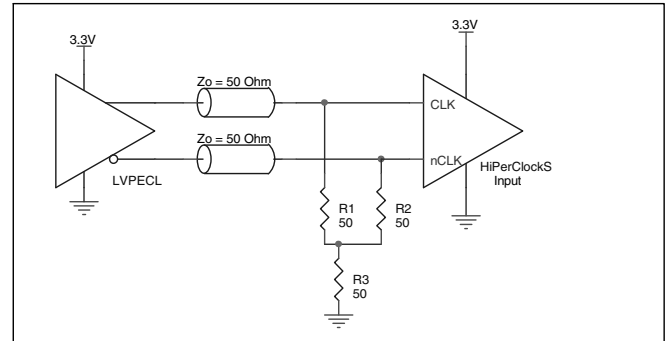
#### DIFFERENTIAL CLOCK INPUT INTERFACE

The HSTL\_CLK/nHSTL\_CLK accepts LVDS, LVPECL, HSTL, SSTL, HCSL and other differential signals. Both  $V_{SWING}$  and  $V_{OH}$  must meet the  $V_{PP}$  and  $V_{CMR}$  input requirements. Figures 2A to 2E show interface examples for the HSTL\_CLK/nHSTL\_CLK input driven by the most common driver types. The input interfaces suggested here are examples only.

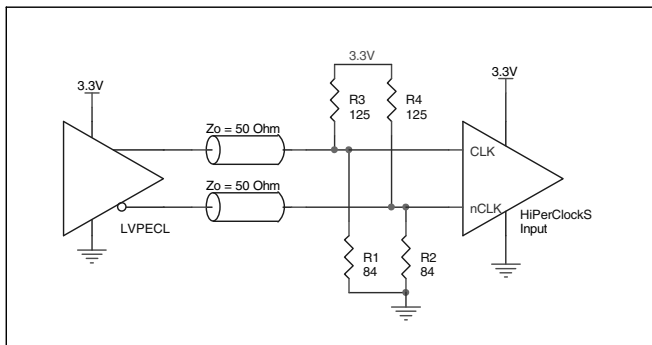
Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 2A*, the input termination applies for HSTL drivers. If you are using an HSTL driver from another vendor, use their termination recommendation.



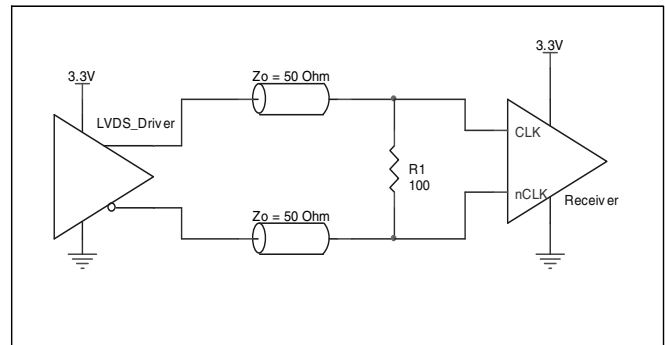
**FIGURE 2A. HSTL\_CLK/nHSTL\_CLK INPUT DRIVEN BY HSTL DRIVER**



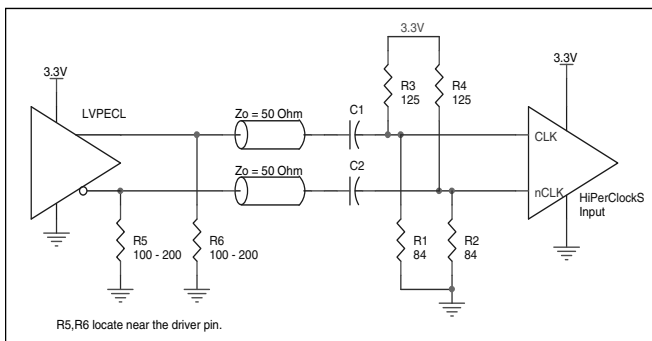
**FIGURE 2B. HSTL\_CLK/nHSTL\_CLK INPUT DRIVEN BY 3.3V LVPECL DRIVER**



**FIGURE 2C. HSTL\_CLK/nHSTL\_CLK INPUT DRIVEN BY 3.3V LVPECL DRIVER**



**FIGURE 2D. HSTL\_CLK/nHSTL\_CLK INPUT DRIVEN BY 3.3V LVDS DRIVER**

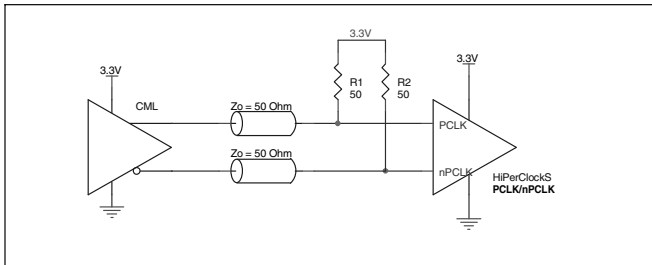


**FIGURE 2E. HSTL\_CLK/nHSTL\_CLK INPUT DRIVEN BY 3.3V LVPECL DRIVER WITH AC COUPLE**

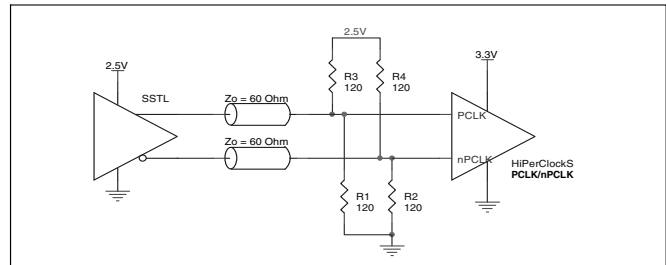
#### LVPECL CLOCK INPUT INTERFACE

The PECL\_CLK/nPECL\_CLK accepts LVPECL, CML, SSTL and other differential signals. Both  $V_{SWING}$  and  $V_{OH}$  must meet the  $V_{PP}$  and  $V_{CMR}$  input requirements. *Figures 3A to 3E* show interface examples for the PECL\_CLK/nPECL\_CLK input driven by the most common driver types.

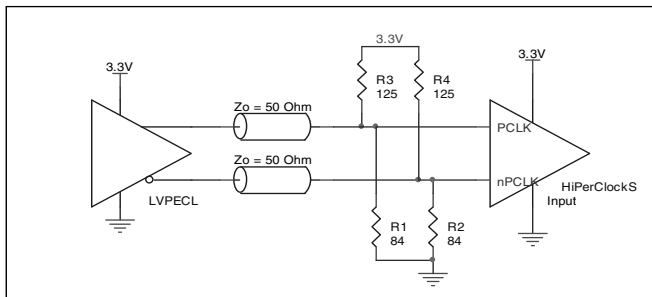
The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.



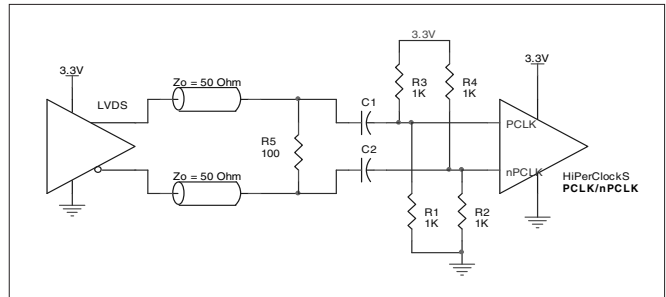
**FIGURE 3A. PECL\_CLK/nPECL\_CLK INPUT DRIVEN BY A CML DRIVER**



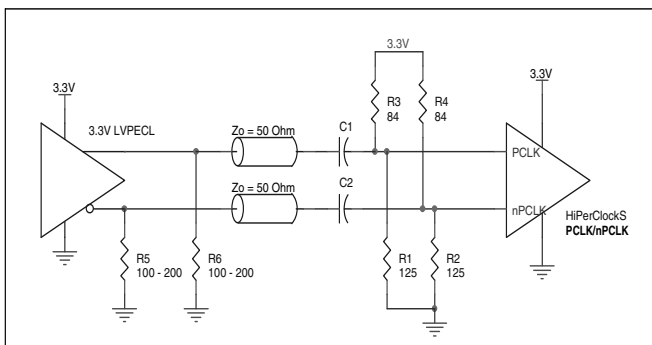
**FIGURE 3B. PECL\_CLK/nPECL\_CLK INPUT DRIVEN BY AN SSTL DRIVER**



**FIGURE 3C. PECL\_CLK/nPECL\_CLK INPUT DRIVEN BY A 3.3V LVPECL DRIVER**



**FIGURE 3D. PECL\_CLK/nPECL\_CLK INPUT DRIVEN BY A 3.3V LVDS DRIVER**



**FIGURE 3E. PECL\_CLK/nPECL\_CLK INPUT DRIVEN BY A 3.3V LVPECL DRIVER WITH AC COUPLE**



### SCHEMATIC EXAMPLE

Figure 4 shows a schematic example of ICS852911I. In this example, the input is driven by an ICS HiPerClockS HSTL driver. The decoupling capacitors should be physically located near the power pin.

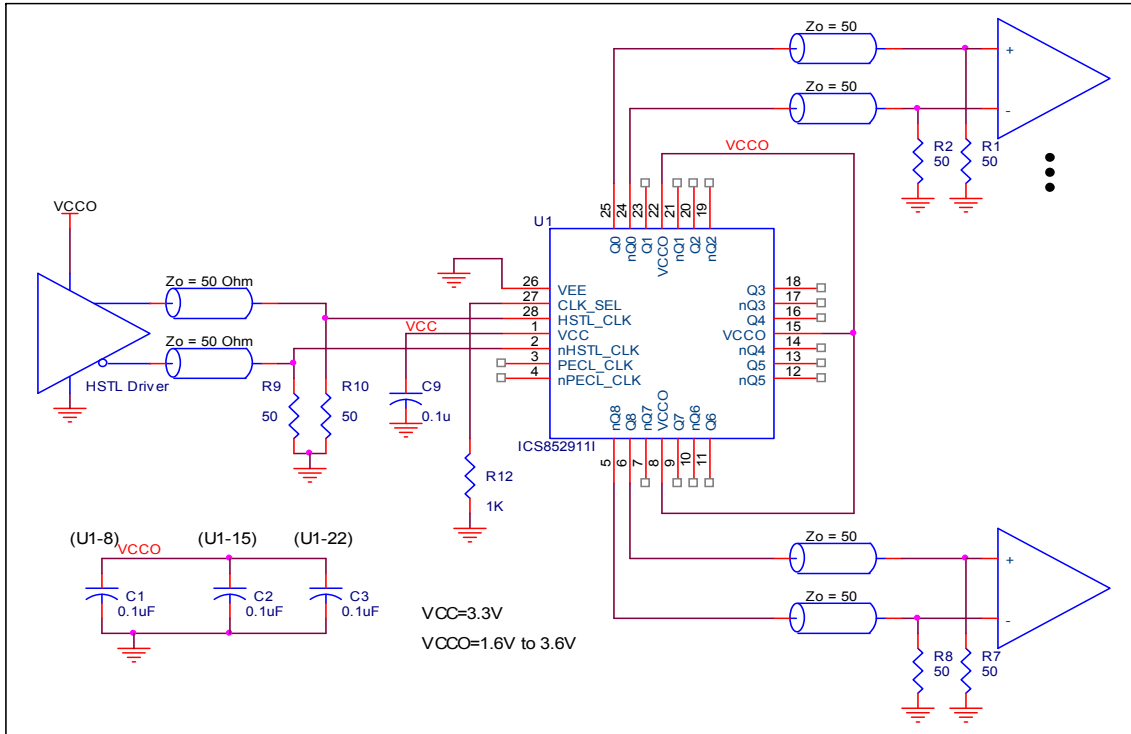


FIGURE 4. ICS852911I HSTL BUFFER SCHEMATIC EXAMPLE

## POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS8529111. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the ICS8529111 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{DD} = 3.3V + 0.3V = 3.6V$ , which gives worst case results.

**NOTE:** Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)<sub>MAX</sub> =  $V_{DD\_MAX} * I_{DD\_MAX} = 3.6V * 95mA = 342mW$
- Power (outputs)<sub>MAX</sub> = **87.2mW/Loaded Output pair**  
 If all outputs are loaded, the total power is  $9 * 87.2mW = 784.8mW$

**Total Power**<sub>MAX</sub> (3.6V, with all outputs switching) =  $342mW + 784.8mW = 1126.8mW$

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for the devices is 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = junction-to-ambient thermal resistance

$Pd\_total$  = Total device power dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 31.1°C/W per Table 6 below.

Therefore,  $T_j$  for an ambient temperature of 85°C with all outputs switching is:

$85^\circ C + 1.127W * 31.1^\circ C/W = 120^\circ C$ . This is below the limit of 125°C.

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

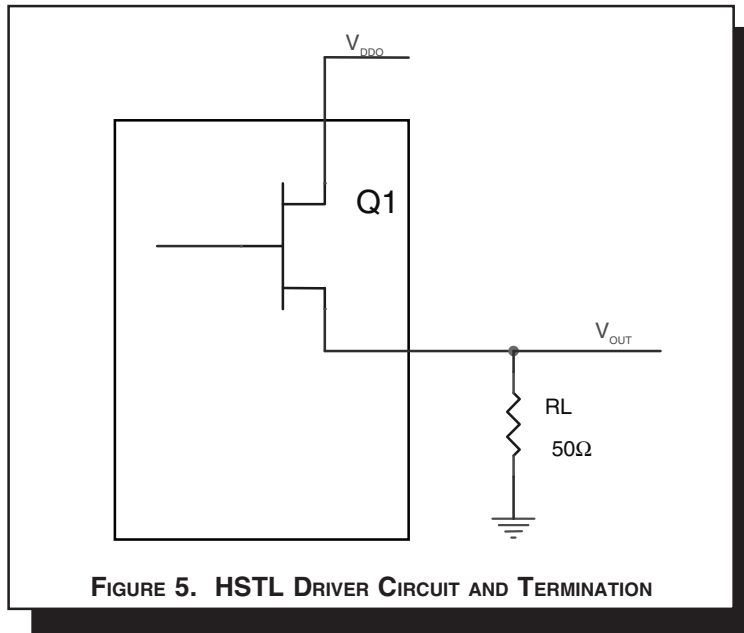
**Table 6. Thermal Resistance  $\theta_{JA}$  for 28-pin PLCC, Forced Convection**

<b><math>\theta_{JA}</math> by Velocity (Linear Feet per Minute)</b>			
	<b>0</b>	<b>200</b>	<b>500</b>
Multi-Layer PCB, JEDEC Standard Test Boards	37.8°C/W	31.1°C/W	28.3°C/W
<b>NOTE:</b> Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.			

### 3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

HSTL output driver circuit and termination are shown in *Figure 5*.



To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load.

Pd\_H is power dissipation when the output drives high.

Pd\_L is the power dissipation when the output drives low.

$$Pd_H = (V_{OH\_MAX} / R_L) * (V_{DDO\_MAX} - V_{OH\_MAX})$$

$$Pd_L = (V_{OL\_MAX} / R_L) * (V_{DDO\_MAX} - V_{OL\_MAX})$$

$$Pd_H = (1.4V/50\Omega) * (3.6V - 1.4V) = \mathbf{61.6mW}$$

$$Pd_L = (0.4V/50\Omega) * (3.6V - 0.4V) = \mathbf{25.6mW}$$

$$\text{Total Power Dissipation per output pair} = Pd_H + Pd_L = \mathbf{87.2mW}$$



## RELIABILITY INFORMATION

TABLE 6.  $\theta_{JA}$  VS. AIR FLOW TABLE FOR 28 LEAD PLCC

$\theta_{JA}$ by Velocity (Linear Feet per Minute)			
	0	200	500
Multi-Layer PCB, JEDEC Standard Test Boards	37.8°C/W	31.1°C/W	28.3°C/W

**NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

### TRANSISTOR COUNT

The transistor count for ICS852911I is: 726

PACKAGE OUTLINE - V SUFFIX FOR 28 LEAD PLCC

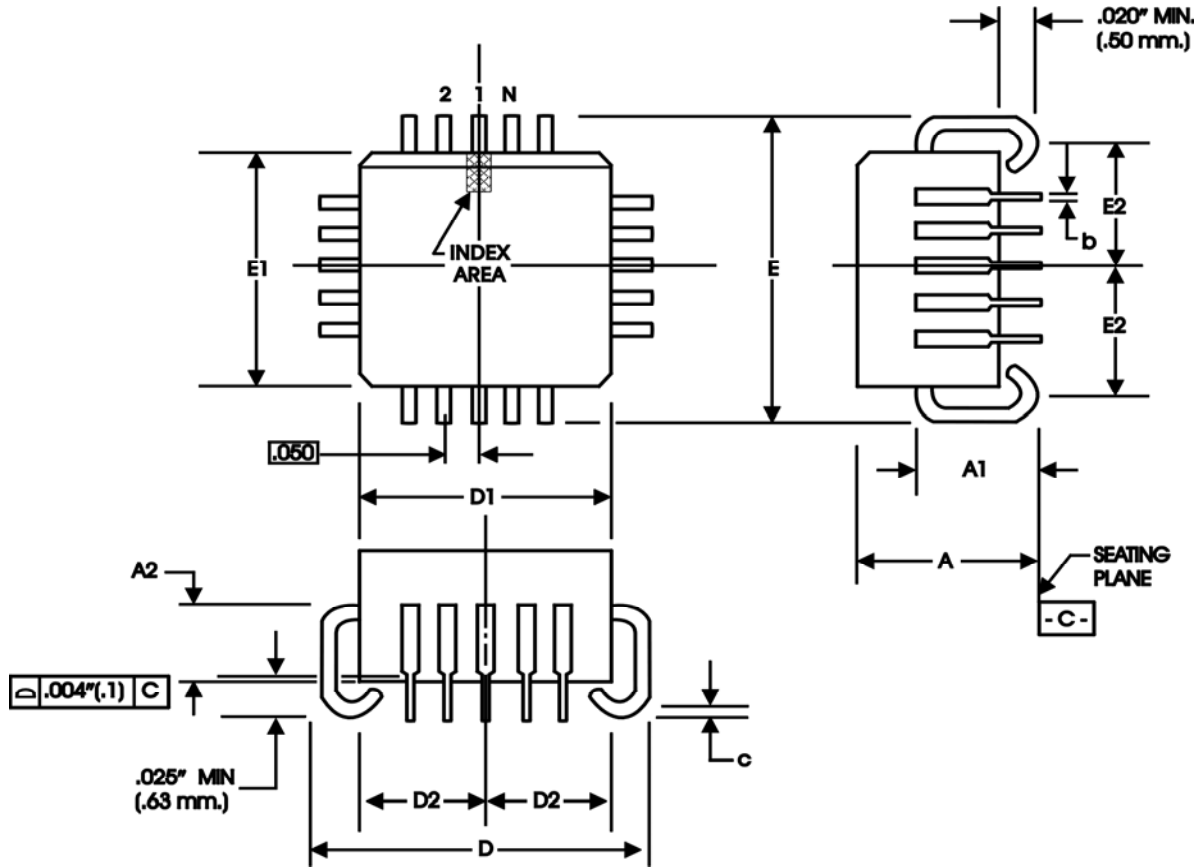


TABLE 7. PACKAGE DIMENSIONS

JEDEC VARIATION		
ALL DIMENSIONS IN MILLIMETERS		
SYMBOL	MINIMUM	MAXIMUM
N	28	
A	4.19	4.57
A1	2.29	3.05
A2	1.57	2.11
b	0.33	0.53
c	0.19	0.32
D	12.32	12.57
D1	11.43	11.58
D2	4.85	5.56
E	12.32	12.57
E1	11.43	11.58
E2	4.85	5.56

Reference Document: JEDEC Publication 95, MS-018



**ICS852911I**  
LOW SKEW, 1-TO-9  
DIFFERENTIAL-TO-HSTL FANOUT BUFFER

**TABLE 8. ORDERING INFORMATION**

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
852911AVI	ICS852911AVI	28 Lead PLCC	Tube	-40°C to 85°C
852911AVIT	ICS852911AVI	28 Lead PLCC	500 Tape & Reel	-40°C to 85°C

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**ICS852911I**  
LOW SKEW, 1-TO-9  
DIFFERENTIAL-TO-HSTL FANOUT BUFFER

REVISION HISTORY SHEET				
Rev	Table	Page	Description of Change	Date
A		1	Block Diagram - corrected drawing.	5/23/05
A	T8	14 16	Updated datasheet's header/footer with IDT from ICS. Removed ICS prefix from Part/Order Number column. Added Contact Page.	8/5/10



**ICS852911I**  
LOW SKEW, 1-TO-9  
DIFFERENTIAL-TO-HSTL FANOUT BUFFER

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