LOW SKEW, 1-TO-4, DIFFERENTIAL-TO-HSTL FANOUT BUFFER

ICS8523

Description

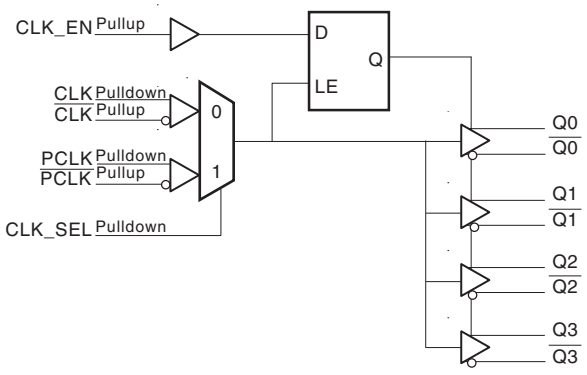
The ICS8523 is a low skew, high performance 1-to-4 Differential-to-HSTL fanout buffer and a member of the HiPerClockS™family of High Performance Clock Solutions from IDT. The ICS8523 has two selectable clock inputs. The CLK, $\overline{CLK}$ pair can accept most standard differential input levels. The PCLK, $\overline{PCLK}$ pair can accept LVPECL, CML, or SSTL input levels. The clock enable is internally synchronized to eliminate runt pulses on the outputs during asynchronous assertion/deassertion of the clock enable pin.

Guaranteed output and part-to-part skew characteristics make the ICS8523 ideal for those applications demanding well defined performance and repeatability.

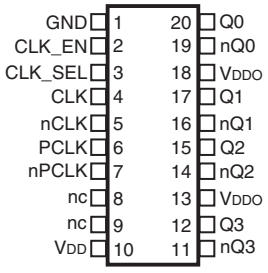
Features

- Four differentialoutput HSTL compatible outputs
- Selectable differential CLK, $\overline{CLK}$ or LVPECL clock inputs
- CLK, $\overline{CLK}$ pair can accept the following differential input levels: LVPECL, LVDS, HSTL, HCSL, SSTL
- PCLK, $\overline{PCLK}$ pair can accept the following differential input levels: LVPECL, CML, SSTL
- Maximum output frequenc: 650MHz
- Translates any single-ended input signal to HSTL levels with resistor bias on $\overline{CLK}$ input
- Output skew: 30ps (maximum)
- Part-to-part skew: 200ps (maximum)
- 3.3V core, 1.8V output operating supply
- 0°C to 70°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

Block Diagram



Pin Assignment



ICS8523
20-Lead TSSOP
6.5mm x 4.4mm x 0.925mm
package body
G Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1	GND	Power		Power supply ground.
2	CLK_EN	Input	Pullup	Synchronizing clock enable. When HIGH, clock outputs follow clock input. When LOW, Qx outputs are forced low, $\overline{Qx}$ outputs are forced high. LVCMOS / LVTTL interface levels.
3	CLK_SEL	Input	Pulldown	Clock select input. When HIGH, selects differential PCLK, $\overline{PCLK}$ inputs. When LOW, selects CLK, $\overline{CLK}$ inputs. LVCMOS / LVTTL interface levels.
4	CLK	Input	Pulldown	Non-inverting differential clock input.
5	$\overline{CLK}$	Input	Pullup	Inverting differential clock input.
6	CLK	Input	Pulldown	Non-inverting differential LVPECL clock input.
7	$\overline{CLK}$	Input	Pullup	Inverting differential LVPECL clock input.
8, 9	nc	Unused		No connect.
10	V_{DD}	Power		Positive supply pin.
11, 12	$\overline{Q3}$, Q3	Output		Differential output pair. HSTL interface levels.
13, 18	V_{DDO}	Power		Output supply pins.
14, 15	$\overline{Q2}$, Q2	Output		Differential output pair. HSTL interface levels.
16, 17	$\overline{Q1}$, Q1	Output		Differential output pair. HSTL interface levels.
19, 20	$\overline{Q0}$, Q0	Output		Differential output pair. HSTL interface levels.

NOTE: *Pullup and Pulldown* refer to intenal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Function Tables

Table 3A. Control Input Function Table

Inputs			Outputs	
CLK_EN	**CLK_SEL**	**Selected Source**	**Q0:Q3**	**$\overline{Q0}$:$\overline{Q3}$**
0	0	CLK, $\overline{CLK}$	Disabled; LOW	Disabled; HIGH
0	1	PCLK, $\overline{PCLK}$	Disabled; LOW	Disabled; HIGH
1	0	CLK, $\overline{CLK}$	Enabled	Enabled
1	1	PCLK, $\overline{PCLK}$	Enabled	Enabled

After CLK_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock edge as shown in Figure 1. In the active mode, the state of the outputs are a function of the CLK, $\overline{CLK}$ and PCLK, $\overline{PCLK}$ inputs as described in Table 3B.

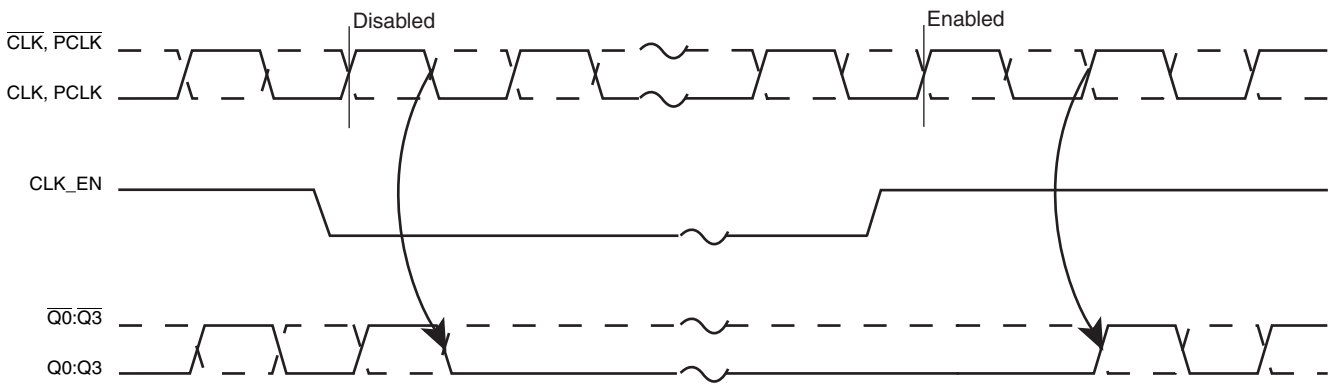


Figure 1. CLK_EN Timing Diagram

Table 3B. Clock Input Function Table

Inputs		Outputs			
CLK or PCLK	**$\overline{CLK}$ or $\overline{PCLK}$**	**Q[0:3]**	**$\overline{Q[0:3]}$**	**Input to Output Mode**	**Polarity**
0	0	LOW	HIGH	Differential to Differential	Non-Inverting
1	1	HIGH	LOW	Differential to Differential	Non-Inverting
0	Baised; NOTE 1	LOW	HIGH	Single-Ended to Differential	Non-Inverting
1	Baised; NOTE 1	HIGH	LOW	Single-Ended to Differential	Non-Inverting
Baised; NOTE 1	0	HIGH	LOW	Single-Ended to Differential	Inverting
Baised; NOTE 1	1	LOW	HIGH	Single-Ended to Differential	Inverting

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characterisitcs* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O (LVPECL) Continous Current Surge Current	 50mA 100mA
Package Thermal Impedance, θ_{JA}	73.2°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. LVDS Power Supply DC Characteristics, V_{DD} = 3.3V ± 5%, V_{DDO} = 1.8V ±0.2V, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		1.6	1.8	2.0	V
I_{DD}	Power Supply Current				50	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, V_{DD} = 3.3V ± 5%, V_{DDO} = 1.8V ±0.2V, T_A = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	CLK_EN	V_{DD} = V_{IN} = 3.465V			5	µA
		CLK_SEL	V_{DD} = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	CLK_EN	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
		CLK_SEL	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA

Table 4C. Differential DC Characteristics, V_{DD} = 3.3V ± 5%, V_{DDO} = 1.8V ±0.2V, T_A = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	$\overline{CLK}$	$V_{DD} = V_{IN}$ = 3.465V			5	µA
		CLK	$V_{DD} = V_{IN}$ = 3.465V			150	µA
I_{IL}	Input Low Current	$\overline{CLK}$	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
		CLK	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
V_{PP}	Peak-to-Peak Voltage			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			0.5		V_{DD} – 0.85	V

NOTE 1: Common mode input voltage is defined as V_{IH}.
NOTE 2: For single-ended applications, the maximum input voltage for CLK, $\overline{CLK}$ is V_{DD} + 0.3V.

Table 4D. LVPECL DC Characteristics, V_{DD} = 3.3V ± 5%, V_{DDO} = 1.8V ±0.2V, T_A = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	$\overline{PCLK}$	$V_{DD} = V_{IN}$ = 3.465V			5	µA
		PCLK	$V_{DD} = V_{IN}$ = 3.465V			150	µA
I_{IL}	Input Low Current	$\overline{PCLK}$	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
		PCLK	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
V_{PP}	Peak-to-Peak Voltage			0.3		1.0	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			1.5		V_{DD}	V

NOTE 1: Common mode input voltage is defined as V_{IH}.
NOTE 2: For single-ended applications, the maximum input voltage for CLK, $\overline{CLK}$ is V_{DD} + 0.3V.

Table 4E. HSTL DC Characteristics, V_{DD} = 3.3V ± 5%, V_{DDO} = 1.8V ±0.2V, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Current; NOTE 1		0.9		1.4	V
V_{OL}	Output Low Current; NOTE 1		0		0.4	V
V_{OX}	Output Crossover Voltage		40% x (V_{OH} – V_{OL}) + V_{OL}		60% x (V_{OH} – V_{OL}) + V_{OL}	V
V_{SWING}	Peak-toPeak Output Voltage Swing		0.75		1.25	V

NOTE 1: Outputs termination with 50Ω to ground.

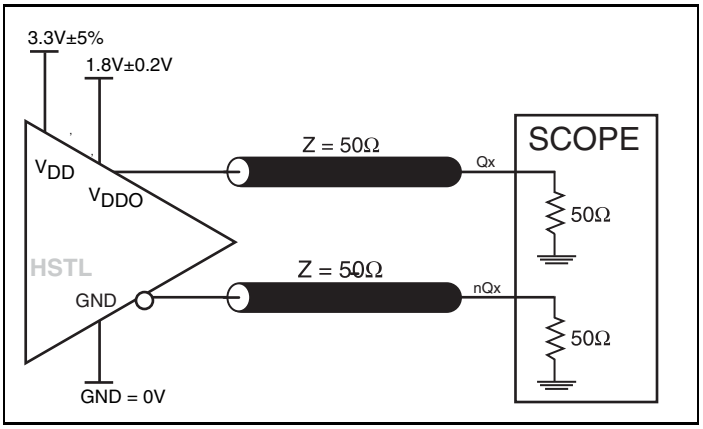
AC Electrical Characteristics

Table 5. AC Characteristics, V_{DD} = 3.3V ± 5%, V_{DDO} = 1.8V ±0.2V, T_A = 0°C to 70°C

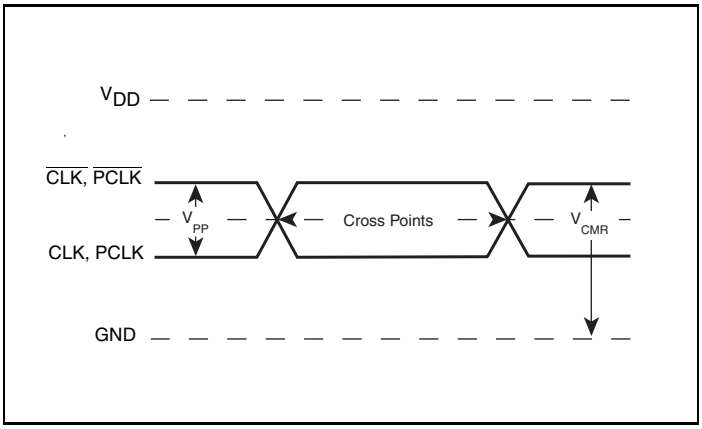
Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency		1.0		650	MHz
t_{PD}	Propagation Delay; NOTE 1	$f \leq$ 650MHz			1.6	ns
*t*sk(o)	Output Skew; NOTE 2, 3				30	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4				200	ps
t_R / t_F	Output Rise/Fall Time	20% to 80% @ 50MHz	250		700	ps
odc	Output Duty Cycle		45		55	%

All parameters measured at 500MHz unless noted otherwise.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.
Measured at output differential cross points.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions.
Using the same type of inputs on each device, the outputs are measured at the differential cross points.

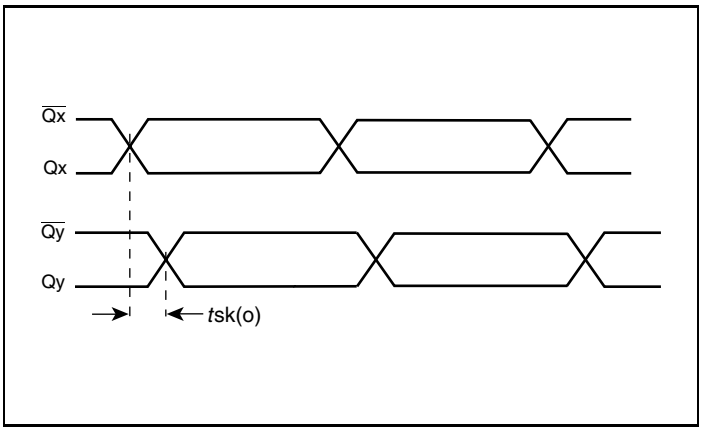
Parameter Measurement Information



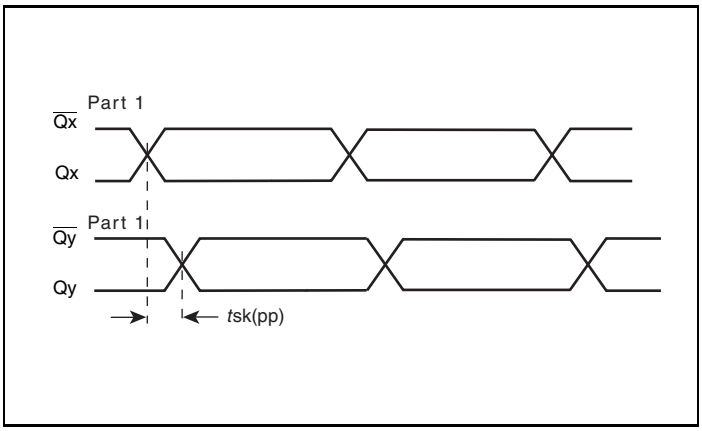
3.3V/1.8V Output Load AC Test Circuit



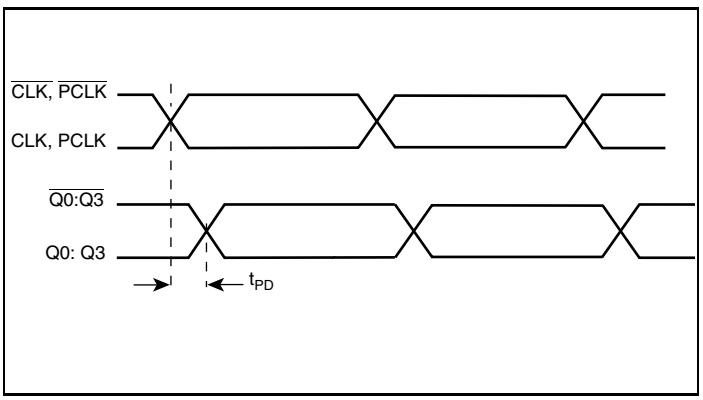
Differential Input Level



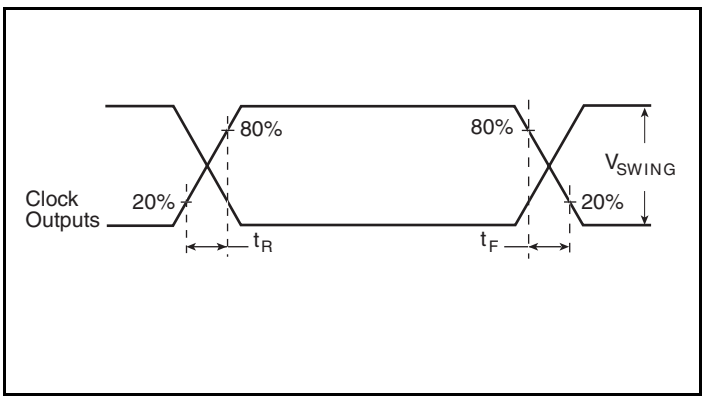
Output Skew



Part-to-Part Skew

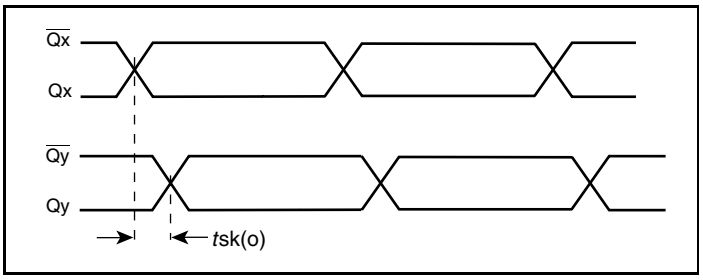


Propagation Delay



Output Rise/Fall Time

Parameter Measurement Information, continued



Output Duty Cycle/Pulse Width/Period

Application Information

Wiring the Differential Input to Accept Single Ended Levels

Figure 2 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

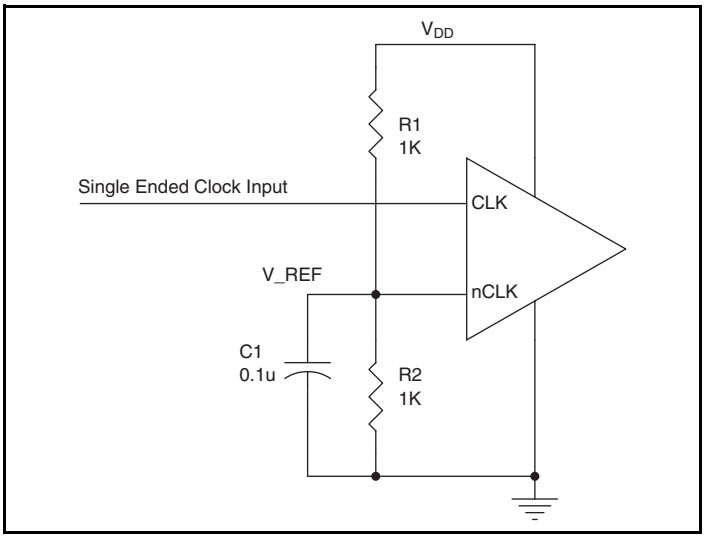


Figure 2. Single-Ended Signal Driving Differential Input

Differential Clock Input Interface

The CLK /$\overline{CLK}$ accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 3A to 3E* show interface examples for the HiPerClockS CLK/$\overline{CLK}$ input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 2A, the input termination applies for IDT HiPerClockS LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

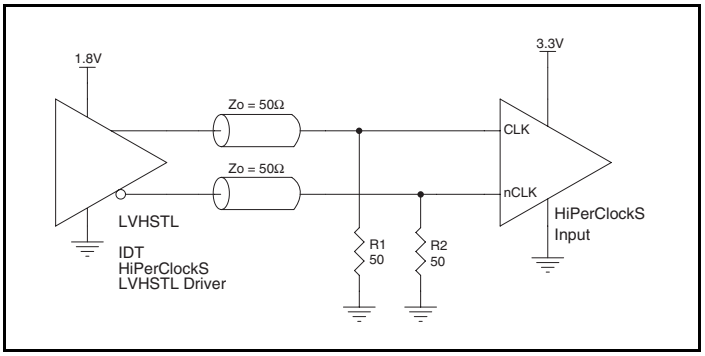


Figure 3A. HiPerClockS CLK/$\overline{CLK}$ Input Driven by an IDT HiPerClockS LVHSTLDriver

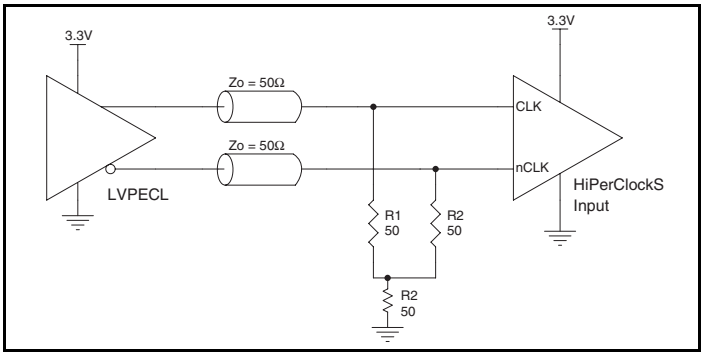


Figure 3B. HiPerClockS CLK/$\overline{CLK}$ Input Driven by a 3.3V LVPECL Driver

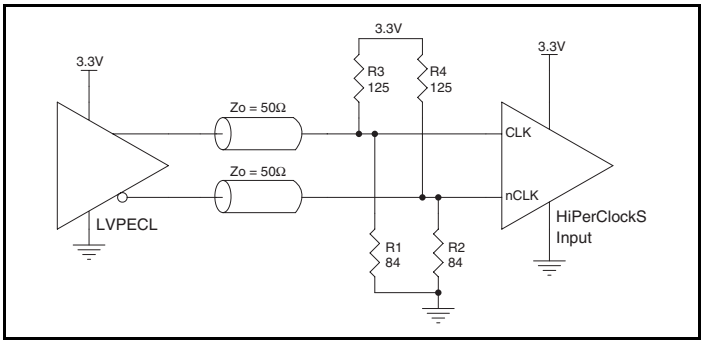


Figure 3C. HiPerClockS CLK/$\overline{CLK}$ Input Driven by a 3.3V LVPECL Driver

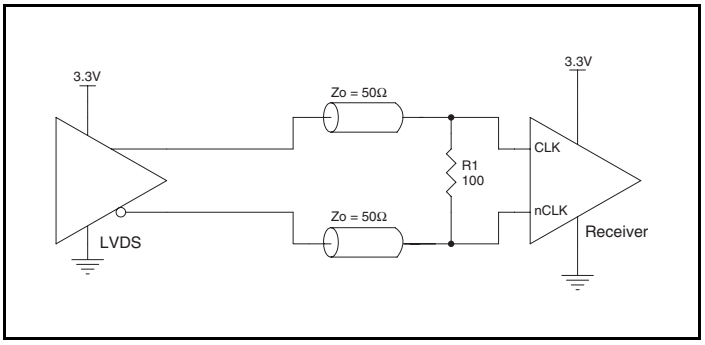


Figure 3D. HiPerClockS CLK/$\overline{CLK}$ Input Driven by a 3.3V LVDS Driver

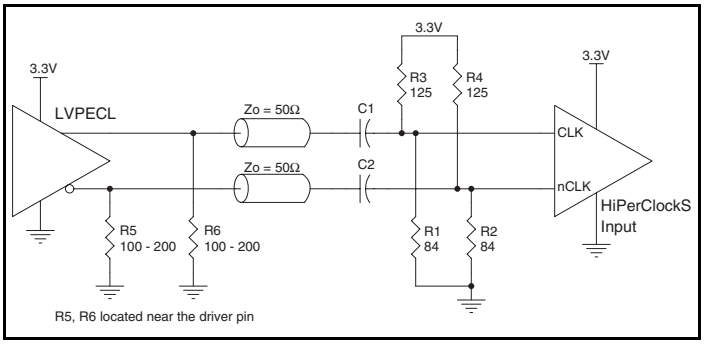


Figure 3E. HiPerClockS CLK/$\overline{CLK}$ Input Driven by a 3.3V LVPECL Driver with AC Couple

LVPECL Clock Input Interface

The PCLK /$\overline{\text{PCLK}}$ accepts LVPECL, CML, SSTL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 4A to 4E* show interface examples for the HiPerClockS PCLK/$\overline{\text{PCLK}}$ input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

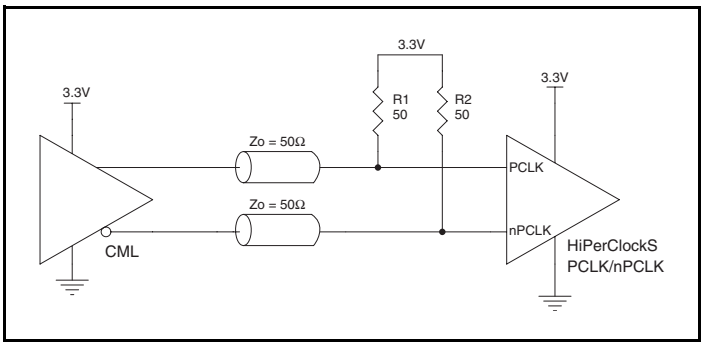


Figure 4A. HiPerClockS PCLK/$\overline{\text{PCLK}}$ Input Driven by an Open Collector CML Driver

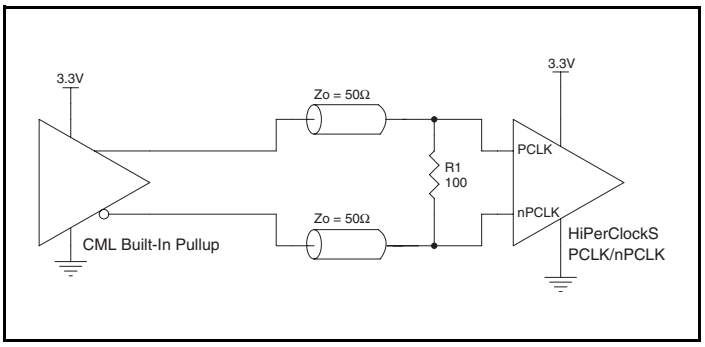


Figure 4B. HiPerClockS PCLK/$\overline{\text{PCLK}}$ Input Driven by a Built-In Pullup CML Driver

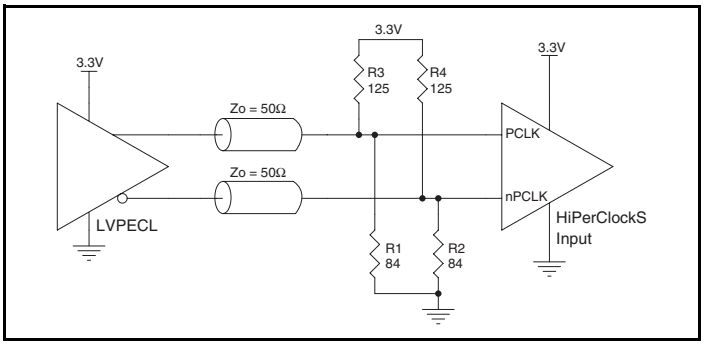


Figure 4C. HiPerClockS PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver

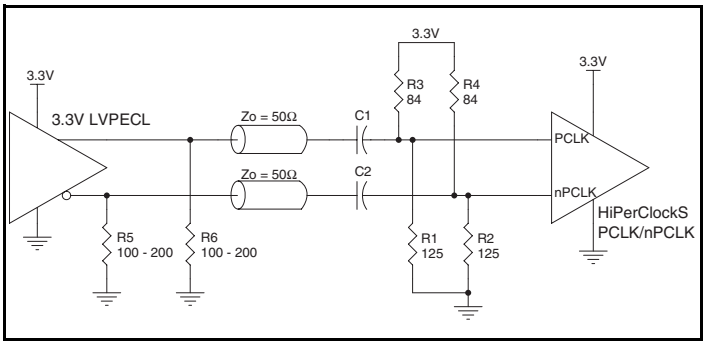


Figure 4D. HiPerClockS PCLK/$\overline{\text{PCLK}}$ Input Driven by a 3.3V LVPECL Driver with AC Couple

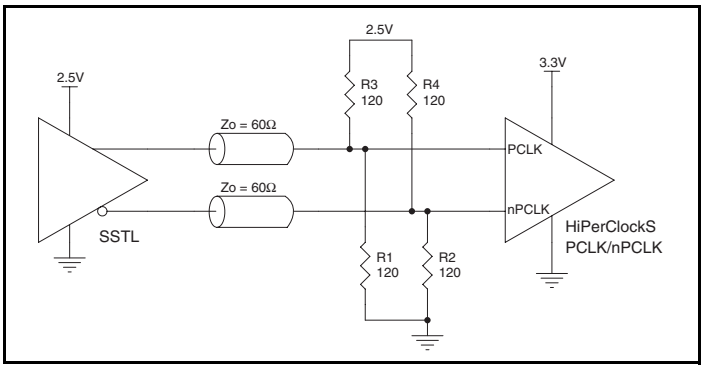


Figure 4E. HiPerClockS PCLK/$\overline{\text{PCLK}}$ Input Driven by an SSTL Driver

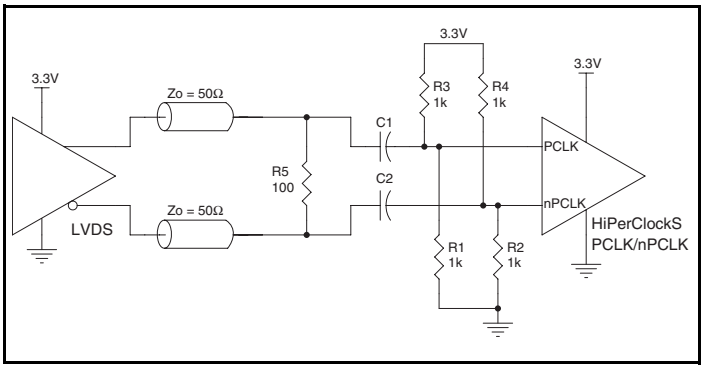


Figure 4F. HiPerClockS PCLK/$\overline{\text{PCLK}}$ Input Driven by a 3.3V LVDS Driver

Recommendations for Unused Input and Output Pins

Inputs:

LVCMOS Control Pins:

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

CLK/$\overline{\text{CLK}}$ Input:

For applications not requiring the use of the differential input, both CLK and $\overline{\text{CLK}}$ can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

PCLK/$\overline{\text{PCLK}}$ Input:

For applications not requiring the use of a differential input, both the PCLK and $\overline{\text{PCLK}}$ pins can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from PCLK to ground.

Outputs:

HSTL Outputs

All unused LVHSTL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Schematic Example

Figure 5 shows a schematic example of the ICS8523. In this example, the input is driven by an IDT HiPerClockS HSTL driver. The decoupling capacitors should be physically located near the power pin. For ICS8523, the unused clock outputs can be left floating.

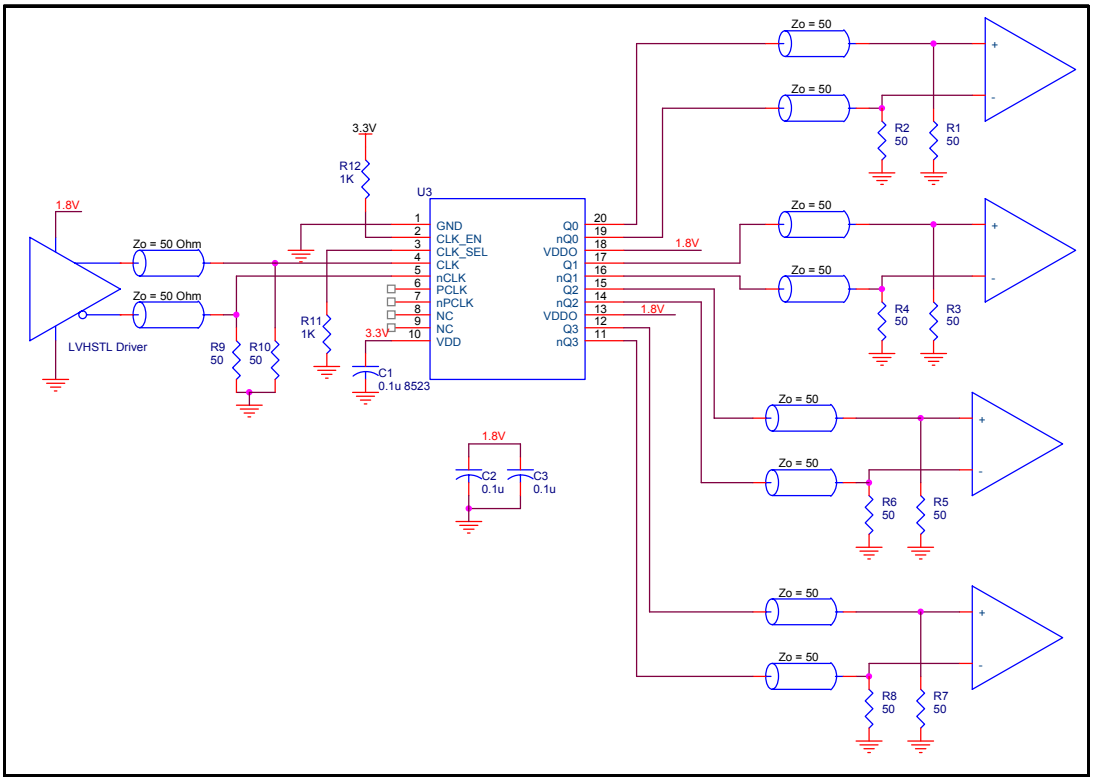


Figure 5. ICS8523 HSTL Buffer Schematic Example

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS8523.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS8523 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{DD\_MAX} * I_{DD\_MAX}$ = 3.465V * 50mA = **173.3mW**
- Power $(outputs)_{MAX}$ = **32.6mW/Loaded Output pair**
  If all outputs are loaded, the total power is 4 x 32.6mW = **130.4mW**

Total Power$_{\_MAX}$ (3.465V, with all outputs switching) = 173.3mW + 130.4mW = **303.7mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 66.6°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:

70°C + 0.304W * 66.6°C/W = 90.2°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (single layer or multi-layer).

Table 6. Thermal Resistance θ_{JA} for 20 Lead TSSOP, Forced Convection

θ_{JA} by Velocity			
Linear Feet per Minute	**0**	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	114.5°C/W	98.0°C/W	88.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	73.2°C/W	66.6°C/W	63.5°C/W

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

HSTL output driver circuit and termination are shown in *Figure 6.*

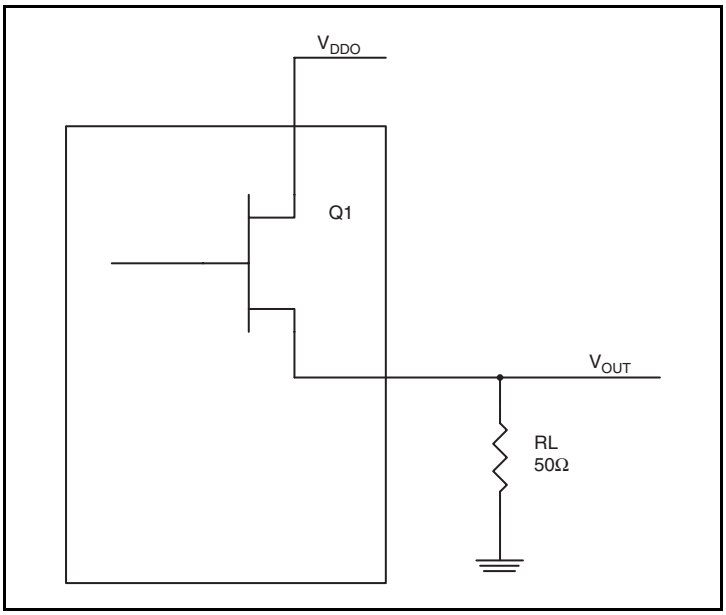


Figure 6. HSTL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load.

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = (V_{OH\_MAX}/R_L) * (V_{DDO\_MAX} - V_{OH\_MAX})$

$Pd\_L = (V_{OL\_MAX}/R_L) * (V_{DDO\_MAX} - V_{OL\_MAX})$

Pd_H = (0.9V/50Ω) * (2V - 0.9V) = **19.8mW**

Pd_L = (0.4V/50Ω) * (2V - 0.4V) = **12.8mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **32.6mW**

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 20 Lead TSSOP

θ_{JA} by Velocity			
Linear Feet per Minute	**0**	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	114.5°C/W	98.0°C/W	88.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	73.2°C/W	66.6°C/W	63.5°C/W

Transistor Count

The transistor count for ICS8523 is: 472

Package Outline and Package Dimension

Package Outline - G Suffix for 20 Lead TSSOP

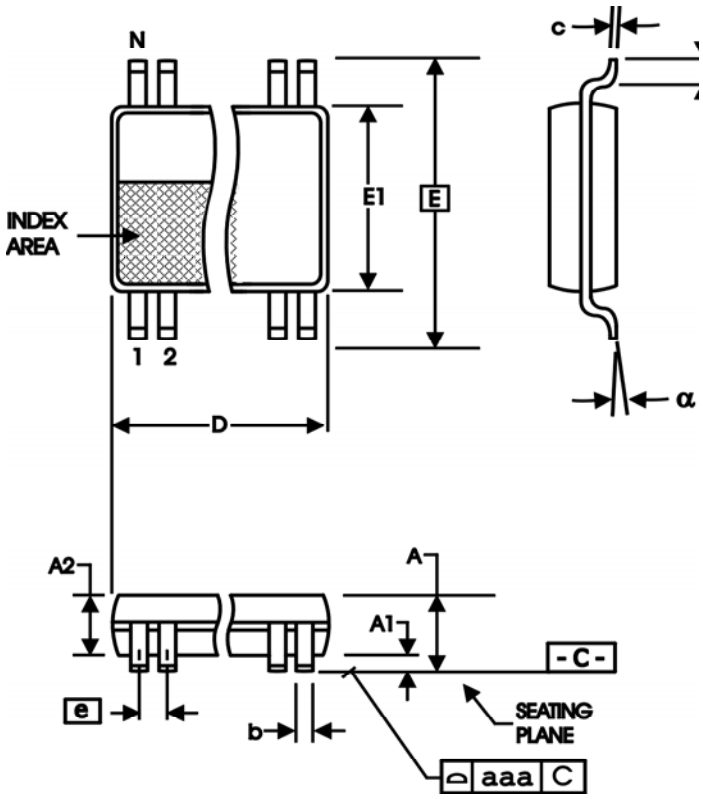


Table 7. Package Dimensions

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	20	
A		1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	6.40	6.60
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
α	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

Ordering Information

Table 8. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8523CG	ICS8523CG	20 Lead TSSOP	Tube	0°C to 70°C
8523CGT	ICS8523CG	20 Lead TSSOP	2500 Tape & Reel	0°C to 70°C
8523CGLF	ICS8523CGLF	“Lead-Free” 20 Lead TSSOP	Tube	0°C to 70°C
8523CGLFT	ICS8523CGLF	“Lead-Free” 20 Lead TSSOP	2500 Tape & Reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Revision History Sheet

Rev	Table	Page	Description of Change	Date
B	T4D T5	5 5	HSTL table - added V_{SWING} row to HSTL DC Characteristics Table. AC Characteristics table - t_{PD} row, added value of 1.3ns to Min.; changed Max. from 2.0ns to 1.6ns.	7/31/01
B		3	Updated Figure 1, CLK_EN Timing Diagram.	10/17/01
B		3	Updated Figure 1, CLK_EN Timing Diagram.	11/2/01
C	T5	5	AC Characteristics table - t_{PD} row, changed Min. from 1.3ns to 1.0ns. tsk(pp) row, changed Max. from 150ps to 200ps.	1/11/02
C		1	Revised Features section, Bullet 1,6 - took out 1.8V	5/6/02
C		8-10	In the Application Information section, added Schematic Examples.	10/25/02
C	T2 T4D 	2 4 5 11 - 12	Pin Characteristics Table - changed C_{IN} 4pF max. to 4pF typical. Absolute Maximum Ratings - changed Output rating. HSTL DC Characteristics Table - changed V_{OH} 1V min. to 0.9V min. Power Considerations - changed Total Power Dissipation to reflect V_{OH} change. Calculations changed due to new Total Power Dissipation. Changed LVHSTL to HSTL throughout data sheet.	6/20/03
C	 T9	1 9 15	Features section - added Lead-Free bullet. Updated LVPECL Clock Input Interface section. Added Lead-Free marking to Ordering Information table.	9/13/04
C	T8	16	Ordering Information Table - in the *Part/Order Number* and *Marking* columns, changed die revision from “B” to “C”.	3/2/07
D	T5	6	AC Characteristics Table - changed t_R/t_F minimum from 300ps to 250ps.	3/13/07

Innovate with IDT and accelerate your future networks. Contact:

www.IDT.com

For Sales
800-345-7015
408-284-8200
Fax: 408-284-2775

For Tech Support
netcom@idt.com
480-763-2056

Corporate Headquarters
Integrated Device Technology, Inc.
6024 Silver Creek Valley Road
San Jose, CA 95138
United States
800 345 7015
+408 284 8200 (outside U.S.)

Asia Pacific and Japan
Integrated Device Technology
Singapore (1997) Pte. Ltd.
Reg. No. 199707558G
435 Orchard Road
#20-03 Wisma Atria
Singapore 238877
+65 6 887 5505

Europe
IDT Europe, Limited
321 Kingston Road
Leatherhead, Surrey
KT22 7TU
England
+44 (0) 1372 363 339
Fax: +44 (0) 1372 378851

www.IDT.com