LOW SKEW, 1-TO-4 MULTIPLEXED DIFFERENTIAL/ LVCMOS-TO-LVCMOS/LVTTL FANOUT BUFFER

ICS8305

General Description

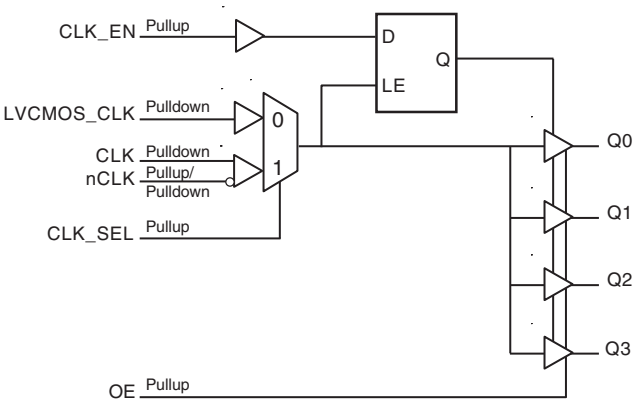
The ICS8305 is a low skew, 1-to-4, Differential/ LVCMOS-to-LVCMOS/LVTTL Fanout Buffer and a member of the HiPerClockS™family of High Performance Clock Solutions from IDT. The ICS8305 has selectable clock inputs that accept either differential or single ended input levels. The clock enable is internally synchronized to eliminate runt pulses on the outputs during asynchronous assertion/deassertion of the clock enable pin. Outputs are forced LOW when the clock is disabled. A separate output enable pin controls whether the outputs are in the active or high impedance state.

Guaranteed output and part-to-part skew characteristics make the ICS8305 ideal for those applications demanding well defined performance and repeatability.

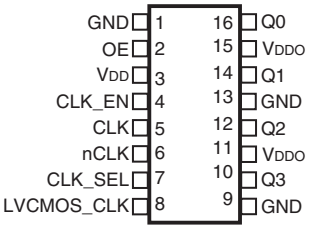
Features

- Four LVCMOS / LVTTL outputs, 7Ω output impedance
- Selectable differential or LVCMOS / LVTTL clock inputs
- CLK, nCLK pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, HCSL, SSTL
- LVCMOS_CLK supports the following input types: LVCMOS, LVTTL
- Maximum output frequency: 350MHz
- Output skew: 35ps (maximum)
- Part-to-part skew: 700ps (maximum)
- Additive phase jitter, RMS: 0.04ps (typical)
- Power supply modes:
  Core/Output
  3.3V/3.3V
  3.3V/2.5V
  3.3V/1.8V
  3.3V/1.5V
- 0°C to 70°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

Block Diagram



Pin Assignment



ICS8305

16-Lead TSSOP
4.4mm x 3.0mm x 0.925mm
package body
G Package

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 9, 13	GND	Power		Power supply ground
2	OE	Input	Pullup	Output enable. When LOW, outputs are in HIGH impedance state. When HIGH, outputs are active. LVCMOS/LVTTL interface levels.
3	V_{DD}	Power		Power supply pin.
4	CLK_EN	Input	Pullup	Synchronizing clock enable. When LOW, the output clocks are disabled. When HIGH, output clocks are enabled. LVCMOS/LVTTL interface levels.
5	CLK	Input	Pulldown	Non-inverting differential clock input.
6	nCLK	Input	Pullup/ Pulldown	Inverting differential clock input. VDD/2 default when left floating.
7	CLK_SEL	Input	Pullup	Clock select input. When HIGH, selects CLK, nCLK inputs. When LOW, selects LVCMOS_CLK input. LVCMOS/LVTTL interface levels.
8	LVCMOS_CLK	Input	Pulldown	Single-ended clock input. LVCMOS/LVTTL interface levels.
10, 12, 14, 16	Q3, Q2, Q1, Q0	Output		Single-ended clock outputs. 7Ω output impedance. LVCMOS/LVTTL interface levels.
11, 15	V_{DDO}	Power		Output supply pins.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
C_{PD}	Power Dissipation Capacitance (per output)			11		pF
R_{OUT}	Output Impedance			7		Ω

Function Tables

Table 3. Control Input Function Table

Inputs				Outputs
OE	**CLK_EN**	**CLK_SEL**	**Selected Source**	**Q0:Q3**
1	0	0	LVCMOS_CLK	Disabled; Low
1	0	1	CLK/nCLK	Disabled; Low
1	1	0	LVCMOS_CLK	Enabled
1	1	1	CLK/nCLK	Enabled
0	X	X		Hi-Z

After CLK_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock edge as shown in Figure 1.

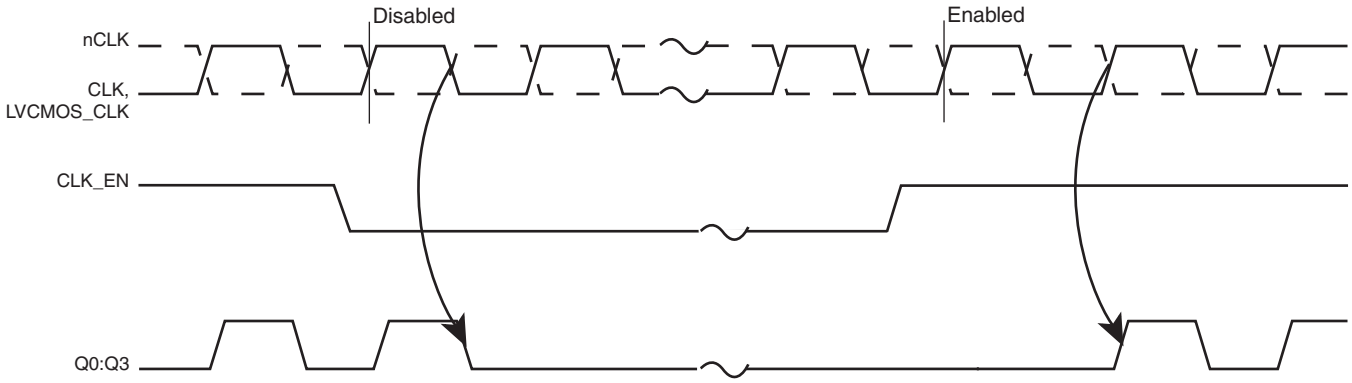


Figure 1. CLK_EN Timing Diagram

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, V_O	-0.5V to V_{DDO}+ 0.5V
Package Thermal Impedance, θ_{JA}	89°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{DD} = 3.3V±5%, V_{DDO} = 3.3V±5% or 2.5V±5% or 1.8V±0.5V or 1.5V±5%, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
			2.375	2.5	2.625	V
			1.65	1.8	1.95	V
			1.425	1.5	1.575	V
I_{DD}	Power Supply Current				21	mA
I_{DDO}	Output Supply Current				5	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, T_A = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	CLK_EN, CLK_SEL, OE		2		V_{DD} + 0.3	V
		LVCMOS_CLK		2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	CLK_EN, CLK_SEL, OE		-0.3		0.8	V
		LVCMOS_CLK		-0.3		1.3	V
I_{IH}	Input High Current	CLK_EN, CLK_SEL, OE	V_{DD} = V_{IN} = 3.465V			5	µA
		LVCMOS_CLK	V_{DD} = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	CLK_EN, CLK_SEL, OE	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
		LVCMOS_CLK	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
V_{OH}	Output High Voltage; NOTE 1		V_{DDO} = 3.3V ± 5%	2.6			V
			V_{DDO} = 2.5V ± 5%	1.8			V
			V_{DDO} = 1.8V ± 0.15V	1.5			V
			V_{DDO} = 1.5V ± 5%	V_{DDO} - 0.3			V
V_{OL}	Output Low Voltage; NOTE 1		V_{DDO} = 3.3V ± 5%			0.5	V
			V_{DDO} = 2.5V ± 5%			0.5	V
			V_{DDO} = 1.8V ± 0.15V			0.4	V
			V_{DDO} = 1.5V ± 5%			0.35	V
I_{OZL}	Output Hi-Z Current Low			-5			µA
I_{OZH}	Output Hi-Z Current High					5	µA

NOTE 1: Outputs terminated with 50Ω to V_{DDO}/2. See Parameter Measurement Information, *Output Load Test Circuit diagrams.*

Table 4C. Differential DC Characteristics, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	nCLK	V_{DD} = V_{IN} = 3.465V			150	µA
		CLK	V_{DD} = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	nCLK	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
		CLK	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
V_{PP}	Peak-to-Peak Voltage; NOTE 1			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 0.5		V_{DD} – 0.85	V

NOTE 1: V_{IL} should not be less than -0.3V.
NOTE 2: Common mode input voltage is defined as V_{IH}.

AC Electrical Characteristics

Table 5A. AC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = 0°C$ to $70°C$

Parameter	Symbol		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency					350	MHz
tp_{LH}	Propagation Delay, Low to High	LVCMOS_CLK; NOTE 1A CLK/nCLK; NOTE 1B		1.75		2.75	ns
*t*sk(o)	Output Skew; NOTE 2, 6		Measured on the Rising Edge			35	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 6					700	ps
tjit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section, NOTE 5				0.04		ps
t_R / t_F	Output Rise/Fall Time; NOTE 4		20% to 80%	100		700	ps
odc	Output Duty Cycle		Ref = CLK/nCLK	45		55	%
			Ref = LVCMOS_CLK, $f \leq 300MHz$	45		55	%
t_{EN}	Output Enable Time; NOTE 4					5	ns
t_{DIS}	Output Disable Time; NOTE 4					5	ns

All parameters measured at $f \leq 350MHz$ unless noted otherwise.
NOTE 1A: Measured from the $V_{DD}/2$ of the input to $V_{DDO}/2$ of the output.
NOTE 1B: Measured from the differential input crossing point to $V_{DDO}/2$ of the output.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 3: Defined as skew between outputs on different devices operating a the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at $V_{DDO}/2$.
NOTE 4: These parameters are guaranteed by characterization. Not tested in production.
NOTE 5: Driving only one input clock.
NOTE 6: This parameter is defined in accordance with JEDEC Standard 65.

Table 5B. AC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 2.5V \pm 5\%$, $T_A = 0°C$ to $70°C$

Parameter	Symbol		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency					350	MHz
tp_{LH}	Propagation Delay, Low to High	LVCMOS_CLK; NOTE 1A CLK/nCLK; NOTE 1B		1.8		2.9	ns
*t*sk(o)	Output Skew; NOTE 2, 6		Measured on the Rising Edge			35	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 6					800	ps
tjit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section, NOTE 5				0.04		ps
t_R / t_F	Output Rise/Fall Time; NOTE 4		20% to 80%	100		700	ps
odc	Output Duty Cycle		Ref = CLK/nCLK	44		56	%
			Ref = LVCMOS_CLK, $f \leq 300MHz$	44		56	%
t_{EN}	Output Enable Time; NOTE 4					5	ns
t_{DIS}	Output Disable Time; NOTE 4					5	ns

For NOTES, see Table 5A above.

Table 5C. AC Characteristics, V_{DD} = 3.3V ± 5%, V_{DDO} = 1.8V ± 0.15V, T_A = 0°C to 70°C

Parameter	Symbol		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency					350	MHz
tp_{LH}	Propagation Delay, Low to High	LVCMOS_CLK; NOTE 1A CLK/nCLK; NOTE 1B		1.95		3.65	ns
*t*sk(o)	Output Skew; NOTE 2, 6		Measured on the Rising Edge			35	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 6					900	ps
tjit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section, NOTE 5				0.04		ps
t_R / t_F	Output Rise/Fall Time; NOTE 4		20% to 80%	100		700	ps
odc	Output Duty Cycle		Ref = CLK/nCLK	44		56	%
			Ref = LVCMOS_CLK, $f \leq$ 300MHz	44		56	%
t_{EN}	Output Enable Time; NOTE 4					5	ns
t_{DIS}	Output Disable Time; NOTE 4					5	ns

All parameters measured at $f \leq$ 350MHz unless noted otherwise.
NOTE 1A: Measured from the V_{DD}/2 of the input to V_{DDO}/2 of the output.
NOTE 1B: Measured from the differential input crossing point to V_{DDO}/2 of the output.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at V_{DDO}/2.
NOTE 3: Defined as skew between outputs on different devices operating a the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at V_{DDO}/2.
NOTE 4: These parameters are guaranteed by characterization. Not tested in production.
NOTE 5: Driving only one input clock.
NOTE 6: This parameter is defined in accordance with JEDEC Standard 65.

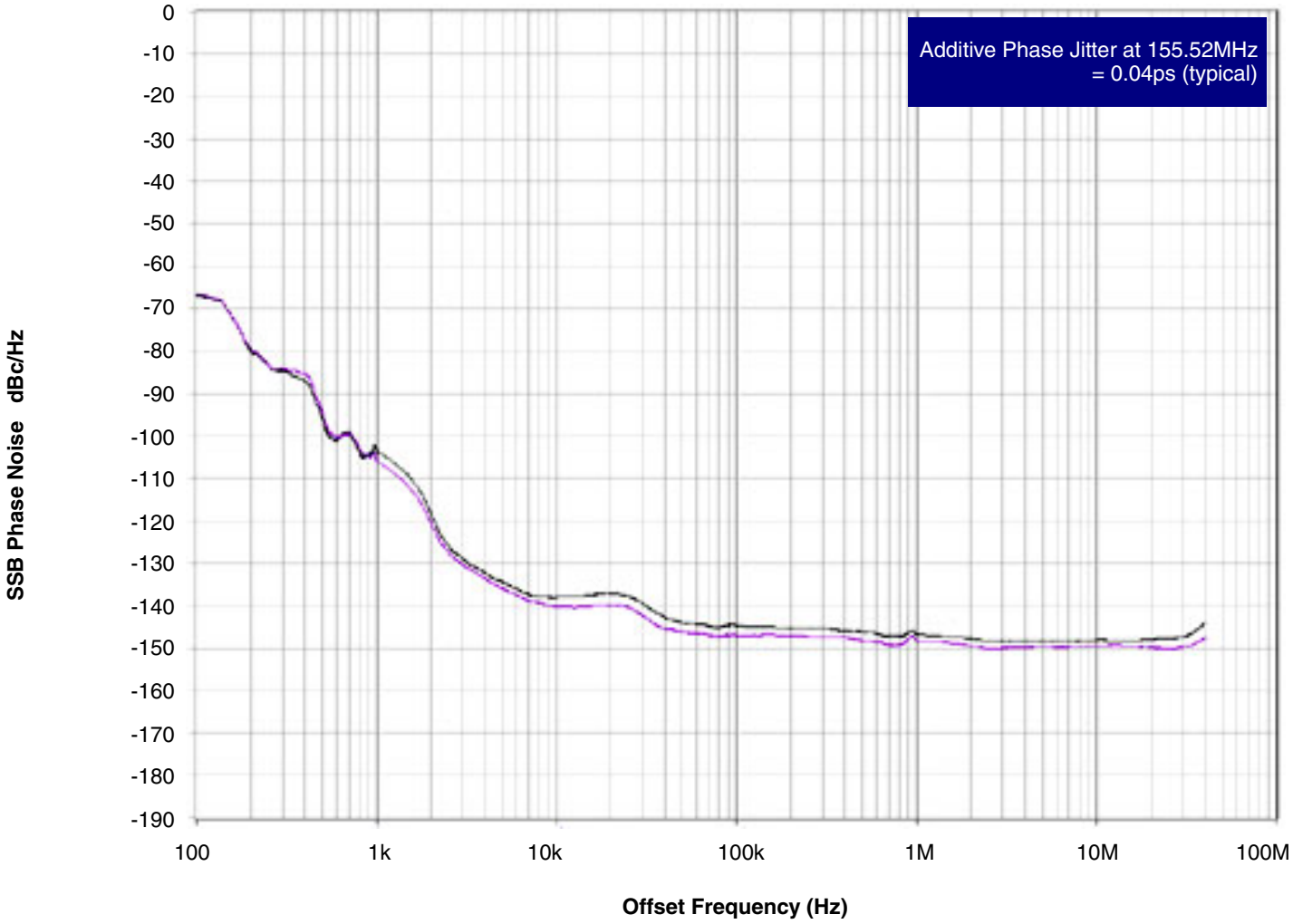
Table 5D. AC Characteristics, V_{DD} = 3.3V ± 5%, V_{DDO} = 1.5V ± 5%, T_A = 0°C to 70°C

Parameter	Symbol		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency					350	MHz
tp_{LH}	Propagation Delay, Low to High	LVCMOS_CLK; NOTE 1A CLK/nCLK; NOTE 1B		2		4	ns
*t*sk(o)	Output Skew; NOTE 2, 6		Measured on the Rising Edge			35	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 6					1	ns
tjit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section, NOTE 5				0.04		ps
t_R / t_F	Output Rise/Fall Time; NOTE 4		20% to 80%	200		900	ps
odc	Output Duty Cycle		$f \leq$ 166MHz	45		55	%
			$f >$ 166MHz	42		58	%
t_{EN}	Output Enable Time; NOTE 4					5	ns
t_{DIS}	Output Disable Time; NOTE 4					5	ns

For NOTES, see Table 5C above.

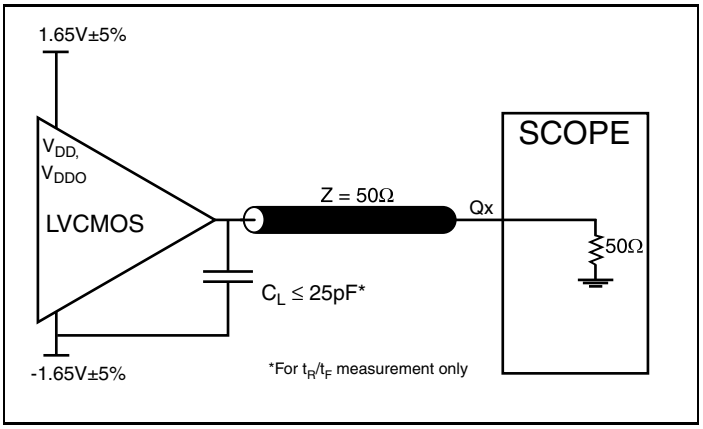
Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

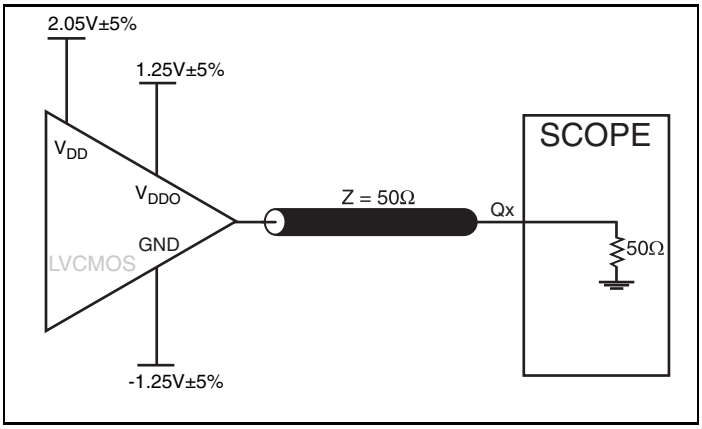


As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

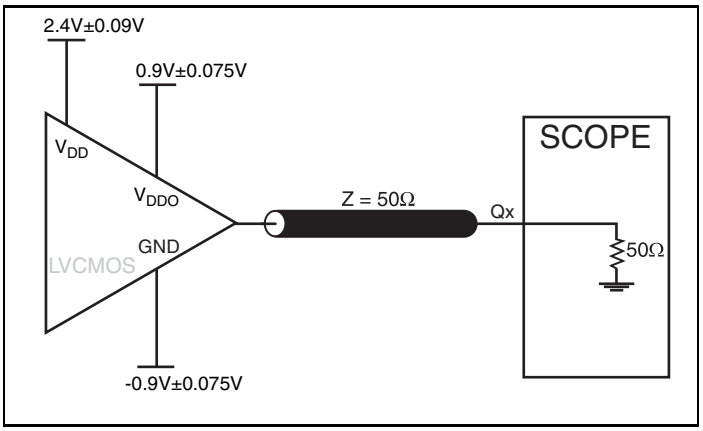
Parameter Measurement Information



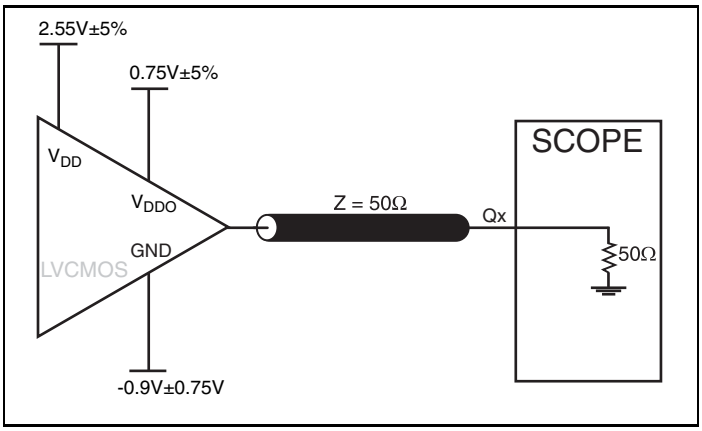
3.3V Core/3.3V LVCMOS Output Load AC Test Circuit



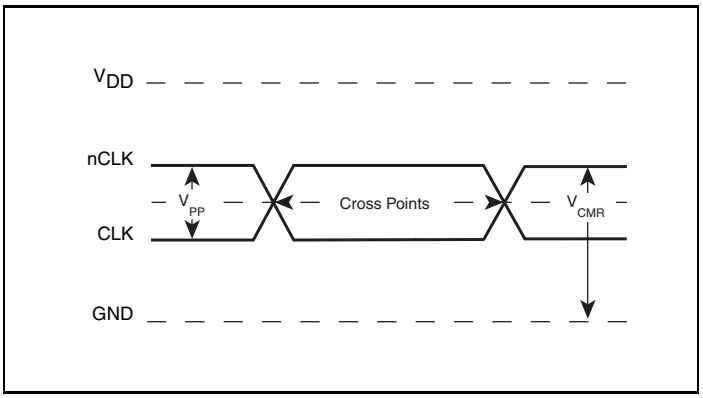
3.3V Core/2.5V LVCMOS Output Load AC Test Circuit



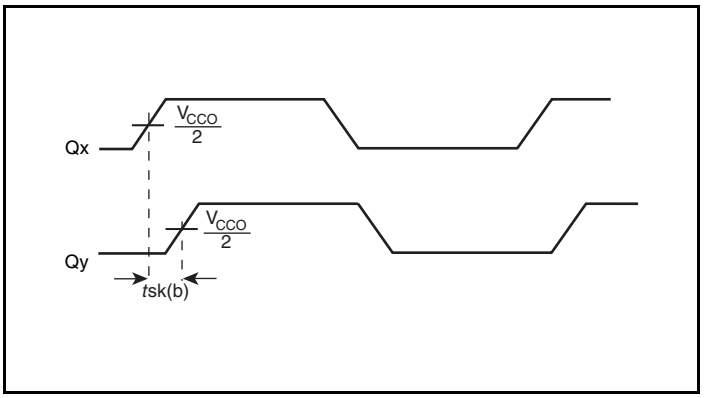
3.3V Core/1.8V LVCMOS Output Load AC Test Circuit



3.3V Core/1.5V LVCMOS Output Load AC Test Circuit

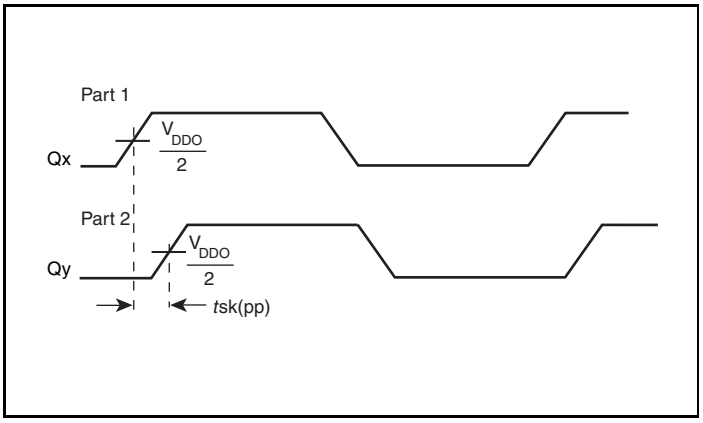


Differential Input Level

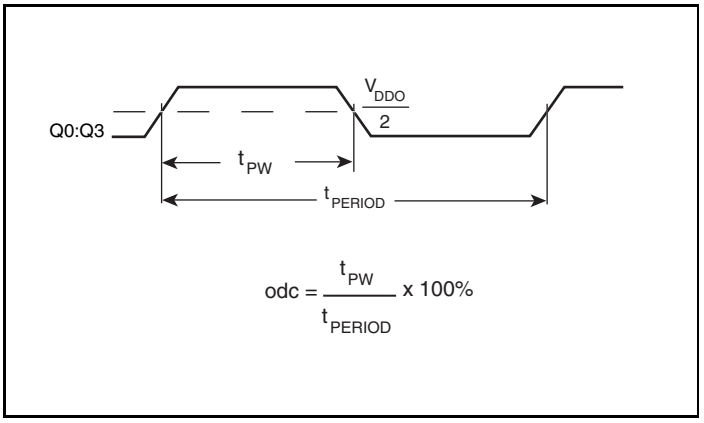


Output Skew

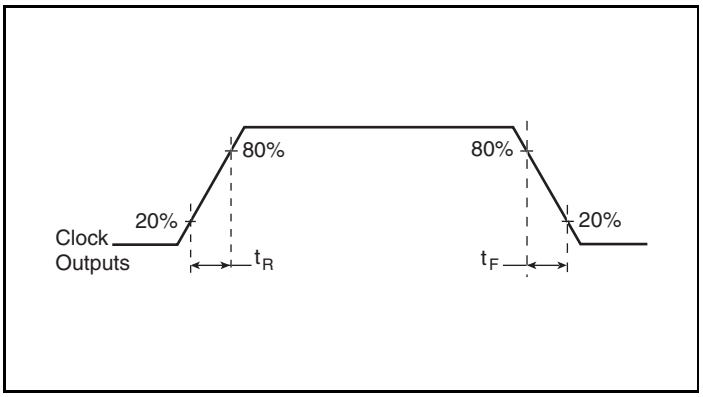
Parameter Measurement Information, continued



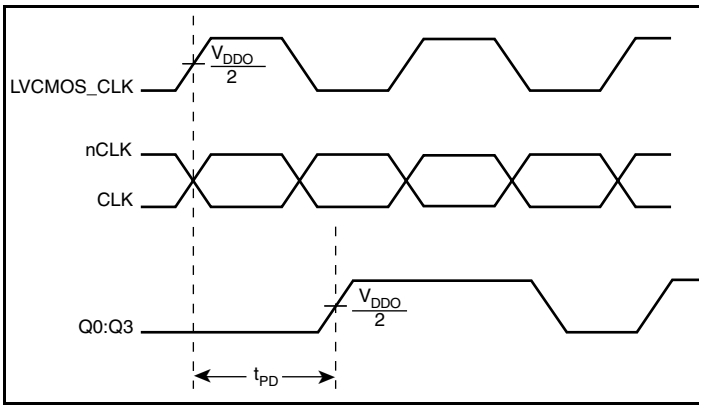
Part-to-Part Skew



Output Duty Cycle/Pulse Width/Period



Output Rise/Fall Time



Propagation Delay

Application Information

Recommendations for Unused Input and Output Pins

Inputs:

LVCMOS_CLK Input

For applications not requiring the use of a clock input, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the LVCMOS_CLK input to ground.

CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

LVCMOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVCMOS Outputs

All unused LVCMOS output can be left floating. There should be no trace attached.

Wiring the Differential Input to Accept Single Ended Levels

Figure 2 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

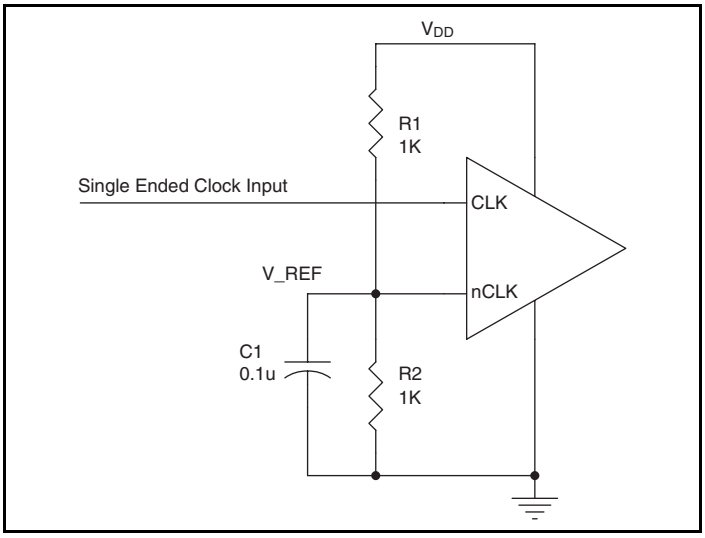


Figure 2. Single-Ended Signal Driving Differential Input

Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both signals must meet the V_{PP} and V_{CMR} input requirements. *Figures 3A to 3F* show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 3A, the input termination applies for IDT HiPerClockS open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

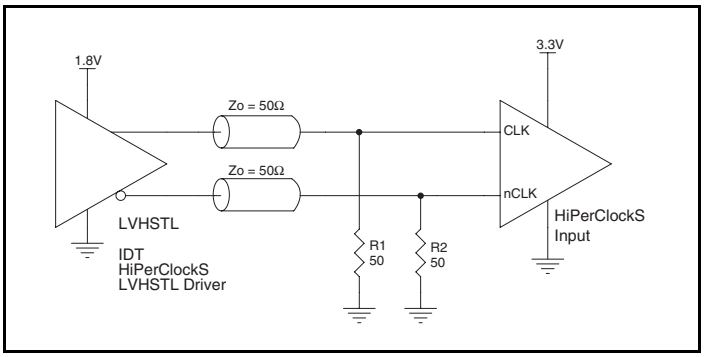


Figure 3A. HiPerClockS CLK/nCLK Input Driven by an IDT Open Emitter HiPerClockS LVHSTL Driver

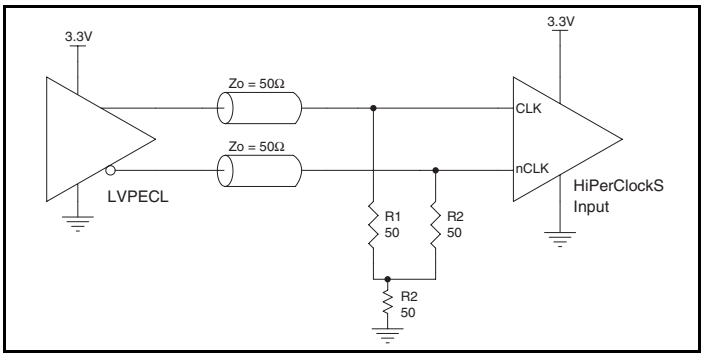


Figure 3B. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVPECL Driver

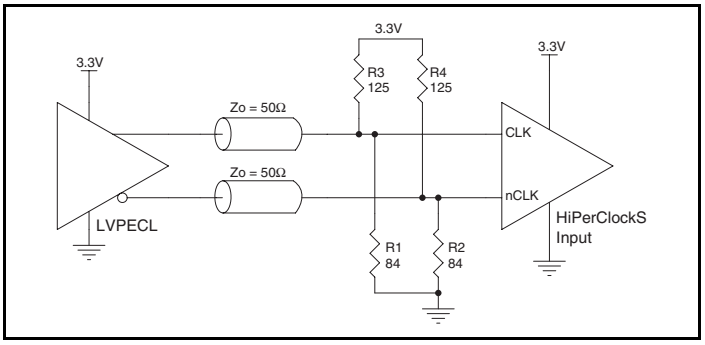


Figure 3C. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVPECL Driver

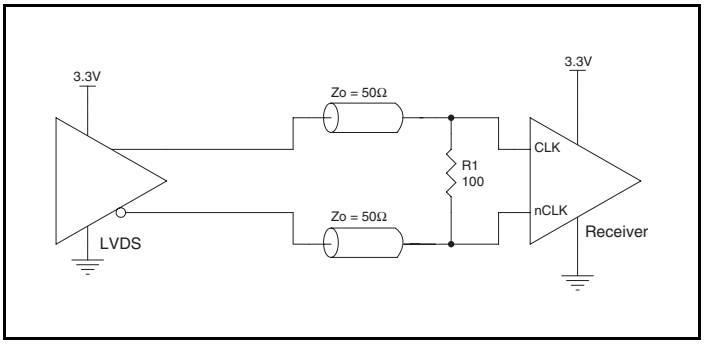


Figure 3D. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVDS Driver

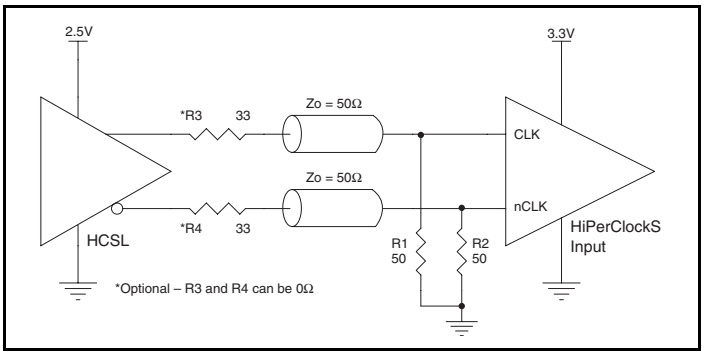


Figure 3E. HiPerClockS CLK/nCLK Input Driven by a 3.3V HCSL Driver

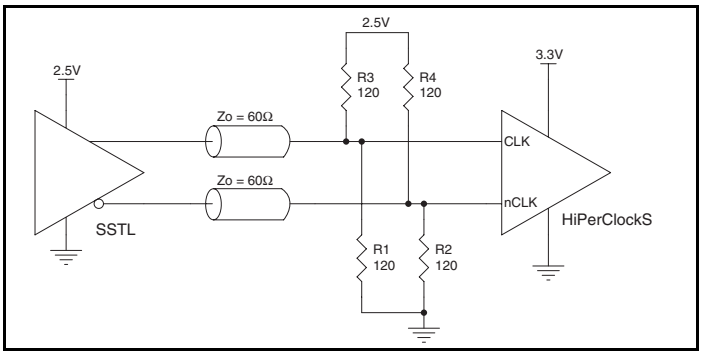


Figure 3F. HiPerClockS CLK/nCLK Input Driven by a 2.5V SSTL Driver

Schematic Example

This application note provides general design guide using ICS8305 LVCMOS buffer. *Figure 4* shows a schematic example of the ICS8305 LVCMOS clock buffer. In this example, the input is driven by an LVCMOS driver. CLK_EN is set at logic low to select LVCMOS_CLK input.

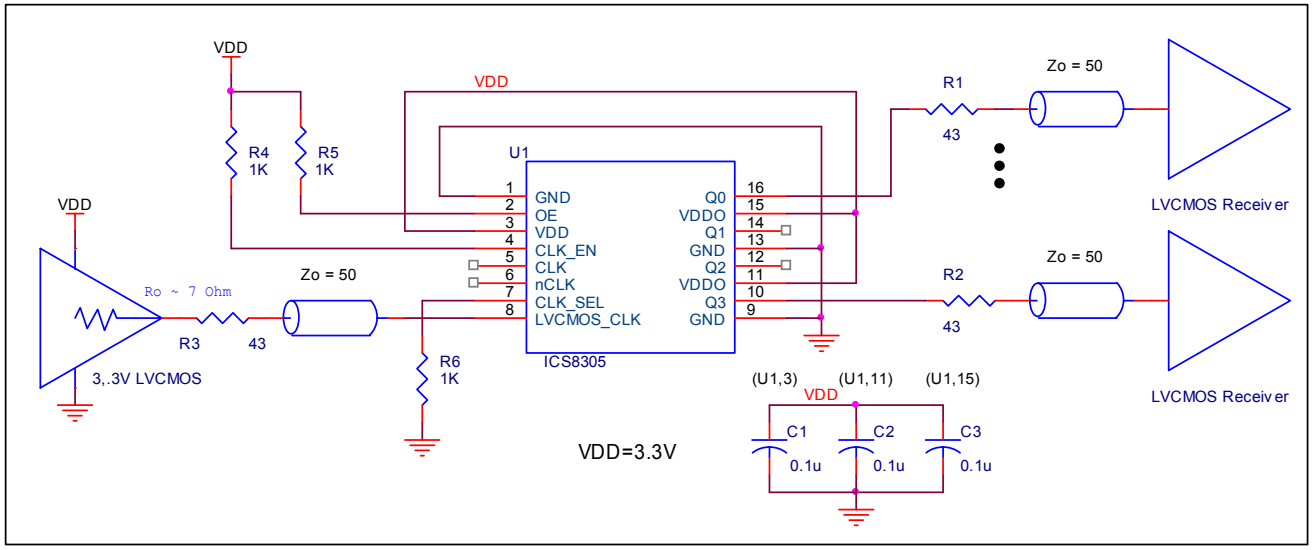


Figure 4. ICS8305 LVCMOS Clock Output Buffer Schematic Example

Reliability Information

Table 6. θ_{JA} vs. Air Flow Table for a 16 Lead TSSOP

θ_{JA} vs. Air Flow			
Linear Feet per Minute	**0**	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	137.1°C/W	118.2°C/W	106.8°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	89.0°C/W	81.8°C/W	78.1°C/W

NOTE: Most modern PCB design use multi-layered boards. The data in the second row pertains to most designs.

Transistor Count

The transistor count for ICS8305: 459

Package Outline and Package Dimensions

Package Outline - G Suffix for 16 Lead TSSOP

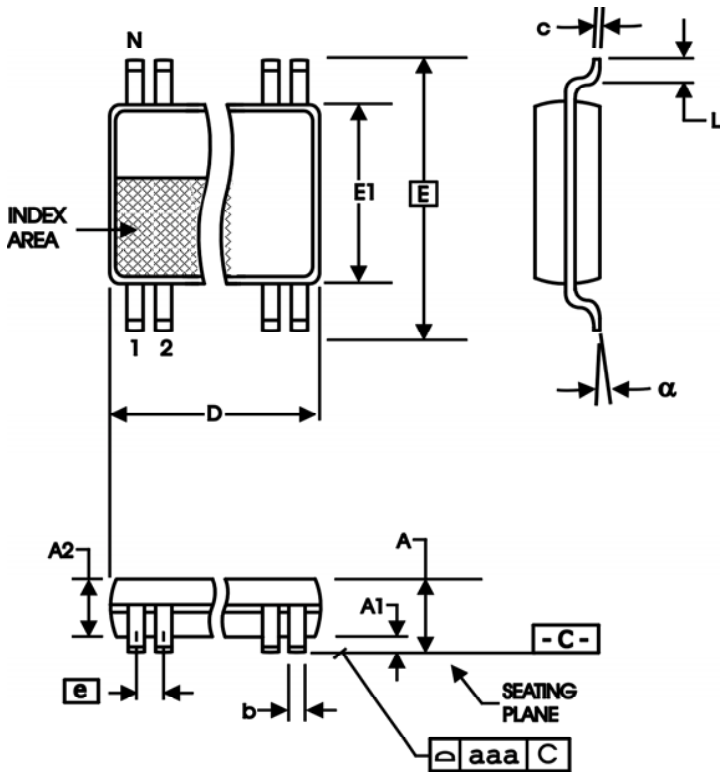


Table 7. Package Dimensions for 16 Lead TSSOP

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	16	
A		1.20
A1	0.5	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
α	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

Ordering Information

Table 8. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8305AG	8305AG	16 Lead TSSOP	Tube	0°C to 70°C
8305AGT	8305AG	16 Lead TSSOP	2500 Tape & Reel	0°C to 70°C
8305AGLF	8305AGLF	“Lead-Free” 16 Lead TSSOP	Tube	0°C to 70°C
8305AGLFT	8305AGLF	“Lead-Free” 16 Lead TSSOP	2500 Tape & Reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A	T8	14	Ordering Information table - corrected Part/Order Number typo from ICS88305AGT to ICS8305AGT.	1/20/04
B	T5A - T5C	5 & 6 7	Added Additive Phase Jitter to AC Characteristics Tables. Added Additive Phase Jitter Section.	2/26/04
B	T1	2	Pin Description Table - corrected CLK_EN description.	12/6/04
C	 T4A T4B T5D T8	1 4 4 7 10 11 16	Features Section - added 1.5V output to Supply Mode bullet and added Lead-Free buttlet. Power Supply DC Characteristics Table - added V_{DDO} 1.5V. LVCMOS DC Characteristics Table - added V_{OH}/V_{OL} 1.5V. Added 3.3V/1.5V AC Characteristics Table. Added 3.3V/1.5V Output Load AC Test Circuit Drawing. Added Recommendations for Unused Input and Output Pins. Added Lead-Free part number.	11/17/05
C	T8	15	Ordering Information Table - added lead-free marking. Corrected non-lead free marking from ICS8305AG to 8305AG.	2/22/08

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