

## General Description



The ICS8543I is a low skew, high performance 1-to-4 Differential-to-LVDS Clock Fanout Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from IDT. Utilizing Low Voltage Differential Signaling (LVDS) the ICS8543I

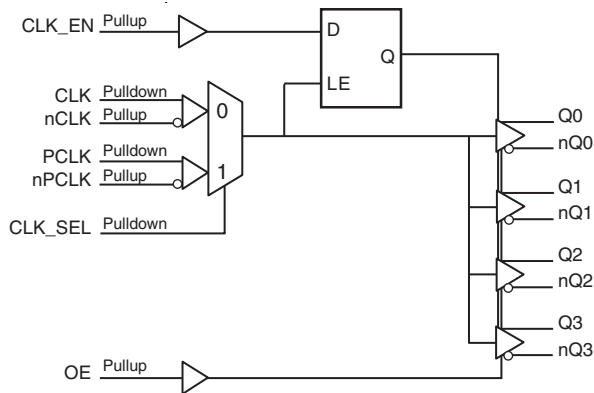
provides a low power, low noise, solution for distributing clock signals over controlled impedances of 100Ω. The ICS8543I has two selectable clock inputs. The CLK, nCLK pair can accept most standard differential input levels. The PCLK, nPCLK pair can accept LVPECL, CML, or SSTL input levels. The clock enable is internally synchronized to eliminate runt pulses on the outputs during asynchronous assertion/deassertion of the clock enable pin.

Guaranteed output and part-to-part skew characteristics make the ICS8543I ideal for those applications demanding well defined performance and repeatability.

## Features

- Four differential LVDS output pairs
- Selectable differential CLK/nCLK or LVPECL clock inputs
- CLK/nCLK pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, SSTL, HCSSL
- PCLK/nPCLK pair can accept the following differential input levels: LVPECL, CML, SSTL
- Maximum output frequency: 650MHz
- Translates any single-ended input signals to LVDS levels with resistor bias on nCLK input
- Additive phase Jitter, RMS: 0.164ps (typical)
- Output skew: 40ps (maximum)
- Part-to-part skew: 600ps (maximum)
- Propagation delay: 2.6ns (maximum)
- Full 3.3V supply mode
- -40°C to 85°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

## Block Diagram



## Pin Assignment

|                 |    |    |                 |
|-----------------|----|----|-----------------|
| GND             | 1  | 20 | Q0              |
| CLK_EN          | 2  | 19 | nQ0             |
| CLK_SEL         | 3  | 18 | V <sub>DD</sub> |
| CLK             | 4  | 17 | Q1              |
| nCLK            | 5  | 16 | nQ1             |
| PCLK            | 6  | 15 | Q2              |
| nPCLK           | 7  | 14 | nQ2             |
| OE              | 8  | 13 | GND             |
| GND             | 9  | 12 | Q3              |
| V <sub>DD</sub> | 10 | 11 | nQ3             |

**ICS8543I**

**20-Lead TSSOP**

**6.5mm x 4.4mm x 0.925mm**

**package body**

**G Package**

**Top View**

**Table 1. Pin Descriptions**

| Number   | Name            | Type   |          | Description   |
|----------|-----------------|--------|----------|---|
| 1, 9, 13 | GND             | Power  |          | Power supply ground.  |
| 2        | CLK_EN          | Input  | Pullup   | Synchronizing clock enable. When HIGH, clock outputs follows clock input. When LOW, Qx outputs are forced low, nQx outputs are forced high. LVCMOS / LVTTTL interface levels. |
| 3        | CLK_SEL         | Input  | Pulldown | Clock select input. When HIGH, selects PCLK/nPCLK inputs. When LOW, selects CLK/nCLK inputs. LVCMOS / LVTTTL interface levels.  |
| 4        | CLK             | Input  | Pulldown | Non-inverting differential clock input.   |
| 5        | nCLK            | Input  | Pullup   | Inverting differential clock input.   |
| 6        | PCLK            | Input  | Pulldown | Non-inverting differential LVPECL clock input.  |
| 7        | nPCLK           | Input  | Pullup   | Inverting differential LVPECL clock input.  |
| 8        | OE              | Input  | Pullup   | Output enable. Controls enabling and disabling of outputs Q0/nQ0 through Q3/nQ3. LVCMOS/LVTTTL interface levels.  |
| 10, 18   | V <sub>DD</sub> | Power  |          | Positive supply pins.   |
| 11, 12   | nQ3, Q3         | Output |          | Differential output pair. LVDS interface levels.  |
| 14, 15   | nQ2, Q2         | Output |          | Differential output pair. LVDS interface levels.  |
| 16, 17   | nQ1, Q1         | Output |          | Differential output pair. LVDS interface levels.  |
| 19, 20   | nQ0, Q0         | Output |          | Differential output pair. LVDS interface levels.  |

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

**Table 2. Pin Characteristics**

| Symbol                | Parameter               | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------------|-------------------------|-----------------|---------|---------|---------|-------|
| C <sub>IN</sub>       | Input Capacitance       |                 |         | 4       |         | pF    |
| R <sub>PULLUP</sub>   | Input Pullup Resistor   |                 |         | 51      |         | kΩ    |
| R <sub>PULLDOWN</sub> | Input Pulldown Resistor |                 |         | 51      |         | kΩ    |

## Function Tables

Table 3A. Control Input Function Table

| Inputs |        |         |                 | Outputs       |                |
|--------|--------|---------|-----------------|---------------|----------------|
| OE     | CLK_EN | CLK_SEL | Selected Source | Q0:Q3         | nQ0:nQ3        |
| 0      | X      | X       |                 | Hi-Z          | Hi-Z           |
| 1      | 0      | 0       | CLK/nCLK        | Disabled; Low | Disabled; High |
| 1      | 0      | 1       | PCLK/nPCLK      | Disabled; Low | Disabled; High |
| 1      | 1      | 0       | CLK/nCLK        | Enabled       | Enabled        |
| 1      | 1      | 1       | PCLK/nPCLK      | Enabled       | Enabled        |

After CLK\_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock edge as shown in Figure 1. In the active mode, the state of the outputs are a function of the CLK/nCLK and PCLK/nPCLK inputs as described in Table 3B.

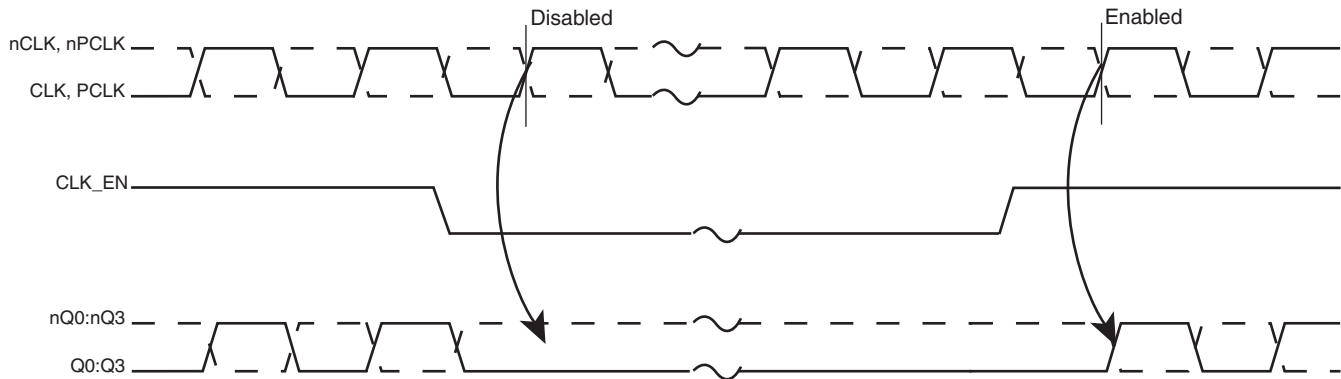


Figure 1. CLK\_EN Timing Diagram

Table 3B. Clock Input Function Table

| Inputs         |                | Outputs |         | Input to Output Mode         | Polarity      |
|----------------|----------------|---------|---------|------------------------------|---------------|
| CLK or PCLK    | nCLK or nPCLK  | Q[0:3]  | nQ[0:3] |                              |               |
| 0              | 1              | LOW     | HIGH    | Differential to Differential | Non-Inverting |
| 1              | 0              | HIGH    | LOW     | Differential to Differential | Non-Inverting |
| 0              | Biased; NOTE 1 | LOW     | HIGH    | Single-Ended to Differential | Non-Inverting |
| 1              | Biased; NOTE 1 | HIGH    | LOW     | Single-Ended to Differential | Non-Inverting |
| Biased; NOTE 1 | 0              | HIGH    | LOW     | Single-Ended to Differential | Inverting     |
| Biased; NOTE 1 | 1              | LOW     | HIGH    | Single-Ended to Differential | Inverting     |

NOTE 1: Please refer to the Application Information section, *Wiring the Differential Input to Accept Single-Ended Levels*.

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

| Item  | Rating                   |
|---|--------------------------|
| Supply Voltage, $V_{DD}$                              | 4.6V                     |
| Inputs, $V_I$   | -0.5V to $V_{DD} + 0.5V$ |
| Outputs, $I_O$<br>Continuous Current<br>Surge Current | 10mA<br>15mA             |
| Package Thermal Impedance, $\theta_{JA}$              | 73.2°C/W (0 lfpm)        |
| Storage Temperature, $T_{STG}$                        | -65°C to 150°C           |

## DC Electrical Characteristics

**Table 4A. Power Supply DC Characteristics,  $V_{DD} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

| Symbol   | Parameter               | Test Conditions | Minimum | Typical | Maximum | Units |
|----------|-------------------------|-----------------|---------|---------|---------|-------|
| $V_{DD}$ | Positive Supply Voltage |                 | 3.135   | 3.3     | 3.465   | V     |
| $I_{DD}$ | Power Supply Current    |                 |         |         | 50      | mA    |

**Table 4B. LVCMOS/LVTTL DC Characteristics,  $V_{DD} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

| Symbol   | Parameter          | Test Conditions | Minimum                        | Typical | Maximum        | Units   |
|----------|--------------------|-----------------|--------------------------------|---------|----------------|---------|
| $V_{IH}$ | Input High Voltage |                 | 2                              |         | $V_{DD} + 0.3$ | V       |
| $V_{IL}$ | Input Low Voltage  |                 | -0.3                           |         | 0.8            | V       |
| $I_{IH}$ | Input High Current | OE, CLK_EN      | $V_{DD} = V_{IN} = 3.465V$     |         | 5              | $\mu A$ |
|          |                    | CLK_SEL         | $V_{DD} = V_{IN} = 3.465V$     |         | 150            | $\mu A$ |
| $I_{IL}$ | Input Low Current  | OE, CLK_EN      | $V_{DD} = 3.465V, V_{IN} = 0V$ | -150    |                | $\mu A$ |
|          |                    | CLK_SEL         | $V_{DD} = 3.465V, V_{IN} = 0V$ | -5      |                | $\mu A$ |

**Table 4C. Differential DC Characteristics,  $V_{DD} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$** 

| Symbol    | Parameter                            | Test Conditions | Minimum                        | Typical | Maximum         | Units   |
|-----------|--------------------------------------|-----------------|--------------------------------|---------|-----------------|---------|
| $I_{IH}$  | Input High Current                   | CLK             | $V_{DD} = V_{IN} = 3.465V$     |         | 150             | $\mu A$ |
|           |                                      | nCLK            | $V_{DD} = V_{IN} = 3.465V$     |         | 5               | $\mu A$ |
| $I_{IL}$  | Input Low Current                    | CLK             | $V_{DD} = 3.465V, V_{IN} = 0V$ | -5      |                 | $\mu A$ |
|           |                                      | nCLK            | $V_{DD} = 3.465V, V_{IN} = 0V$ | -150    |                 | $\mu A$ |
| $V_{PP}$  | Peak-to-Peak Voltage; NOTE 1         |                 | 0.15                           |         | 1.3             | V       |
| $V_{CMR}$ | Common Mode Input Voltage; NOTE 1, 2 |                 | 0.5                            |         | $V_{DD} - 0.85$ | V       |

NOTE 1:  $V_{IL}$  should not be less than -0.3V.NOTE 2: Common mode input voltage is defined as  $V_{IH}$ .**Table 4D. LVPECL DC Characteristics,  $V_{DD} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$** 

| Symbol    | Parameter                            | Test Conditions | Minimum                        | Typical | Maximum  | Units   |
|-----------|--------------------------------------|-----------------|--------------------------------|---------|----------|---------|
| $I_{IH}$  | Input High Current                   | PCLK            | $V_{DD} = V_{IN} = 3.465V$     |         | 150      | $\mu A$ |
|           |                                      | nPCLK           | $V_{DD} = V_{IN} = 3.465V$     |         | 5        | $\mu A$ |
| $I_{IL}$  | Input Low Current                    | PCLK            | $V_{DD} = 3.465V, V_{IN} = 0V$ | -5      |          | $\mu A$ |
|           |                                      | nPCLK           | $V_{DD} = 3.465V, V_{IN} = 0V$ | -150    |          | $\mu A$ |
| $V_{PP}$  | Peak-to-Peak Voltage; NOTE 1         |                 | 0.3                            |         | 1        | V       |
| $V_{CMR}$ | Common Mode Input Voltage; NOTE 1, 2 |                 | 1.5                            |         | $V_{DD}$ | V       |

NOTE 1:  $V_{IL}$  should not be less than -0.3V.NOTE 2: Common mode input voltage is defined as  $V_{IH}$ .**Table 4E. LVDS DC Characteristics,  $V_{DD} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$** 

| Symbol          | Parameter                                 | Test Conditions | Minimum | Typical | Maximum | Units   |
|-----------------|---|-----------------|---------|---------|---------|---------|
| $V_{OD}$        | Differential Output Voltage               |                 | 200     | 280     | 360     | mV      |
| $\Delta V_{OD}$ | $V_{OD}$ Magnitude Change                 |                 |         | 0       | 40      | mV      |
| $V_{OS}$        | Offset Voltage                            |                 | 1.125   | 1.25    | 1.375   | V       |
| $\Delta V_{OS}$ | $V_{OS}$ Magnitude Change                 |                 |         | 5       | 25      | mV      |
| $I_{OZ}$        | High Impedance Leakage                    |                 | -10     |         | +10     | $\mu A$ |
| $I_{OFF}$       | Power Off Leakage                         |                 | -20     | $\pm 1$ | +20     | $\mu A$ |
| $I_{OSD}$       | Differential Output Short Circuit Current |                 |         | -3.5    | -5      | mA      |
| $I_{OS}$        | Output Short Circuit Current              |                 |         | -3.5    | -5      | mA      |
| $V_{OH}$        | Output Voltage High                       |                 |         | 1.34    | 1.6     | V       |
| $V_{OL}$        | Output Voltage Low                        |                 | 0.9     | 1.06    |         | V       |

## AC Electrical Characteristics

Table 5. AC Characteristics,  $V_{DD} = 3.3V \pm 5\%$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$

| Parameter    | Symbol  | Test Conditions                            | Minimum | Typical | Maximum | Units |
|--------------|---|--|---------|---------|---------|-------|
| $f_{MAX}$    | Maximum Output Frequency  |  |         |         | 650     | MHz   |
| $f_{jit}$    | Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section | 153.6MHz, Integration Range: 12kHz – 20MHz |         | 0.164   |         | ps    |
| $t_{PD}$     | Propagation Delay; NOTE 1   | $f \leq 650MHz$                            | 1.5     |         | 2.6     | ns    |
| $t_{sk(o)}$  | Output Skew; NOTE 2, 4  |  |         |         | 40      | ps    |
| $t_{sk(pp)}$ | Part-to-Part Skew; NOTE 3, 4  |  |         |         | 600     | ps    |
| $t_R / t_F$  | Output Rise/Fall Time   | 20% to 80% @ 50MHz                         | 150     |         | 450     | ps    |
| odc          | Output Duty Cycle   | odc  | 45      | 50      | 55      | %     |

All parameters measured at 500MHz unless noted otherwise.

NOTE 1: Measured from the differential input crossing point to the differential output crossing point.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.

Measured at the differential output cross points.

NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions.

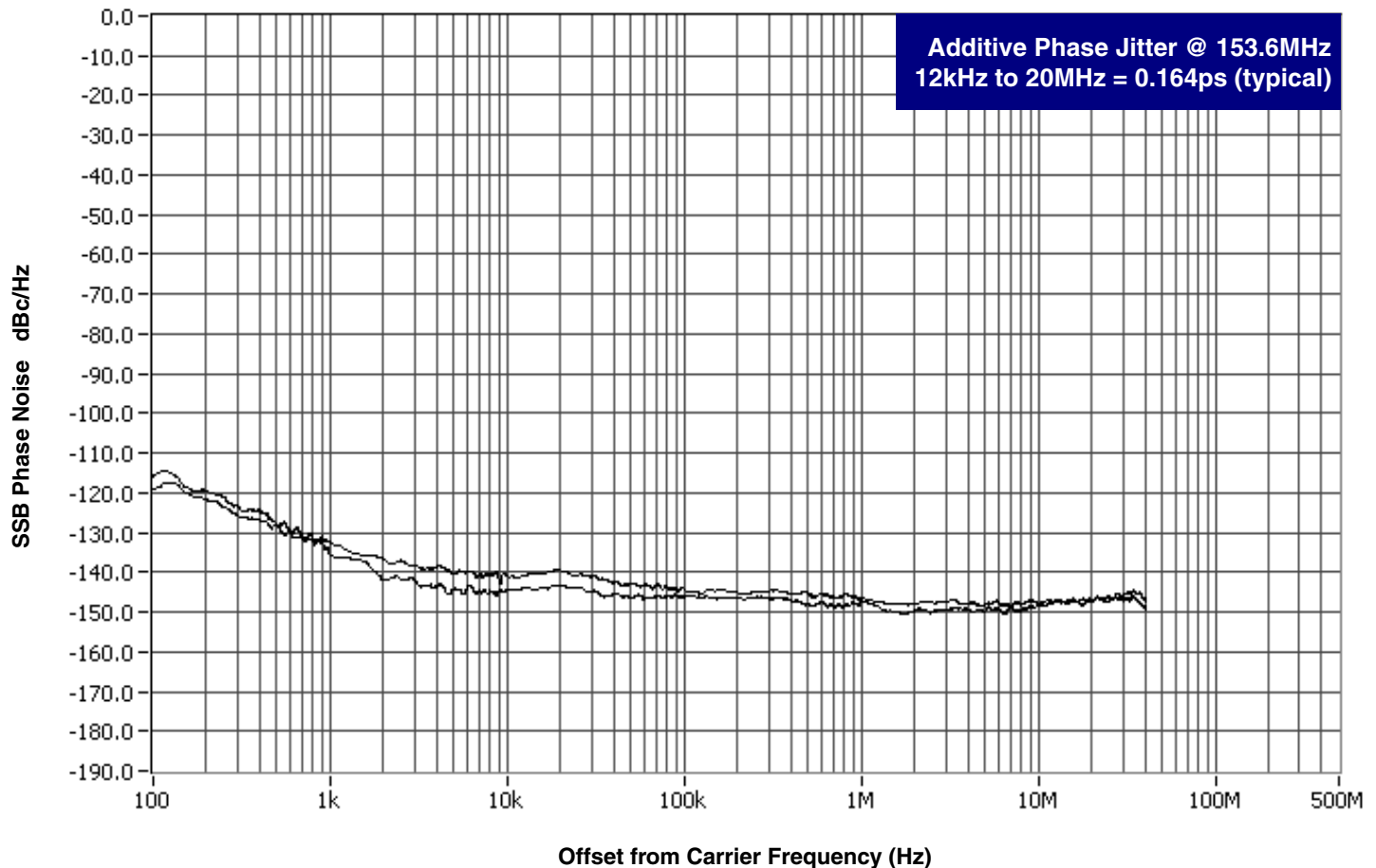
Using the same type of inputs on each device, the outputs are measured at the differential cross points.

NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

## Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the **dBc Phase Noise**. This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band

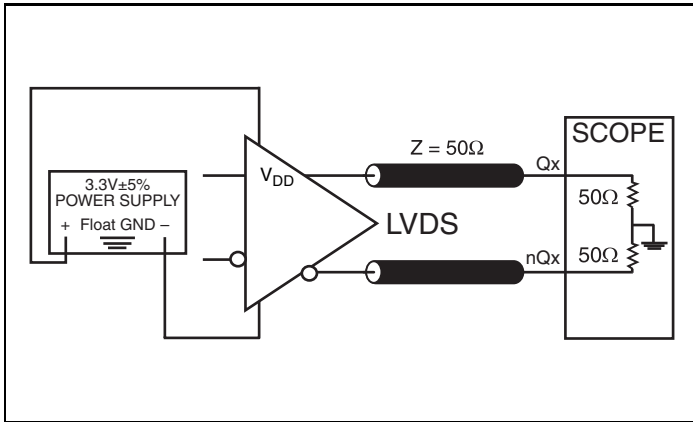
to the power in the fundamental. When the required offset is specified, the phase noise is called a **dBc** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



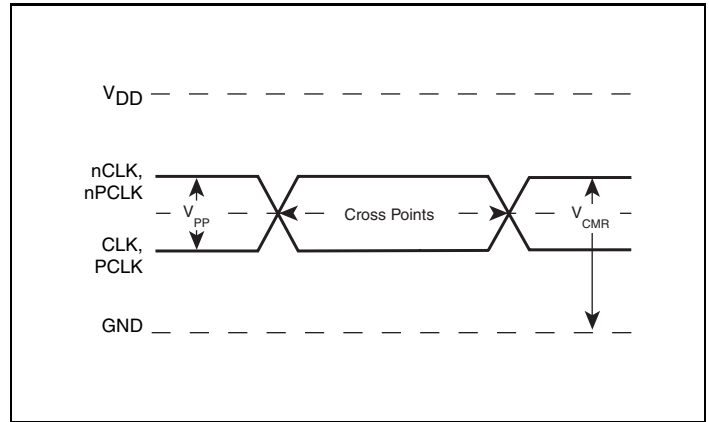
As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the

device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

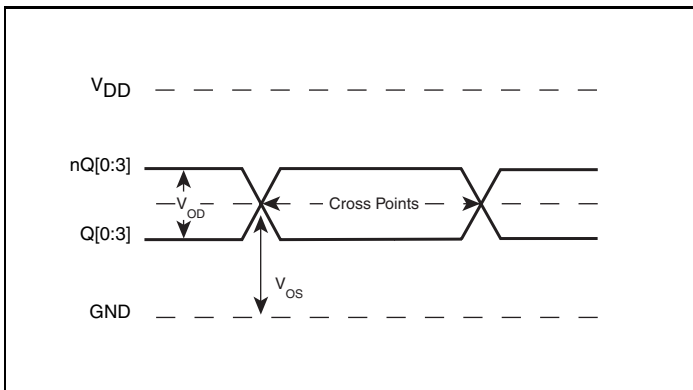
### Parameter Measurement Information



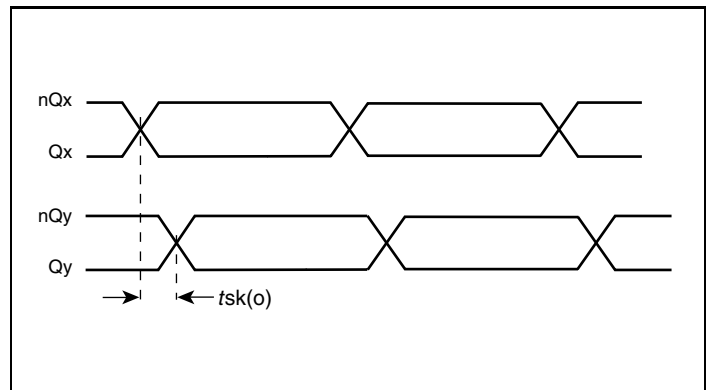
3.3V LVDS Output Load AC Test Circuit



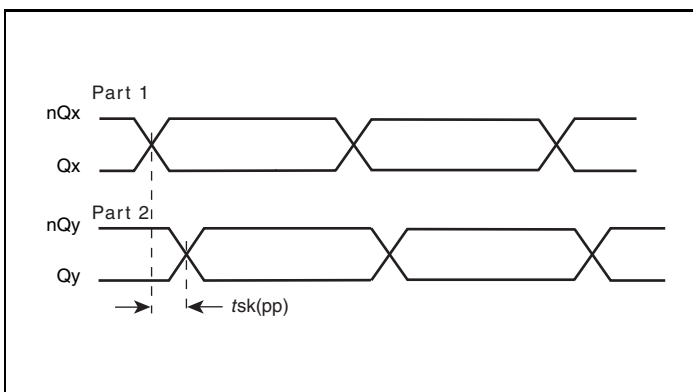
Differential Input Level



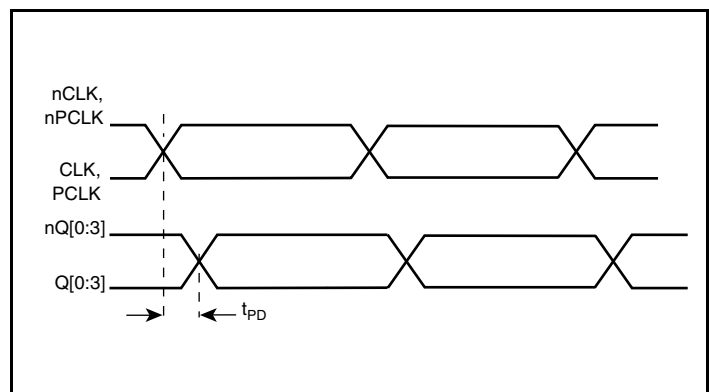
Differential Output Level



Output Skew



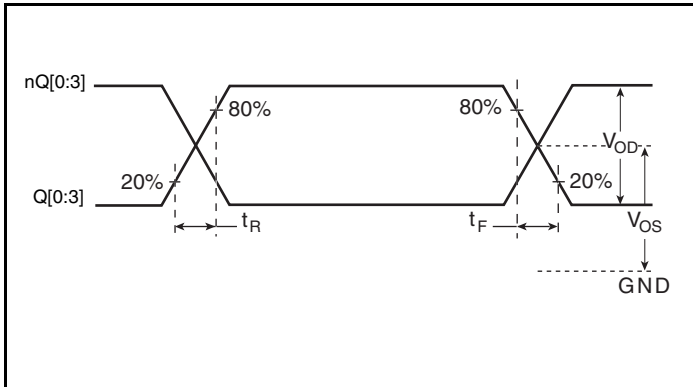
Part-to-Part Skew



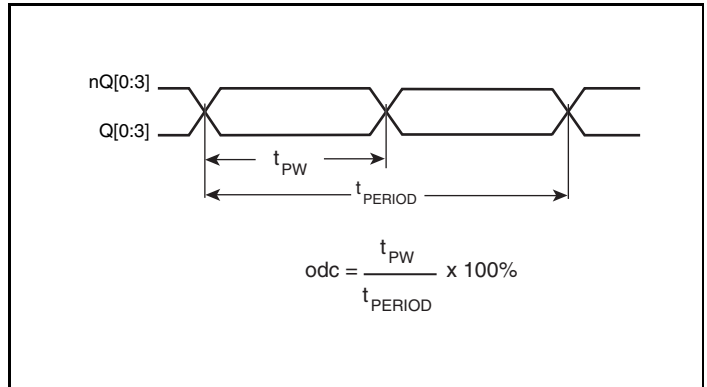
Propagation Delay



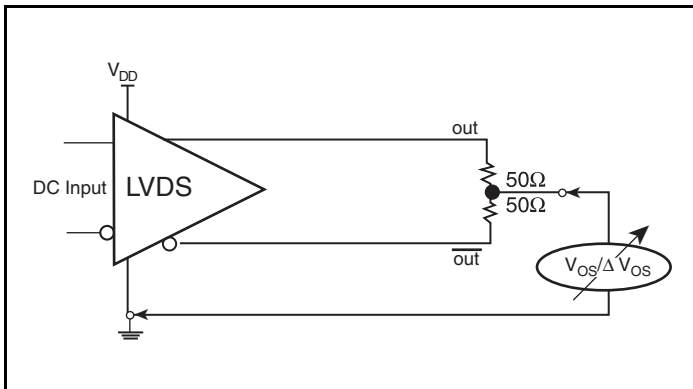
### Parameter Measurement Information, continued



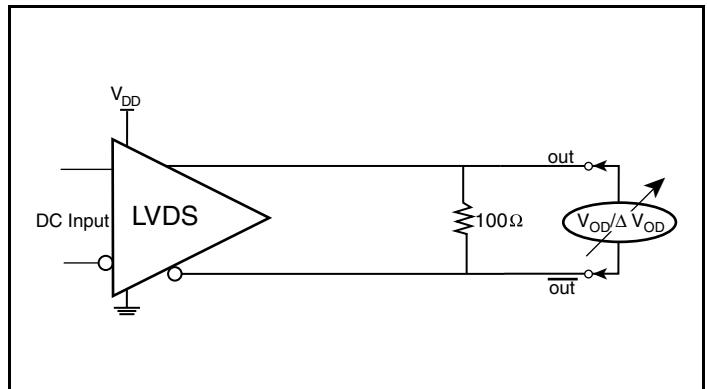
Output Rise/Fall Time



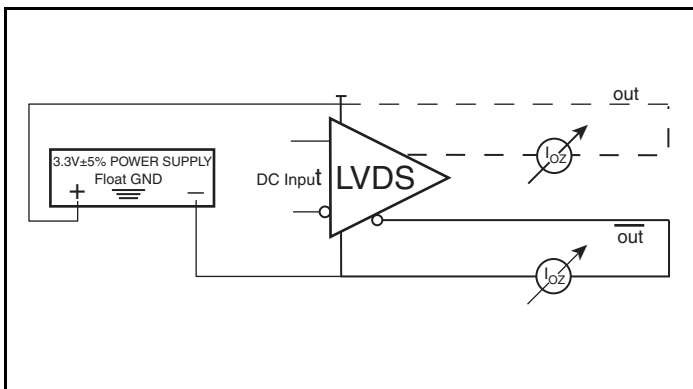
Output Duty Cycle/Pulse Width/Period



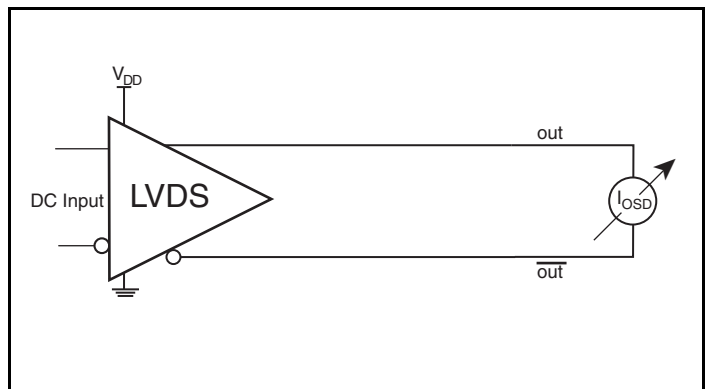
Offset Voltage Setup



Differential Output Voltage Setup

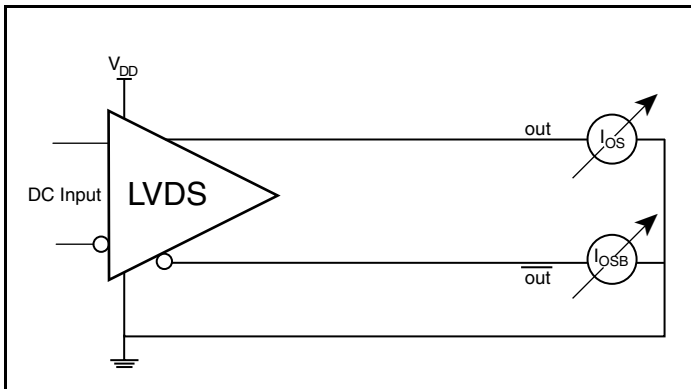


High Impedance Leakage Current Setup

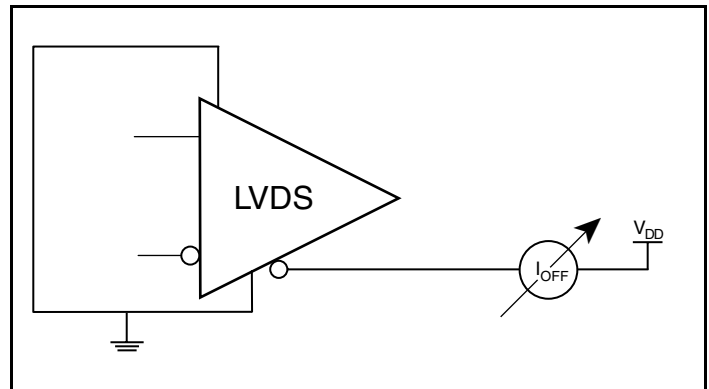


Differential Output Short Circuit Setup

## Parameter Measurement Information, continued



Output Short Circuit Current Setup



Power Off Leakage Setup

## Application Information

### Wiring the Differential Input to Accept Single Ended Levels

Figure 2 shows how the differential input can be wired to accept single ended levels. The reference voltage  $V_{REF} = V_{DD}/2$  is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the  $V_{REF}$  in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and  $V_{DD} = 3.3V$ ,  $V_{REF}$  should be 1.25V and  $R2/R1 = 0.609$ .

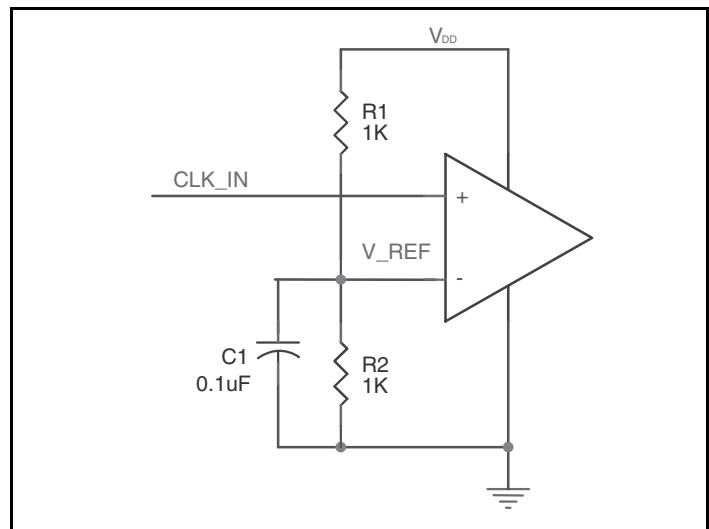
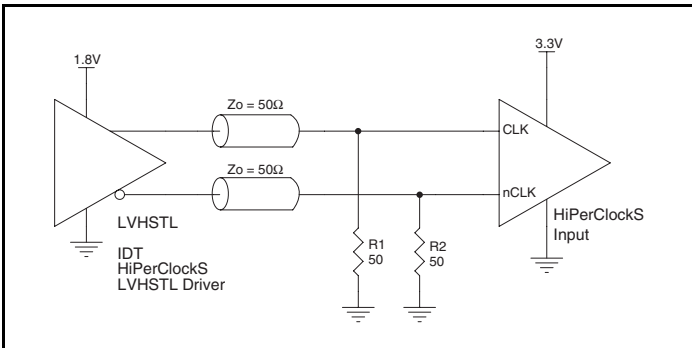


Figure 2. Single-Ended Signal Driving Differential Input

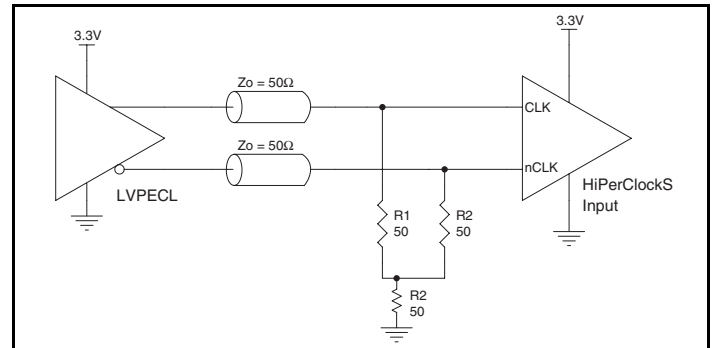
### Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both signals must meet the  $V_{PP}$  and  $V_{CMR}$  input requirements. Figures 3A to 3F show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver

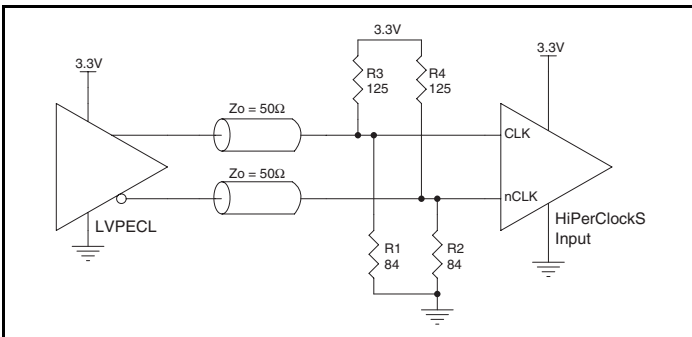
component to confirm the driver termination requirements. For example, in Figure 3A, the input termination applies for IDT HiPerClockS open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.



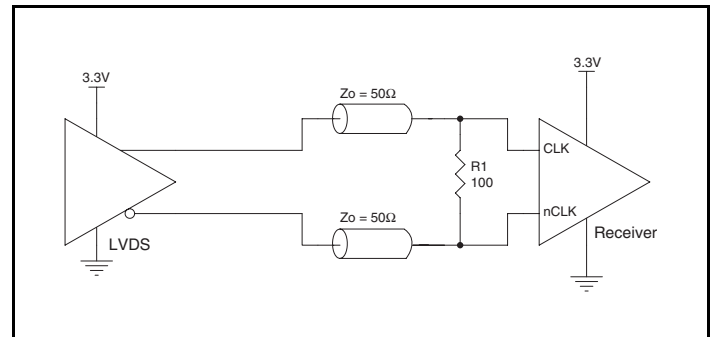
**Figure 3A. HiPerClockS CLK/nCLK Input Driven by an IDT Open Emitter HiPerClockS LVHSTL Driver**



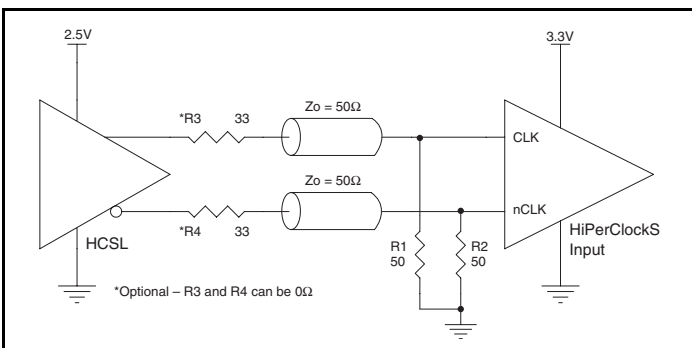
**Figure 3B. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVPECL Driver**



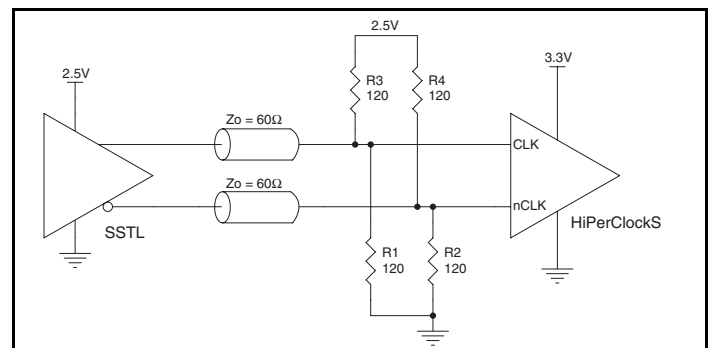
**Figure 3C. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVPECL Driver**



**Figure 3D. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVDS Driver**



**Figure 3E. HiPerClockS CLK/nCLK Input Driven by a 3.3V HCSL Driver**

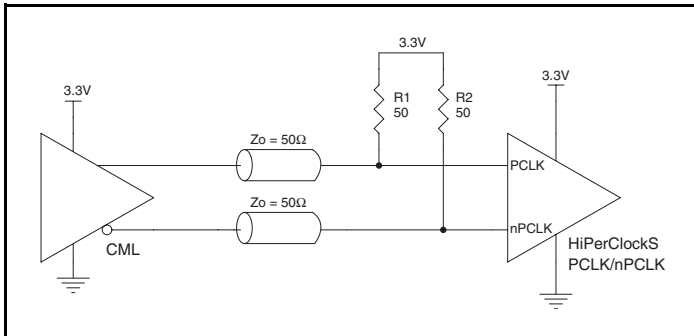


**Figure 3F. HiPerClockS CLK/nCLK Input Driven by a 2.5V SSTL Driver**

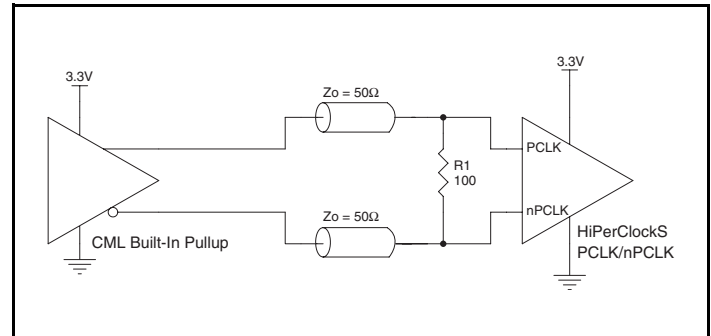
## LVPECL Clock Input Interface

The PCLK /nPCLK accepts LVPECL, CML, SSTL and other differential signals. Both signals must meet the  $V_{PP}$  and  $V_{CMR}$  input requirements. Figures 4A to 4F show interface examples for the HiPerClockS PCLK/nPCLK input driven by the most common

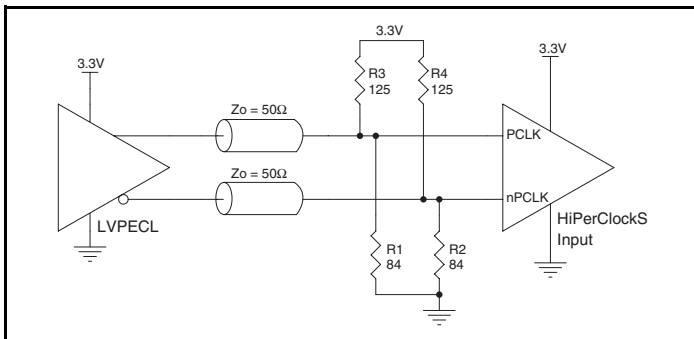
driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.



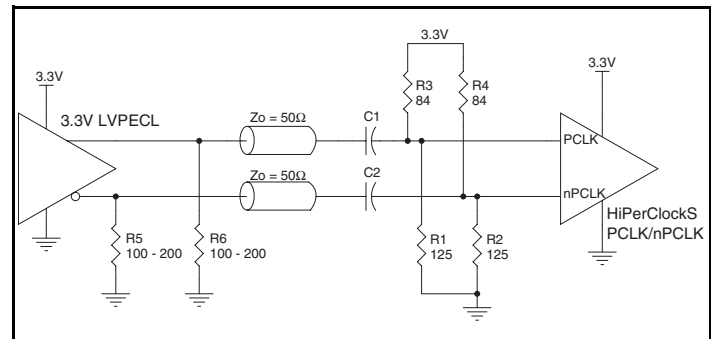
**Figure 4A. HiPerClockS PCLK/nPCLK Input Driven by a CML Driver**



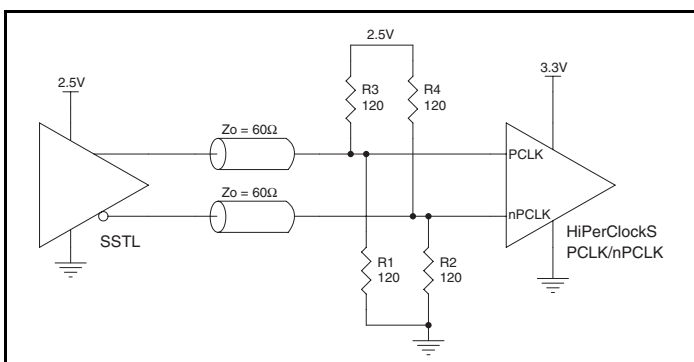
**Figure 4B. HiPerClockS PCLK/nPCLK Input Driven by a Built-In Pullup CML Driver**



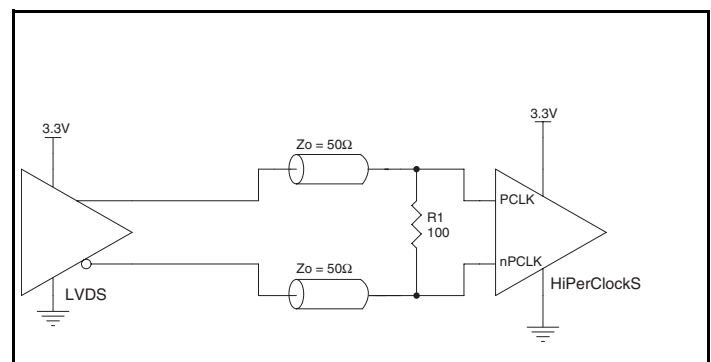
**Figure 4C. HiPerClockS PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver**



**Figure 4D. HiPerClockS PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver with AC Couple**



**Figure 4E. HiPerClockS PCLK/nPCLK Input Driven by an SSTL Driver**



**Figure 4F. HiPerClockS PCLK/nPCLK Input Driven by a 3.3V LVDS Driver**

## Recommendations for Unused Input and Output Pins

### Inputs:

#### CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a  $1\text{k}\Omega$  resistor can be tied from CLK to ground.

#### PCLK/nPCLK Inputs

For applications not requiring the use of the differential input, both PCLK and nPCLK can be left floating. Though not required, but for additional protection, a  $1\text{k}\Omega$  resistor can be tied from PCLK to ground.

#### LVC MOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A  $1\text{k}\Omega$  resistor can be used.

### Outputs:

#### LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with  $100\Omega$  across. If they are left floating, there should be no trace attached.

## 3.3V LVDS Driver Termination

A general LVDS interface is shown in Figure 5. In a  $100\Omega$  differential transmission line environment, LVDS drivers require a matched load termination of  $100\Omega$  across near the receiver input.

For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.

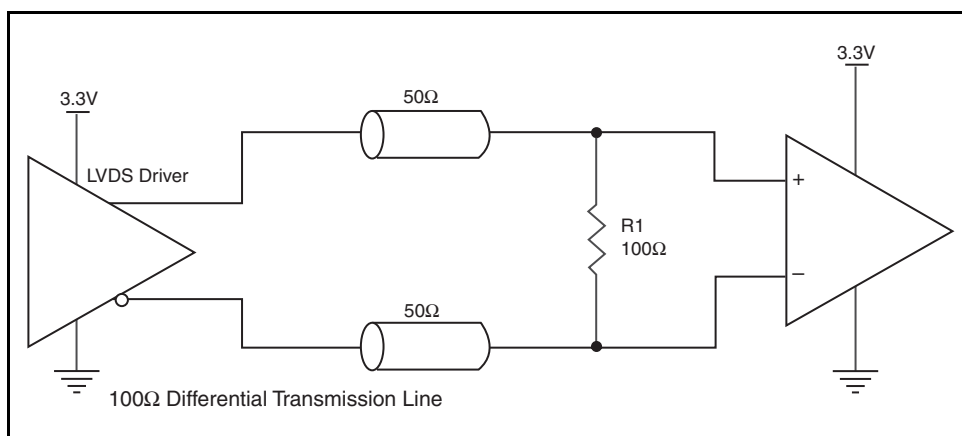


Figure 5. Typical LVDS Driver Termination

## Power Considerations

This section provides information on power dissipation and junction temperature for the ICS8543I. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the ICS8543I is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{DD} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)<sub>MAX</sub> =  $V_{DD\_MAX} * I_{DD\_MAX} = 3.465V * 50mA = 173.25mW$

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS devices is 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd\_total$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming no air flow and a multi-layer board, the appropriate value is 73.2°C/W per Table 6 below.

Therefore,  $T_j$  for an ambient temperature of 85°C with all outputs switching is:

$$85^\circ\text{C} + 0.173\text{W} * 73.2^\circ\text{C/W} = 97.7^\circ\text{C}. \text{ This is well below the limit of } 125^\circ\text{C}.$$

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (single layer or multi-layer).

**Table 6. Thermal Resistance  $\theta_{JA}$  for 20 Lead TSSOP, Forced Convection**

| Linear Feet per Minute                       | $\theta_{JA}$ by Velocity |          |          |
|--|---------------------------|----------|----------|
|  | 0                         | 200      | 500      |
| Single-Layer PCB, JEDEC Standard Test Boards | 114.5°C/W                 | 98.0°C/W | 88.0°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards  | 73.2°C/W                  | 66.6°C/W | 63.5°C/W |

## Reliability Information

Table 7.  $\theta_{JA}$  vs. Air Flow Table for a 20 Lead TSSOP

| Linear Feet per Minute                       | $\theta_{JA}$ by Velocity |          |          |
|--|---------------------------|----------|----------|
|  | 0                         | 200      | 500      |
| Single-Layer PCB, JEDEC Standard Test Boards | 114.5°C/W                 | 98.0°C/W | 88.0°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards  | 73.2°C/W                  | 66.6°C/W | 63.5°C/W |

## Transistor Count

The transistor count for ICS8543I is: 636

## Package Outline and Package Dimensions

Package Outline - G Suffix for 20 Lead TSSOP

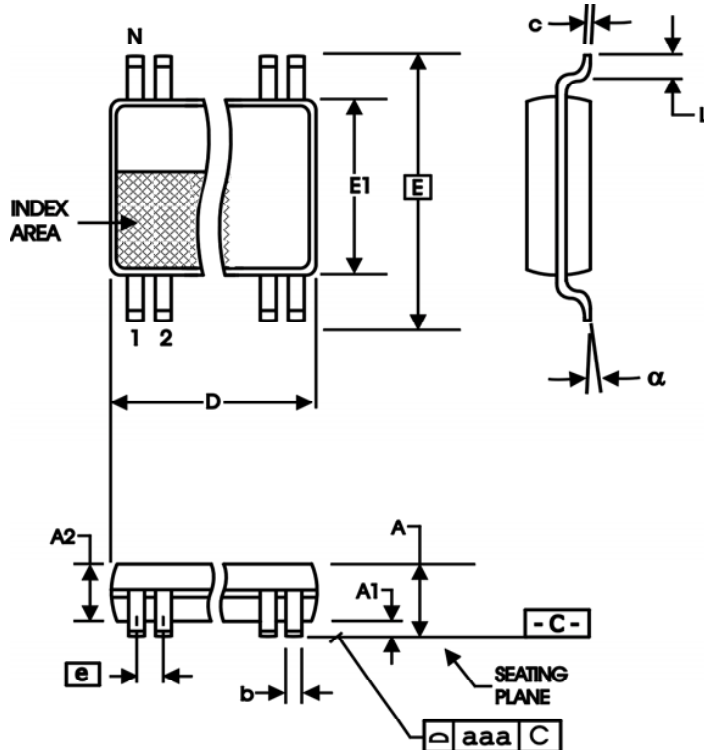


Table 8. Package Dimensions

| All Dimensions in Millimeters |            |         |
|-------------------------------|------------|---------|
| Symbol                        | Minimum    | Maximum |
| N                             | 20         |         |
| A                             |            | 1.20    |
| A1                            | 0.05       | 0.15    |
| A2                            | 0.80       | 1.05    |
| b                             | 0.19       | 0.30    |
| c                             | 0.09       | 0.20    |
| D                             | 6.40       | 6.60    |
| E                             | 6.40 Basic |         |
| E1                            | 4.30       | 4.50    |
| e                             | 0.65 Basic |         |
| L                             | 0.45       | 0.75    |
| $\alpha$                      | 0°         | 8°      |
| aaa                           |            | 0.10    |

Reference Document: JEDEC Publication 95, MO-153

## Ordering Information

Table 9. Ordering Information

| Part/Order Number | Marking      | Package                   | Shipping Packaging | Temperature   |
|-------------------|--------------|---------------------------|--------------------|---------------|
| 8543BGI           | ICS8543BGI   | 20 Lead TSSOP             | Tube               | -40°C to 85°C |
| 8543BGIT          | ICS8543BGI   | 20 Lead TSSOP             | 2500 Tape & Reel   | -40°C to 85°C |
| 8543BGILF         | ICS8543BGILF | "Lead-Free" 20 Lead TSSOP | Tube               | -40°C to 85°C |
| 8543BGILFT        | ICS8543BGILF | "Lead-Free" 20 Lead TSSOP | 2500 Tape & Reel   | -40°C to 85°C |

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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## Revision History Sheet

| Rev | Table | Page                    | Description of Change   | Date     |
|-----|-------|-------------------------|---|----------|
| A   |       | 3                       | Updated Figure 1, CLK_EN Timing Diagram.  | 10/17/01 |
| A   |       | 3                       | Updated Figure 1, CLK_EN Timing Diagram.  | 11/2/01  |
| A   |       | 1<br>6 - 10             | Features section, Bullet 6 to read 3.3V LVDS levels instead of LVPECL.<br>Updated Parameter Measurement Information figures.  | 5/6/02   |
| B   |       | 1                       | Features - deleted bullet ""Designed to meet or exceed the requirements of ANSI TIA/EIA-644"".  | 9/19/02  |
|     | 4E    | 5                       | LVDS Table - changed $V_{OD}$ typical value from 350mV to 280mV.  |          |
| C   | T2    | 2<br>4<br>9<br>10<br>11 | Pin Characteristics - changed $C_{IN}$ 4pF max. to 4pF typical.<br>Absolute Maximum Ratings - changed Output rating.<br>Added Differential Clock Input Interface section.<br>Added LVPECL Clock Input Interface section.<br>Added LVDS Driver Termination section.<br>Updated format throughout data sheet. | 1/5/04   |
| D   | T4B   | 1<br>3<br>4             | Features section - added lead-free bullet.<br>Updated Figure 1, CLK_EN Timing Diagram.<br>LVCMOS DC Characteristics Table - corrected typo in $V_{IH}$ max. from $V_{DD} - 0.3V$ to $V_{DD} + 0.3V$ .   | 2/27/08  |
|     |       | 10<br>11                | Updated <i>Differential Clock Input Interface</i> section.<br>Updated <i>LVPECL Clock Input Interface</i> section.  |          |
|     |       | 12<br>13                | Added <i>Recommendation for Unused Input and Output Pins</i> section.<br>Added <i>Power Considerations</i> section.   |          |
|     | T9    | 15                      | Ordering Information Table - added lead-free Part/Order Number, Marking and note.<br>Updated format throughout the datasheet.   |          |
| E   | T5    | 1<br>6<br>7<br>9        | Features Section - added Additive Phase Jitter bullet.<br>AC Characteristics Table - added Additive Phase Jitter spec.<br>Added Additive Phase Jitter Plot.<br>Parameter Measurement Information - updated <i>Output Rise/Fall Time</i> diagram.  | 9/9/08   |

ICS8543I

LOW SKEW, 1-TO-4, DIFFERENTIAL-TO-LVDS FANOUT BUFFER

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