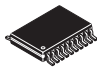
2.5/3.3V 1:4 PECL CLock Driver with 2:1 Input MUX

MC100ES6130

The MC100ES6130 is a 2.5 GHz differential PECL 1:4 fanout buffer. The ES6130 offers a wide operating range of 2.5 V and 3.3 V and also features a 2:1 input MUX which is ideal for redundant clock switchover applications. This device also includes a synchronous enable pin that forces the outputs into a fixed logic state. Enable or disable state is initiated only after the outputs are in a LOW state to eliminate the possibility of a runt clock pulse.

Features

- 2 GHz maximum output frequency
- 25 ps maximum output-to-output skew
- 150 ps part-to-part skew
- 350 ps typical propagation delay
- 2:1 differential MUX input
- 2.5 / 3.3 V operating range
- LVPECL and HSTL input compatible
- 16-lead TSSOP package
- Temperature range –40°C to +85°C
- 16-lead Pb-free package available



DT SUFFIX
16-LEAD TSSOP PACKAGE
CASE 948F-01

EJ SUFFIX
16-LEAD TSSOP PACKAGE
Pb-FREE PACKAGE
CASE 948F-01

ORDERING INFORMATION	
Device	**Package**
MC100ES6130DT	TSSOP-16
MC100ES6130DTR2	TSSOP-16
MC100ES6130EJ	TSSOP-16 (Pb-Free)
MC100ES6130EJR2	TSSOP-16 (Pb-Free)

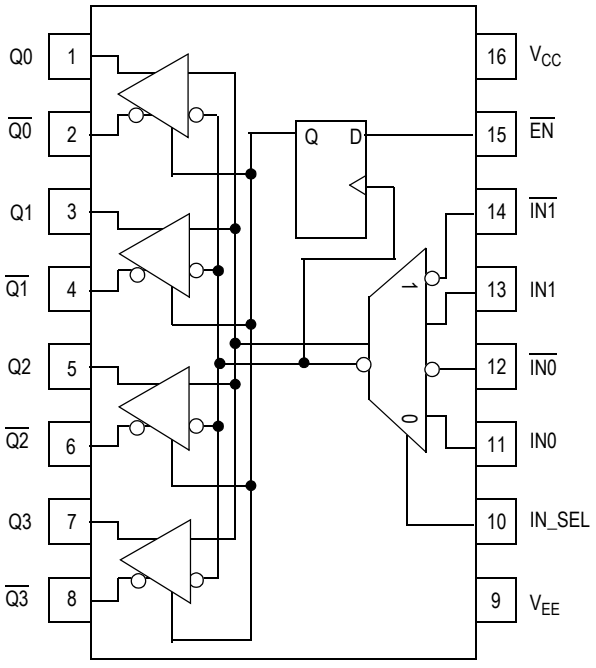


Figure 1. 16-Lead Pinout (Top View) and Logic Diagram

Table 1. Pin Description

Number	Name	Description
1, 2, 3, 4, 5, 6, 7, 8	$\overline{Q0}$ to $\overline{Q3}$ Q0 to Q3	LVPECL differential outputs: Terminate with 50Ω to V_{CC} – 2 V. For single-ended applications, terminate the unused output with 50Ω to V_{CC} – 2 V.
9	V_{EE}	Negative power supply: For LVPECL applications, connect to GND.
10	IN_SEL	LVPECL compatible 2:1 mux input signal select: When IN_SEL is LOW, the IN0 input pair is selected. When IN_SEL is HIGH, the IN1 input pair is selected. Includes a 75 kΩ pulldown. Default state is LOW and IN0 is selected.
11, 12, 13, 14	IN0, $\overline{IN0}$ IN1, $\overline{IN1}$	LVPECL, HSTL clock or data inputs. Internal 75 kΩ pulldown resistors on IN0 and IN1. Internal 75 kΩ pullup and 75 kΩ pulldown resistors on $\overline{IN0}$, $\overline{IN1}$. $\overline{IN0}$, $\overline{IN1}$ default condition is V_{CC}/2 when left floating. IN0, IN1 default condition is LOW when left floating.
15	$\overline{EN}$	LVPECL compatible synchronous enable: When $\overline{EN}$ goes HIGH, Q_{OUT} will go LOW and $\overline{Q}_{OUT}$ will go HIGH on the next LOW input clock transition. Includes a 75 kΩ pulldown. Default state is LOW when left floating. The internal latch is clocked on the falling edge of the input (IN0, IN1).
16	V_{CC}	Positive power supply: Bypass with 0.1 µF//0.01 µF low ESR capacitors.

Table 2. Truth Table(1)

IN0	IN1	IN_SEL	$\overline{EN}$	Q
L	X	L	L	L
H	X	L	L	H
X	L	H	L	L
X	H	H	L	H
Z	X	L	H	L
X	Z	H	H	L

1. Z = HIGH to LOW Transition
   X = Don't Care

Table 3. General Specifications

Characteristics		Value
Internal Input Pulldown Resistor		75 kΩ
Internal Input Pullup Resistor		75 kΩ
ESD Protection	Human Body Model Machine Model Charged Device Model	> 2000 V > 200 V > 1500 V
θ_{JA} Thermal Resistance (Junction-to-Ambient)	0 LFPM, 16 TSSOP 500 LFPM, 16 TSSOP	138°C/W 108°C/W

Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test

Table 4. Absolute Maximum Ratings(1)

Symbol	Rating	Conditions	Rating	Units
V_{SUPPLY}	Power Supply Voltage	Difference between V_{CC} & V_{EE}	3.9	V
V_{IN}	Input Voltage	$V_{CC} - V_{EE} \leq 3.6$ V	V_{CC} + 0.3 V_{EE} – 0.3	V V
I_{out}	Output Current	Continuous Surge	50 100	mA mA
T_A	Operating Temperature Range		–40 to +85	°C
T_{STG}	Storage Temperature Range		–65 to +150	°C

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 5. DC Characteristics (V_{CC} = 0 V, V_{EE} = –2.5 V ±5% or V_{CC} = 2.5 V ±5%, V_{EE} = 0 V)

Symbol	Characteristic	–40°C			0°C to 85°C			Unit
		Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		45	70		45	70	mA
V_{OH}	Output HIGH Voltage(1)	V_{CC} – 1250	V_{CC} – 990	V_{CC} – 800	V_{CC} – 1200	V_{CC} – 960	V_{CC} – 750	mV
V_{OL}	Output LOW Voltage(1)	V_{CC} – 2000	V_{CC} – 1550	V_{CC} – 1150	V_{CC} – 1925	V_{CC} – 1630	V_{CC} – 1200	mV
V_{outPP}	Output Peak-to-Peak Voltage	200			200			mV
V_{IH}	Input HIGH Voltage	V_{CC} – 1165		V_{CC} – 880	V_{CC} – 1165		V_{CC} – 880	mV
V_{IL}	Input LOW Voltage	V_{CC} – 1810		V_{CC} – 1475	V_{CC} – 1810		V_{CC} – 1475	mV
V_{PP}	Differential Input Voltage(2)	0.12		1.3	0.12		1.3	V
V_{CMR}	Differential Cross Point Voltage(3)	V_{EE} + 0.2		V_{CC} – 1.0	V_{EE} + 0.2		V_{CC} – 1.0	V
I_{IN}	Input Current			±150			±150	µA

1. Output termination voltage V_{TT} = 0 V for V_{CC} = 2.5 V operation is supported but the power consumption of the device will increase.
2. V_{PP} (DC) is the minimum differential input voltage swing required to maintain device functionality.
3. V_{CMR} (DC) is the cross point of the differential input signal. Functional operation is obtained when the cross point is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.

Table 6. DC Characteristics (V_{CC} = 0 V, V_{EE} = –3.8 to 3.135 V or V_{CC} = 3.135 to 3.8 V, V_{EE} = 0 V)

Symbol	Characteristic	–40°C			0°C to 85°C			
		Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		48	70		48	70	mA
V_{OH}	Output HIGH Voltage(1)	V_{CC} – 1150	V_{CC} – 1020	V_{CC} – 800	V_{CC} – 1200	V_{CC} – 970	V_{CC} – 750	mV
V_{OL}	Output LOW Voltage(1)	V_{CC}– 1950	V_{CC} – 1620	V_{CC} – 1250	V_{CC} – 2000	V_{CC} – 1680	V_{CC} – 1300	mV
V_{outPP}	Output Peak-to-Peak Voltage	200			200			mV
V_{IH}	Input HIGH Voltage	V_{CC} – 1165		V_{CC} – 880	V_{CC} – 1165		V_{CC} – 880	mV
V_{IL}	Input LOW Voltage	V_{CC} – 1810		V_{CC} – 1475	V_{CC} – 1810		V_{CC} – 1475	mV
V_{PP}	Differential Input Voltage(2)	0.12		1.3	0.12		1.3	V
V_{CMR}	Differential Cross Point Voltage(3)	V_{EE} + 0.2		V_{CC} - 1.1	V_{EE} + 0.2		V_{CC} – 1.1	V
I_{IN}	Input Current			±150			±150	µA

1. Output termination voltage V_{TT} = 0 V for V_{CC} = 2.5 V operation is supported but the power consumption of the device will increase.
2. V_{PP} (DC) is the minimum differential input voltage swing required to maintain device functionality.
3. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.

Table 7. AC Characteristics (V_{CC} = 0 V, V_{EE} = –3.8 V to –2.375 V; V_{CC} = 2.375 to 3.8 V, V_{EE} = 0 V)[1]

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Frequency	2			2			2			GHz
t_{PLH} / t_{PHL}	Propagation Delay to Output Differential CLK to Q, $\overline{Q}$	300	340	450	300	350	450	300	350	475	ps
t_{SKEW}	Skew[2] output-to-output part-to-part		15	25 125		15	25 150		15	25 150	ps ps
t_{JITTER}	Cycle-to-Cycle Jitter RMS (1σ)			1			1			1	ps
V_{PP}	Minimum Input Swing	200		1200	200		1200	200		1200	mV
V_{CMR}	Differential Cross Point Voltage	V_{EE} + 0.2		V_{CC} – 1.2	V_{EE} + 0.2		V_{CC} – 1.2	V_{EE} + 0.2		V_{CC} – 1.2	V
t_r / t_f	Output Rise/Fall Times (20% – 80% @ 50 MHz)	70		225	70		250	70		275	ps

1. Measured using a 750 mV source, 50% Duty Cycle clock source. All loading with 50 ohms to V_{CC} – 2.0 V.
2. Skew is measured between outputs under identical transitions.

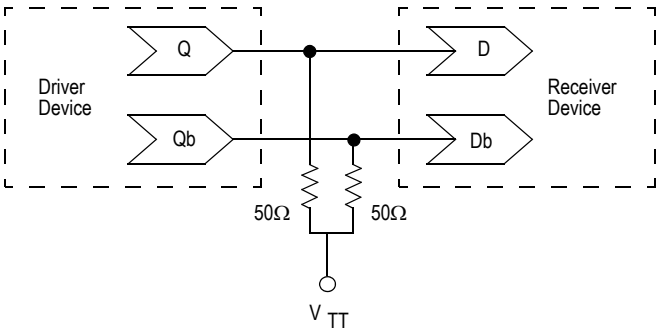
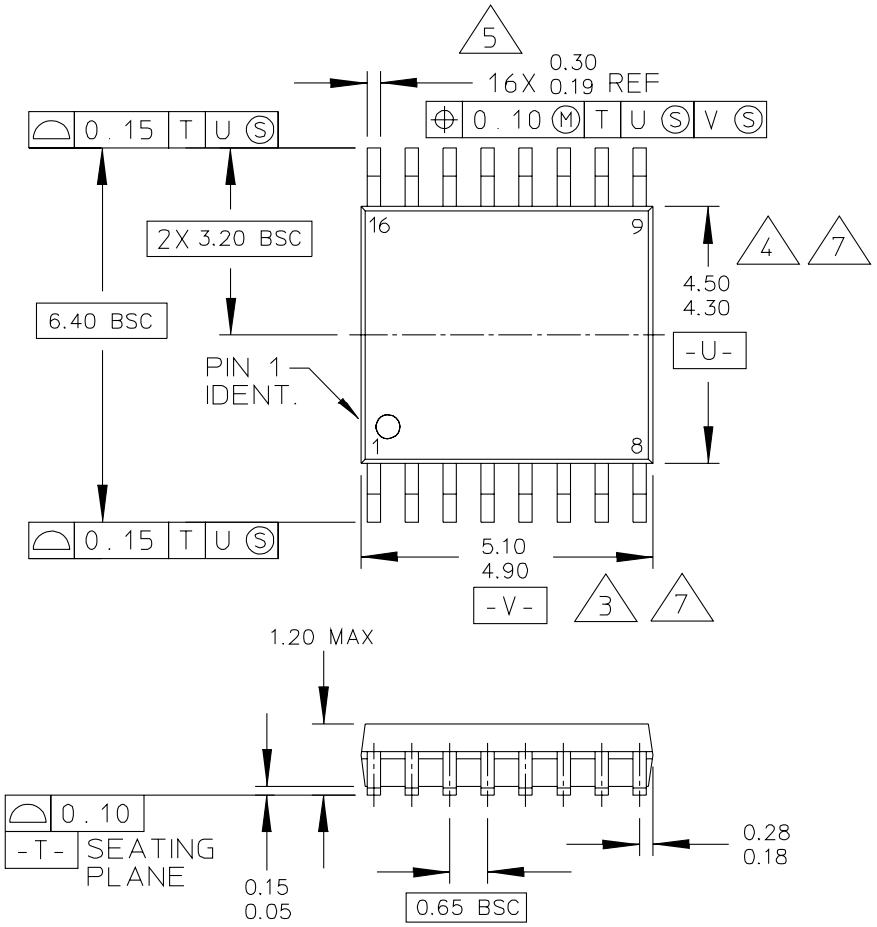


Figure 2. Typical Termination for Output Driver and Device Evaluation

PACKAGE DIMENSIONS



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CASE 948F-01
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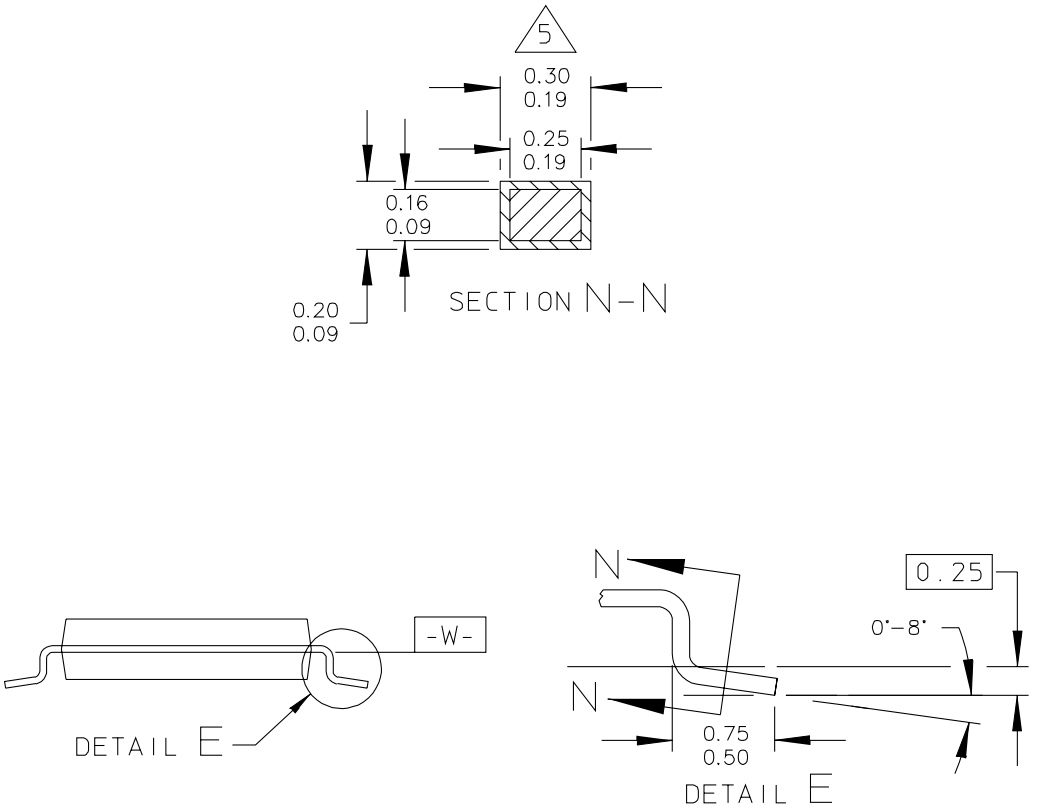
PACKAGE DIMENSIONS



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CASE 948F-01
ISSUE B
16-LEAD TSSOP PACKAGE

PACKAGE DIMENSIONS

NOTES:

1. CONTROLLING DIMENSION: MILLIMETER
2. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M-1982.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
5. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF THE DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSIONS ARE TO BE DETERMINED AT DATUM PLANE -W-.

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