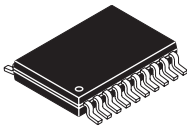
3.3V LVCMOS-to-LVPECL 1:4 Fanout Buffer **MC100ES6535**

DATA SHEET

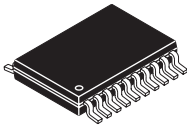
The MC100ES6535 is a low skew, high performance 3.3 V 1-to-4 LVCMOS to LVPECL fanout buffer. The ES6535 has two selectable inputs that allow LVCMOS or LVTTL input levels which translate to LVPECL outputs. The clock enable is internally synchronized to eliminate runt pulses on the outputs during asynchronous assertion/deassertion of the clock enable pin. The ES6535 is ideal for high performance clock distribution applications.

Features

- 4 differential LVPECL outputs
- 2 selectable LVCMOS/LVTTL inputs
- 1 GHz maximum output frequency
- Translates LVCMOS/LVTTL levels to LVPECL levels
- 30 ps maximum output skew
- 190 ps part-to-part skew
- 3.3 V operating range
- 20-lead TSSOP package
- Ambient temperature range –40°C to +85°C
- 20-lead Pb-free package available



DT SUFFIX
20-LEAD TSSOP PACKAGE
CASE 948E-02



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ORDERING INFORMATION	
Device	**Package**
MC100ES6535DT	TSSOP-20
MC100ES6535DTR2	TSSOP-20
MC100ES6535EJ	TSSOP-20 (Pb-Free)
MC100ES6535EJR2	TSSOP-20 (Pb-Free)

Table 1. Pin Description

Number	Name	Type		Description
1	V_{EE}	Power		Negative supply pin
2	CLK_EN	Input	Pullup(1)	Synchronizing clock enable. When HIGH, clock outputs follow clock input. When LOW, Q outputs are forced low, $\overline{Q}$ outputs are forced high. LVCMOS/LVTTL interface levels
3	CLK_SEL	Input	Pulldown(1)	Clock select input. When HIGH, selects CLK1 input.. When LOW, selects CLK0 input. LVCMOS/LVTTL interface levels
4	CLK0	Input	Pulldown(1)	LVCMOS/LVTTL clock input
6	CLK1	Input	Pulldown(1)	LVCMOS/LVTTL clock input
5, 7, 8, 9	NC	Unused		No connect
10, 13, 18	V_{CC}	Power		Positive supply pin
11, 12	Q3, $\overline{Q3}$	Output		LVPECL differential output pair
14, 15	Q2, $\overline{Q2}$	Output		LVPECL differential output pair
16, 17	Q1, $\overline{Q1}$	Output		LVPECL differential output pair
19, 20	Q0, $\overline{Q0}$	Output		LVPECL differential output pair

1. Pullup and Pulldown refer to internal input resistors.

Table 2. Control Input Function Table(1)

Inputs			Outputs	
CLK_EN	CLK_SEL	Selected Source	Q0:Q3	$\overline{Q0}$:$\overline{Q3}$
0	0	CLK0	Disabled; LOW	Disabled; HIGH
0	1	CLK1	Disabled; LOW	Disabled; HIGH
1	0	CLK0	Enabled	Enabled
1	1	CLK1	Enabled	Enabled

1. After CLK_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock edge. In the active mode, the state of the outputs are a function of the CLK0 and CLK1 inputs as described in .

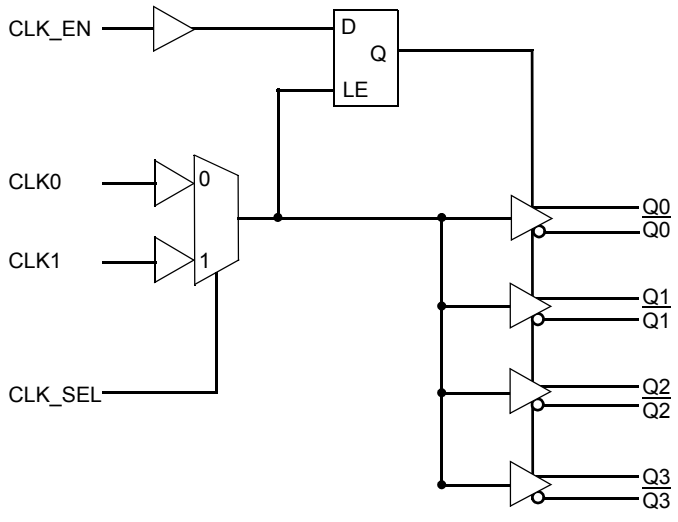


Figure 1. Logic Diagram

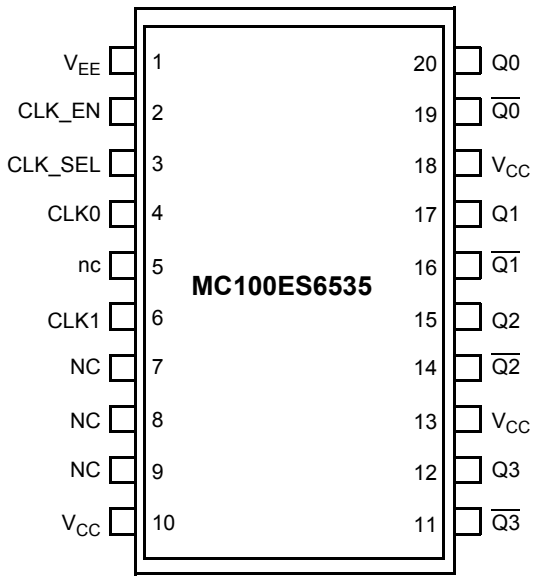


Figure 2. 20-Lead Pinout (Top View)

. Clock Input Function Table

Inputs	Outputs	
CLK0 or CLK1	**Q0:Q3**	**$\overline{Q0}$:$\overline{Q3}$**
0	LOW	HIGH
1	HIGH	LOW

Table 3. General Specifications

Characteristics		Value
Internal Input Pulldown Resistor		75 kΩ
Internal Input Pullup Resistor		75 kΩ
ESD Protection	Human Body Model Machine Model	4000 V 200 V
θ_{JA} Thermal Resistance (Junction-to-Ambient)	0 LFPM, 20 TSSOP 500 LFPM, 20 TSSOP	140°C/W 100°C/W

Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test

Table 4. Absolute Maximum Ratings(1)

Symbol	Rating	Conditions	Rating	Units
V_{SUPPLY}	Power Supply Voltage	Difference between V_{CC} & V_{EE}	3.9	V
V_{IN}	Input Voltage	$V_{CC} - V_{EE} \leq 3.6$ V	V_{CC} +0.3 V_{EE} –0.3	V V
I_{out}	Output Current	Continuous Surge	50 100	mA mA
T_A	Operating Temperature Range		–40 to +85	°C
T_{store}	Storage Temperature Range		–65 to +150	°C

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 5. DC Characteristics (V_{CC} = 3.135 V to 3.8 V; V_{EE} = 0 V)

Symbol	Characteristic	–40°C			0°C to 85°C			Unit
		Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current			35			45	mA
V_{OH}(1)	Output HIGH Voltage	V_{CC}–1150	V_{CC}–1020	V_{CC}–800	V_{CC}–1200	V_{CC}–970	V_{CC}–750	mV
V_{OL}	Output LOW Voltage	V_{CC}–1950	V_{CC}–1620	V_{CC}–1250	V_{CC}–2000	V_{CC}–1680	V_{CC}–1300	mV

1. Outputs are terminated through a 50Ω resistor to V_{CC} – 2 volts.

Table 6. LVTTL / LVCMOS Input DC Characteristics (V_{CC} = 3.135 V to 3.8 V)

Symbol	Characteristic	Condition	-40°C			0°C to 85°C			Unit
			Min	Typ	Max	Min	Typ	Max	
I_{IN}	Input Current	$V_{IN} = V_{CC}$			±150			±150	µA
V_{IK}	Input Clamp Voltage	I_{IN} = –18 mA			–1.2			–1.2	V
V_{IH}	Input HIGH Voltage		2.0		V_{CC} +0.3	2.0		V_{CC} +0.3	V
V_{IL}	Input LOW Voltage				0.8			0.8	V

Table 7. AC Characteristics (V_{CC} = 3.135 V to 3.8 V, V_{EE} = 0 V)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Toggle Frequency			1			1			1	GHz
t_{PD}	Propagation Delay to Output Differential	150	350	500	175	360	550	200	380	600	ps
t_{SKEW}	Skew Output-to-Output Part-to-Part		20	30 190		20	30 190		20	30 190	ps ps
t_{JITTER}	Cycle-to-Cycle Jitter RMS (1σ)			1			1			1	ps
V_{outPP}	Output Peak-to-Peak Voltage	350	750		350	750		350	750		mV
t_r/t_f	Output Rise/Fall Time (20%–80% @ 50 MHz)	50		400	50		400	50		400	ps

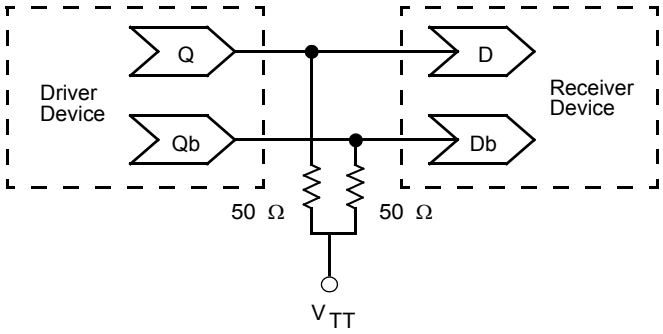
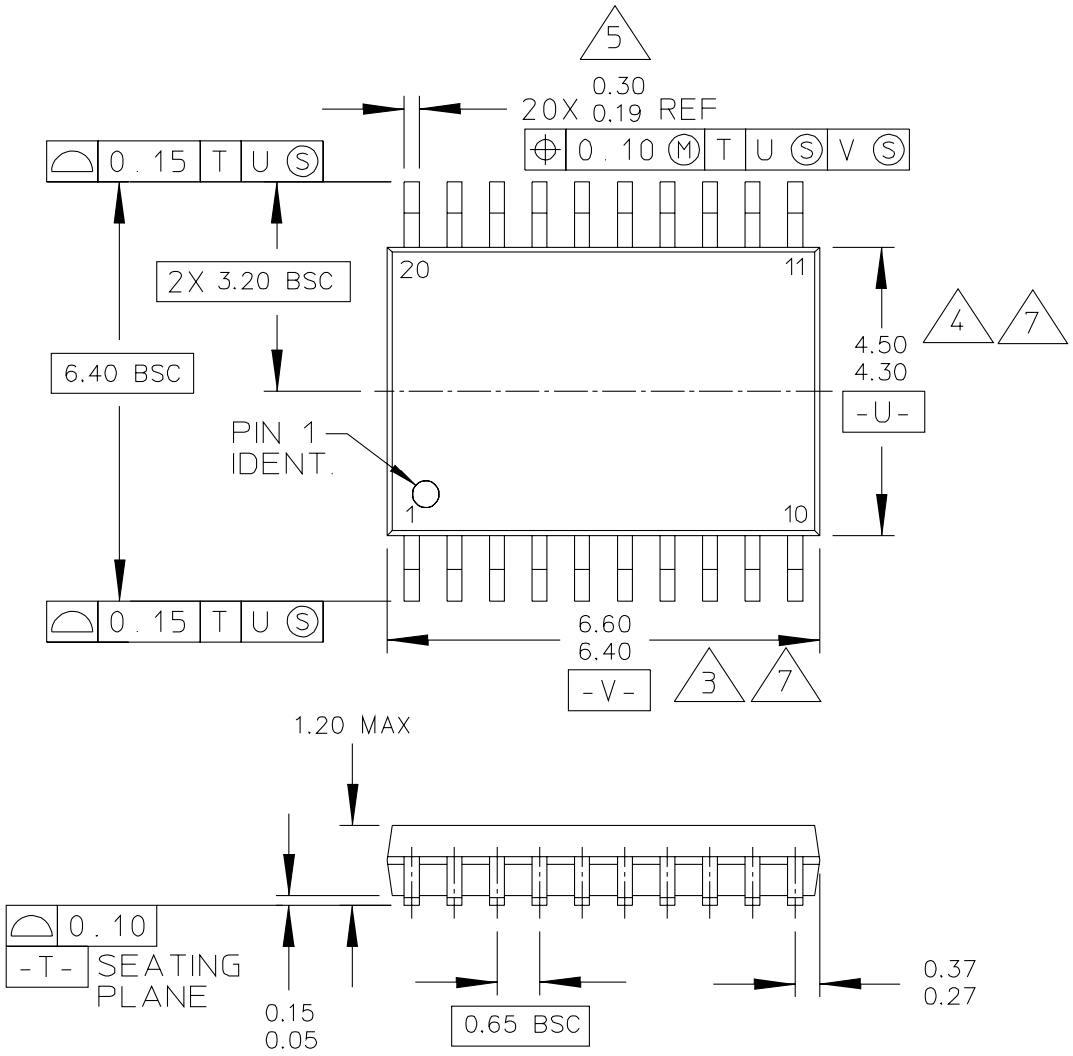


Figure 3. Typical Termination for Output Driver and Device Evaluation

PACKAGE DIMENSIONS



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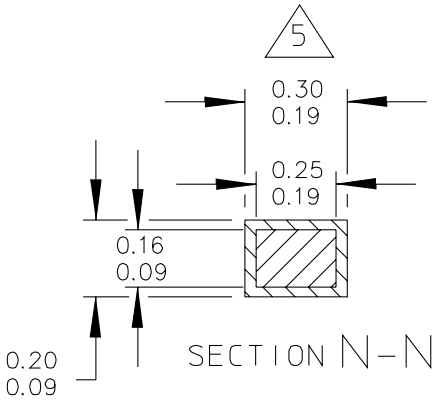
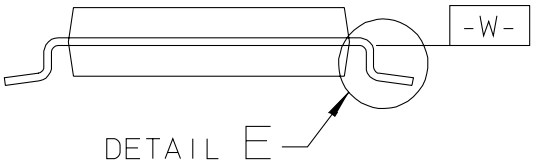
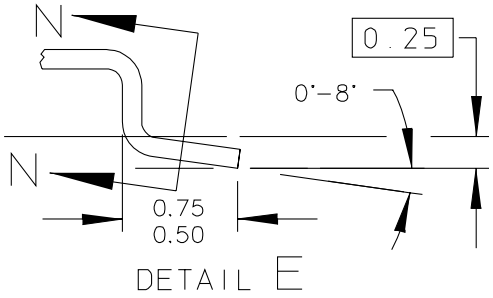
CASE 948E-02
ISSUE C
20-LEAD TSSOP PACKAGE

PACKAGE DIMENSIONS







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PACKAGE DIMENSIONS

NOTES:

1. CONTROLLING DIMENSION: MILLIMETER
2. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M-1982.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
5. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF THE DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSIONS ARE TO BE DETERMINED AT DATUM PLANE -W-.

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