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# 2.5V LVDS 1:6 CLOCK BUFFER TERABUFFER™ II

# IDT5T9306

### FEATURES:

- Guaranteed Low Skew < 25ps (max)
- Very low duty cycle distortion < 125ps (max)
- High speed propagation delay < 1.75ns (max)
- Additive phase jitter, RMS 0.159ps (typical) @ 125MHz
- Up to 1GHz operation
- Selectable inputs
- Hot insertable and over-voltage tolerant inputs
- 3.3V / 2.5V LVTTL, HSTL, eHSTL, LVEPECL (2.5V), LVPECL (3.3V), CML, or LVDS input interface
- Selectable differential inputs to six LVDS outputs
- Power-down mode
- 2.5V VDD
- Available in VFQFPN package

#### APPLICATIONS:

Clock distribution

# DESCRIPTION:

The IDT5T93062.5V differential clock buffer is a user-selectable differential input to six LVDS outputs. The fanout from a differential input to six LVDS outputs reduces loading on the preceding driver and provides an efficient clock distribution network. The IDT5T9306 can act as a translator from a differential HSTL, eHSTL, LVEPECL (2.5V), LVPECL (3.3V), CML, or LVDS input to LVDS outputs. A single-ended 3.3V/2.5V LVTTL input can also be used to translate to LVDS outputs. The redundant input capability allows for an asynchronous change-over from a primary clock source to a secondary clock source. Selectable reference inputs are controlled by SEL.

The IDT5T9306 outputs can be asynchronously enabled/disabled. When disabled, the outputs will drive to the value selected by the GL pin. Multiple power and grounds reduce noise.



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# FUNCTIONAL BLOCK DIAGRAM

#### PINCONFIGURATION



TOP VIEW

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#### Symbol Description Max Unit VDD Power Supply Voltage -0.5 to +3.6 ٧ Vı ٧ Input Voltage -0.5 to +3.6 Vo Output Voltage<sup>(2)</sup> -0.5 to VDD +0.5 V °C Tstg Storage Temperature -65 to +150 °C TJ Junction Temperature 150

#### ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

#### NOTES:

 Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2. Not to exceed 3.6V.

### **RECOMMENDED OPERATING RANGE**

Symbol	Description	Min.	Тур.	Max.	Unit
TA	Ambient Operating Temperature	-40	+25	+85	°C
Vdd	Internal Power Supply Voltage	2.3	2.5	2.7	V

Symbol

CIN

NOTE:

CAPACITANCE<sup>(1)</sup> (TA =  $+25^{\circ}$ C, F = 1.0MHz)

1. This parameter is measured at characterization but not tested

Min

Typ.

Max.

3

Unit

рF

Parameter

Input Capacitance

#### PINDESCRIPTION

Symbol	I/O	Туре	Description
A[1:2]	Ι	Adjustable <sup>(1,4)</sup>	Clock input. A[1:2] is the "true" side of the differential clock input.
<b>A</b> [1:2]	I	Adjustable <sup>(1,4)</sup>	Complementary clock inputs. A[1:2] is the complementary side of A[1:2]. For LVTTL single-ended operation, A[1:2] should be set to the desired toggle voltage for A[1:2]:
			3.3V LVTTL VREF = 1650mV
			2.5V LVTTL VREF = 1250mV
G	I	LVTTL	Gate control for differential outputs $Q_1$ and $Q_1$ through $Q_6$ and $Q_6$ . When G is LOW, the differential outputs are active. When G is HIGH, the differential outputs are asynchronously driven to the level designated by $GL^{(2)}$ .
GL	I	LVTTL	Specifies output disable level. If HIGH, "true" outputs disable HIGH and "complementary" outputs disable LOW. If LOW, "true" outputs disable LOW and "complementary" outputs disable HIGH.
Qn	0	LVDS	Clock outputs
Qn	0	LVDS	Complementary clock outputs
SEL	Ι	LVTTL	Reference clock select. When LOW, selects A2 and A2. When HIGH, selects A1 and A1.
FD	I	LVTTL	Power-down control. Shuts off entire chip. If LOW, the device goes into low power mode. Inputs and outputs are disabled. Both "true" and "complementary" outputs will pull to VDD. Set HIGH for normal operation. <sup>(3)</sup>
Vdd		PWR	Power supply for the device core and inputs
GND		PWR	Power supply return for all power
NC			No connect; recommended to connect to GND

#### NOTES:

1. Inputs are capable of translating the following interface standards:

Single-ended 3.3V and 2.5V LVTTL levels

Differential HSTL and eHSTL levels

Differential LVEPECL (2.5V) and LVPECL (3.3V) levels

Differential LVDS levels

Differential CML levels

2. Because the gate controls are asynchronous, runt pulses are possible. It is the user's responsibility to either time the gate control signals to minimize the possibility of runt pulses or be able to tolerate them in down stream circuitry.

3. It is recommended that the outputs be disabled before entering power-down mode. It is also recommended that the outputs remain disabled until the device completes powerup after asserting PD.

4. The user must take precautions with any differential input interface standard being used in order to prevent instability when there is no input signal.

#### IDT<sup>™</sup>/ICS<sup>™</sup> LVDS CLOCK BUFFER TERABUFFER<sup>™</sup> II

# DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE FOR LVTTL<sup>(1)</sup>

Symbol	Parameter	Test Conditions	Min.	Typ. <sup>(2)</sup>	Max	Unit	
Input Characteristics							
Ін	Input HIGH Current	$V_{DD} = 2.7 V$	—	—	±5	μA	
lı.	Input LOW Current	$V_{DD} = 2.7 V$	—	-	±5		
Viк	Clamp Diode Voltage	VDD = 2.3V, IN = -18mA	—	- 0.7	- 1.2	V	
Vin	DC Input Voltage		- 0.3	_	+3.6	V	
Vih	DC Input HIGH		1.7	_	_	V	
Vil	DC Input LOW		-	_	0.7	V	
Vтні	DC Input Threshold Crossing Voltage		-	Vdd /2	_	V	
VREF	Single-Ended Reference Voltage <sup>(3)</sup>	3.3V LVTTL	_	1.65	_	V	
		2.5VLVTTL	—	1.25	—		

NOTES:

1. See RECOMMENDED OPERATING RANGE table.

2. Typical values are at VDD = 2.5V,  $+25^{\circ}C$  ambient.

3. For  $A_{[1:2]}$  single-ended operation,  $A_{[1:2]}$  is tied to a DC reference voltage.

# DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE FOR DIFFERENTIAL INPUTS<sup>(1)</sup>

Symbol	Parameter	Test Conditions	Min.	Typ. <sup>(2)</sup>	Max	Unit		
Input Charac	Input Characteristics							
Ін	Input HIGH Current	$V_{DD} = 2.7 V$	—	—	±5	μA		
lı.	Input LOW Current	$V_{DD} = 2.7 V$	—	—	±5			
Vik	Clamp Diode Voltage	Vdd = 2.3V, Iin = -18mA	—	- 0.7	- 1.2	V		
Vin	DC Input Voltage		- 0.3	—	+3.6	V		
Vdif	DC Differential Voltage <sup>(3)</sup>		0.1	—	—	V		
Vсм	DC Common Mode Input Voltage <sup>(4)</sup>		0.05	_	Vdd	V		

NOTES:

1. See RECOMMENDED OPERATING RANGE table.

2. Typical values are at VDD = 2.5V, +25°C ambient.

3. VDIF specifies the minimum input differential voltage (VTR - VCP) required for switching where VTR is the "true" input level and VCP is the "complement" input level. The DC differential voltage must be maintained to guarantee retaining the existing HIGH or LOW input. The AC differential voltage must be achieved to guarantee switching to a new state.

4. Vcm specifies the maximum allowable range of (VTR + VcP) /2.

# DC ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING RANGE FOR LVDS<sup>(1)</sup>

Symbol	Parameter	Test Conditions	Min.	Typ. <sup>(2)</sup>	Max	Unit		
Output Char	Output Characteristics							
Vot(+)	Differential Output Voltage for the True Binary State		247	—	454	mV		
Vot(-)	Differential Output Voltage for the False Binary State		247	_	454	mV		
$\Delta V$ от	Change in VoT Between Complementary Output States		—	_	50	mV		
Vos	Output Common Mode Voltage (Offset Voltage)		1.125	1.2	1.375	V		
$\Delta Vos$	Change in Vos Between Complementary Output States		—	_	50	mV		
los	Outputs Short Circuit Current	Vout + and Vout - = 0V	—	12	24	mA		
losd	Differential Outputs Short Circuit Current	Vout + = Vout -	—	6	12	mA		

NOTES:

1. See RECOMMENDED OPERATING RANGE table.

2. Typical values are at VDD = 2.5V, TA =  $+25^{\circ}C$  ambient.

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# DIFFERENTIAL INPUT AC TEST CONDITIONS FOR HSTL

Symbol	Parameter	Value	Units
Vdif	Input Signal Swing <sup>(1)</sup>	1	V
Vx	Differential Input Signal Crossing Point <sup>(2)</sup>	750	mV
Dн	Duty Cycle	50	%
Vтні	Input Timing Measurement Reference Level <sup>(3)</sup>	Crossing Point	V
tR, tF	Input Signal Edge Rate <sup>(4)</sup>	2	V/ns

NOTES:

1. The 1V peak-to-peak input pulse level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the VDIF (AC) specification under actual use conditions.

2. A 750mV crossing point level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the Vx specification under actual use conditions.

3. In all cases, input waveform timing is marked at the differential cross-point of the input signals.

4. The input signal edge rate of 2V/ns or greater is to be maintained in the 20% to 80% range of the input waveform.

# DIFFERENTIAL INPUT AC TEST CONDITIONS FOR eHSTL

Symbol	Parameter	Value	Units
Vdif	Input Signal Swing <sup>(1)</sup>	1	V
Vx	Differential Input Signal Crossing Point <sup>(2)</sup>	900	mV
Dн	Duty Cycle	50	%
Vтні	Input Timing Measurement Reference Level <sup>(3)</sup>	Crossing Point	V
tR, tF	Input Signal Edge Rate <sup>(4)</sup>	2	V/ns

NOTES:

1. The 1V peak-to-peak input pulse level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the VDIF (AC) specification under actual use conditions.

2. A 900mV crossing point level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the Vx specification under actual use conditions.

3. In all cases, input waveform timing is marked at the differential cross-point of the input signals.

4. The input signal edge rate of 2V/ns or greater is to be maintained in the 20% to 80% range of the input waveform.

# DIFFERENTIAL INPUT AC TEST CONDITIONS FOR LVEPECL (2.5V) AND LVPECL (3.3V)

Symbol	Parameter		Value	Units
Vdif	Input Signal Swing <sup>(1)</sup>		732	mV
Vx	Differential Input Signal Crossing Point <sup>(2)</sup>	LVEPECL	1082	mV
		LVPECL	1880	
Dн	Duty Cycle		50	%
Vтні	Input Timing Measurement Reference Level <sup>(3)</sup>		Crossing Point	V
tr, tr	Input Signal Edge Rate <sup>(4)</sup>		2	V/ns

NOTES:

1. The 732mV peak-to-peak input pulse level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the VDIF (AC) specification under actual use conditions.

2. 1082mV LVEPECL (2.5V) and 1880mV LVPECL (3.3V) crossing point levels are specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the Vx specification under actual use conditions.

3. In all cases, input waveform timing is marked at the differential cross-point of the input signals.

4. The input signal edge rate of 2V/ns or greater is to be maintained in the 20% to 80% range of the input waveform.

# DIFFERENTIAL INPUT AC TEST CONDITIONS FOR LVDS

Symbol	Parameter	Value	Units
Vdif	Input Signal Swing <sup>(1)</sup>	400	mV
Vx	Differential Input Signal Crossing Point <sup>(2)</sup>	1.2	V
Dн	Duty Cycle	50	%
Vтні	Input Timing Measurement Reference Level <sup>(3)</sup>	Crossing Point	V
tR, tF	Input Signal Edge Rate <sup>(4)</sup>	2	V/ns

NOTES:

1. The 400mV peak-to-peak input pulse level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the VDIF (AC) specification under actual use conditions.

2. A 1.2V crossing point level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the Vx specification under actual use conditions.

3. In all cases, input waveform timing is marked at the differential cross-point of the input signals.

4. The input signal edge rate of 2V/ns or greater is to be maintained in the 20% to 80% range of the input waveform.

# AC DIFFERENTIAL INPUT SPECIFICATIONS<sup>(1)</sup>

Symbol	Parameter	Min.	Тур.	Max	Unit
Vdif	AC Differential Voltage <sup>(2)</sup>	0.1		3.6	V
Vix	Differential Input Crosspoint Voltage	0.05	—	Vdd	V
Vсм	Common Mode Input Voltage Range <sup>(3)</sup>	0.05	—	Vdd	V
VIN	InputVoltage	- 0.3		+3.6	V

NOTES:

1. The output will not change state until the inputs have crossed and the minimum differential voltage range defined by VDIF has been met or exceeded.

2. VDIF specifies the minimum input voltage (VTR - VCP) required for switching where VTR is the "true" input level and VCP is the "complement" input level. The AC differential voltage must be achieved to guarantee switching to a new state.

3. Vcm specifies the maximum allowable range of (VTR + VcP) /2.

#### POWER SUPPLY CHARACTERISTICS FOR LVDS OUTPUTS<sup>(1)</sup>

Symbol	Parameter	Test Conditions	Тур.	Max	Unit
Iddq	Quiescent VDD Power Supply Current	VDD = Max., All Input Clocks = LOW <sup>(2)</sup>	-	240	mA
		Outputs enabled			
Ітот	Total Power Vod Supply Current	VDD = 2.7V., FREFERENCE CLOCK = 1GHz	_	250	mA
IPD	Total Power Down Supply Current	PD=LOW	—	5	mA

NOTES:

1. These power consumption characteristics are for all the valid input interfaces and cover the worst case conditions.

2. The true input is held LOW and the complementary input is held HIGH.

# AC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE<sup>(1,5)</sup>

Symbol	Parameter	Min.	Тур.	Max	Unit
Skew Parameters					
tsk(o)	Same Device Output Pin-to-Pin Skew <sup>(2)</sup>	—	—	25	ps
tsk(P)	Pulse Skew <sup>(3)</sup>	_	—	125	ps
tsk(PP)	Part-to-Part Skew <sup>(4)</sup>	_	_	300	ps
<b>Propagation Delay</b>				•	
<b>t</b> PLH	Propagation Delay A, A Crosspoint to Qn, Qn Crosspoint	_	1.25	1.75	ns
<b>t</b> PHL					
fo	Frequency Range <sup>(6)</sup>	_	_	1	GHz
Output Gate Enabl	e/Disable Delay				
<b>t</b> PGE	Output Gate Enable Crossing VTHI to Qn/Qn Crosspoint	_	—	3.5	ns
tPGD	Output Gate Disable Crossing VTHI to Qn/Qn Crosspoint Driven to GL Designated Level	_	_	3.5	ns
Power Down Tim	ing				
<b>t</b> PWRDN	PD Crossing VTHI to Qn = VDD, Qn = VDD	—	—	100	μS
<b>t</b> PWRUP	Output Gate Disable Crossing VTHI to Qn/Qn Driven to GL Designated Level	_	_	100	μS
<b>RMS Additive Pha</b>	se Jitter				
	RMS Additive Phase Jitter @ 25MHz (12kHz – 10MHz Integration Range)		0.541		ps
tır	RMS Additive Phase Jitter @ 125MHz (12kHz – 20MHz Integration Range)		0.159		ps
	RMS Additive Phase Jitter @ 156.25MHz (12kHz – 20MHz Integration Range)		0.185		ps
Output Rise/Fall T	Time .				
tR/tF	Output Rise/Fall Time <sup>(6)</sup> , (20% - 80%)	125		600	ps

NOTES:

1. AC propagation measurements should not be taken within the first 100 cycles of startup.

2. Skew measured between crosspoints of all differential output pairs under identical input and output interfaces, transitions and load conditions on any one device.

3. Skew measured is the difference between propagation delay times tPHL and tPLH of any differential output pair under identical input and output interfaces, transitions and load conditions on any one device.

4. Skew measured is the magnitude of the difference in propagation times between any single differential output pair of two devices, given identical transitions and load conditions at identical VDD levels and temperature.

5. All parameters are tested with a 50% input duty cycle.

6. Guaranteed by design but not production tested.

# DIFFERENTIAL ACTIMING WAVEFORMS



**Output Propagation and Skew Waveforms** 

#### NOTES:

1. Pulse skew is calculated using the following expression:

tsk(p) = | tphl - tplh |

- Note that the tPHL and tPLH shown above are not valid measurements for this calculation because they are not taken from the same pulse.
- 2. AC propagation measurements should not be taken within the first 100 cycles of startup.

#### IDT5T9306 2.5V LVDS 1:6 CLOCK BUFFER TERABUFFER™II



#### NOTE:

#### Differential Gate Disable/Enable Showing Runt Pulse Generation

1. As shown, it is possible to generate runt pulses on gate disable and enable of the outputs. It is the user's responsibility to time the G signal to avoid this problem.



#### Power Down Timing

#### NOTES:

1. It is recommended that outputs be disabled before entering power-down mode. It is also recommended that the outputs remain disabled until the device completes power-up after asserting PD.

2. The POWER DOWN TIMING diagram assumes that GL is HIGH.

3. It should be noted that during power-down mode, the outputs are both pulled to VDD. In the POWER DOWN TIMING diagram this is shown when Qn-Qn goes to VDIF = 0.

#### IDT<sup>™</sup>/ICS<sup>™</sup> LVDS CLOCK BUFFER TERABUFFER<sup>™</sup> II

# TEST CIRCUITS AND CONDITIONS



Test Circuit for Differential Input

DIFFERENTIAL	INPUTTEST	<b>CONDITIONS</b>
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Symbol	$V_{DD} = 2.5V \pm 0.2V$	Unit
Vтні	Crossing of A and A	V



Test Circuit for DC Outputs and Power Down Tests



Test Circuit for Propagation, Skew, and Gate Enable/Disable Timing

Symbol	$V_{DD} = 2.5V \pm 0.2V$	Unit
CL	O <sup>(1)</sup>	pF
	8(1,2)	
RL	50	Ω

#### LVDS OUTPUT TEST CONDITION

#### NOTES:

1. Specifications only apply to "Normal Operations" test condition. The TIA/EIA specification load is for reference only.

2. The scope inputs are assumed to have a 2pF load to ground. TIA/EIA - 644 specifies 5pF between the output pair. With CL = 8pF, this gives the test circuit appropriate 5pF equivalent load.

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#### RECOMMENDED LANDING PATTERN



NL 28 pin

NOTE: All dimensions are in millimeters.

July 23, 2002 Datasheet creation October 8, 2002 Page 1, entire page changed; page 2, both diagrams; page 3, Pin Description and notes; page 4, DC Cha. for LVPECL and Differential Input tables; page 6, DC Cha. and Power Supply tables; page 7, entire page; page 9, added note 3; page 10, entire page; page 10, entire page; page 11, entire page; page 12, Ordering Info; added 3 new pages (10 thru 12) of diagrams. October 10, 2002 Page 1, entire page changed; page 2, both diagrams; page 3, Pin Description and notes; page 7, AC Cha. table; page 8, added new LVPECL table; page 10, removed Input Clock Switching diagram; page 11, deleted entire page; page 12, changed Power Down Timing; page 15, Ordering Info. Page 2, added note 1 to TQFP TOP VIEW text; page 3, aded note 4 to Pin Description; page 4, replaced "Compliant devices October 24, 2002 must meet" with the text "This device meets" in four instances; page 5, Differential Input table, note 1, changed 1V to 732mV and replaced "Compliant devices must meet" with the text "This device meets"; page 6, DC Electrical table, Vdif row, changed Min. value to 0.1, and under Differential Input table replaced "Compliant devices must meet" with the text "This device meets" page 7, Power Supply table, replaced ((TBD)) with 800MHz, and under AC Electrical table, replaced ((TBD)) with 500; page 8, completely altered AC Differential table; page 12, LVDS Output table, replaced ((TBD)) with 3. November 1, 2002 Radical changes to entire document. December 12, 2002 Radical changes to entire document, using 5T9316 as a base. December 16, 2002 Throughout document, removed "Differential" from title; page 7, Power Supply table, changed Max values, changed FREFERENCE value; page 10, note 1, changed Gx to G. Page 2, corrected pinout diagram. May 8, 2003 August 7, 2003 Page 1, Features text, 3rd bullet, changed 2ns to 1.75ns, 4th bullet, changed 800MHz to 1GHz, and 7th bullet, added CML, on Description, 3rd line, added CML to list; page 4, Pin Descr., note 1, added "Differential CML levels", for Description of PD row, replaced 2nd sentence with "Both 'true' and 'complementary' output will pull to Vdd"; page 5, DC... for Differential Inputs table, removed note 5 and changed Vcm Max. from 3.5 to Vdd; page 7, Power Supply table, changed 800MHz to 1GHz; page 8, AC Differential table, changed Vix and Vcm Max specs from 3.5V to Vdd, removed notes 4 and 5, and placed entire table on page 7, for AC Elect. table, added notes 5 and 6, changed ((TBD)) to 300ps, tplh Type to 1.25ns, and Max from 2ns to 1.75ns, and changed fo Max from 800MHz to 1GHz. Page 1, Features, 7th bullet, added "3.3V / 2,5V LVTTL" to front, Description, added to 1st paragraph "A single-ended October 2, 2003 3.3V / 2.5V LVTTL input can also be used to translate to LVDS outputs."; page 4, Pin Description table, added large block of text to 2nd row, added "Single-ended 3.3V and 2.5V LVTTL levels" to note 1; page 5, DC for LVTTL table, added Vref row and note 3, for DC for LVDS table, changed los ratings from 5 Typ, 7.5 Max to 12 Typ, 24 Max, and changed losd ratings from 5 Typ, 7.5 Max to 6 Typ, 12 Max; page 7, Power Supply table, changed lpd from 3 to 5. Page 2, changed pin 22 to NC; page 3, changed pin 25 to NC; page 4, added NC row to Pin Description. March 26, 2004 June 22, 2004 Removed TQFP package. Inserted a page before Ordering Info and added Landing Pattern. October 26, 2004 October 27, 2004 Added note to Landing Pattern. October 29, 2004 Changed landing pattern diagram. March 9, 2005 Page 6, switched Iddq and Itot values. Page 7, added Additive Phase Jitter, RMS specs to the AC Electrical Characterisitcs Table. October 23, 2007 Page 7, added Rise/Fall Time spec. to the AC Electrical Characteristics Table. April 15, 2008

#### **ORDERING INFORMATION**



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#### **Corporate Headquarters**

Integrated Device Technology, Inc. 6024 Silver Creek Valley Road San Jose, CA 95138 United States 800-345-7015 (inside USA) +408-284-8200 (outside USA)



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