Sup*IR*Buck™

USER GUIDE FOR IR3802 EVALUATION BOARD

DESCRIPTION

The IR3802 is a synchronous buck converter, providing a compact, high performance and flexible solution in a small 5mmx6mm Power QFN package.

Key features offered by the IR3802 include programmable soft-start ramp, precision 0.6V reference voltage, thermal protection, fixed 600kHz switching frequency requiring no external component, input under-voltage lockout for proper start-up, and pre-bias start-up.

An output over-current protection function is implemented by sensing the voltage developed across the on-resistance of the synchronous rectifier MOSFET for optimum cost and performance.

This user guide contains the schematic and bill of materials for the IR3802 evaluation board. The guide describes operation and use of the evaluation board itself. Detailed application information for IR3802 is available in the IR3802 data sheet.

BOARD FEATURES

- V_{in} = +12V (13.2V Max)
- V_{out} = +3.3V @ 0- 4A
- L = 3.3uH
- C_{in}= 1x10uF (ceramic 1206)
- C_{out}= 1x22uF (ceramic 0805), 1x220uF/6.3V (SP-Cap)

CONNECTIONS and OPERATING INSTRUCTIONS

A well regulated +12V input supply should be connected to VIN+ and VIN-. A maximum 4A load should be connected to VOUT+ and VOUT-. The connection diagram is shown in Fig. 1 and inputs and outputs of the board are listed in Table I.

IR3802 has two input supplies, one for biasing (Vcc) and the other as input voltage (Vin). These inputs are connected on the board with a 330 ohm resistor (R13). Separate supplies can be applied to these inputs. Vcc input cannot be connected unless R13 is removed. Vcc input should be a well regulated 5V-12V supply and it would be connected to Vcc+ and Vcc-.

Table I. Connections

Connection	Signal Name
VIN+	V_{in} (+12V)
VIN-	Ground of V_{in}
Vcc+	Optional Vcc input
Vcc-	Ground for Optional Vcc input
VOUT-	Ground of V_{out}
VOUT+	V_{out} (+3.3V)

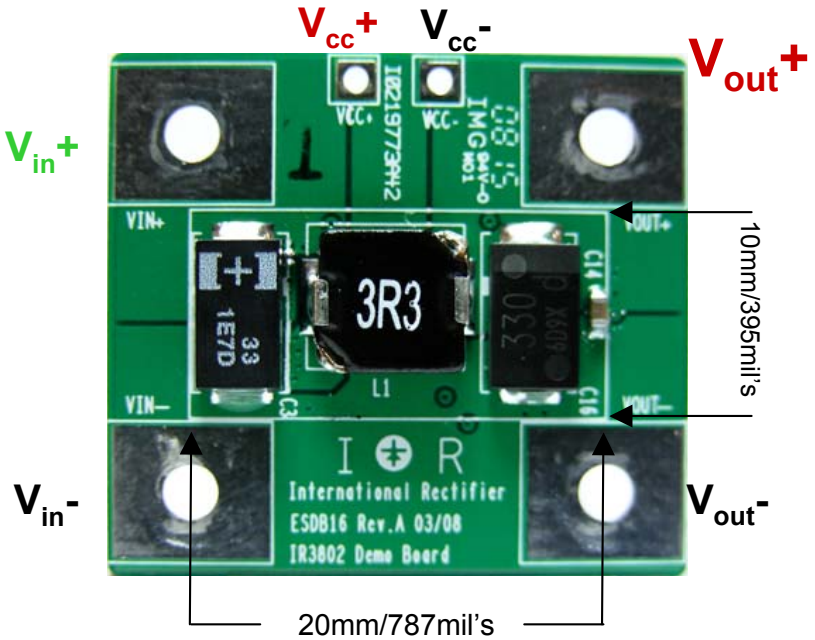
LAYOUT

The PCB is a 4-layer board. All of layers are 2 Oz. copper. The IR3802A SupIRBuck and all of the passive components are mounted on the bottom side of the board. The Inductor, Input and Output Bulk Capacitors are located on the top side of the board.

Power supply decoupling capacitors, the charge-pump capacitor and feedback components are located close to IR3802A. The feedback resistors are connected to the output voltage at the point of regulation and are located close to the SupIRBuck.

To improve efficiency, the circuit board is designed to minimize the length of the on-board power ground current path.

Connection Diagram



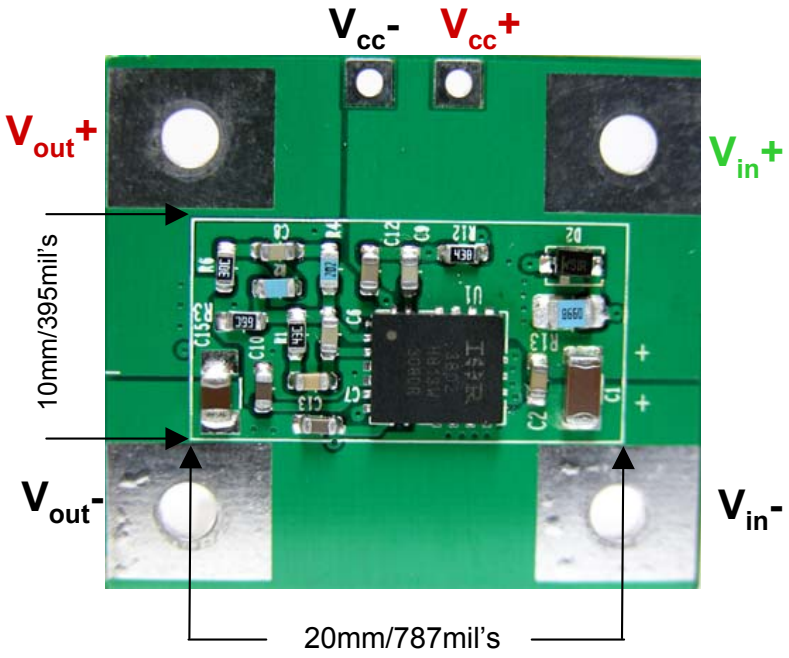


Fig. 1: Connection diagram of IR3802A evaluation board

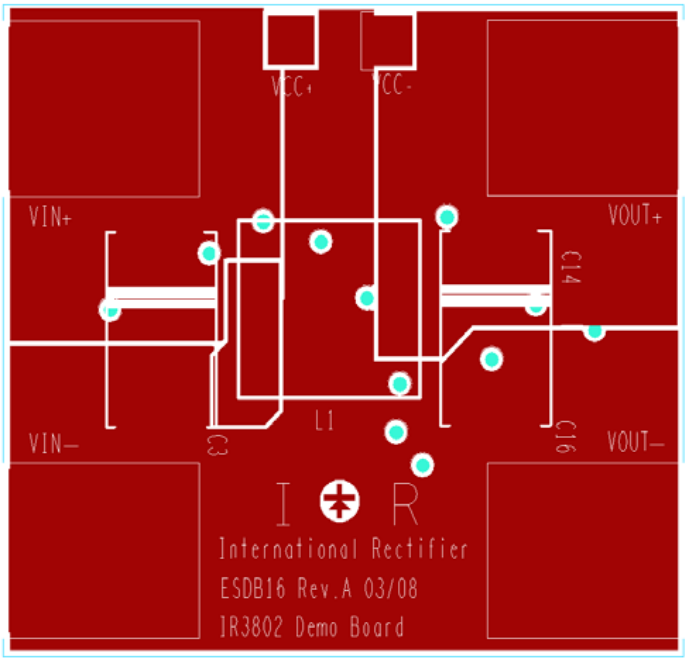


Fig. 2: Board layout, top overlay

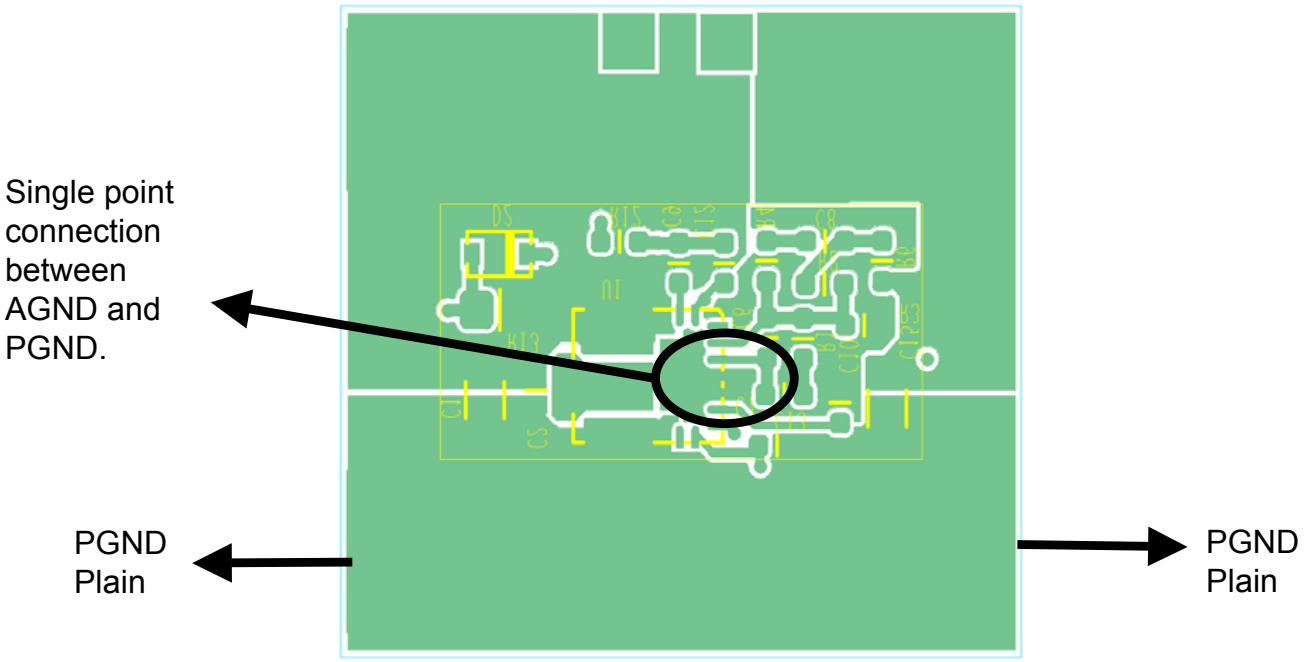


Fig. 3: Board layout, bottom overlay (rear view)

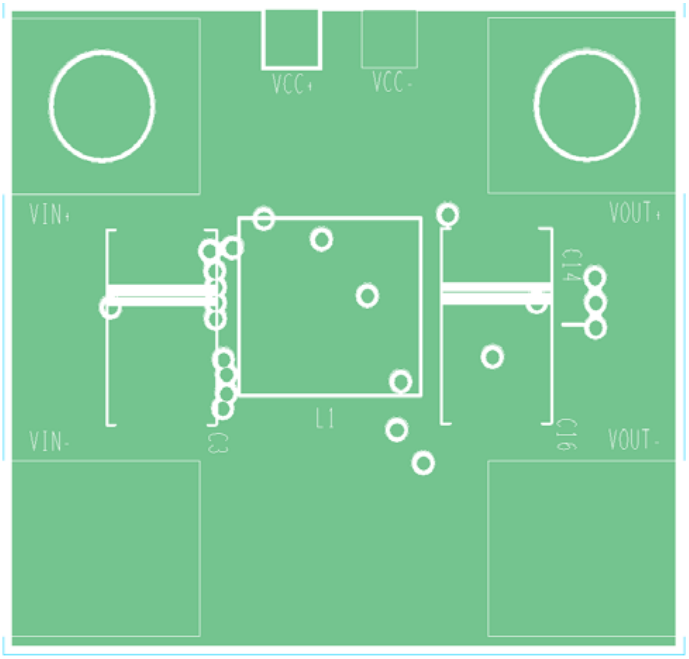


Fig. 4: Board layout, mid-layer I.

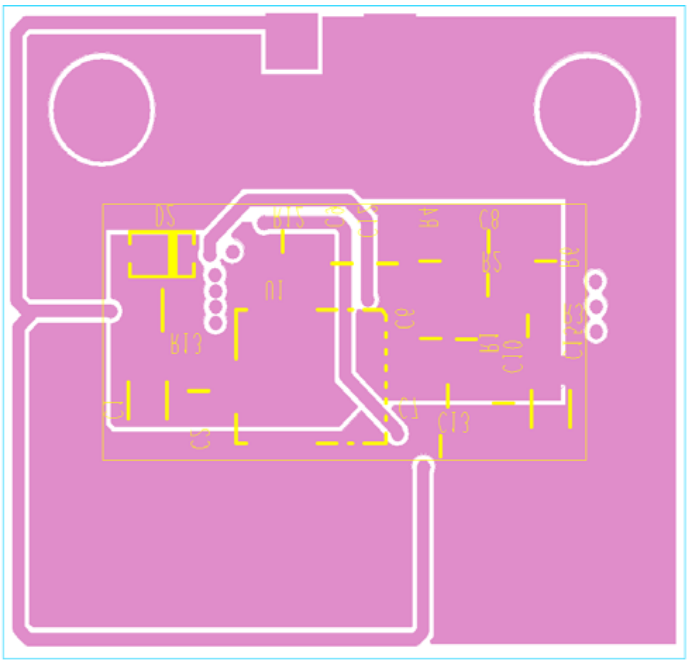


Fig. 5: Board layout, mid-layer II.

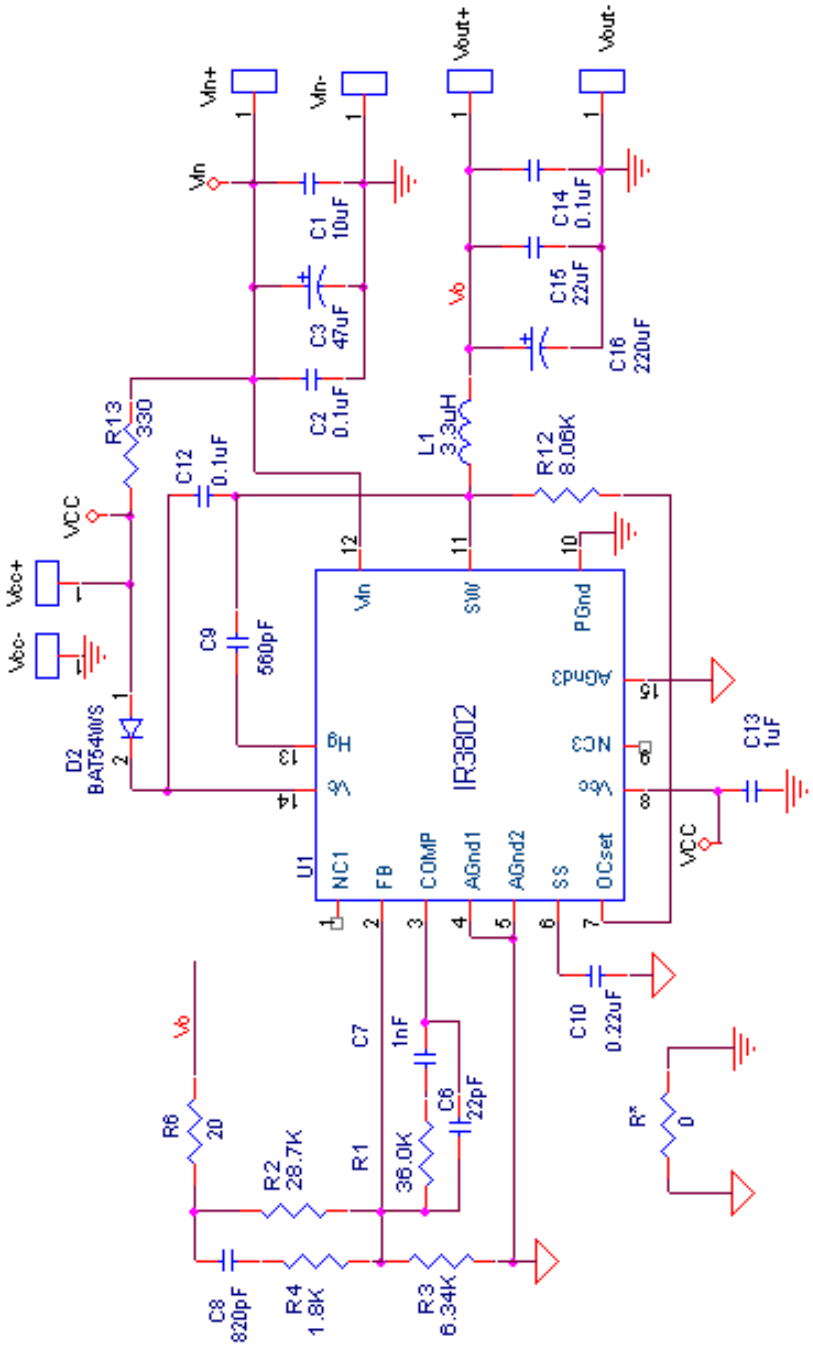


Fig. 6: Schematic of the IR3802 evaluation board

Bill of Materials

Item Number	Quantity	Part Reference	Value	Description	Manufacturer	Part Number
1	1	B1	ESDB016,Rev A	ESDB016,Rev A, PCB	International Rectifier	ESDB016,Rev A
2	1	C1	10uF	Ceramic,16V,1206,X7R,10%	TDK Corporation	C3216X7R1C106K
3	3	C2 C12 C14	0.1uF	Ceramic,25V,0603,X7R,10%	Panasonic - ECG	ECJ-1VB1E104K
4	1	C3	47uF	Poscap,16V,D2,Polomer-Aluminum	Sanyo	16TQC47M
5	1	C6	22pF	Ceramic,50V,0603,NPO,5%	Panasonic - ECG	ECJ-1VC1H220J
6	1	C7	1000pF	Ceramic,50V,0603,C0G,10%	Kemet	C0603C102J5GACTU
7	1	C8	820pF	Ceramic,50V,0603,X7R,10%	Murata	GRM188R71H821KA01D
8	1	C9	560pF	Ceramic,50V,0603,X7R,10%	Murata	GRM188R71H561KA01D
9	1	C10	0.22uF	Ceramic,10V,0603,X5R,10%	Panasonic - ECG	ECJ-1VB1A224K
10	1	C13	1uF	Ceramic,16V,0603,X5R,10%	Panasonic - ECG	ECJ-BVB1C105K
11	1	C15	22uF	Ceramic,6.3V,0805,X5R,20%	TDK	C2012X5R0J226M
12	1	C16	220uF	SP-Cap,4.0V,D4,Polymer-Aluminum	Panasonic	EEFUE0G221XE
13	1	D2	BAT54WS	Diode,Schotky,40V,SOD323,200mA	International Rectifier	BAT54WS
14	1	L1	3.3uH	SMT-Inductor,18mOhms,7.5x7.5mm,20%	ACT	STS704-3R3M
15	1	R1	36.0K	Thick-film,0603,1/10W,1%	Panasonic - ECG	ERJ-3EKF3602V
16	1	R2	28.7K	Thick-film,0603,1/10W,1%	Rohm	MCR03EZPFX2872
17	1	R3	6.34K	Thick-film,0603,1/10W,1%	Rohm	MCR03EZPFX6341
18	1	R4	1.8K	Thick-film,0603,1/10W,1%	Rohm	MCR03EZPFX1801
19	1	R6	20	Thick-film,0603,1/10 W,1%	Vishey/Dale	CRCW060320R0FKEA
20	1	R12	8.06K	Thick-film,0603,1/10 W,1%	Rohm	MCR03EZPFX8061
21	1	R13	330	Thick-film,0805,1/8W,1%	Rohm	MCR10EZPF3300
22	1	U1	IR3802	IR3802, Controller,PQFN,5x6mm	International Rectifier	IR3802

TYPICAL OPERATING WAVEFORMS

Vin=12.0V, Vcc = 6.3V, Vo=3.3V, Io=0- 4A, Room Temperature, No Air Flow

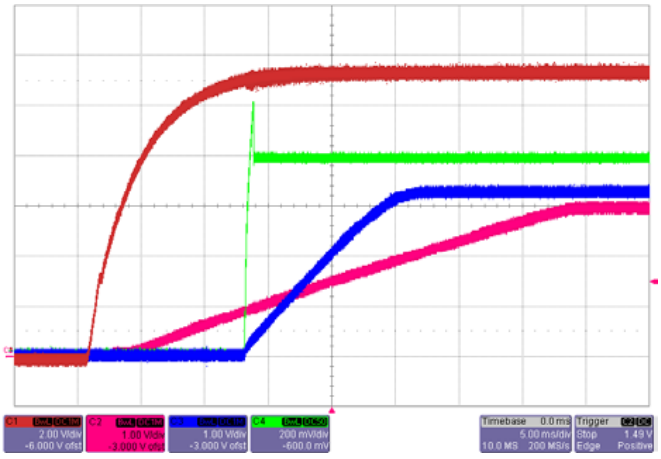


Fig. 7: Start up at 4A Load
Ch_1:V_{in}, Ch_2:V_{SS}, Ch_3:V_{out}, Ch_4:I_{out}

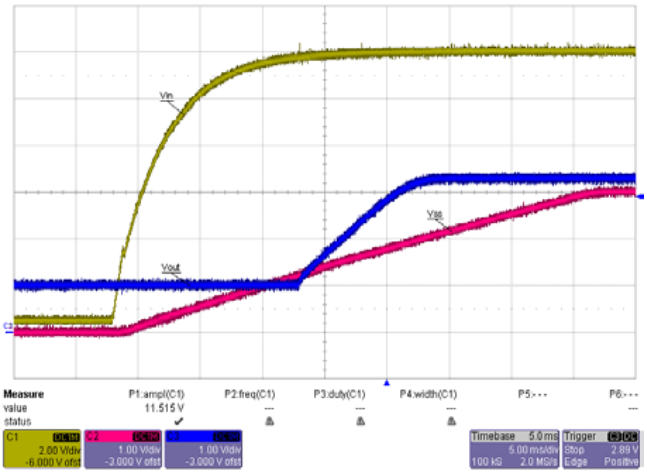


Fig. 8: Pre-Bias Start up, 0A Load
Ch_1:V_{in}, Ch_2:V_{SS}, Ch_3:V_{out}

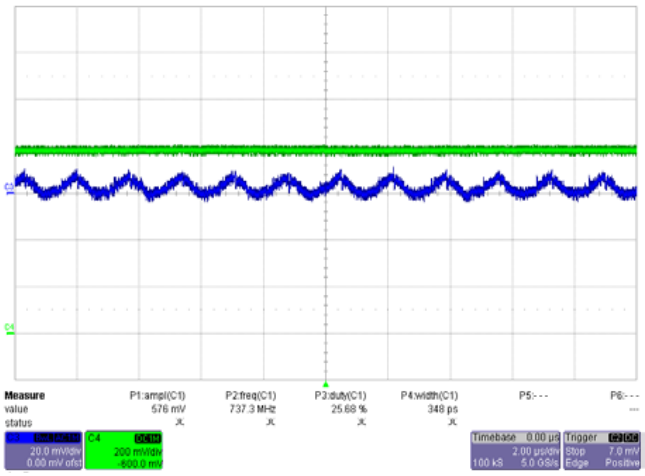


Fig. 9: Output Voltage Ripple, 4A load
Ch_1: V_{out} , Ch_4: I_{out}

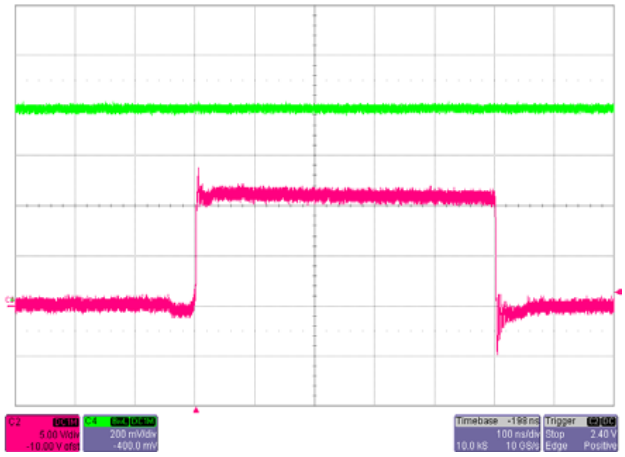


Fig. 10: Inductor node at 4A load
Ch_1:LX, Ch_4:I_{out}

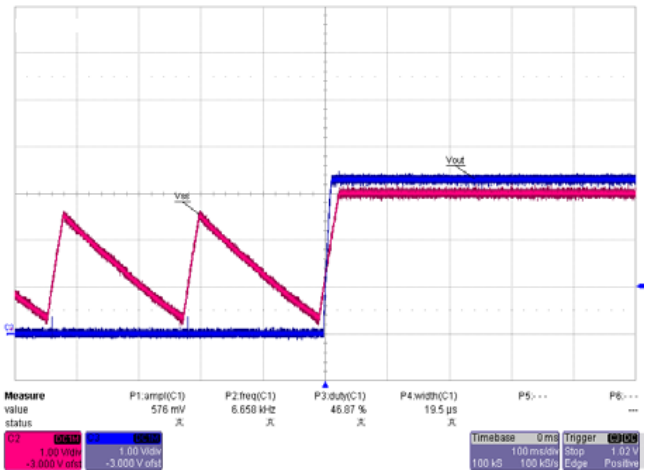
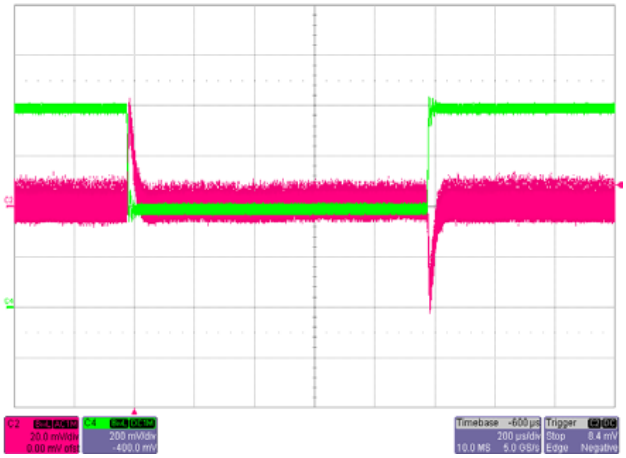
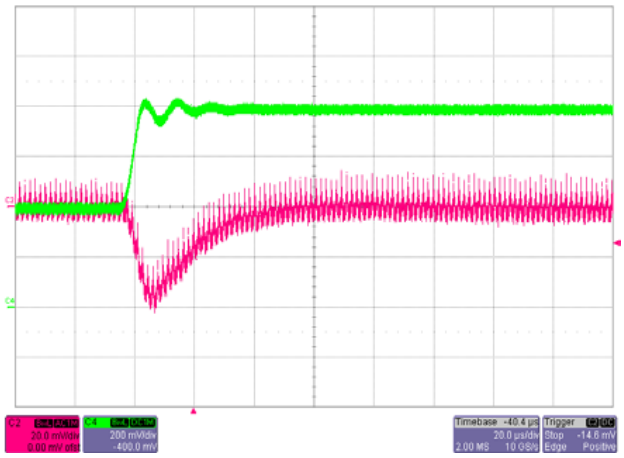


Fig. 11: Short (Hiccup) Recovery
Ch_1:V_{SS} , Ch_2:V_{out}

TYPICAL OPERATING WAVEFORMS
Vin=12.0V, Vcc = 6.3V, Vo=3.3V, Io=0- 4A, Room Temperature, No Air Flow





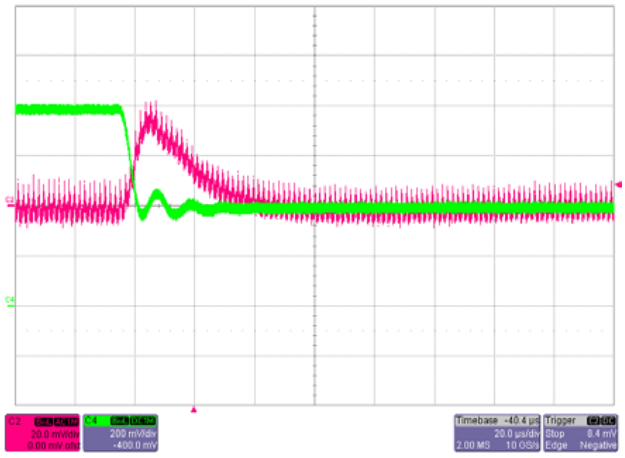


Fig. 12: Transient Response, 2A to 4A step
Ch_1:V_{out}, Ch_4:I_{out}

TYPICAL OPERATING WAVEFORMS
Vin=12.0V, Vcc = 6.3V, Vo=3.3V, Io=0- 4A, Room Temperature, No Air Flow

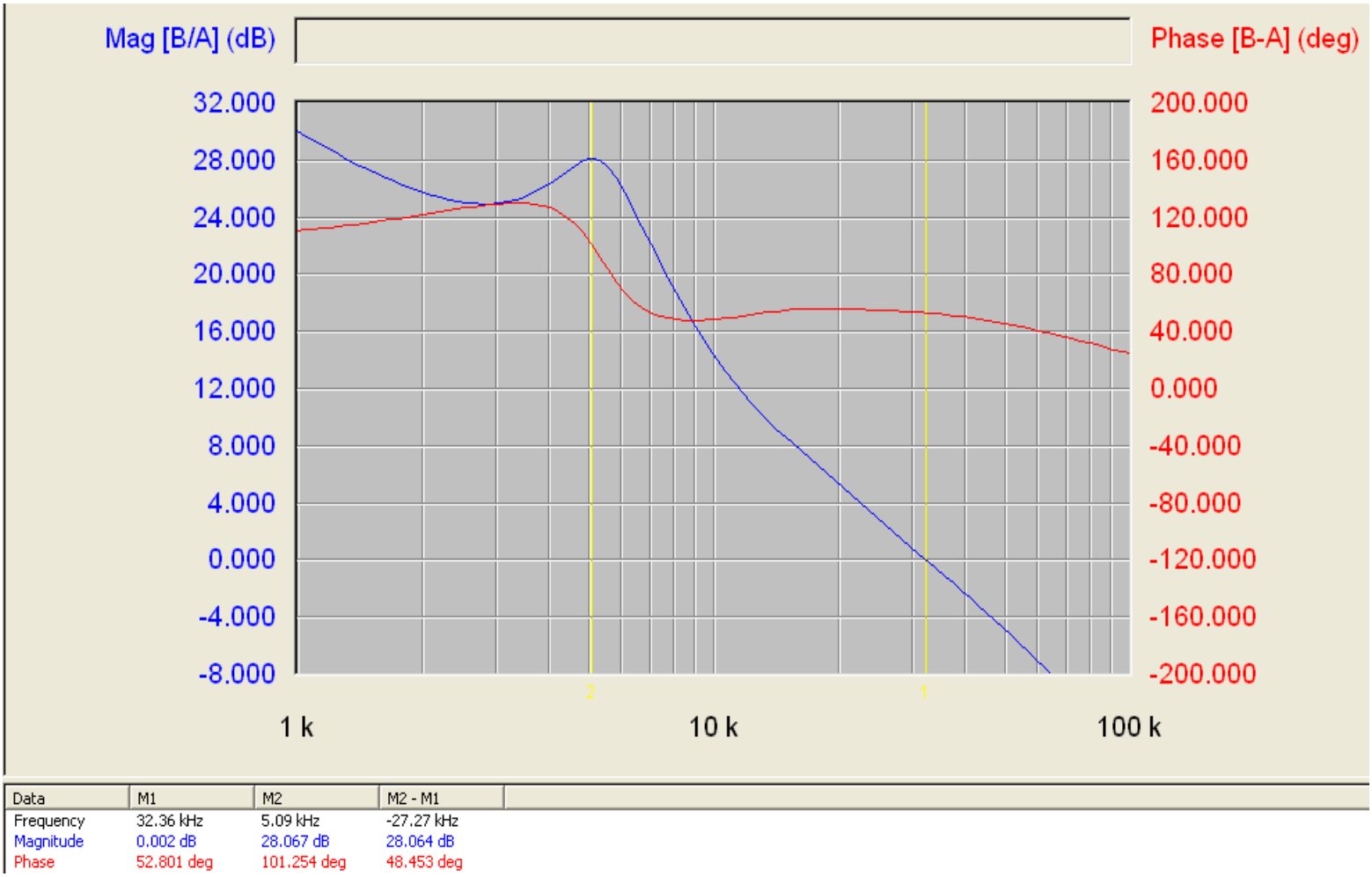


Fig. 13: Bode Plot at 4A load shows a bandwidth of 32+kHz and phase margin of 52+degrees

TYPICAL OPERATING WAVEFORMS
Vin=12.0V, Vcc = 6.3V, Vo=3.3V, Io=0- 4A, Room Temperature, No Air Flow

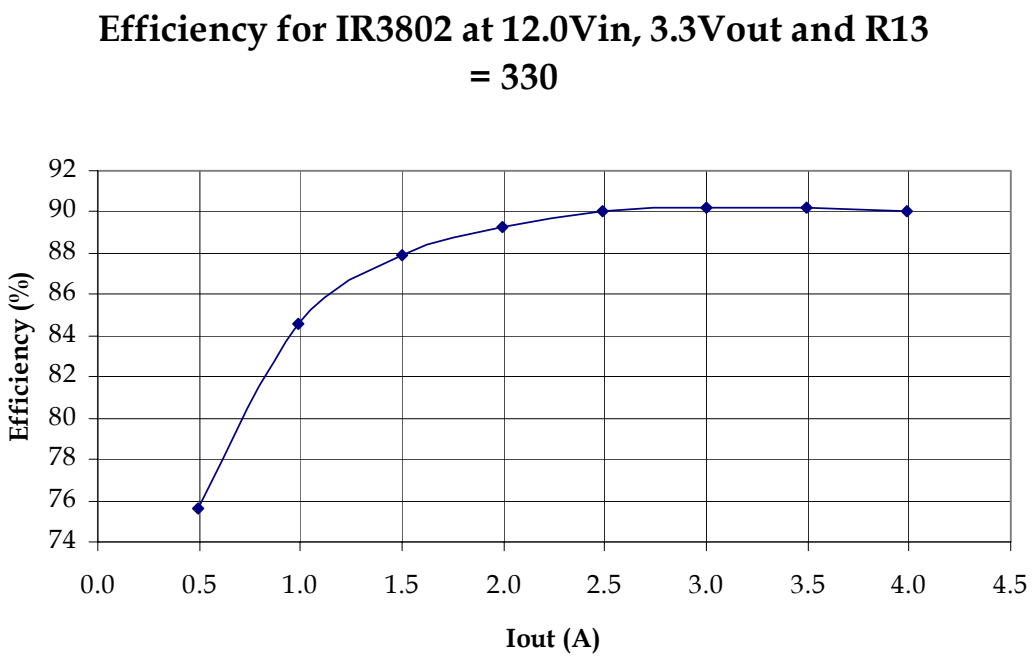


Fig.14: Efficiency versus load current

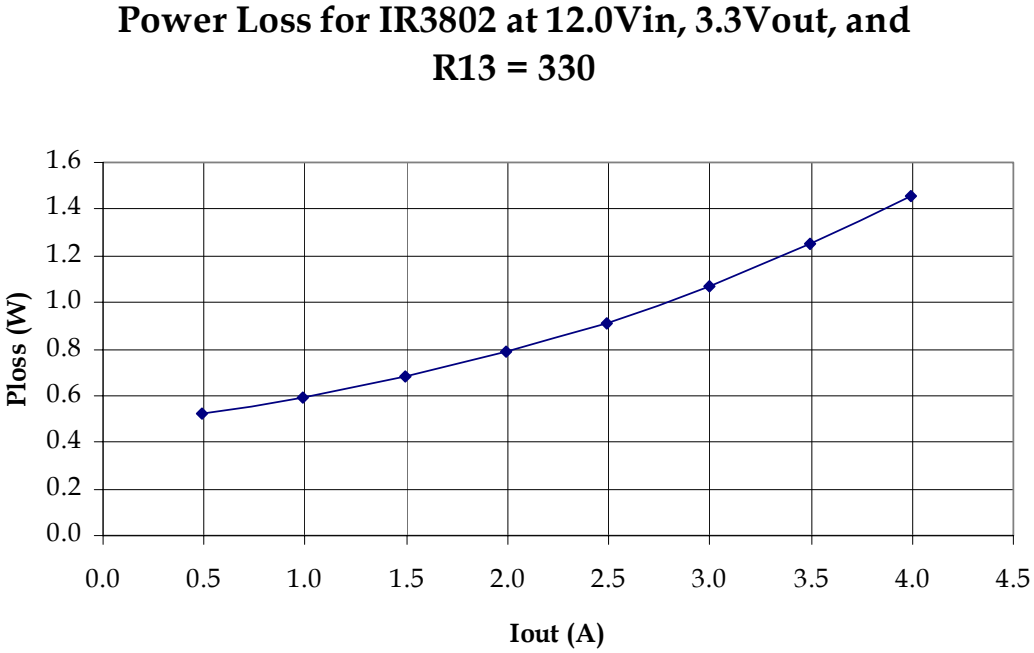


Fig.15: Power loss versus load current

TYPICAL OPERATING WAVEFORMS
Vin=12.0V, Vcc = 6.3V, Vo=3.3V, Io=0- 4A, Room Temperature, No Air Flow

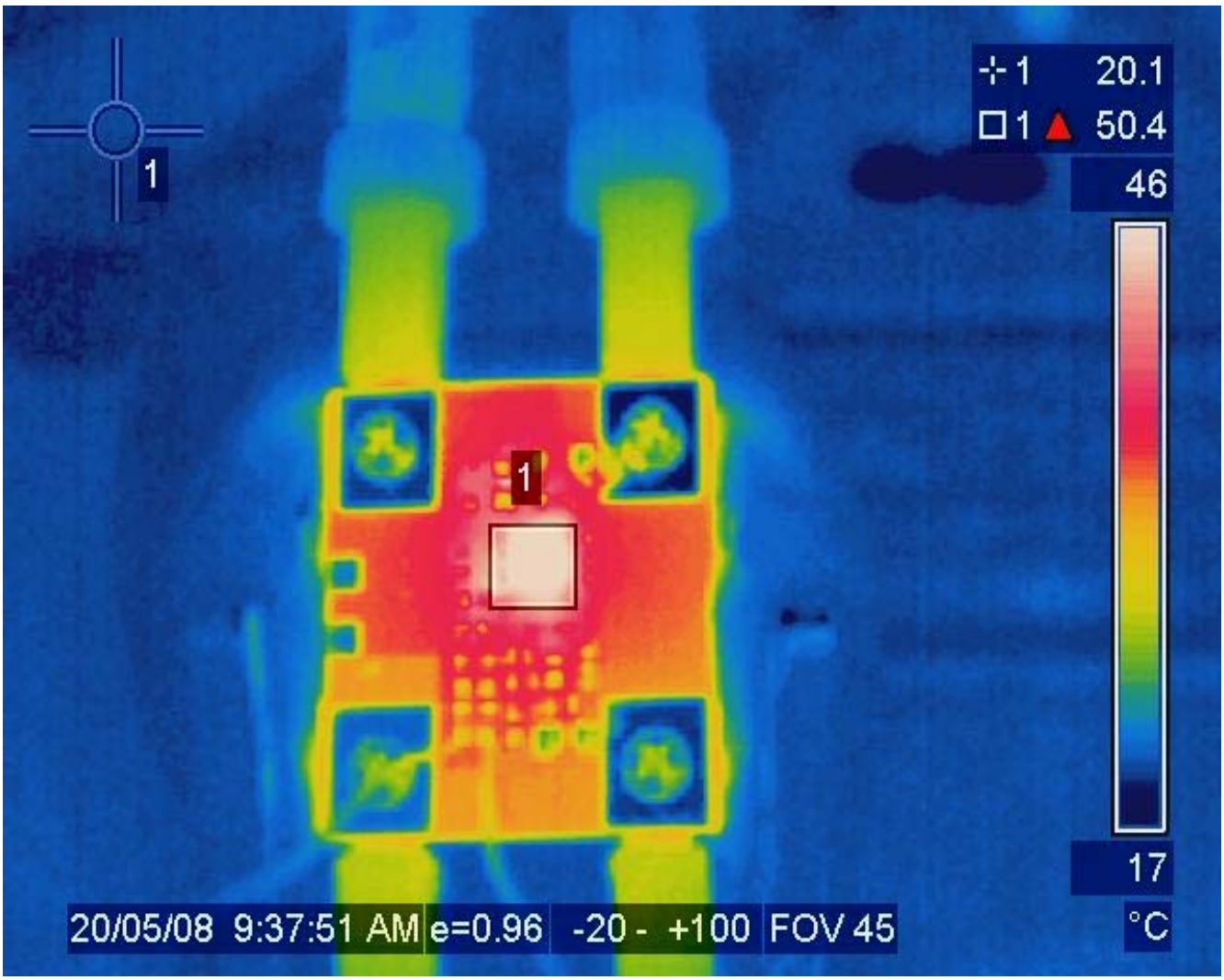


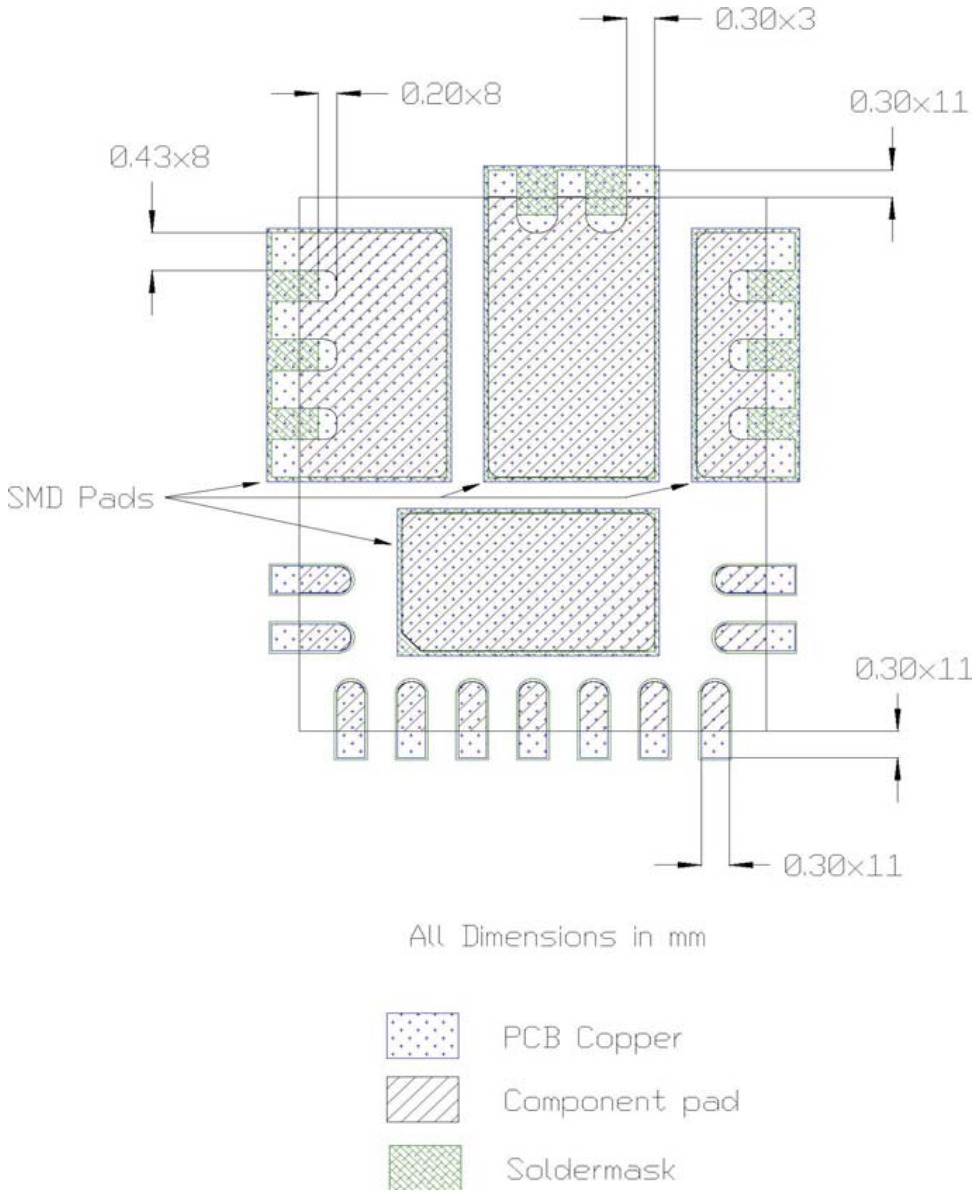
Fig. 16: Thermal Image at 4A load at 50.4° C
Test point (square) 1 is IR3802

PCB Metal and Components Placement

The lead lands (the 11 IC pins) width should be equal to the nominal part lead width. The minimum lead to lead spacing should be ⩾ 0.2mm to minimize shorting.

Lead land length should be equal to the maximum part lead length + 0.3 mm outboard extension. The outboard extension ensures a large and inspectable toe fillet.

The pad lands (the 4 big pads other than the 11 IC pins) length and width should be equal to maximum part pad length and width. However, the minimum metal to metal spacing should be no less than 0.17mm for 2 oz. Copper; no less than 0.1mm for 1 oz. Copper and no less than 0.23mm for 3 oz. Copper.

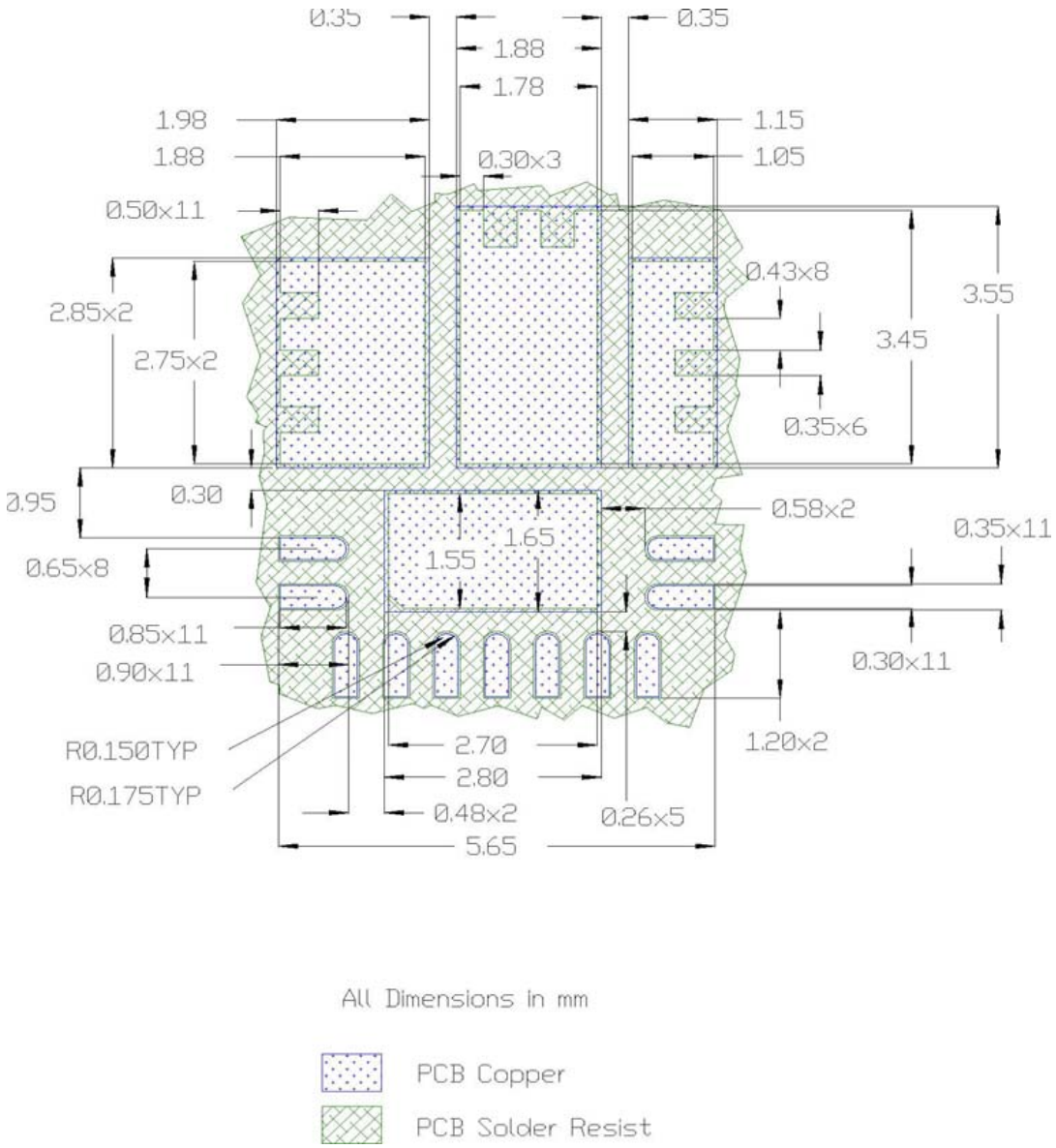


Solder Resist

It is recommended that the lead lands are Non Solder Mask Defined (NSMD). The solder resist should be pulled away from the metal lead lands by a minimum of 0.025mm to ensure NSMD pads.

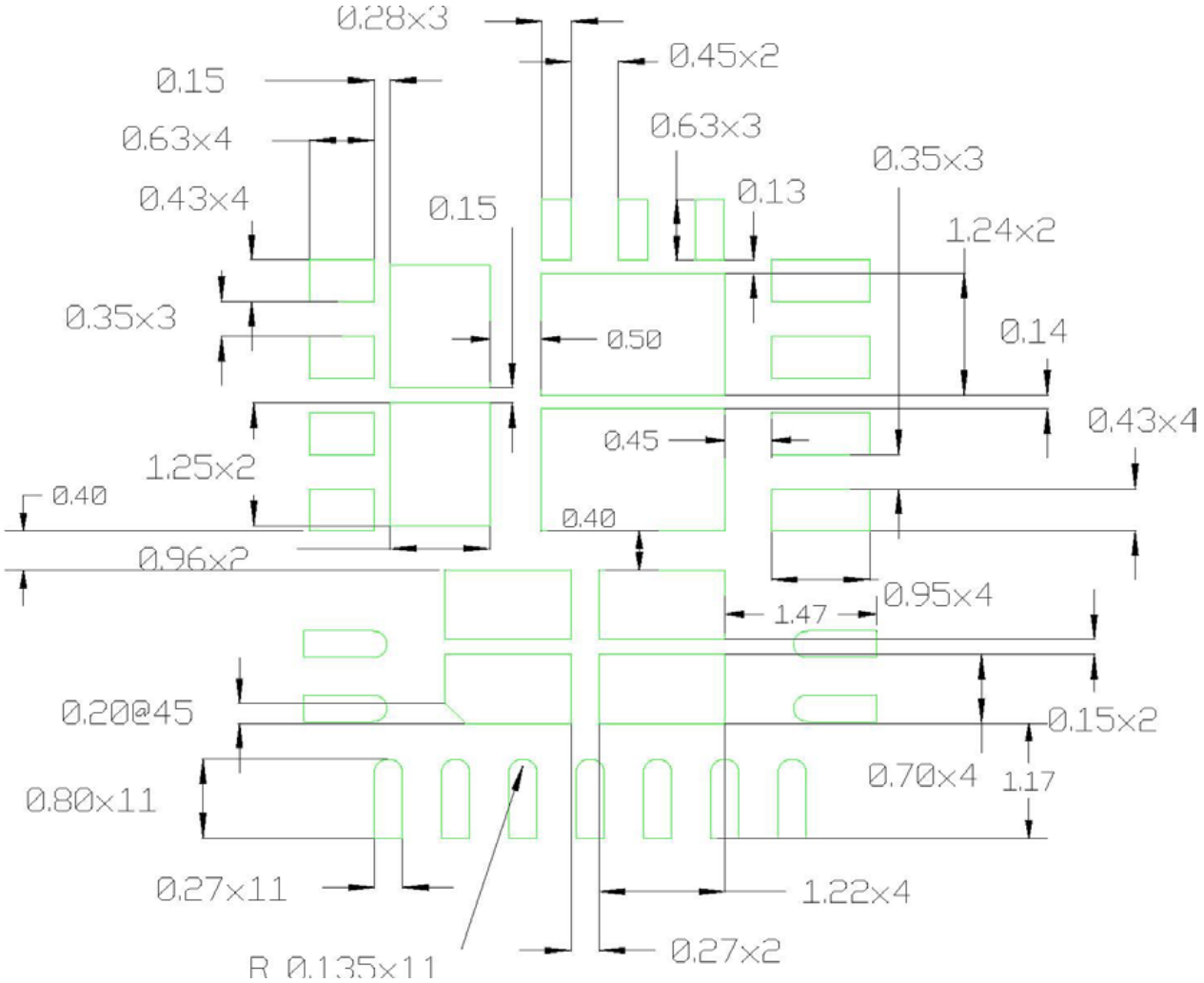
The land pad should be Solder Mask Defined (SMD), with a minimum overlap of the solder resist onto the copper of 0.05mm to accommodate solder resist mis-alignment.

Ensure that the solder resist in between the lead lands and the pad land is $\geqslant$ 0.15mm due to the high aspect ratio of the solder resist strip separating the lead lands from the pad land.

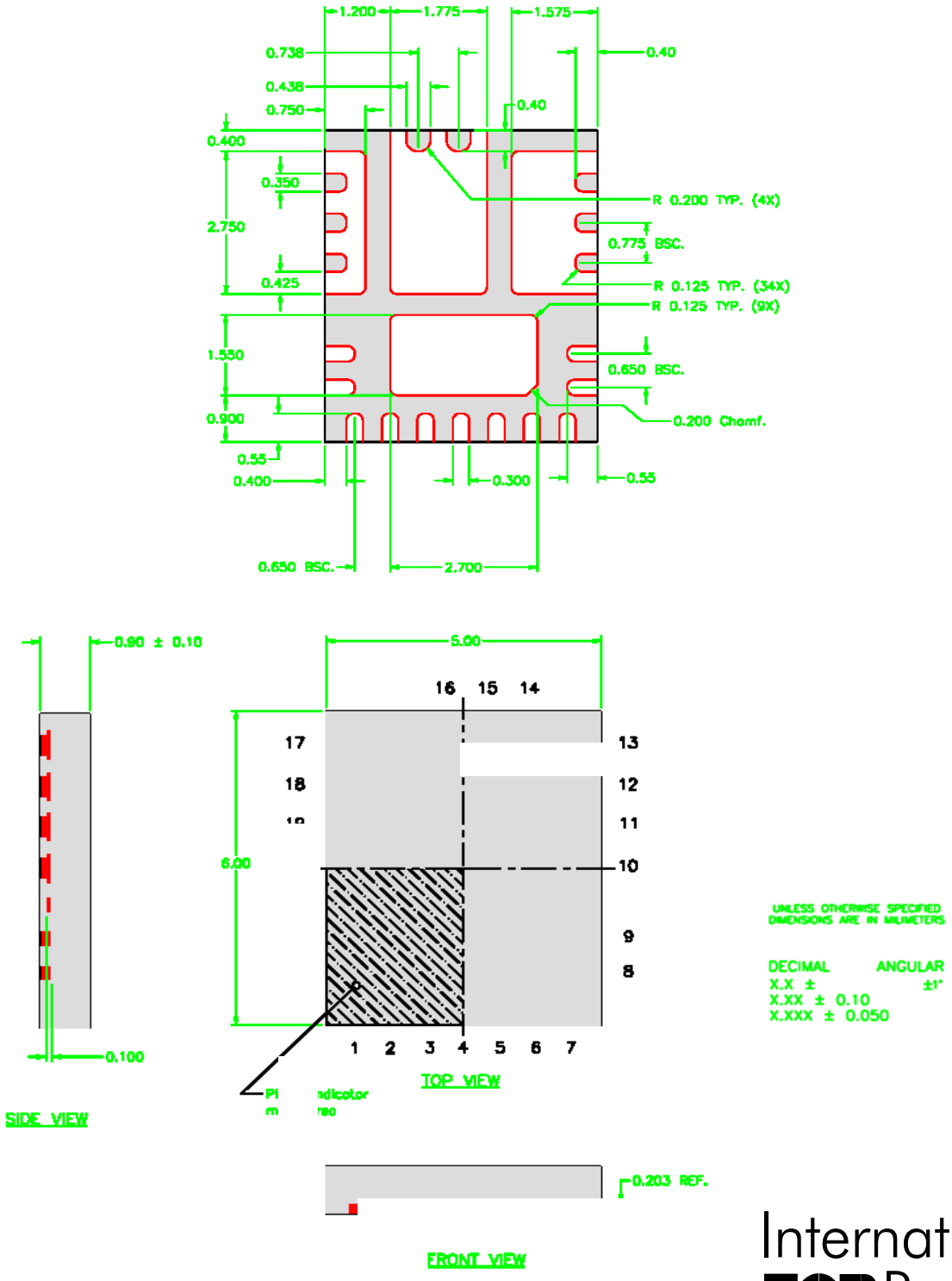


Stencil Design

- The Stencil apertures for the lead lands should be approximately 80% of the area of the lead lads. Reducing the amount of solder deposited will minimize the occurrences of lead shorts. If too much solder is deposited on the center pad the part will float and the lead lands will be open.
- The maximum length and width of the land pad stencil aperture should be equal to the solder resist opening minus an annular 0.2mm pull back to decrease the incidence of shorting the center land to the lead lands when the part is pushed into the solder paste.



Stencil Aperture
All Dimensions in mm



International
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Data and specifications subject to change without notice. 11/07

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