Features

- **Programmable DMUX Ratio:**
  - **1:4: Data Rate Max = 750 Msps**
  - **PD (8b/10b) < 4.3/4.7 W (ECL 50Ω output)**
  - **1:8: Data Rate Max = 1.5 Gsps**
  - **PD (8b/10b) < 6/6.9 W (ECL 50Ω output)**
  - **1:16 with 1 TS8388B or 1 TS83102G0B and 2 DMUX**
- **Parallel Output Mode**
- **8-/10-bit**
- **ECL Differential Input Data**
- **Data Ready or Data Ready/2 Input Clock**
- **Input Clock Sampling Delay Adjust**
- **Single-ended Output Data:**
  - **Adjustable Common Mode and Swing**
  - **Logic Threshold Reference Output**
  - **(ECL, PECL, TTL)**
- **Asynchronous Reset**
- **Synchronous Reset**
- **ADC + DMUX Multi-channel Applications:**
  - **Stand-alone Delay Adjust Cell for ADCs Sampling Instant Alignment**
- **Differential Data Ready Output**
- **Built-in Self Test (BIST)**
- **Dual Power Supply V_{EE} = -5V, V_{CC} = +5V**
- **Radiation Tolerance Oriented Design (More than 100 Krad (Si) Expected)**
- **TBGA 240 (Cavity Down) Package**

Description

The TS81102G0 is a monolithic 10-bit high-speed (up to 1.5 GHz) demultiplexor, designed to run with all kinds of ADCs and more specifically with Atmel's high-speed ADC 8-bit 1 Gsps TS8388B and ADC 10-bit 2 Gsps TS83102G0B.

The TS81102G0 uses an innovative architecture, including a sampling delay adjust and tunable output levels. It allows users to process the high-speed output data stream down to processor speed and uses the high-speed bipolar technology (25 GHz NPN cut-off frequency).

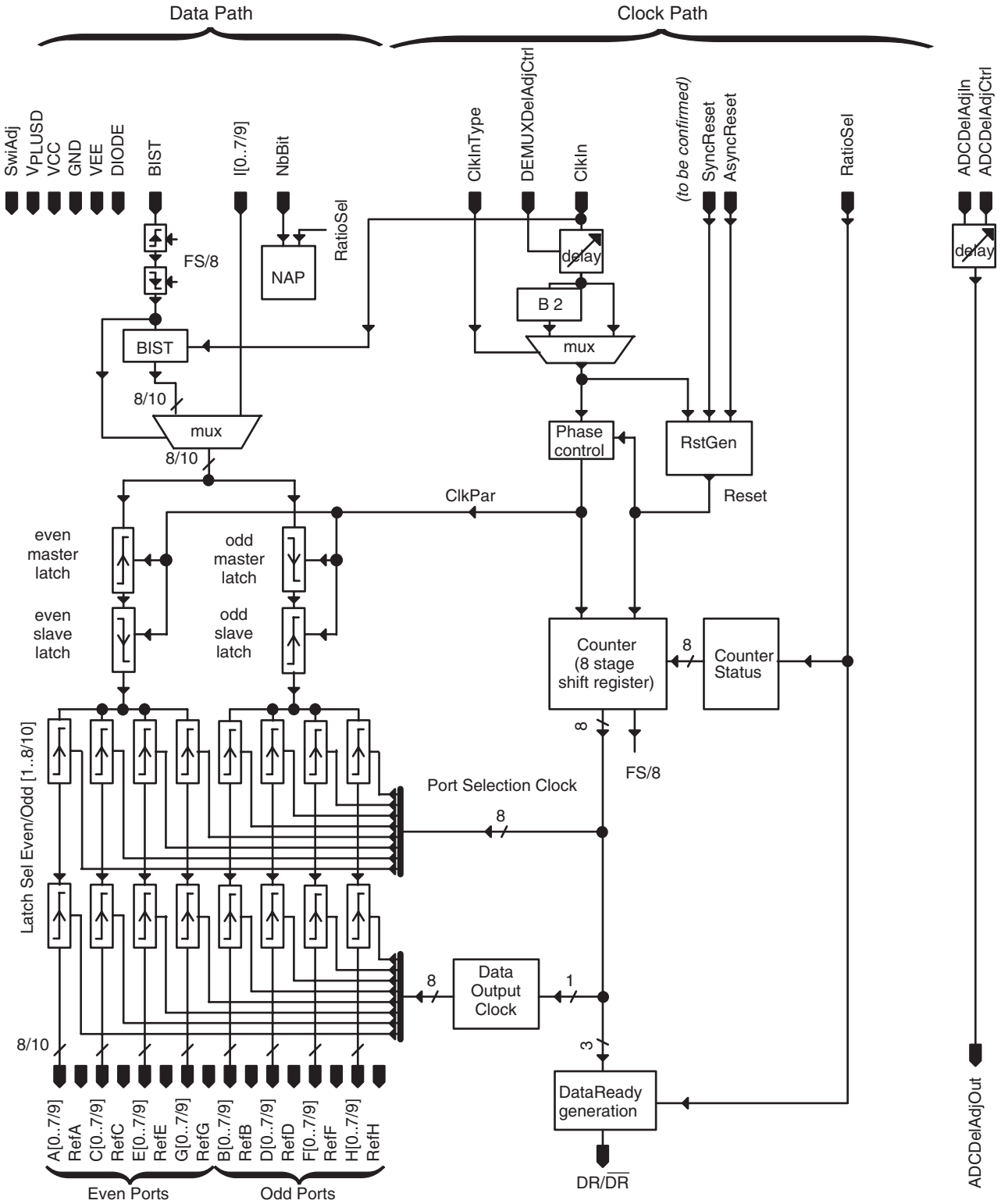
DMUX 8/10-bit 1.5 GHz 1:4/8

TS81102G0

2105D–BDC–07/05

1. Block Diagram

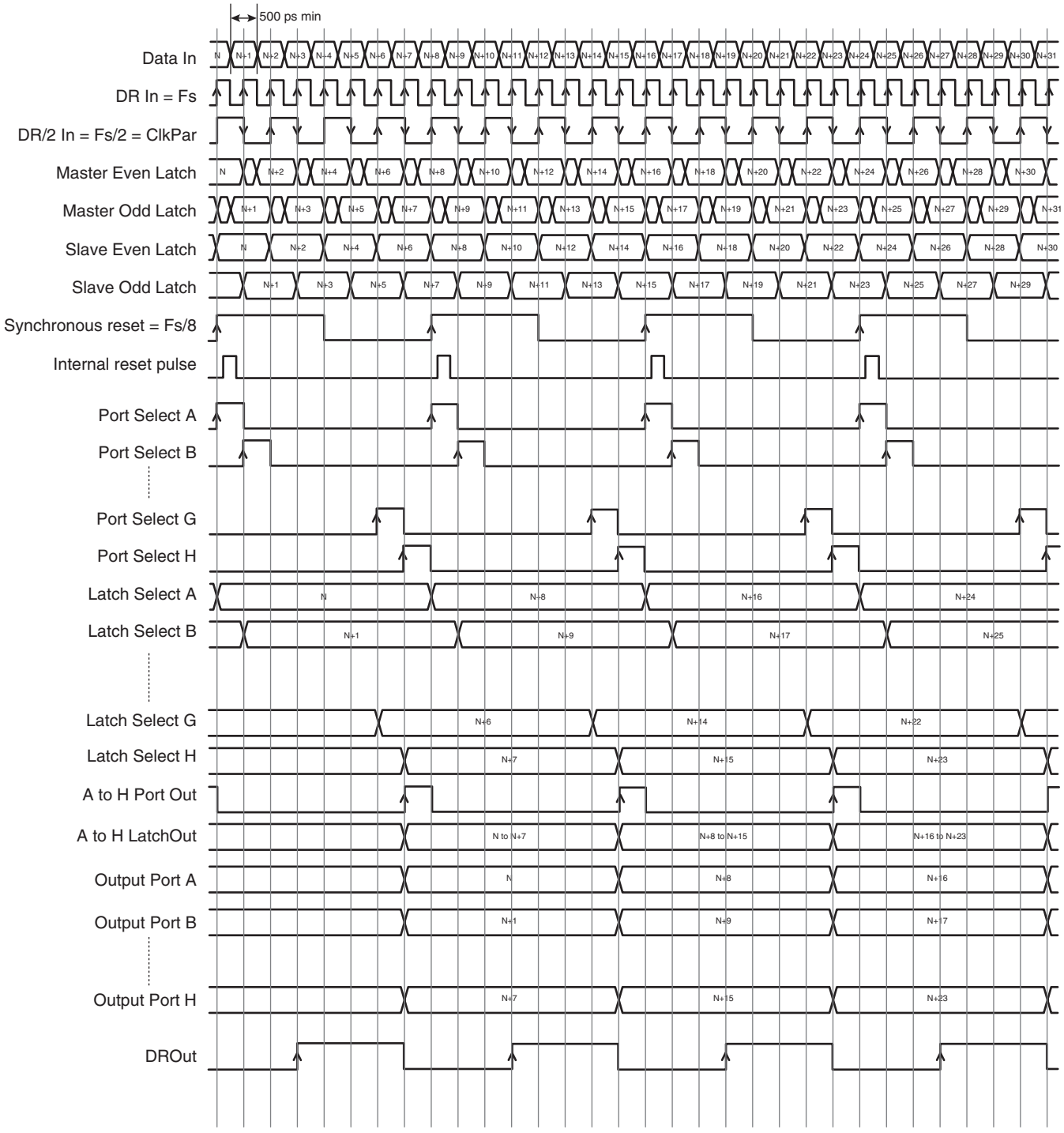
Figure 1. Block Diagram



2. Internal Timing Diagram

This diagram corresponds to an established operation of the DMUX with Synchronous Reset.

Figure 2-1. Internal Timing Diagram



3. Functional Description

The TS81102G0 is a demultiplexer based on an advanced high-speed bipolar technology featuring a cutoff frequency of 25 GHz. Its role is to reduce the data rate so that the data can be processed at the DMUX output. The TS81102G0 provides 2 programmable ratios: 1:4 and 1:8. The maximum data rate is 750 Msps for the 1:4 ratio and 1.5 Gsps for the 1:8 ratio. The TS81102G0 is able to process 8 or 10-bit data flows.

The input clock can be an ECL differential signal or single-ended DC coupled signal. Moreover it can be a Data Ready or Data Ready/2 clock. The input digital data must be an ECL differential signal. The output signals (Data Ready, digital data and reference voltage) are adjustable with V_{PLUSD} independent power supply. Typical output modes are ECL, PECL or TTL.

The Data Ready output is a differential signal. The digital output data and reference voltages are single-ended signals. The TS81102G0 is started by an asynchronous reset. A synchronous reset enables the user to re-synchronize the output port selection and to minimize loss of data that could occur within the DMUX. A delay adjust cell is available to ensure a good phase between the DMUX' input clock and input data. Another delay adjust cell is available to control the ADCs sampling instant alignment, in case of the ADCs interleaving.

A 10-bit generator is implemented in the TS81102G0, the Built-In Self Test (BIST). This test sequence is very useful for testing the DMUX at first use. A fine tuning of the output swing is also available.

The Enter Title of Manual can be used with the following Atmel ADCs:

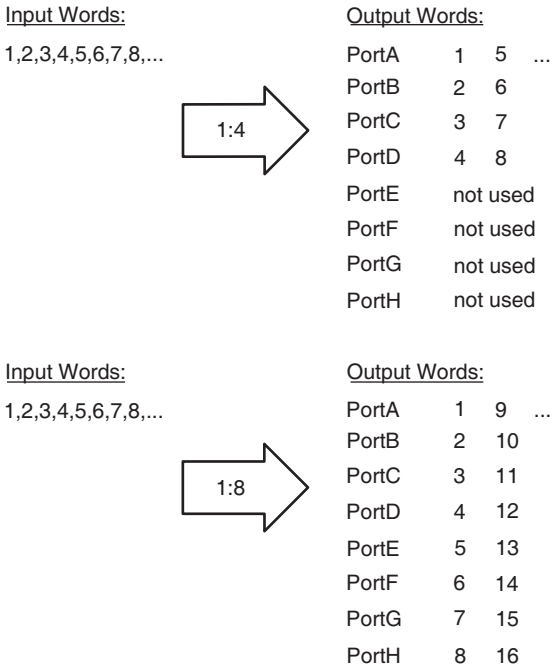
- TS8388B(F/FS/GL), 8-bit 1 Gsps ADC
- TS83102G0B, 10-bit 2 Gsps ADC

4. Main Function Description

4.1 Programmable DMUX Ratio

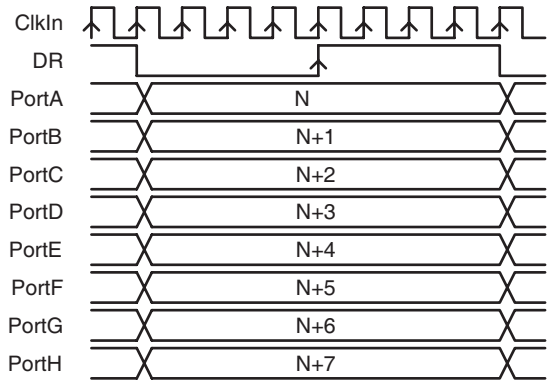
The conversion ratio is programmable: 1:4 or 1:8.

Figure 4-1. Programmable DMUX Ratio



4.2 Parallel Output Mode

Figure 4-2. Parallel Mode

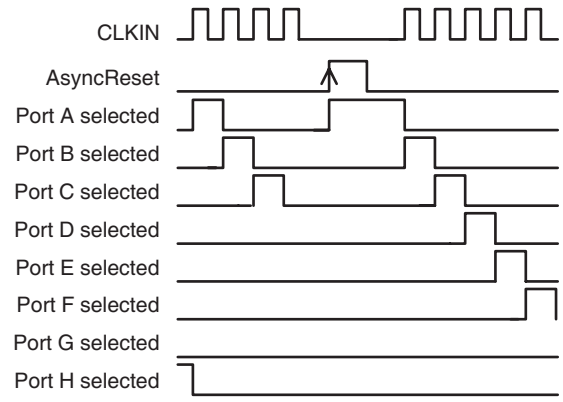


4.3 Input Clock Sampling Delay Adjust (DEMUXDELADJCTRL)

The input clock phase can be adjusted with an adjustable delay (from 250 to 750 ps). This is to ensure a proper phase between the clock and input data of the DMUX.

4.4 Asynchronous Reset (ASYNCRESET)

Figure 4-3. Asynchronous Reset

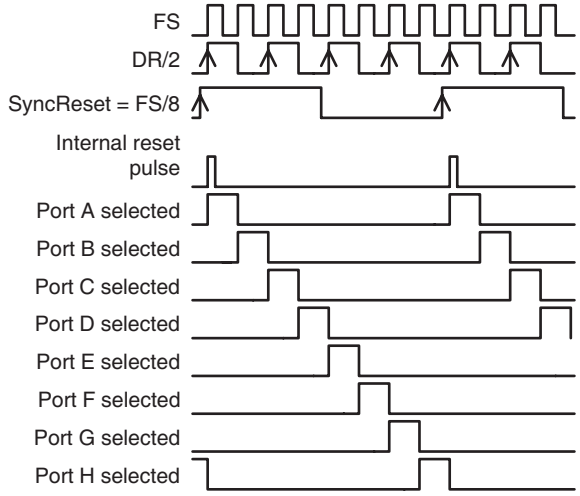


The asynchronous reset is a master reset of the port selection, which works on TTL levels. It is active on the high level. During an asynchronous reset, the clock must be in a known state. It is used to start the DMUX.

When it is active, it paralyzes the outputs (the output clock and output data remain at the same level as before the asynchronous reset). When it comes back to its low level, the DMUX starts: the outputs are active and the first processed data is on port A.

4.5 Synchronous Reset (SYNCRESET)

Figure 4-4. Synchronous Reset



The DMUX can be synchronously reset to a programmable state depending on the conversion ratio. The clock must not be stopped during reset. The synchronization signal is a clock (SyncRest) whose frequency is FS/8*n where n is an integer (n = 1,2,3 etc.) in 1:8 mode and FS/4*n in 1:4 mode.

The front edge of this clock is synchronized with ClkIn inside the DMUX, and generates a 200 ps reset pulse. This reset pulse occurs during a fixed level of ClkIn.

If the DMUX was synchronized with Syncreset previous to a possible loss of synchronization, then the output data is immediately correct, no modification can be seen at the output of the DMUX, and no data is lost ("Internal Timing Diagram" on page 3).

If the DMUX was not synchronized with SyncReset previous to a possible loss of synchronization, then the output data and data ready of the DMUX are changed. The output data is correct after a number of input clocks corresponding to the pipeline delay ("Timing Diagrams with Synchronous Reset" on page 20).

4.6 Counter Programmable State

When the counter is reset, its initial states depends on the conversion ratio:

- 1:8: counting on 8 bits
- 1:4: counting on 4 bits

4.7 Pipeline Delay

The maximum pipeline delay depends on the conversion ratio:

- 1:8: pipeline delay = 7
- 1:4: pipeline delay = 3

4.8 8-/10-bit, with NAP Mode for the 2 Unused Bit

The DMUX is a 10-bit parallel device. The last two bits (bits 8 and 9) may not be used, and the corresponding functions are set to nap mode to reduce power consumption.

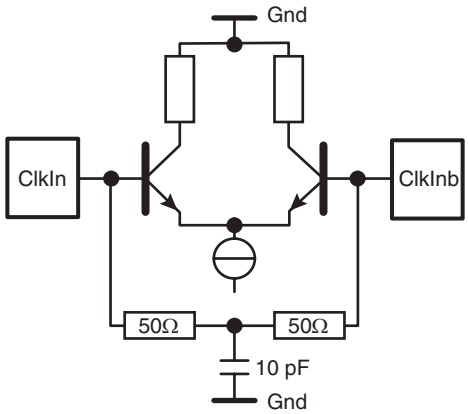
4.9 ECL Differential Input Data

Input data are ECL compatible (Voh = -0.8V, Vol = -1.8V).

The minimum swing required is 100 mV differential.

All inputs have a 100Ω differential termination resistor. The middle point of these resistors is connected to ground through a 10 pF capacitor.

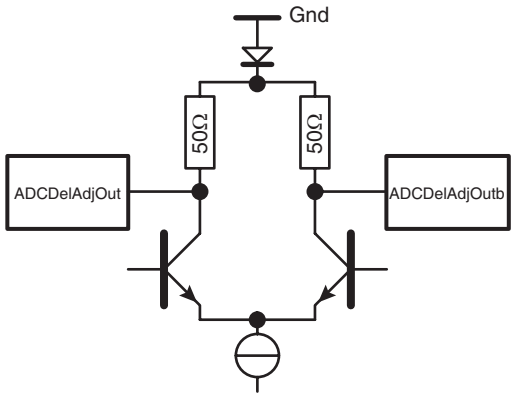
Figure 4-5. ECL Differential Input Data



4.10 50Ω Differential Output Data

The output clock for the ADC is generated through a 50Ω loaded long tailed. The 50Ω resistor is connected to the ground pad via a diode. The levels are (on the 100Ω differential termination resistor): Vol = -1.4V, Voh = -1.0V.

Figure 4-6. 50Ω Differential Output Data



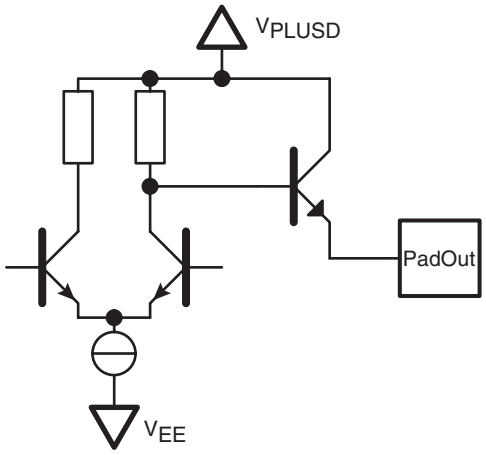
4.11 Single-ended Output Data

To reduce the pin number and power consumption of the DMUX, the eight output ports are single-ended.

To reach the high frequency output (up to 93.75 MHz, i.e. 187.5 Msps rate) with a reasonable power consumption, the swing must be limited to a maximum of ±500 mV. The common mode is adjustable from -1.3V to +2V, with V_{PLUSD} Dout pins. To ensure better noise immunity, a reference level (common mode) is available (one level by output port).

The output buffers are of ECL type (open emitters – not resistive adapted impedances). They are designed for a 15 mA average output current, and may be used with a 50Ω termination impedance.

Figure 4-7. Single-ended Output Data



Following are three application examples for these buffers: ECL/PECL/TTL. Please note that it is possible to have any other odd output format as far as current (36 mA max) and voltage (Vplus Dout – $V_{EE} \leq 8.3V$) limits are not overridden. The maximum frequency in TTL output mode depends on the load to be driven.

Table 4-1. Examples of Application of Buffers

Parameter	ECL	PECL	TTL	Unit
V_{PLUSD}	0	3.3	3.3	V
Vtt	-2	1.3	0	V
Swing	±0.5	±0.5	±1	V
Reference	-1.3	2	1.5	V
Voh	-0.8	2.5	2.5	V
Vol	-1.8	1.5	0.5	V
Load	50	50	≥75	Ω
Average Output Current	14	14	15	mA
Output Data rate max.	187.5	187.5	187.5	Msps

This corresponds to the “Adjustable Logic Single” in the pinout description.

The “Adjustable Single” buffers for reference voltage are the same buffers, but the information available at the output of these buffers is more like analog than logic.

Note: The Max Output Data Rate is given for a typical 50Ω/2 pF load.

4.12 Differential Data Ready Output

The front edge of the Data Ready output occurs when data is available on the corresponding port. The frequency of this clock depends on the conversion ratio (1:8 or 1:4), with a duty cycle of 50%.

The definition is the same as for single-ended output data, but the buffers are differential.

This corresponds to the “Adjustable Logic Differential” in the pinout description.

4.13 Built-in Self Test (BIST)

A pseudo-random 10-bit generator is implemented in the DMUX. It generates a 10-bit signal in the output of the DMUX, with a period of 512 input clocks. The probability of occurrence of codes is uniformly spread over the 1024 possible codes: 0 or 1/1024.

Note that the 256 codes of bits 1 to 8 occur at least once. They start with a BIST command, in phase with the FS/8 clock on Port A. The logic output obtained on the A to H ports depends on the conversion ratio. The driving clock of BIST is ClkIn. The ClkInType must be set to ‘1’ (Data Ready ADC clock) to have a different 10-bit code on each output.

The complete BIST sequence is available on request.

5. Specifications

5.1 Absolute Maximum Ratings

Table 5-1. Absolute Maximum Ratings

Parameter	Symbol	Comments	Value	Unit
Positive supply voltage	V_{CC}		GND to 6	V
Positive output buffer supply voltage	V_{PLUSD}		GND to 4	V
Negative supply voltage	V_{EE}		GND to -6	V
Analog input voltages	ADCDelAdjCtrl, ADCDelAdjCtrlb or DMUXDelAdjCtrl, DMUXDelAdjCtrlb or SwiAdj	Voltage range for each pad Differential voltage range	-1 to +1 -1 to +1	V
ECL 50Ω input voltage	ClkIn or ClkInb or I[0…9] or I[0…9]b or SyncReset or SyncResetb or ADCDelAdjIn or ADCDelAdjInb	Voltage range for each pad	-2.2 to +0.6	V
Maximum difference between ECL 50Ω input voltages	ClkIn – ClkInb or I[0…9] - I[0…9]b or SyncReset – Syncresetb or ADCDelAdjIn - ADCDelAdjInb	Minimum differential swing Maximum differential swing	0.1 2	V
Data output current	A[0…9] to H[0…9] or RefA to RefH or DR or DRb	Maximum current	36	mA
TTL input voltage	ClkIn Type RatioSel NbBit AsyncReset BIST		GND to V_{CC}	V
Maximum input voltage on diode for temperature measurement	DIODE		700	mV
Maximum input current on diode	DIODE		8	mA
Maximum junction temperature	T_j		135	°C
Storage temperature	T_{stg}		-65 to 150	°C

Note: Absolute maximum ratings are limiting values, to be applied individually, while other parameters are within specified operating conditions. Long exposure to maximum rating may affect device reliability. The use of a thermal heat sink is mandatory. See "Thermal and Moisture Characteristics" on page 28.

5.2 Recommended Operating Conditions

Table 5-2. Recommended Operating Conditions

Parameter	Symbol	Comments	Recommended Value			Unit
			Min	Typ	Max	
Positive supply voltage	V_{CC}		4.45	5	5.25	V
Positive output buffer supply voltage	V_{PLUSD}	ECL output compatibility	–	0	–	V
Positive output buffer supply voltage	V_{PLUSD}	PECL output compatibility	–	3.3	–	V
Positive output buffer supply voltage	V_{PLUSD}	TTL output compatibility	–	3.3	–	V
Negative supply voltage	V_{EE}		-5.25	-5	-4.75	V
Operating temperature range	T_J	Commercial grade: “C” Industrial grade: “V”	0 < Tc; Tj < 90 -40 < Tc; Tj < 110			°C

5.3 Electrical Operating Characteristics

Tj (typical) = 70°C. Full Temperature Range: -40°C < Tc; Tj < 110°C.

(Guaranteed temperature range are depending on part number)

Table 5-3. Electrical Specifications

Parameter	Symbol	Test Level	Value			Unit
			Min	Typ	Max	
Positive supply voltage						
• V_{CC}	V_{CC}	1	4.75	5	5.25	V
• V_{PLUSD}						
– ECL	V_{PLUSD}		-0.25	0	0.25	
– PECL	V_{PLUSD}		3.135	3.3	3.465	
Positive supply voltage						
• V_{PLUSD}						
– TTL	V_{PLUSD}	4	3.135	3.3	3.465	V
Negative supply voltage						
• V_{EE}	V_{EE}	1	-5.25	-5	-4.75	V

Table 5-3. Electrical Specifications (Continued)

Parameter	Symbol	Test Level	Value			Unit
			Min	Typ	Max	
Supply Currents						
ECL (50Ω) and PECL (50Ω)						
V_{CC} (for every configuration)	I_{CC}		–	31	50	
• 1:8, 8 bits	I_{PLUSD}		540	1180	1820	
	I_{EE}		–	720	800	
• 1:8, 10 bits	I_{PLUSD}		640	1140	2240	
	I_{EE}	1	–	790	850	mA
• 1:4, 8 bits	I_{PLUSD}		270	590	910	
	I_{EE}		–	590	650	
• 1:4, 10 bits	I_{PLUSD}		320	720	1120	
	I_{EE}		–	640	700	
TTL (75Ω)						
V_{CC} (for every configuration)	I_{CC}		–	30	50	
• 1:8, 8 bits	I_{PLUSD}		760	1610	2440	
	I_{EE}		–	870	930	
• 1:8, 10 bits	I_{PLUSD}		900	1770	3010	
	I_{EE}	4	–	980	1060	mA
• 1:4, 8 bits	I_{PLUSD}		380	810	1220	
	I_{EE}		–	670	730	
• 1:4, 10 bits	I_{PLUSD}		450	880	1510	
	I_{EE}		–	730	800	
Nominal power dissipation						
ECL (50Ω)						
• 1:8, 8 bits	PD		5.2	5.6	6.0	W
• 1:8, 10 bits	PD	1	5.9	6.4	6.9	W
• 1:4, 8 bits	PD		3.9	4.1	4.3	W
• 1:4, 10 bits	PD		4.2	4.5	4.7	W
PECL (50Ω)						
• 1:8, 8 bits	PD		5.8	6.2	6.6	W
• 1:8, 10 bits	PD	1	6.6	7.1	7.6	W
• 1:4, 8 bits	PD		4.2	4.4	4.6	W
• 1:4, 10 bits	PD		4.6	4.8	5.1	W

Table 5-3. Electrical Specifications (Continued)

Parameter	Symbol	Test Level	Value			Unit
			Min	Typ	Max	
TTL (75Ω)						
• 1:8, 8 bits	PD	4	6.8	7.3	7.7	W
• 1:8, 10 bits	PD		7.8	8.4	9	W
• 1:4, 8 bits	PD		4.7	4.9	5.1	W
• 1:4, 10 bits	PD		5.2	5.5	5.8	W
Delay Adjust Control						
DMUXDelAdjCtrl differential voltage	DDAC					
• 250 ps		5	–	-0.5	–	V
• 500 ps			–	0	–	V
• 750 ps			–	0.5	–	V
• Input current	IDDAC		–	20	–	µA
ADCDelAdjCtrl differential voltage	ADAC					
• 250 ps		5	–	-0.5	–	V
• 500 ps			–	0	–	V
• 750 ps			–	0.5	–	V
• Input current	IADAC		–	20	–	µA
Digital Outputs						
ECL Output (assuming V_{PLUSD} = 0V, SWIADJ = 0V, 50Ω termination resistor on board)						
• Logic “0” voltage	V_{OL}	4		-1.90	-1.80	V
• Logic “1” voltage	V_{OH}		-1.50	-1.10		V
• Reference voltage	V_{REF}		-1.90	-1.60	-1.30	V
PECL Output (assuming V_{PLUSD} = 3.3V, SWIADJ = 0V, 50Ω termination resistor on board)						
• Logic “0” voltage	V_{OL}	4		1.30	1.45	V
• Logic “1” voltage	V_{OH}	4	2.00	2.30		V
• Reference voltage	V_{REF}	4	1.40	1.70	2.00	V
TTL Output (assuming V_{PLUSD} = 3.3V, SWIADJ = 0V, 75Ω termination resistor on board)		4				
• Logic “0” voltage	V_{OL}			1.00	1.20	V
• Logic “1” voltage	V_{OH}		1.95	2.20		V
• Reference voltage	V_{REF}		1.30	1.60	1.90	V
Output level drift with temperature (data and DR outputs)		4		-1.3		mV/°C
Output level drift with temperature (reference outputs)				-0.9		mV/°C

Table 5-3. Electrical Specifications (Continued)

Parameter	Symbol	Test Level	Value Min	Value Typ	Value Max	Unit
Digital Inputs						
DATA Input Voltages (ECL)						
• Logic “0” voltage	V_{IL}	1			-1.6	V
• Logic “1” voltage	V_{IH}		-1.1			V
CTRL Input Voltages (TTL)						
• Logic “0” voltage	V_{IL}	4			0.6	V
• Logic “1” voltage	V_{IH}		2.0			V

Note: 1. The supply current I_{PLUSD} and the power dissipation depend on the state of the output buffers:
- the minimum values correspond to all the output buffers at low level,
- the maximum values correspond to all the output buffers at high level,
- the typical values correspond to an equal sharing-out of the output buffers between high and low levels.

5.4 Switching Performance and Characteristics

50% clock duty cycle (CLKIN, CLKINB). Tj (typical) = 70°C.

Full temperature range: -40°C < Tc; Tj < 110°C.

(Guaranteed temperature ranges depend on the part number)

See Timing Diagrams Figure 5-1 on page 17 to Figure 5-10 on page 23.

Table 5-4. Switching Performances

Parameter	Symbol	Test Level	Value Min	Value Typ	Value Max	Unit	Note
Input Clock							
Maximum clock frequency							
1:8 ratio	FMAX	4	1500	–		MHz	
1:4 ratio			750	–			
Clock pulse width (high)	TC1	4	225	–	–	ps	
Clock pulse width (low)	TC2	4	225	–	–	ps	
Clock Path pipeline delay							
DR input clock	TCPD	4	–	980	–	ps	(1)
DR/2 input clock	TCPD		–	1090	–	ps	(2)
Clock rise/fall time	TRCKIN TFCKIN	4	–	100	–	ps	
Asynchronous Reset							
Asynchronous Reset pulse width	PWAR	4	2000	–	–	ps	
Setup time from Asynchronous to Clkln	TSAR	4	–	200	–	ps	

Table 5-4. Switching Performances (Continued)

Parameter	Symbol	Test Level	Value			Unit	Note
			Min	Typ	Max		
Synchronous Reset							
Setup time from SyncReset to ClkIn							
DR input clock	TSSR	4	–	-580	–	ps	(3)
DR/2 input clock			–	-480	–	ps	(4)
Hold time from ClkIn to SyncReset							
DR input clock	THSR	4	–	780	–	ps	(5)
DR/2 input clock			–	680	–	ps	(6)
Rise/fall for (10% – 90%)	TSRR/TFSR	4	100	–	–	ps	
Input Data							
Setup time from I[0…9] to ClkIn							
DR input clock	TSCKIN	4	–	-800	–	ps	(7)
DR/2 input clock			–	-690	–	ps	(8)
Hold time from ClkIn to I[0…9]							
DR input clock	THCKIN	4	–	1000	–	ps	(9)
DR/2 input clock			–	890	–	ps	(10)
Rise/fall for (10% – 90%)	TRDI/TFDI	4	100	–	–	ps	
Output Data							
Data output delay							
DR input clock	TOD	4	–	1820	–	ps	(11)
DR/2 input clock			–	1720	–	ps	(12)
Data pipeline delay							
DR input clock, 1:4 ratio			–	3	–		
DR input clock, 1:8 ratio	TPD	4	–	7	–	Number of input clock	(13)
DR/2 input clock, 1:4 ratio			–	3/2	–		
DR/2 input clock, 1:8 ratio			–	7/2	–		
Rise/fall for (10% – 90%)	TROD/TFOD	4	–	500/500	–	ps	(14)
Data Ready							
Clock to data ready falling edge							
DR input clock	TDRF	4	–	3080	–	ps	(15)
DR/2 input clock			–	2500	–	ps	(16)
Clock to data ready rising edge							
DR input clock	TDRR	4	–	3180	–	ps	(17)
DR/2 input clock			–	2750	–	ps	(18)
Asynchronous reset to DataReady delay	TARDR	4	–	2820	–	ps	(19)
Synchronous reset to DataReady delay	TSRDR	4	–	1500	–	ps	(20)
Rise/fall for (10% – 90%)	TRDR/TFDR	4	–	380/260	–	ps	(21)
Rising edge uncertainty	JITTER	4	–	20	–	ps rms	
Setup time from Bist to ClkIn	TSBIST	4	–	1000	–	ps	

Table 5-4. Switching Performances (Continued)

Parameter	Symbol	Test Level	Value			Unit	Note
			Min	Typ	Max		
Rise/fall time for (10% – 90%)	TRBIST/ TFBIST	4	1000	–	–	ps	
ADC Delay Adjust							
Input frequency	FMADA	4	1.5	–		GHz	
Input pulse width (high)	TC1ADA	4	180	–	–	ps	
Input pulse width (low)	TC2ADA	4	180	–	–	ps	
Input rise/fall time	TRIADA/ TFIADA	4	70 60	150 150	– –	ps	
Output rise/fall time	TROADA/ TFOADA	4	– –	150 100	– –	ps	(22)
Data output delay (typical delay adjust setting)	TADA	4	– –	800 900	– –	ps	(23) (24)
Output delay drift with temperature	TADAT	4	–	2.5	–	ps/°C	
Output delay uncertainly	JITADA	4	–	20	–	ps rms	

Notes:
1. TCPD is tuned with DMUXDelAdjCtrl: TCPD = 980 ± 250 ps.
2. TCPD is tuned with DMUXDelAdjCtrl: TCPD = 1090 ± 250 ps.
3. TSSR depends on DMUXDelAdjCtrl: TSSR = -580 ± 250 ps. TSSR < 0 because of Clock Path internal delay.
4. TSSR depends on DMUXDelAdjCtrl: TSSR = -480 ± 250 ps. TSSR < 0 because of Clock Path internal delay.
5. THSR depends on DMUXDelAdjCtrl: THSR = 780 ± 250 ps.
6. THSR depends on DMUXDelAdjCtrl: THSR = 680 ± 250 ps.
7. TSCKIN depends on DMUXDelAdjCtrl: TSCKIN = -800 ± 250 ps. TSCKIN < 0 because of Clock Path internal delay.
8. TSCKIN depends on DMUXDelAdjCtrl: TSCKIN = -690 ± 250 ps. TSCKIN < 0 because of Clock Path internal delay.
9. THCKIN depends on DMUXDelAdjCtrl: THCKIN = 1000 ± 250 ps.
10. THCKIN depends on DMUXDelAdjCtrl: THCKIN = 890 ± 250 ps.
11. TOD depends on DMUXDelAdjCtrl: TOD = 1820 ± 250 ps. TOD is given for ECL 50Ω/2 pFoutput load.
12. TOD depends on DMUXDelAdjCtrl: TOD = 1720 ± 250 ps. TOD is given for ECL 50Ω/2 pFoutput load.
13. TPD is the number of ClkIn clock cycle from selection of Port A to selection of Port H in 1:8 conversion mode, and from selection of Port A to selection of Port D in 1:4 conversion mode. It is the maximum number of ClkIn clock cycle, or pipeline delay, that a data has to stay in the DMUX before being sorted out. This maximum delay occurs for the data sent to Port A. For instance, the data sent to Port H goes directly from the input to the Port H, and its pipeline is 0. But even for this data, there is an additional delay due to physical propagation time in the DMUX.
14. TROD and TFOD are given for ECL 50Ω/2 pF output load. In TTL mode, the TROD and TFOD are twice the ones for ECL. (For other termination topology, apply proper derating value 50 ps/pF in ECL, 100 ps/pF in TTL mode.)
15. TDRF depends on DMUXDelAdjCtrl: TDRF = 3080 ± 250 ps. It is given for ECL 50Ω/2 pF output load.
16. TDRF depends on DMUXDelAdjCtrl: TDRF = 2500 ± 250 ps. It is given for ECL 50Ω/2 pF output load.
17. TDRR depends on DMUXDelAdjCtrl: TDRR = 3180 ± 250 ps. It is given for ECL 50Ω/2 pF output load.
18. TDRR depends on DMUXDelAdjCtrl: TDRR = 2750 ± 250 ps. It is given for ECL 50Ω/2 pF output load.
19. TARDR is given for ECL 50Ω/2 pF output load.
20. TSRDR is given for ECL 50Ω/2 pF output load. It is minimum value since RstSync clock is synchronized with ClkIn clock.
21. TRDR and TFDR are given for ECL 50Ω/2 pF output load.
22. With transmission line (ZO = 50Ω) and output load R = 50Ω; C = 2 pF.
23. Without output load.
24. With transmission line (ZO = 50Ω) and output load R = 50Ω; C = 2 pF.

5.5 Explanation of Test Levels

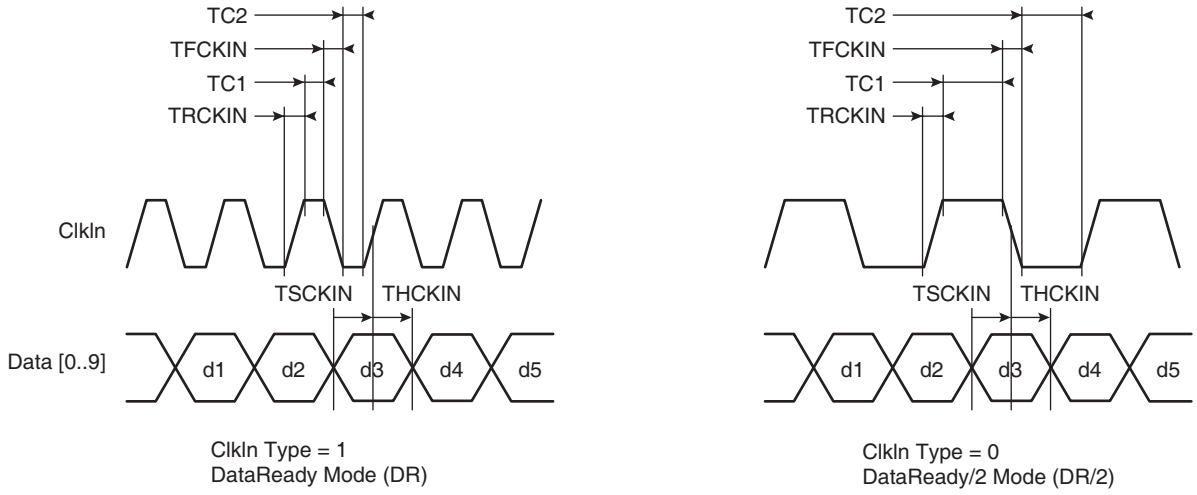
Table 5-5. Explanation of Test Levels

Num	Characteristics
1	100% production tested at +25°C.(1)
2	100% production tested at +25°C, and sample tested at specified temperatures.(1)
3	Sample tested only at specified temperatures.
4	Parameter is guaranteed by design and characterization testing (thermal steady-state conditions at specified temperature).
5	Parameter is a typical value only.

Notes: 1. The level 1 and 2 tests are performed at 50 MHz.
2. Only MIN and MAX values are guaranteed (typical values are issuing from characterization results).

5.5.1 Input Clock Timings

Figure 5-1. Input Clock

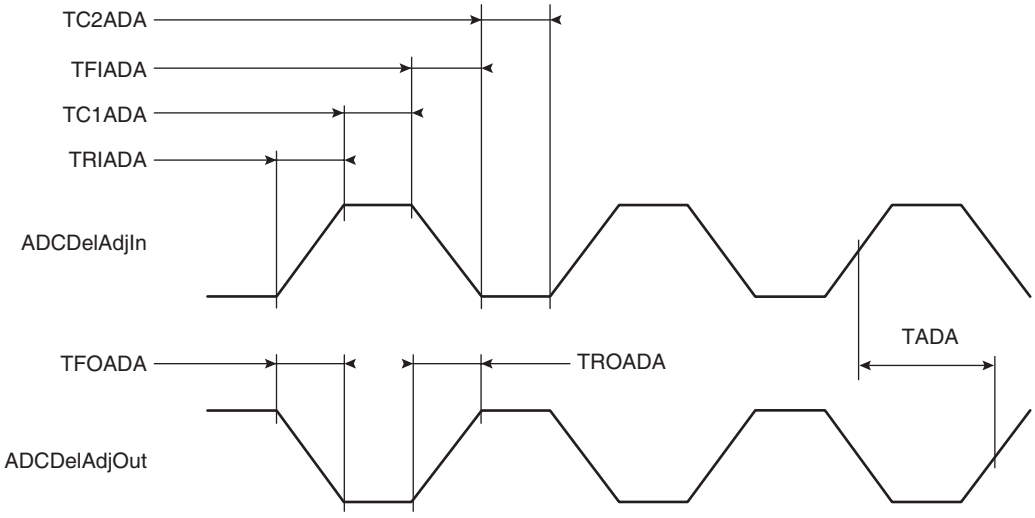


ClkIn Type = 1
DataReady Mode (DR)

ClkIn Type = 0
DataReady/2 Mode (DR/2)

5.5.2 ADC Delay Adjust Timing Diagram

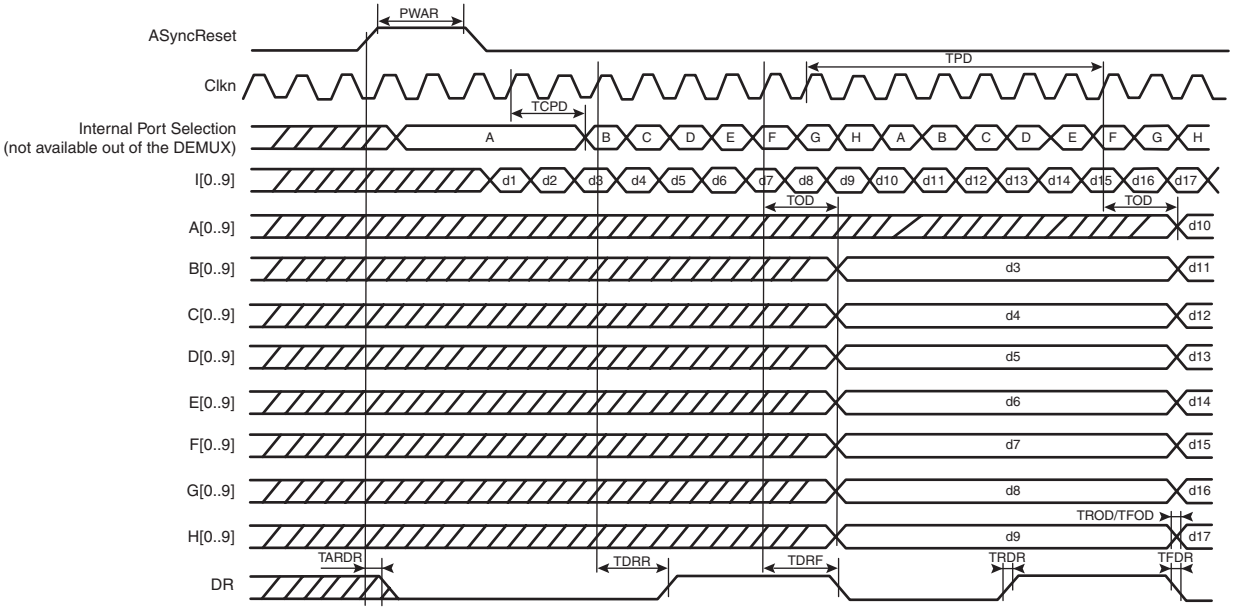
Figure 5-2. ADC Delay Adjust Timing Diagram



5.5.3 Timing Diagrams with Asynchronous Reset

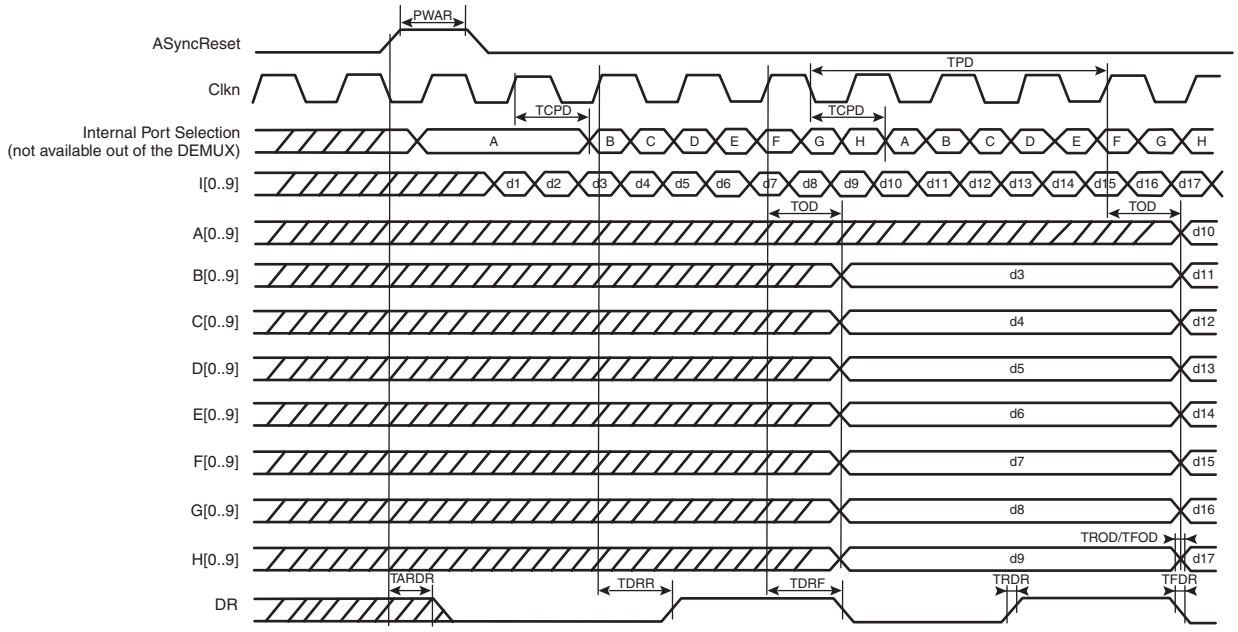
With a nominal tuning of DMUXDelAdj at a frequency of 1.5 GHz, d1 and d2 data is lost because of the internal clock's path propagation delay TCPD. TCPD is tuned with DMUXDelAdjCtrl pins to obtain good setup and hold times between ClkIn and the data.

Figure 5-3. Start with Asynchronous Rest, 1:8 Ratio, DR Mode



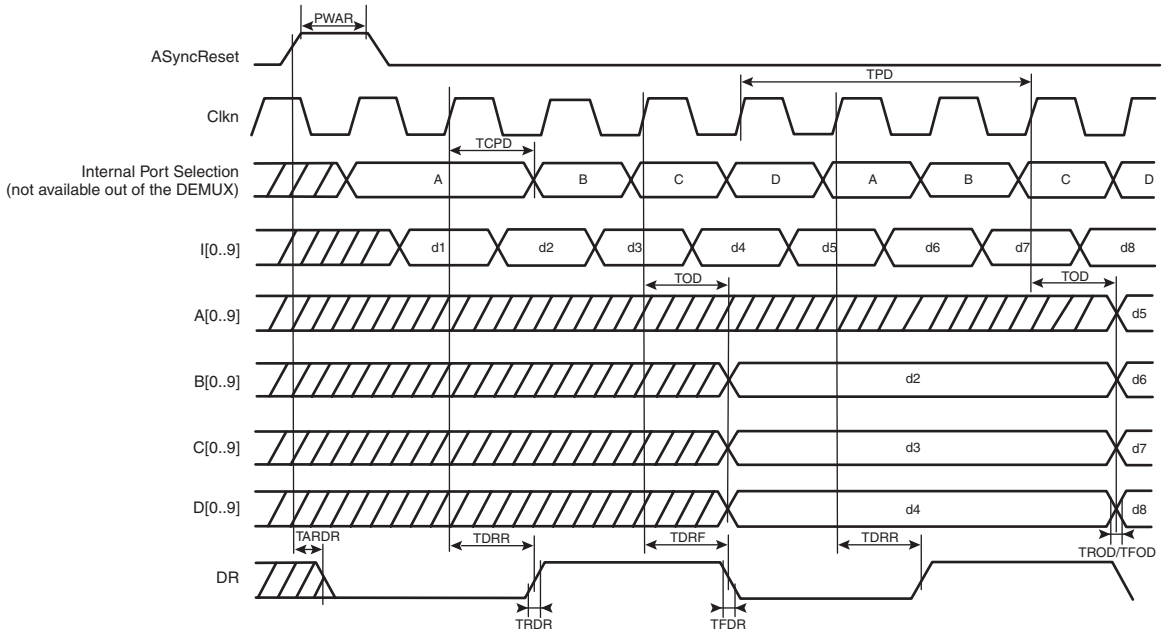
With a nominal tuning of DMUXDelAdj at 1.5 GHz, d1 and d2 data is lost because of the internal clock's path propagation delay TCPD. TCPD is tuned with DMUXDelAdjCtrl pins to obtain good setup and hold times between ClkIn and the input data. This timing diagram does not change with the opposite phase of ClkIn.

Figure 5-4. Start with Asynchronous Rest, 1:8 Ratio, DR/2 Mode



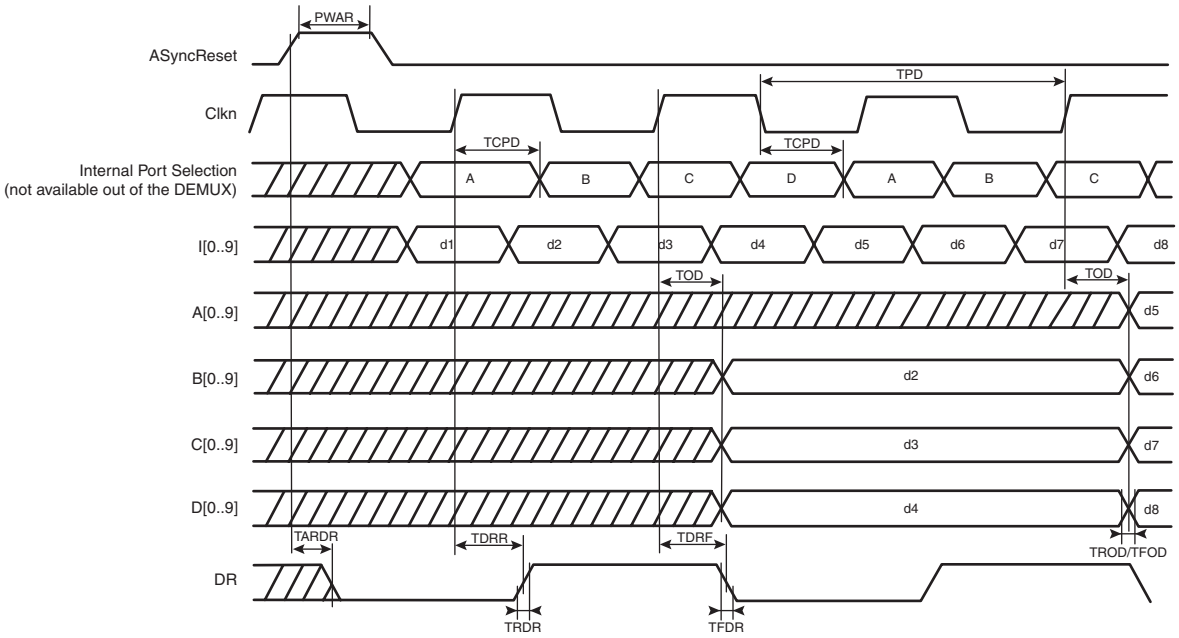
With a nominal tuning of DMUXDelAdj, at 750 MHz (1:4 mode) d1 data is lost because of the internal clock's path propagation delay TCPD. TCPD is tuned with DMUXDelAdjCtrl pins and is used to obtain good setup and hold times between ClkIn and the input data.

Figure 5-5. Start with Asynchronous Reset, 1:4 Ratio, DR Mode



With a nominal tuning of DMUXDelAdj, at 750 MHz (1:4 mode) d1 data is lost because of the internal clock's path propagation delay TCPD. TCPD is tuned with DMUXDelAdjCtrl pins and is used to obtain good setup and hold times between ClkIn and the input data. This timing diagram does not change with the opposite phase of ClkIn.

Figure 5-6. Start with Asynchronous Reset, 1:4 Ratio, DR/2 Mode



5.5.4 Timing Diagrams with Synchronous Reset

Examples of Synchronous Reset usefulness in case of desynchronization of DMUX output port selection.

5.5.4.1 Synchronous Reset, 1:8 Ratio, DR Mode

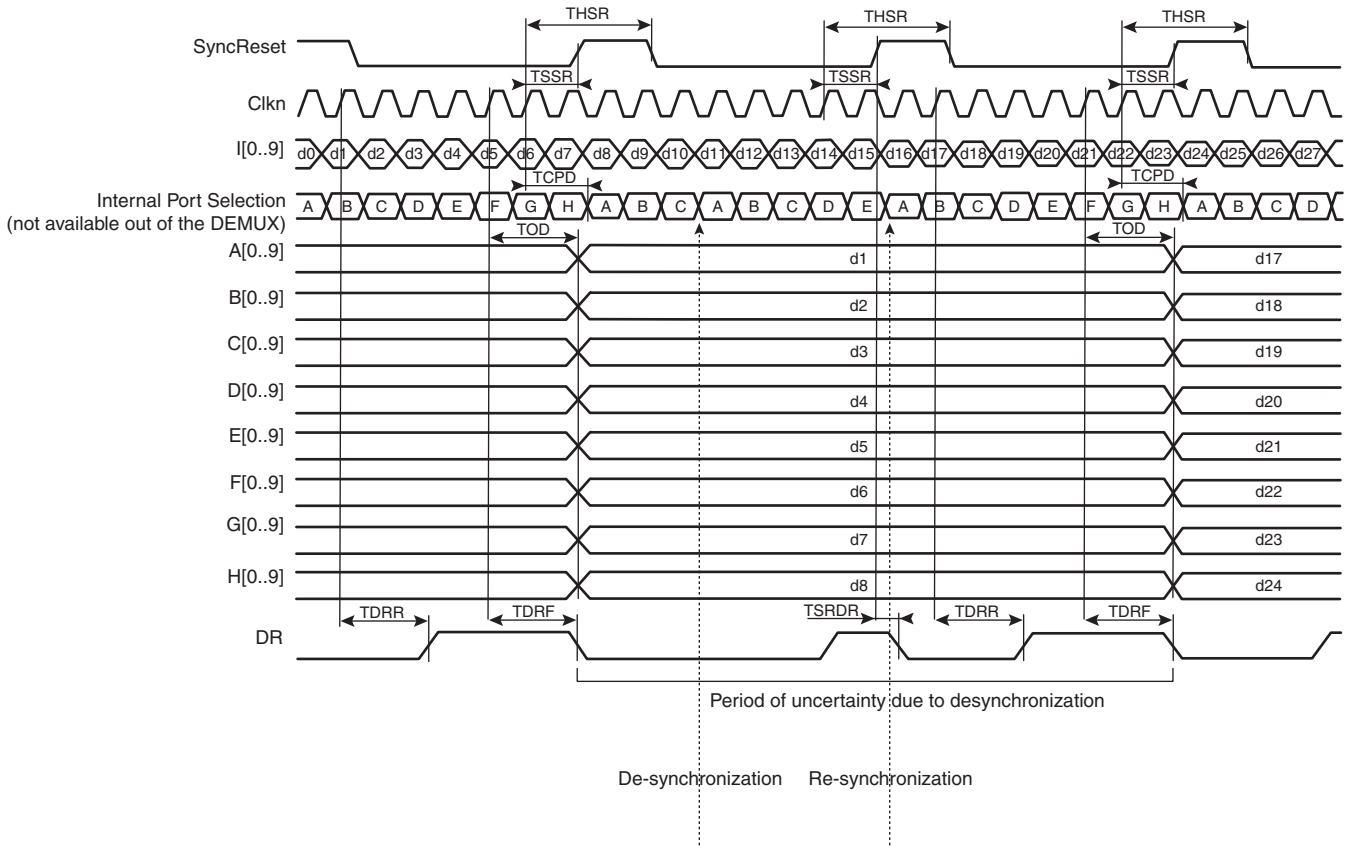
The desynchronization event happens after the selection of Port C.

DMUXDelAdjCtrl value is nominal. TSSR < 0 because of Clkln internal propagation delay TCPD.

After selection of port C, instead of selecting port D, the de-synchronization makes the port selection to restart on port A. Since port H was not selected, the data are not output to the ports but the last data (d1 to d8) are latched till next selection of port H. d9 to d16 are lost.

The synchronous reset ensures a re-synchronization of the port selection.

Figure 5-7. Synchronous Reset, 1:8 Ratio, DR Mode



5.5.4.2 Synchronous Reset, 1:4 Ratio, DR Mode

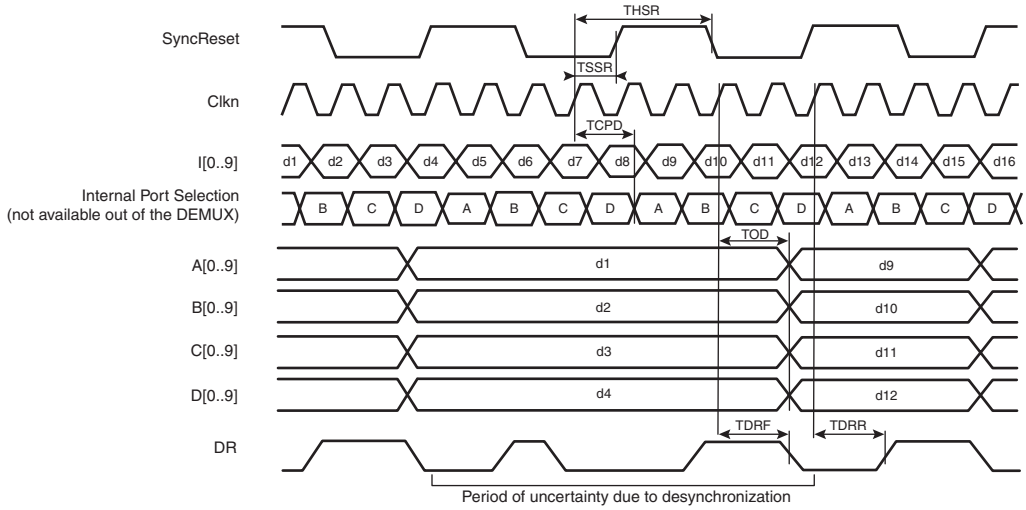
The desynchronization event happens after the selection of Port C.

DMUXDelAdjCtrl value is nominal. TSSR < 0 because of ClkIn internal propagation delay TCPD.

After selection of port C, instead of selecting port D, the de-synchronization makes the port selection to restart on port A. Since port D was not selected, the data are not output to the ports but the last data (d1 to d4) are latched till next selection of port D. d5 to d8 are lost.

The synchronous reset ensures a re-synchronization of the port selection.

Figure 5-8. Synchronous Reset, 1:4 Ratio, DR Mode



5.5.4.3 Synchronous Reset, 1:8 Ratio, DR/2 Mode

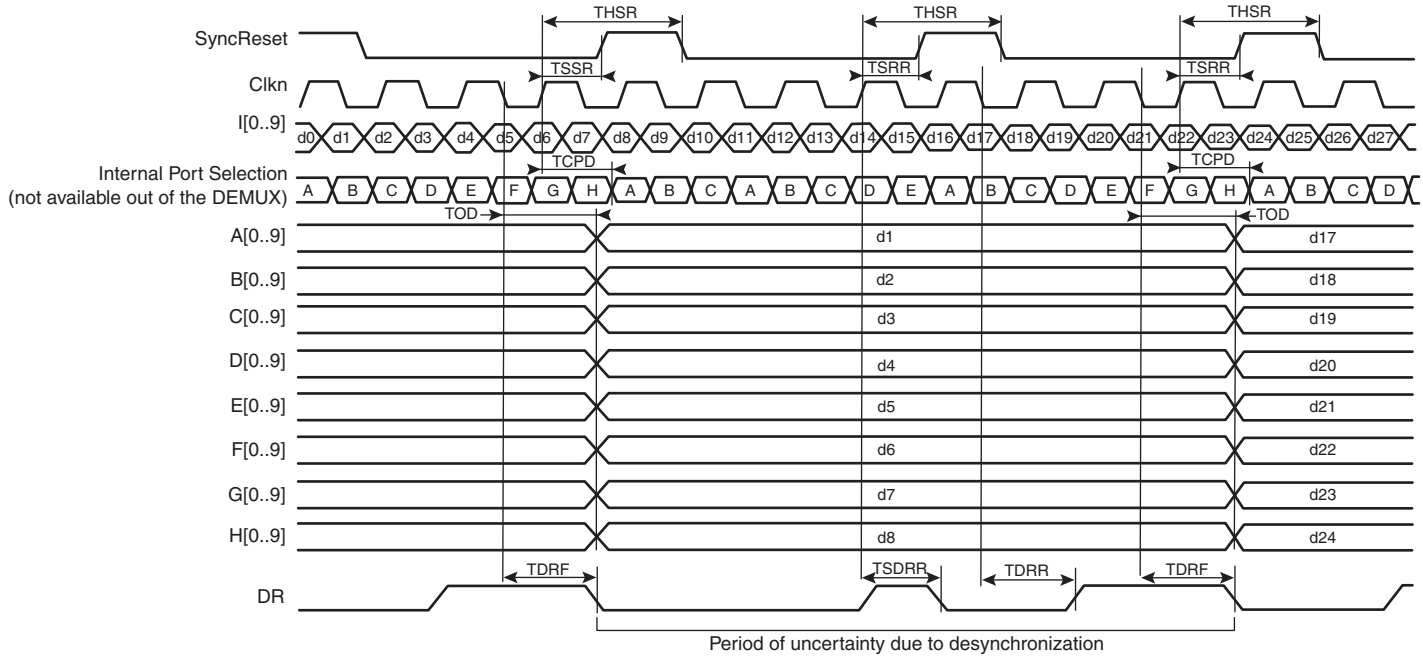
The desynchronization event happens after the selection of Port C.

DMUXDelAdjCtrl value is nominal. TSSR < 0 because of Clkln internal propagation delay TCPD.

After selection of port C, instead of selecting port D, the de-synchronization makes the port selection to restart on port A. Since port H was not selected, the data are not output to the ports but the last data (d1 to d8) are latched till next selection of port H. d9 to d16 are lost.

The synchronous reset ensures a re-synchronization of the port selection.

Figure 5-9. Synchronous Reset, 1:8 ratio, DR/2 Mode

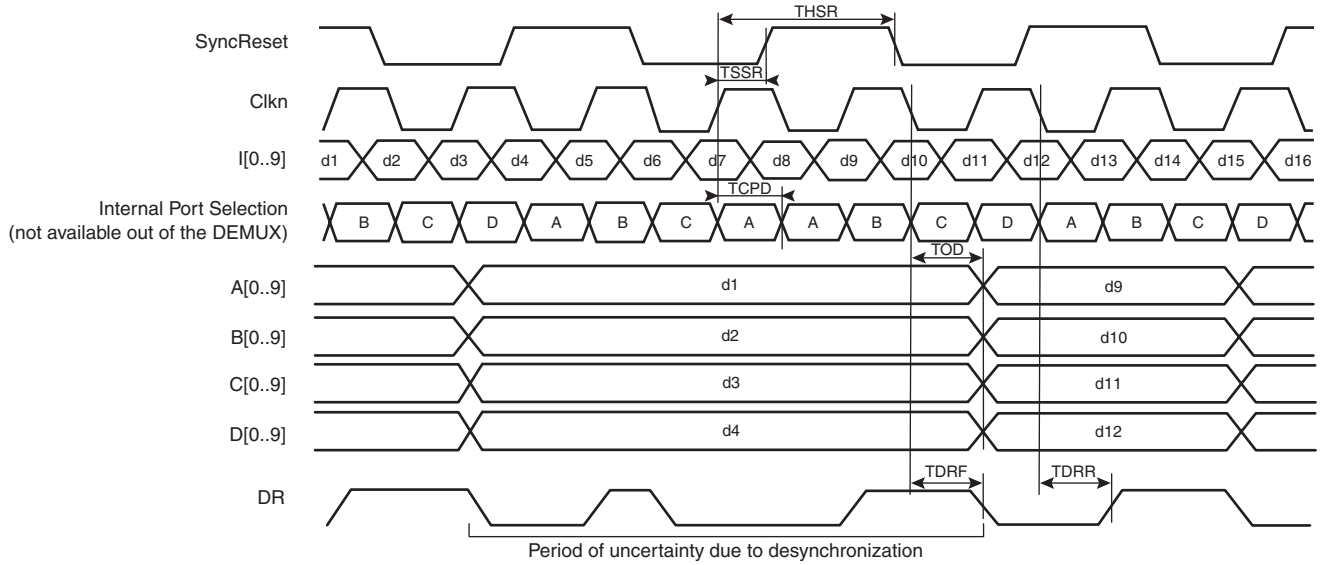


5.5.4.4 Synchronous Reset, 1:4 Ratio, DR/2 Mode

The desynchronization event happens after the selection of Port C.

DMUXDelAdjCtrl value is nominal. TSSR < 0 because of ClkIn internal propagation delay TCPD.

Figure 5-10. Synchronous Reset, 1:4 ratio, DR/2 Mode



After selection of port C, instead of selecting port D, the de-synchronization makes the port selection to restart on port A. Since port D was not selected, the data are not output to the ports but the last data (d1 to d4) are latched till next selection of port D. d5 to d8 are lost.

The synchronous reset ensures a re-synchronization of the port selection.

Note: In case of low clock frequency and start with asynchronous reset, only the first data is lost and the first data to be processed is the second one. This data goes out of the DEMUX by the port B.

6. Package Description

6.1 Pin Description

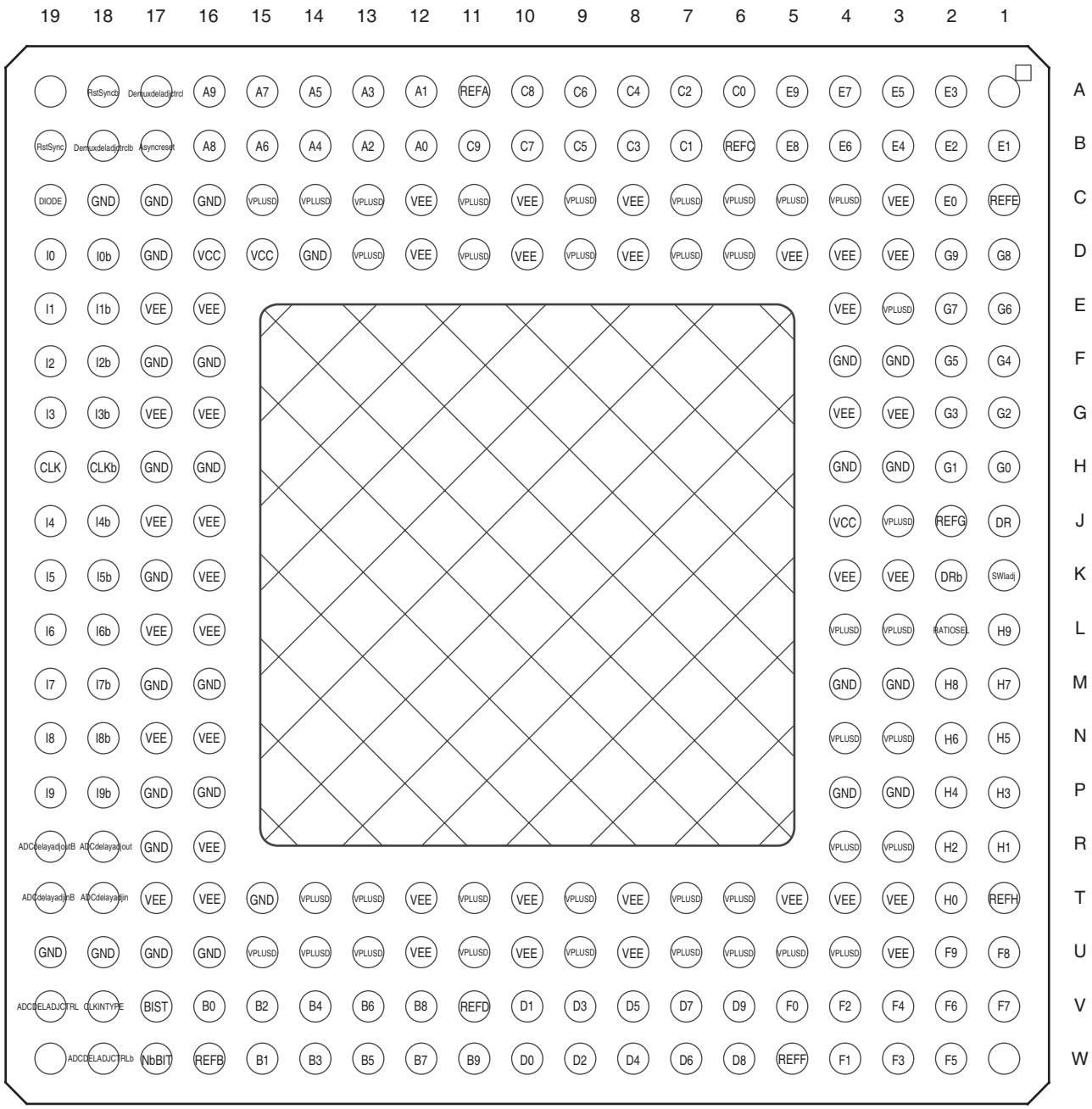
Table 6-1. Enter Title of Manual Pin Description

Type	Name	Levels	Comments
Digital Inputs	I[0…9]	Differential ECL	Data input. On-chip 100Ω differential termination resistor.
	ClkIn	Differential ECL	Clock input (Data Ready ADC). On-chip 100Ω differential termination resistor.
Outputs	A[0…9] → H[0…9]	Adjustable Logic Single	Data ready for port A to H. Common mode is adjusted with V_{PLUSD}. Swing is adjusted with SwiAdj. 50Ω termination possible.
	DR	Adjustable Logic Differential	Data ready for channel A to H. Common mode is adjusted with V_{PLUSD}. Swing is adjusted with SwiAdj. 50Ω termination possible.
	RefA → RefH	Adjustable Single	Reference voltage for output channels A to H. Common mode is adjustable with V_{PLUSD}. 50Ω termination possible.
Control Signals	ClkInType	TTL	Data Ready or Datar Ready/2: logic 1: Data Ready.
	RatioSel	TTL	DMUX ratio; logic 1: 1:4
	Bist	TTL	Reset and Switch of built-in Self Test (BIST): logic 0: BIST active.
	SwiAdj	0V ± 0.5V	Swing fine adjustment of output buffers.
	Diode	Analog	Diode for chip temperature measurement.
	NbBit	TTL	Number of bit 8 or 10: logic 1: 10-bit.
Synchronization	AsyncReset	TTL	Asynchronous reset: logic 1: reset on.
	SyncReset	Differential ECL	Synchronous reset: active on rising edge.
	DMUXDelAdjCtrl	Differential analog input of ±0.5V around 0V common mode	Control of the delay line of Data Ready input: differential input = -0.5V: delay = 250 ps differential input = 0V: delay = 500 ps differential input = 0.5V: delay = 750 ps
	ADCDelAdjCtrl	Differential analog input of ±0.5V around 0V common mode	Control of the delay line for ADC: differential input = - 0.5V: delay = 250 ps differential input = 0V: delay = 500 ps differential input = 0.5V: delay = 750 ps
	ADCDelAdjIn	Differential ECL	Stand-alone delay adjust input for ADC. Differential termination of 100Ω inside the buffer.
	ADCDelAdjOut	50Ω differential output	Stand-alone delay adjust output for ADC.
Power Supplies	GND	Ground 0V	Common ground.
	V_{EE}	Power -5V	Digital negative power supply.
	V_{PLUSD}	Adjustable power from 0V to +3.3V	Common mode adjustment of output buffers.
	V_{CC}	Power +5V	Digital positive power supply.

6.2 TBGA 240 Package – Pinout

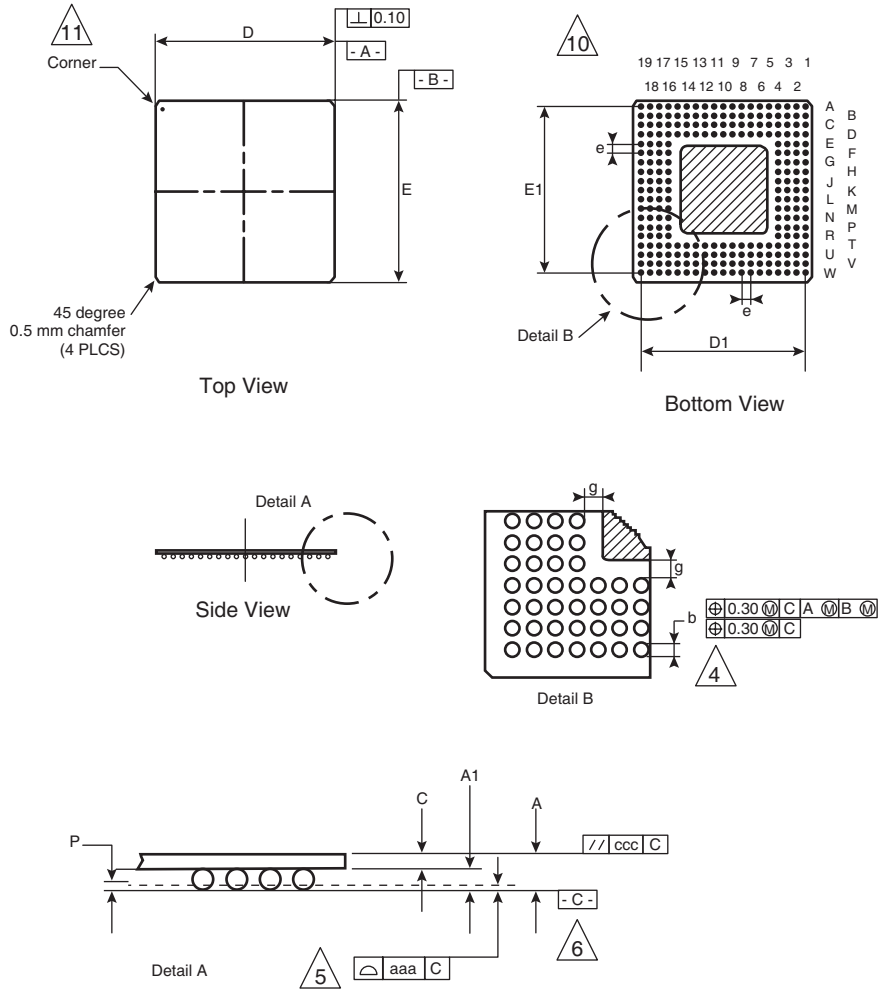
Row	Col	Name	Row	Col	Name	Row	Col	Name	Row	Col	Name
A	1	NC	D	4	VEE	K	16	VEE	T	17	VEE
A	2	E3	D	5	VEE	K	17	GND	T	18	ADCDELADJIN
A	3	E5	D	6	V_{PLUSD}	K	18	I5B	T	19	ADCDELADJINB
A	4	E7	D	7	V_{PLUSD}	K	19	I5	U	1	F8
A	5	E9	D	8	VEE	L	1	H9	U	2	F9
A	6	C0	D	9	V_{PLUSD}	L	2	RATIOSEL	U	3	VEE
A	7	C2	D	10	VEE	L	3	V_{PLUSD}	U	4	V_{PLUSD}
A	8	C4	D	11	V_{PLUSD}	L	4	V_{PLUSD}	U	5	V_{PLUSD}
A	9	C6	D	12	VEE	L	16	VEE	U	6	V_{PLUSD}
A	10	C8	D	13	V_{PLUSD}	L	17	VEE	U	7	V_{PLUSD}
A	11	REFA	D	14	GND	L	18	I6B	U	8	VEE
A	12	A1	D	15	VCC	L	19	I6	U	9	V_{PLUSD}
A	13	A3	D	16	VCC	M	1	H7	U	10	VEE
A	14	A5	D	17	GND	M	2	H8	U	11	V_{PLUSD}
A	15	A7	D	18	I0B	M	3	GND	U	12	VEE
A	16	A9	D	19	I0	M	4	GND	U	13	V_{PLUSD}
A	17	DEMUXDELADJCTRL	E	1	G6	M	16	GND	U	14	V_{PLUSD}
A	18	RSTSYNCB	E	2	G7	M	17	GND	U	15	V_{PLUSD}
A	19	NC	E	3	V_{PLUSD}	M	18	I7B	U	16	GND
B	1	E1	E	4	VEE	M	19	I7	U	17	GND
B	2	E2	E	16	VEE	N	1	H5	U	18	GND
B	3	E4	E	17	VEE	N	2	H6	U	19	GND
B	4	E6	E	18	I1B	N	3	V_{PLUSD}	V	1	F7
B	5	E8	E	19	I1	N	4	V_{PLUSD}	V	2	F6
B	6	REFC	F	1	G4	N	16	VEE	V	3	F4
B	7	C1	F	2	G5	N	17	VEE	V	4	F2
B	8	C3	F	3	GND	N	18	I8B	V	5	F0
B	9	C5	F	4	GND	N	19	I8	V	6	D9
B	10	C7	F	16	GND	P	1	H3	V	7	D7
B	11	C9	F	17	GND	P	2	H4	V	8	D5
B	12	A0	F	18	I2B	P	3	GND	V	9	D3
B	13	A2	F	19	I2	P	4	GND	V	10	D1
B	14	A4	G	1	G2	P	16	GND	V	11	REFD
B	15	A6	G	2	G3	P	17	GND	V	12	B8
B	16	A8	G	3	VEE	P	18	I9B	V	13	B6
B	17	ASYNCRESET	G	4	VEE	P	19	I9	V	14	B4
B	18	DEMUXDELADJCTRLB	G	16	VEE	R	1	H1	V	15	B2
B	19	RSTSYNC	G	17	VEE	R	2	H2	V	16	B0
C	1	REFE	G	18	I3B	R	3	V_{PLUSD}	V	17	BIST
C	2	E0	G	19	I3	R	4	V_{PLUSD}	V	18	CLKINTYPE
C	3	VEE	H	1	G0	R	16	VEE	V	19	ADCDELADJCTRL
C	4	V_{PLUSD}	H	2	G1	R	17	GND	W	1	NC
C	5	V_{PLUSD}	H	3	GND	R	18	ADCDELADJOUT	W	2	F5
C	6	V_{PLUSD}	H	4	GND	R	19	ADCDELADJOUTB	W	3	F3
C	7	V_{PLUSD}	H	16	GND	T	1	REFH	W	4	F1
C	8	VEE	H	17	GND	T	2	H0	W	5	REFF
C	9	V_{PLUSD}	H	18	CLKINB	T	3	VEE	W	6	D8
C	10	VEE	H	19	CLKIN	T	4	VEE	W	7	D6
C	11	V_{PLUSD}	J	1	DR	T	5	VEE	W	8	D4
C	12	VEE	J	2	REFG	T	6	V_{PLUSD}	W	9	D2
C	13	V_{PLUSD}	J	3	V_{PLUSD}	T	7	V_{PLUSD}	W	10	D0
C	14	V_{PLUSD}	J	4	VCC	T	8	VEE	W	11	B9
C	15	V_{PLUSD}	J	16	VEE	T	9	V_{PLUSD}	W	12	B7
C	16	GND	J	17	VEE	T	10	VEE	W	13	B5
C	17	GND	J	18	I4B	T	11	V_{PLUSD}	W	14	B3
C	18	GND	J	19	I4	T	12	VEE	W	15	B1
C	19	DIODE	K	1	SWIADJ	T	13	V_{PLUSD}	W	16	REFB
D	1	G8	K	2	DRB	T	14	V_{PLUSD}	W	17	NBBIT
D	2	G9	K	3	VEE	T	15	GND	W	18	ADCDELADJCTRLB
D	3	VEE	K	4	VEE	T	16	VEE	W	19	NC

Figure 6-1. TBGA 240 Package: Bottom View



6.3 Outline Dimensions

Figure 6-2. Package Dimension – 240 Tape Ball Grid Array



Dimensional References			
Ref.	Min.	Nom.	Max.
A	1.30	1.50	1.70
A1	0.50	0.60	0.70
D	24.80	25.00	25.20
D1		22.86 (BSC.)	
E	24.80	25.00	25.20
E1		22.86 (BSC.)	
b	0.60	0.75	0.90
c	0.80	0.90	1.00
M		19.00	
N		240.00	
aaa	-	-	0.15
ccc	-	-	0.25
e		1.27 TYP.	
g	0.35	-	-
P	0.15	-	-

Notes:
1. All dimensions are in millimeters.
2. "e" represents the basic solder ball grid pitch.
3. "M" represents the basic solder ball matrix size, and symbol "N" is the maximum allowable number of balls after depopulating.
4. "b" is measured at the maximum solder ball diameter parallel to primary datum - C -
5. Dimension "aaa" is measured parallel to primary datum - C -
6. Primary datum - C - and seatin plane are defined by the spherical crowns of the solder balls.
7. Package surface shall be black oxide.
8. Cavity depth various with die thickness.
9. Substrate material base is copper.
10. Bilateral tolerance zone is applied to each side of package body.
11. 45 deg. 0.5 mm chamfer corner and white dot for pin 1 identification.

6.4 Thermal and Moisture Characteristics

6.4.1 Thermal Resistance from Junction to Case: RTHJC

The Rth from junction to case for the TBGA package is estimated at 1.05°C/W that can be broken down as follows:

- Silicon: 0.1°C/W
- Die attach epoxy: 0.5°C/W (thickness # 50 µm)
- Copper block (back side of the package): 0.1°C/W
- Black Ink: 0.251°C/W.

6.4.2 Thermal Resistance from Junction to Ambient: RTHJA

A pin-fin type heat sink of a size 40 mm x 40 mm x 8 mm can be used to reduce thermal resistance. This heat sink should not be glued to the top of the package as Atmel cannot guarantee the attachment to the board in such a configuration. The heat sink could be clipped or screwed on the board.

With such a heat sink, the Rthj-a is about 6°C/W (if we take 10°C/W for Rth from the junction to air through the package and heat sink in parallel with 15°C/W from the junction to the board through the package body, through balls and through board copper).

Without the heat sink, the Rth junction to air for a package reported on-board can be estimated at 13 to 20°C/W (depending on the board used).

The worst value 20°C/W is given for a 1-layer board (13°C for a 4-layer board).

6.4.3 Thermal Resistance from Junction to Bottom of Balls

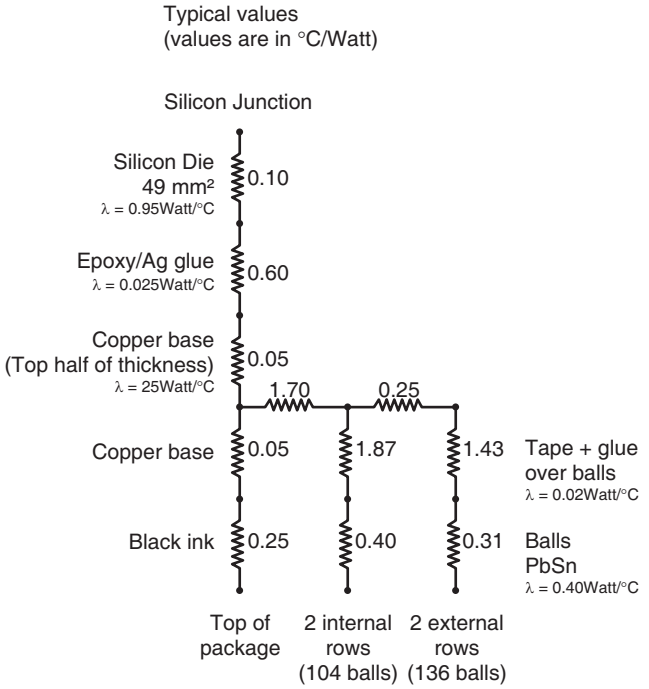
The thermal resistance from the junction to the bottom of the balls of the package corresponds to the total thermal resistance to be considered from the silicon's die junction to the interface with a board. This thermal resistance is estimated to be 4.8°C/W max.

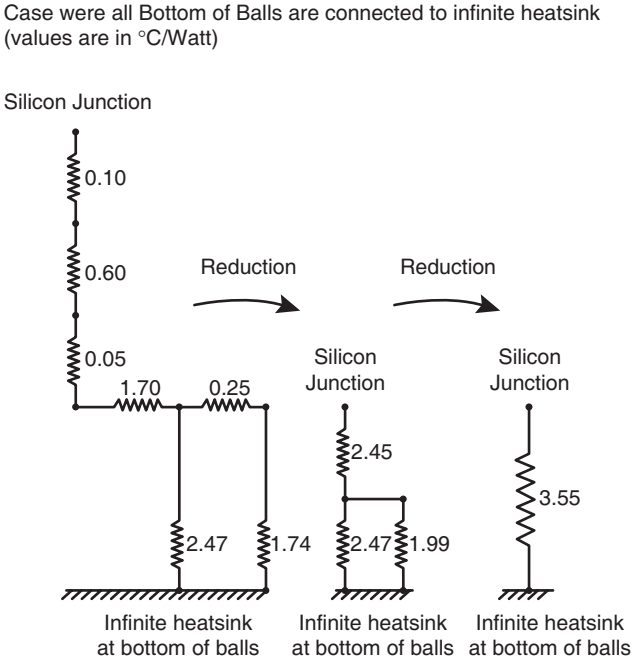
The following diagram points out how the previous thermal resistances were calculated for this packaged device.

Figure 6-3. Thermal Resistance from Junction to Bottom of Balls

DEMUX – Axpproximative Model for 240 TBGA

Assumptions:
Square die 7.0 x 7.0 = 49 mm², 75 µm thick Epoxy/Ag glue, 0.40 mm copper thickness under die,
Sn60Pb40 columns diameter 0.76 mm, 23 x 23 mm TBGA





Thermal Resistance Junction to case typical =
0.10 + 0.60 + 0.05 + 0.05 + 0.25 = 1.05°C/W

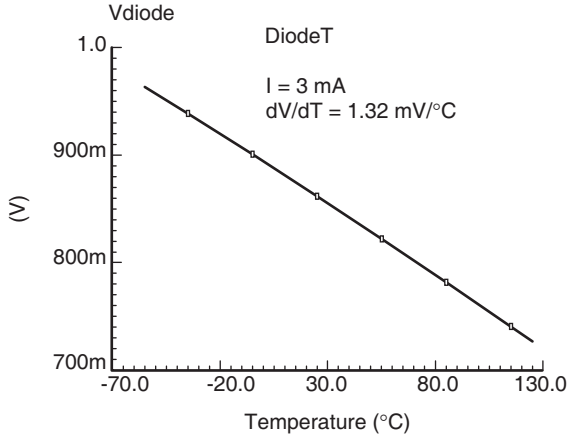
Thermal Resistance Junction to case Max = 1.40°C/W

Thermal Resistance Junction to bottom of balls = 4.8°C/W Max

6.4.4 Temperature Diode Characteristic

The theoretical characteristic of the diode according to the temperature when I = 3 mA is depicted below.

Figure 6-4. Temperature Diode Characteristic



6.4.5 Moisture Characteristic

This device is sensitive to moisture (MSL3 according to the JEDEC standard).

The shelf life in a sealed bag is 12 months at < 40°C and < 90% relative humidity (RH).

After this bag is opened, devices that might be subjected to infrared reflow, vapor-phase reflow, or equivalent processing (peak package body temperature 220°C) must be:

- mounted within 168 hours at factory conditions of ≤ 30°C/60% RH, or
- stored at ≤ 20% RH.

The devices require baking before mounting, if the humidity indicator is > 20% when read at 23°C ±5°C.

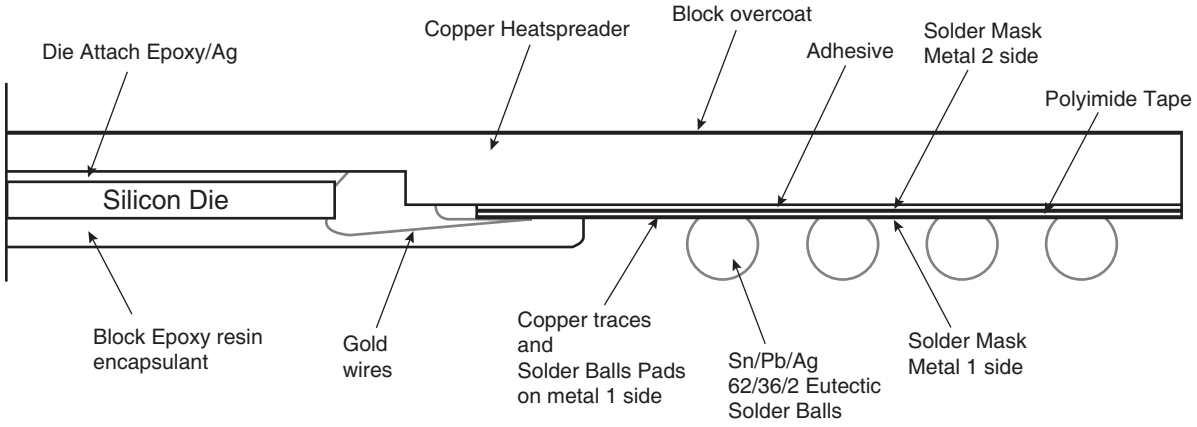
If baking is required, the devices may be baked for:

- 192 hours at 40°C + 5°C/-0°C and < 5% RH for low temperature device containers, or
- 24 hours at 125°C ± 5°C for high-temperature device containers.

6.5 Detailled Cross Section

The following diagram depicts a detailed cross section of the DMUX TBGA package.

Figure 6-5. TBGA 240: 1/2 Cross Section



In the DMUX package shown above, the die's rear side is attached to the copper heat spreader, so the copper heat spreader is at -5V.

It is necessary to use a heat sink tied to the copper heat speader.

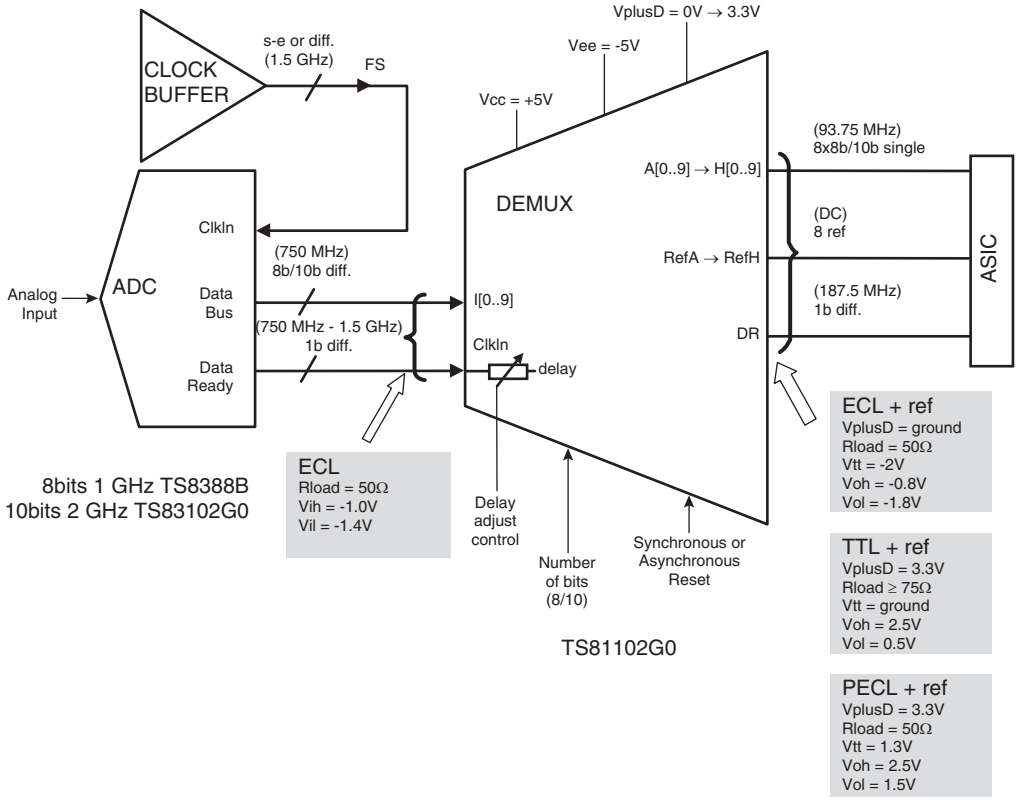
Moreover, there is only a little layer of painting over the copper heat spreader which does not isolate it.

It is therefore recommended to either isolate the heat sink from the other components of the board or to electrically isolate the copper heat spreader from the heat sink. In the latter case, one should use adequate low Rth electrical isolation.

7. Applying the Enter Title of Manual DMUX

The TSEV81102G0 DMUX evaluation board is designed to be connected with the TSEV8388G and TSEV83102G0 ADC evaluation boards.

Figure 7-1. TSEV81102G0 DMUX Evaluation Boards



Please refer to the "ADC and DMUX Application Note" for more information.

7.1 ADC to DMUX Connections

The DMUX inputs configuration has been optimized to be connected to the TS8388B ADC.

The die in the TBGA package is up. For the ADC, different types of packages can be used such as CBGA with die up or the CQFP68 down. The DMUX device being completely symmetrical, both ADC packages can be connected to the TBGA package of the DMUX criss-crossing the lines (see Table 7-1).

Table 7-1. ADC to DMUX Connections

ADC Digital Outputs CQFP68 Package	DMUX Data Inputs TBGA Package	ADC Digital Outputs CBGA Package	DMUX Data Inputs TBGA Package
D0	I7	D0	I0
D1	I6	D1	I1
D2	I5	D2	I2
D3	I4	D3	I3
D4	I3	D4	I4
D5	I2	D5	I5
D6	I1	D6	I6
D7	I0	D7	I7
–	18 not connected	–	18 not connected
–	19 not connected	–	19 not connected

Note: The connection between the ADC evaluation board and the DMUX evaluation board requires a 4-pin shift to make the D0 pin match either the I7 or I0 pin of the DMUX evaluation board.

8. TSEV81102G0TP: Device Evaluation Board

8.1 General Description

The TSEV81102G0TP DMUX Evaluation Board (EB) is designed to simplify the characterization and the evaluation of the Enter Title of Manual device (1.5 Gsps DMUX). The DMUX EB enables testing of all the DMUX functions: Synchronous and Asynchronous reset functions, selection of the DMUX ratio (1:4 or 1:8), selection of the number of bits (8 or 10), output data common mode and swing adjustment, die junction temperature measurements over military temperature range, etc.

The DMUX EB has been designed to enable easy connection to Atmel's ADC Evaluation Boards (such as TSEV8388BGL or TSEV83102G0BGL) for an extended functionality evaluation (ADC and DMUX multi-channel applications).

The DMUX EB comes fully assembled and tested, with a Enter Title of Manual device implemented on the board and a heat sink assembled on the device.

9. Ordering Information

Table 9-1. Ordering Information

Part Number	Package	Temperature Range	Screening	Comments
TS81102G0VTP	TBGA 240	"V" grade -40°C < Tc; Tj < 110°C	Standard	
TSEV81102G0TPZR3	TBGA 240	Ambient	Prototype	Evaluation board (delivered with heatsink)

10. Datasheet Status Description

Table 10-1. Datasheet Status

Datasheet Status		Validity
Objective specification	This datasheet contains target and goal specifications for discussion with customer and application validation.	Before design phase
Target specification	This datasheet contains target or goal specifications for product development.	Valid during the design phase
Preliminary specification α-site	This datasheet contains preliminary data. Additional data may be published later; could include simulation results.	Valid before characterization phase
Preliminary specification β-site	This datasheet contains also characterization results.	Valid before the industrialization phase
Product specification	This datasheet contains final product specification.	Valid for production purposes
Limiting Values		
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.		
Application Information		
Where application information is given, it is advisory and does not form part of the specification.		

10.1 Life Support Applications

These products are not designed for use in life-support appliances, devices or systems where malfunction of these products can reasonably be expected to result in personal injury. Atmel customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Atmel for any damages resulting from such improper use or sale.

10.2 Addendum

This section has been added to the description of the device for better understanding of the synchronous reset operation. It puts particular stress on the setup and hold times defined in the switching characteristics table (Table 5-4), linked with the device performances when used at full-speed (1.5 Gsps).

10.3 Synchronous Reset Operation

It first describes the operation of the synchronous reset in case the DMUX is used in DR mode and then when used in the DR/2 mode.

As a reminder, the synchronous reset has to be a signal frequency of Fs/8N in 1:8 ratio or Fs/4N in 1:4 ratio, where N is an integer.

The effect of the synchronous reset is to ensure that at each new port selection cycle, the first port to be selected is port A. The synchronous reset ensures the internal cyclic synchronization of the device during operation. It is also highly recommended in the case of multichannel applications using 2 synchronized DMUXs.

10.3.1 SETUP and HOLD Timings

The setup and hold times for the reset are defined as follows:

- SETUP from SynchReset to Clkin:

Required delay between the rising edge of the reset and the rising edge of the clock to ensure that the reset will be taken into account at the next clock edge. If the reset rising edge occurs at less than this setup time, it will be taken into account only at the second next rising edge of the clock.

A margin of ± 100ps has to be added to this setup time to compensate for the delays from the drivers and lines.

- HOLD from Clkin and SynchReset:

Minimum duration of the reset signal at a high level to be taken into account by the DMUX. This means that the reset signal has to satisfy 2 requirements: a frequency of Fs/8N or Fs/4N (N is an integer) depending on the ratio and a duty cycle such that it is high during at least the hold time.

10.3.2 Operation in DR Mode

In DR mode, the DMUX input clock can run at up to 1.5 GHz in 1:8 ratio or 1 GHz in 1:4 ratio. Both cases are described in the following timing diagrams.

Figure 10-1. Synchronous Reset Operation in DR Mode, 1:4 ratio, 750 MHz (Full-speed) – Principle of Operation

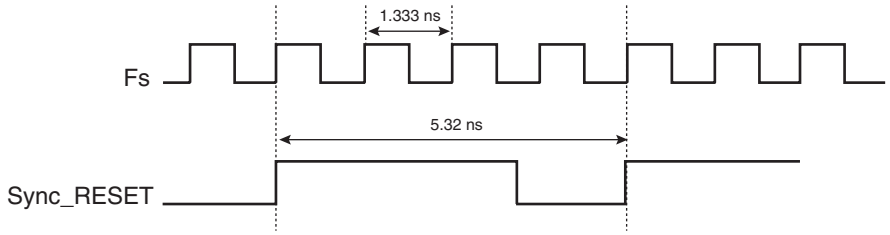
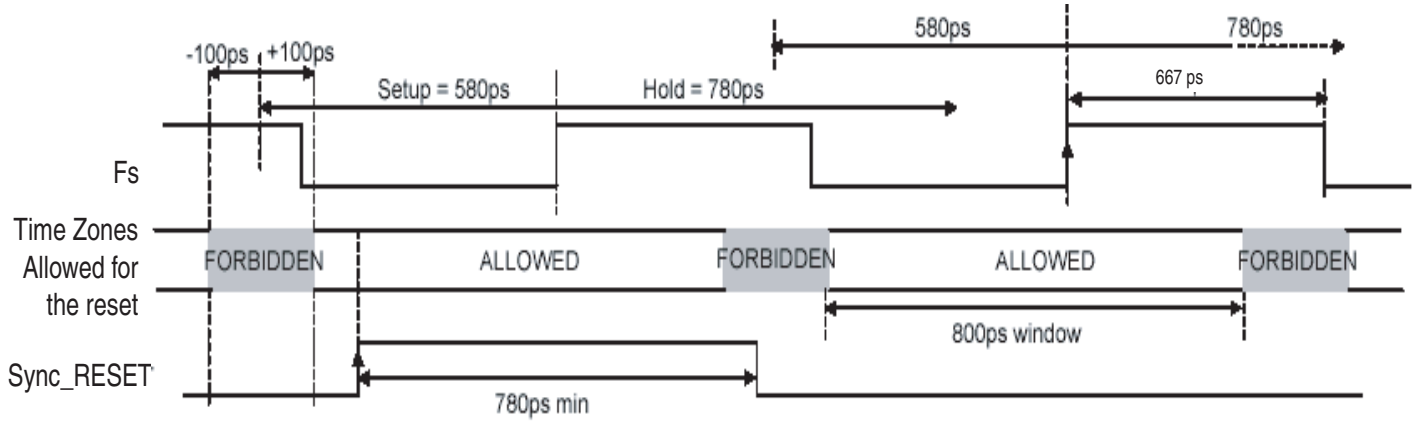


Figure 10-2. Synchronous Reset Operation in DR Mode, 1:4 ratio, 750 MHz (Full-speed) – TIMINGS



Note: The clock edge to which the reset applies is the one identified by the arrow.

If the reset rising edge had occurred in the second allowed window, the reset would have been effective on the third clock rising edge (not represented, on the right of the edge represented with the arrow).

Figure 10-3. Synchronous Reset Operation in DR Mode, 1:8 ratio, 1.5 GHz (Full-speed) – Principle of Operation

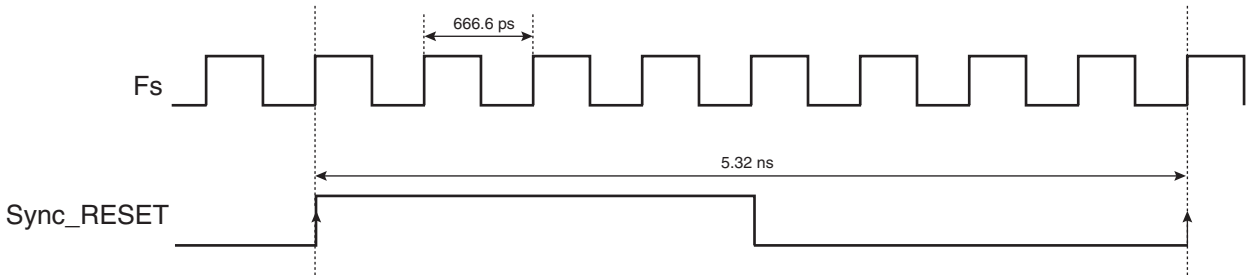
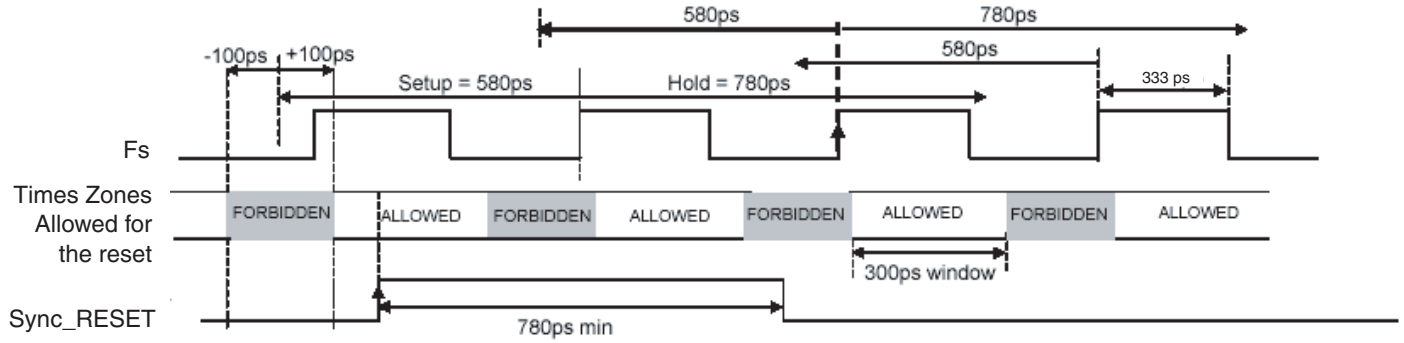


Figure 10-4. Synchronous Reset Operation in DR Mode, 1:8 ratio, 1.5 GHz (Full-speed) – Timings



Note: The clock edge to which the reset applies is the one identified by the arrow.

If the reset rising edge had occurred in the second allowed window, the reset would have been effective on the fourth clock rising edge (last clock rising edge, on the right of the edge represented with the arrow).

This case is the most critical one with only a 300 ps window for the reset.

10.4 Operation in DR/2 Mode

In DR/2 mode, the DMUX input clock can run at up to 750 MHz in 1:8 ratio or 375 MHz in 1:4 ratio, since the DR/2 clock from the ADC is half the sampling frequency.

Both cases are described in the following timing diagrams.

Figure 10-5. Synchronous Reset Operation in DR/2 Mode, 1:4 ratio, 375 MHz (Full-speed) – Principle of Operation

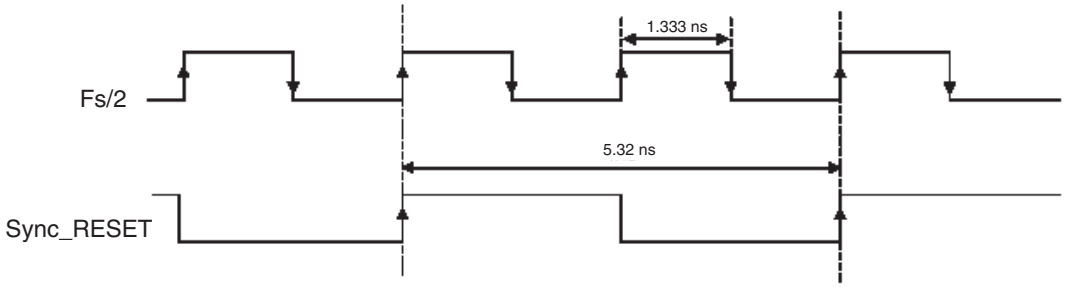
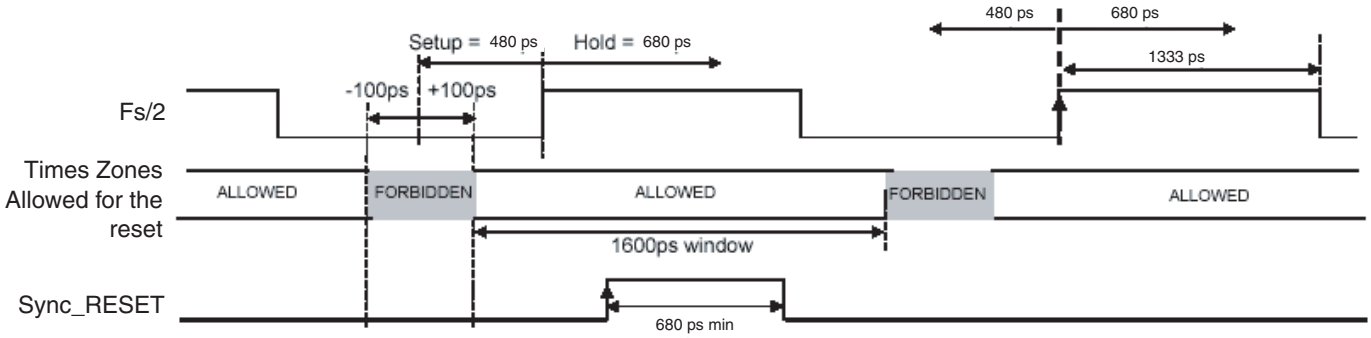


Figure 10-6. Synchronous Reset Operation in DR/2 Mode, 1:4 ratio, 375 MHz (Full-speed) – Timings



Note: The clock edge to which the reset applies is the one identified by the arrow.

If the reset rising edge had occurred in the first allowed window (on the left), the reset would have been effective on the first represented clock rising edge (first clock rising edge of the schematic, on the left of the edge represented with the arrow).

Figure 10-7. Synchronous Reset Operation in DR/2 Mode, 1:8 ratio, 750 MHz (Full-speed) – Principle of Operation

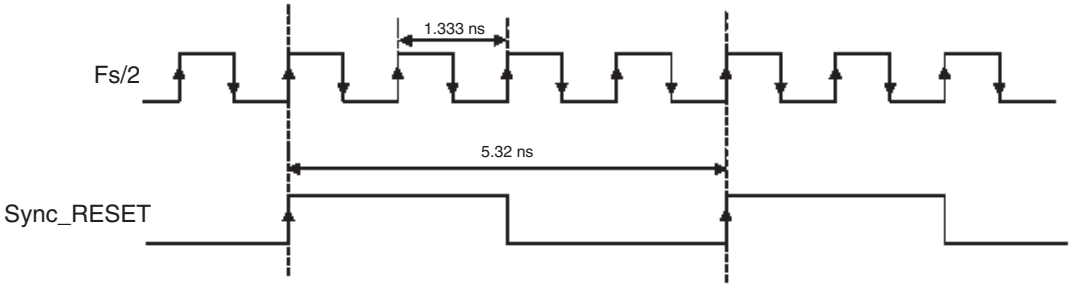
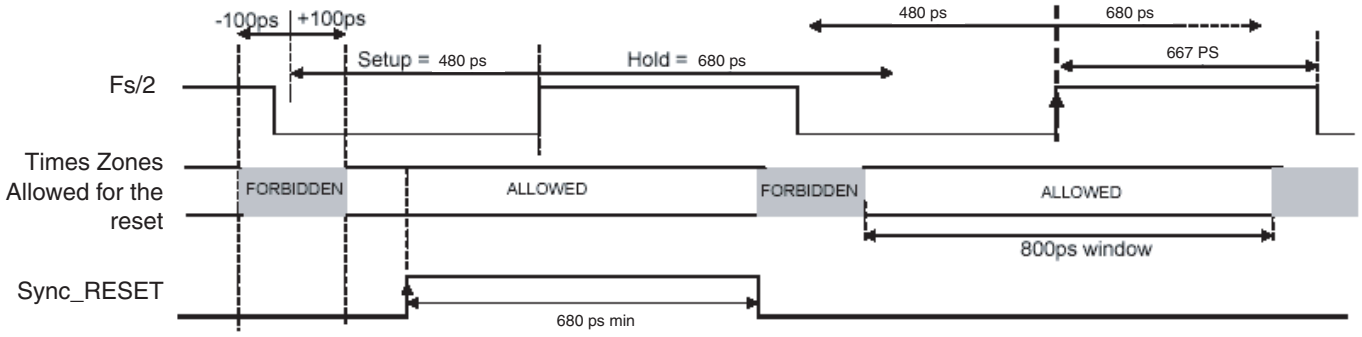


Figure 10-8. Synchronous Reset Operation in DR/2 Mode, 1:8 ratio, 750 MHz (Full-speed) – Timings



Note: The clock edge to which the reset applies is the one identified by the arrow.

If the reset rising edge had occurred in the second allowed window, the reset would have been effective on the fourth clock rising edge (not represented, on the right of the edge represented with the arrow).

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