Freescale Semiconductor
Data Sheet: Technical Data

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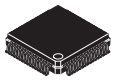
MCF51CN128

MCF51CN128 ColdFire Microcontroller Cover: MCF51CN128


80 LQFP
14 mm × 14 mm


64 LQFP
10 mm × 10 mm


48 QFN
7 mm × 7 mm

The MCF51CN128 device is a low-cost, low-power, high-performance 32-bit ColdFire V1 microcontroller (MCU) featuring 10/100 BASE-T/TX fast ethernet controller (FEC), media independent interface (MII) to connect an external physical transceiver (PHY), and multi-function external bus interface.

MCF51CN128 also has multiple communication interfaces for various ethernet gateway applications. MCF51CN128 is the first ColdFire V1 device to incorporate ethernet and external bus interface along with new features to minimize power consumption and increase functionality in low-power modes.

The MCF51CN128 features the following functional units:

- 32-bit ColdFire V1 Central Processing Unit (CPU)
  - Up to 50.33 MHz ColdFire CPU from 3.6 V to 3.0 V, up to 40 MHz CPU from 3.0 V to 2.1 V, and up to 20 MHz CPU from 2.1 V to 1.8 V across temperature range of –40 °C to 85 °C
  - Provides 0.94 Dhrystone 2.1 MIPS per MHz performance when running from internal RAM (0.76 DMIPS/MHz from flash)
  - ColdFire Instruction Set Revision C (ISA_C)
  - Support for up to 45 peripheral interrupt requests and 7 software interrupts
- On-Chip Memory
  - 128 KB Flash, 24 KB RAM
  - Flash read/program/erase over full operating voltage and temperature
  - On-chip memory aliased to create a contiguous memory space with off-chip memory
  - Security circuitry to prevent unauthorized access to Peripherals, RAM, and flash contents
- Ethernet
  - FEC—10/100 BASE-T/TX, bus-mastering fast ethernet controller with direct memory access (DMA); supports half or full duplex; operation is limited to 3.0 V to 3.6 V
  - MII—media independent interface to connect ethernet controller to external PHY; includes output clock for external PHY
- External Bus
  - Mini-FlexBus—Multi-function external bus interface; supports up to 1 MB memories, gate-array logic, simple slave device or glueless interfaces to standard chip-selected asynchronous memories
  - Programmable options: access time per chip select, burst and burst-inhibited transfers per chip select, transfer direction, and address setup and hold times
- Power-Saving Modes
  - Two low-power stop modes, one of which allows limited use of some peripherals (ADC, KBI, RTC)
  - Reduced-power wait mode shuts off CPU and allows full use of all peripherals; FEC can remain active and conduct DMA transfers to RAM and assert an interrupt to wake up the CPU upon completion
  - Low-power run and wait modes allow peripherals to run while the voltage regulator is in standby
  - Peripheral clock enable register can disable clocks to unused modules, thereby reducing currents
  - Low-power external oscillator that can be used in stop3 mode to provide accurate clock source to active peripherals
  - Low-power real-time counter for use in run, wait, and stop modes with internal and external clock sources
  - 6 µs typical wake-up time from stop3 mode
  - Pins and clocks to peripherals not available in smaller packages are automatically disabled for reduced current consumption; no user interaction is needed
- Clock Source Options
  - Oscillator (XOSC) — Loop-control pierce oscillator; crystal or ceramic resonator range of 31.25 kHz to 38.4 kHz or 1 MHz to 25 MHz
  - Multi-Purpose Clock Generator (MCG) — Freescale reserves the right to change the detail specifications as may be required to permit improvements in the design of its products.

includes precision trimming of internal reference, allowing 0.2% resolution and 2% deviation over temperature and voltage. PLL derives a higher accuracy clock source derived by an external reference

- System Protection
  - Watchdog computer operating properly (COP) reset with option to run from dedicated 1-kHz internal clock source or bus clock
  - Low-voltage detection with reset or interrupt; selectable trip points
  - Illegal opcode and illegal address detection with programmable reset or exception response
  - Flash block protection
- Development Support
  - Single-wire background debug module (BDM) interface; supports same electrical interface used by the S08, 9S12, and 9S12x families debug modules
  - 4 PC plus 2 address (optional data) breakpoint registers with programmable 1- or 2-level trigger response
  - 64-entry processor status and debug data trace buffer with programmable start/stop conditions
- Peripherals
  - ADC—Up to 12 channel, 12-bit resolution; 2.5 µs conversion time; automatic compare function; 1.7 mV/°C temperature sensor; internal bandgap reference channel; operation in stop3; fully functional from 3.6 V to 1.8 V
  - SCI—Three modules with optional 13-bit break
  - SPI—Two interfaces with full-duplex or single-wire bi-directional; double-buffered transmit and receive; master or slave mode; MSB-first or LSB-first shifting
  - IIC—Two IICs with up to 100 kbps with maxmimum bus loading; multi-master operation; programmable slave address; interrupt-driven byte-by-byte data transfer; supports broadcast mode and 11-bit addressing
  - TPM—Two 3-channel, 16-bit resolution modules; selectable input capture, output compare, or buffered edge- or center-aligned PWM on each channel
  - RTC—8-bit modulus counter with binary- or decimal-based prescaler; external clock source for precise time base, time-of-day, calendar- or task-scheduling functions; free-running on-chip low-power oscillator (1 kHz) for cyclic wake-up without external components; runs in all MCU modes
  - MTIM—Two 8-bit resolution modulo timers with 8-bit prescaler
- Input/Output
  - Up to 70 general-purpose input/output (GPIO) pins, all with pin mux controls to select alternate functions
  - 16 keyboard interrupt (KBI) pins with selectable polarity
  - Hysteresis and configurable pull-up device or input filtering on all input pins; configurable slew rate and drive strength on all output pins
  - 16 Rapid GPIO pins connected to the CPU's high-speed local bus with set, clear, and toggle functionality (PTD and PTF)

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1 MCF51CN128 Series Comparison

1.1 Device Comparison

The following table compares the various device derivatives available within the MCF51CN128 series.

Table 1. MCF51CN128 Series Device Comparison

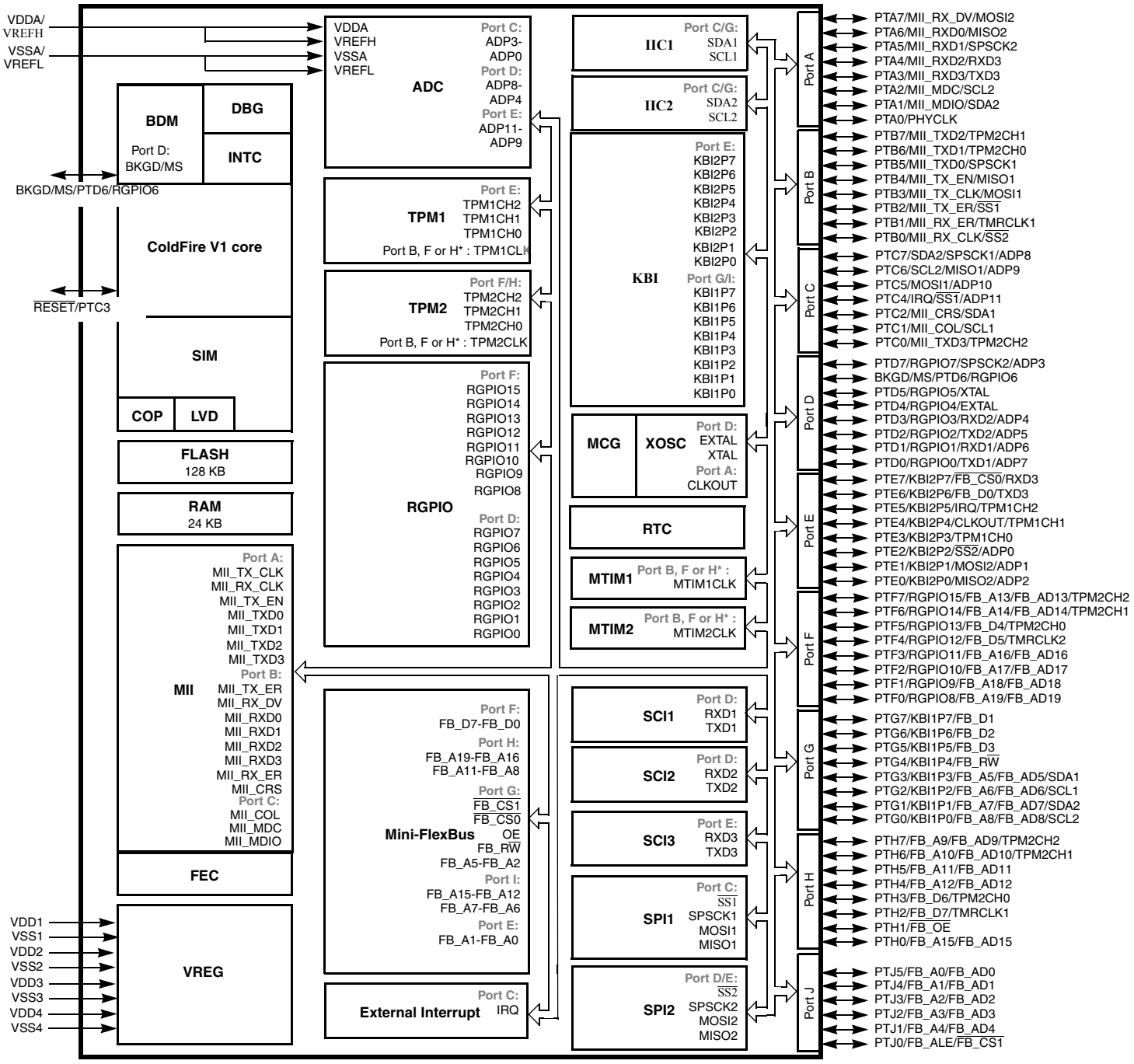
Feature	MCF51CN128		
	80-pin	64-pin	48-pin
Flash memory size (KB)	128		
RAM size (KB)	24		
V1 ColdFire core equiped with BDM (background debug module) and 2X3 Crossbar switch	Yes		
ADC (analog-to-digital converter) channels (12-bit)	12		
FEC (Fast Ethernet Controller with MII Interface)	Yes		
COP (computer operating properly)	Yes		
IIC1 (inter-integrated circuit)	Yes		
IIC2	Yes		
IRQ (interrupt request input)	Yes		
KBI (keyboard interrupts)	16	12	6
LVD (low-voltage detector)	Yes		
MCG (multipurpose clock generator)	Yes		
Port I/O[1]	70	54	38
RGPIO (rapid general-purpose I/O)	16	16	8
RTC (real-time counter)	Yes		
SCI1, SCI2 & SCI3 (serial communications interface)	Yes		
SPI1 & SPI2 (serial peripheral interface)	Yes		
TPM1 (Timer/PWM Module) channels	3	3	3
TPM2 channels	3	3	3
MTIM1 & MTIM2	Yes[2]		
External Timer Clocks	2	1	1
Mini-FlexBus	Yes	0	0
XOSC (crystal oscillator)	Yes		

1 All GPIO are muxed with other functions

2 TMRCLK2 is not available on the 48 pin package, although MTIM2 can be used as an internal timebase using on-chip clock sources.

1.2 Block Diagram

The following figure shows the connections between the MCF51CN128 series pins and modules.



* TPMx and MTIMx external clocks each have the choice of being assigned to either TMRCLK1 or TMRCLK2.

Figure 1. MCF51CN128 Series Block Diagram

2 Pin Assignments

This section describes the pin assignments for the available packages. See for pin availability by package pin-count.

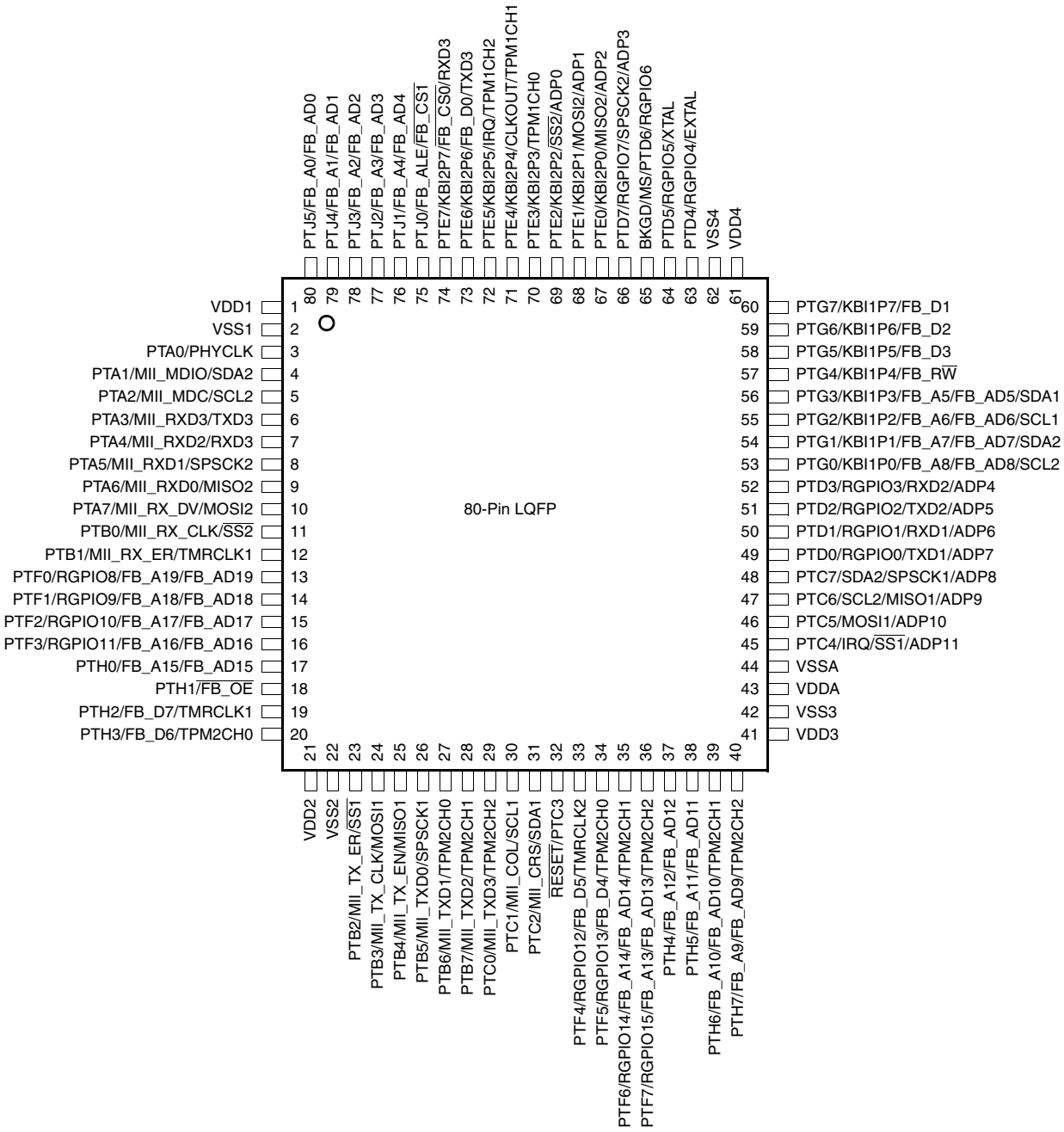


Figure 2. Pin Assignments in 80-Pin LQFP Package

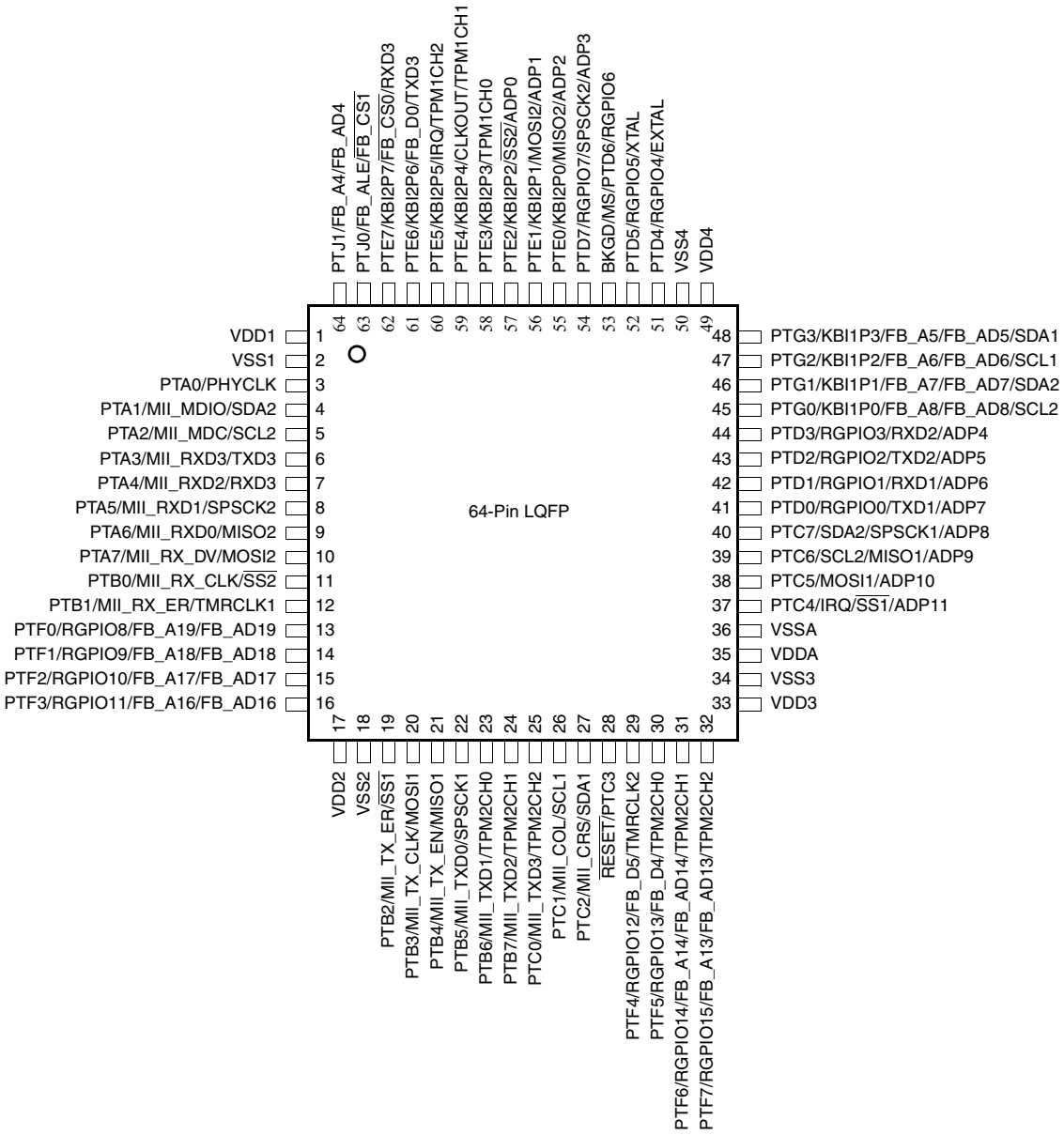


Figure 3. Pin Assignments in 64-Pin LQFP Package

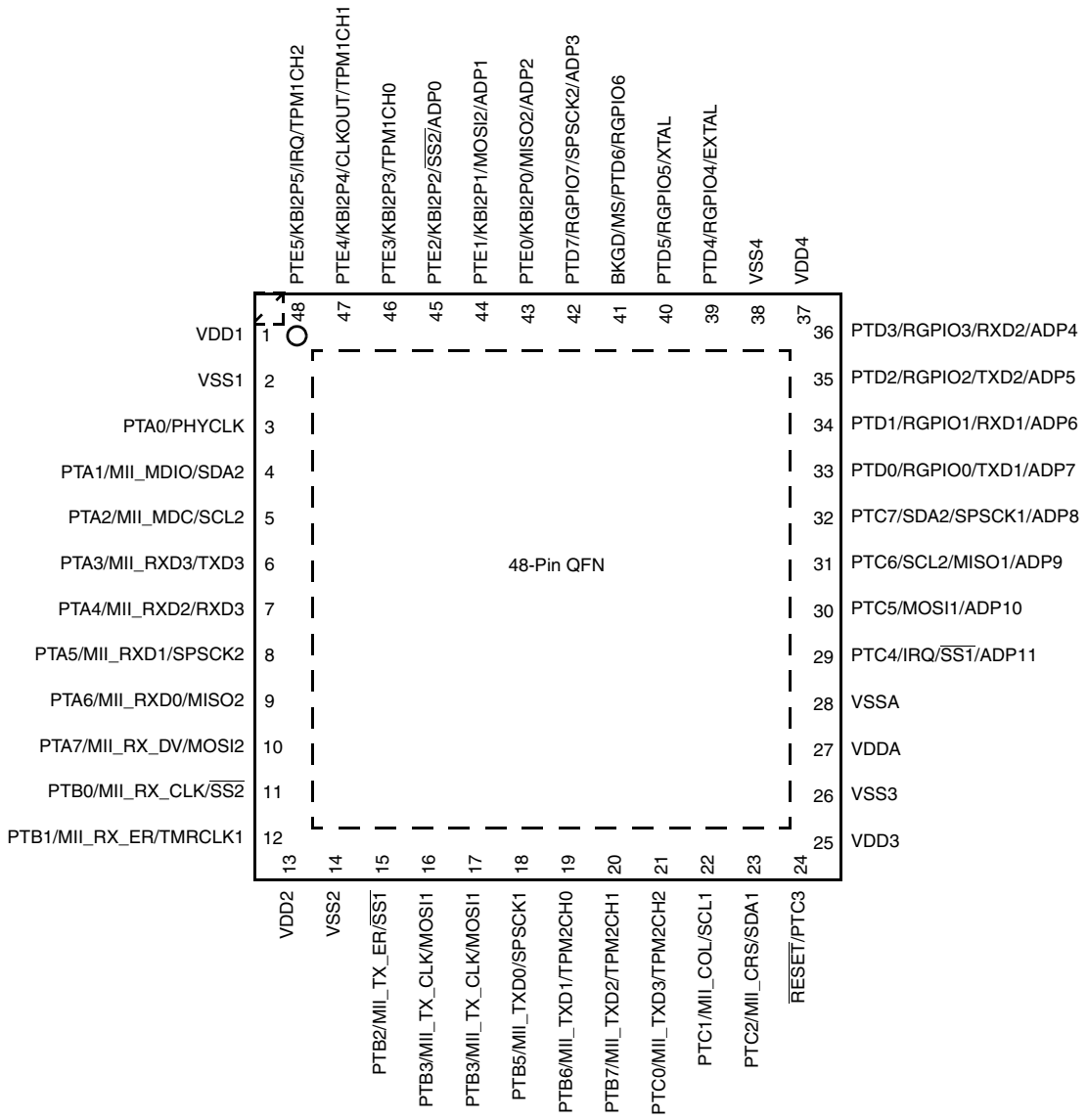


Figure 4. Pin Assignments in 48-Pin QFN Package

NOTE

There is no electrical connection to the flag for 48-pin QFN packages.

Table 2. Package Pin Assignments

80-Pin	64-Pin	48-Pin	Default Function	Alt 1	Alt 2	Alt 3	Comment
1	1	1	VDD1	—	—	—	—
2	2	2	VSS1	—	—	—	—
3	3	3	PTA0	PHYCLK	—	—	—

Table 2. Package Pin Assignments (continued)

80-Pin	64-Pin	48-Pin	Default Function	Alt 1	Alt 2	Alt 3	Comment
4	4	4	PTA1	MII_MDIO	—	SDA2	—
5	5	5	PTA2	MII_MDC	—	SCL2	—
6	6	6	PTA3	MII_RXD3	TXD3	—	—
7	7	7	PTA4	MII_RXD2	RXD3	—	—
8	8	8	PTA5	MII_RXD1	SPSCK2	—	—
9	9	9	PTA6	MII_RXD0	MISO2	—	—
10	10	10	PTA7	MII_RX_DV	MOSI2	—	—
11	11	11	PTB0	MII_RX_CLK	$\overline{SS2}$	—	—
12	12	12	PTB1	MII_RX_ER	—	TMRCLK1	—
13	13	—	PTF0/RGPIO8	—	FB_A19/FB_AD19	—	RGPIO_ENB selects between standard GPIO and RGPIO
14	14	—	PTF1/RGPIO9	—	FB_A18/FB_AD18	—	
15	15	—	PTF2/RGPIO10	—	FB_A17/FB_AD17	—	
16	16	—	PTF3/RGPIO11	—	FB_A16/FB_AD16	—	
17	—	—	PTH0	—	FB_A15/FB_AD15	—	—
18	—	—	PTH1	—	$\overline{FB\_OE}$	—	—
19	—	—	PTH2	—	FB_D7	TMRCLK1	—
20	—	—	PTH3	—	FB_D6	TPM2CH0	—
21	17	13	VDD2	—	—	—	—
22	18	14	VSS2	—	—	—	—
23	19	15	PTB2	MII_TX_ER	$\overline{SS1}$	—	—
24	20	16	PTB3	MII_TX_CLK	MOSI1	—	—
25	21	17	PTB4	MII_TX_EN	MISO1	—	—
26	22	18	PTB5	MII_TXD0	SPSCK1	—	—
27	23	19	PTB6	MII_TXD1	—	TPM2CH0	—
28	24	20	PTB7	MII_TXD2	—	TPM2CH1	—
29	25	21	PTC0	MII_TXD3	—	TPM2CH2	—
30	26	22	PTC1	MII_COL	—	SCL1	—
31	27	23	PTC2	MII_CRS	—	SDA1	—

Table 2. Package Pin Assignments (continued)

80-Pin	64-Pin	48-Pin	Default Function	Alt 1	Alt 2	Alt 3	Comment
32	28	24	$\overline{\text{RESET}}$	PTC3	—	—	This pin is a bi-directional open drain pin and has an internal pullup. There is no clamp diode to VDD. DSE and SRE port controls for this bit have no effect.
33	29	—	PTF4/RGPIO12	—	FB_D5	TMRCLK2	RGPIO_ENB selects between standard GPIO and RGPIO
34	30	—	PTF5/RGPIO13	—	FB_D4	TPM2CH0	
35	31	—	PTF6/RGPIO14	—	FB_A14/FB_AD14	TPM2CH1	
36	32	—	PTF7/RGPIO15	—	FB_A13/FB_AD13	TPM2CH2	
37	—	—	PTH4	—	FB_A12/FB_AD12	—	—
38	—	—	PTH5	—	FB_A11/FB_AD11	—	—
39	—	—	PTH6	—	FB_A10/FB_AD10	TPM2CH1	—
40	—	—	PTH7	—	FB_A9/FB_AD9	TPM2CH2	—
41	33	25	VDD3	—	—	—	—
42	34	26	VSS3	—	—	—	—
43	35	27	VDDA	—	—	—	—
44	36	28	VSSA	—	—	—	—
45	37	29	PTC4	IRQ	$\overline{\text{SS1}}$	ADP11	—
46	38	30	PTC5	—	MOSI1	ADP10	—
47	39	31	PTC6	SCL2	MISO1	ADP9	—
48	40	32	PTC7	SDA2	SPSCK1	ADP8	—
49	41	33	PTD0/RGPIO0	—	TXD1	ADP7	RGPIO_ENB selects between standard GPIO and RGPIO
50	42	34	PTD1/RGPIO1	—	RXD1	ADP6	
51	43	35	PTD2/RGPIO2	—	TXD2	ADP5	
52	44	36	PTD3/RGPIO3	—	RXD2	ADP4	
53	45	—	PTG0	KBI1P0	FB_A8/FB_AD8	SCL2	—
54	46	—	PTG1	KBI1P1	FB_A7/FB_AD7	SDA2	—
55	47	—	PTG2	KBI1P2	FB_A6/FB_AD6	SCL1	—
56	48	—	PTG3	KBI1P3	FB_A5/FB_AD5	SDA1	—
57	—	—	PTG4	KBI1P4	FB_$\overline{\text{RW}}$	—	—
58	—	—	PTG5	KBI1P5	FB_D3	—	—
59	—	—	PTG6	KBI1P6	FB_D2	—	—

Table 2. Package Pin Assignments (continued)

80-Pin	64-Pin	48-Pin	Default Function	Alt 1	Alt 2	Alt 3	Comment
60	—	—	PTG7	KBI1P7	FB_D1	—	—
61	49	37	VDD4	—	—	—	—
62	50	38	VSS4	—	—	—	—
63	51	39	PTD4/RGPIO4	—	—	EXTAL	RGPIO_ENB selects between standard GPIO and RGPIO
64	52	40	PTD5/RGPIO5	—	—	XTAL	
65	53	41	BKGD/MS	PTD6/RGPIO6	—	—	This pin has an internal pullup. PTD6/RGPIO6 can only be programmed as an output.[1]
66	54	42	PTD7RGPIO7	—	SPSCK2	ADP3	RGPIO_ENB selects between standard GPIO and RGPIO
67	55	43	PTE0	KBI2P0	MISO2	ADP2	—
68	56	44	PTE1	KBI2P1	MOSI2	ADP1	—
69	57	45	PTE2	KBI2P2	$\overline{SS2}$	ADP0	—
70	58	46	PTE3	KBI2P3	—	TPM1CH0	—
71	59	47	PTE4	KBI2P4	CLKOUT	TPM1CH1	—
72	60	48	PTE5	KBI2P5	IRQ	TPM1CH2	—
73	61	—	PTE6	KBI2P6	FB_D0	TXD3	—
74	62	—	PTE7	KBI2P7	$\overline{FB\_CS0}$	RXD3	—
75	63	—	PTJ0	FB_ALE	$\overline{FB\_CS1}$	—	—
76	64	—	PTJ1	—	FB_A4/FB_AD4	—	—
77	—	—	PTJ2	—	FB_A3/FB_AD3	—	—
78	—	—	PTJ3	—	FB_A2/FB_AD2	—	—
79	—	—	PTJ4	—	FB_A1/FB_AD1	—	—
80	—	—	PTJ5	—	FB_A0/FB_AD0	—	—

[1] RGPIO_ENB selects between standard GPIO and RGPIO. When PTD6 is set as RGPIO output, and "1" is driven to PTD6 via RGPIO function, a read of register RGPIODATA6 always returns a "0" because V1 RGPIO design looks for IO enable when the return value of RGPIO function reads data. As PTD6 is set to RGPIO output only, it returns "0" always to RGPIODATA6, athough PTD6 pin is driven to high.

3 Electrical Characteristics

3.1 Introduction

This section contains electrical and timing specifications for the MCF51CN128 series of microcontrollers available at the time of publication.

3.2 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 3. Parameter Classifications

P	These parameters are guaranteed during production testing on each individual device.
C	These parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	These parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	These parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

3.3 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table 4 may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}) or the programmable pull-up resistor associated with the pin is enabled.

Table 4. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.3 to +3.8	V
Maximum current into V_{DD}	I_{DD}	120	mA
Digital input voltage	V_{In}	–0.3 to V_{DD} + 0.3	V
Instantaneous maximum current Single pin limit (applies to all port pins)[1, 2, 3]	I_D	± 25	mA
Storage temperature range	T_{stg}	–55 to 150	°C

1 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

2 All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

3 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low (which would reduce overall power consumption).

3.4 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 5. Thermal Characteristics

Rating		Symbol	Value	Unit
Operating temperature range (packaged)		T_A	T_L to T_H (–40 to 85 or 0 to 70)[1]	°C
Maximum junction temperature		T_{JM}	95	°C
Thermal resistance Single-layer board				
	48-pin QFN	θ_{JA}	81	°C/W
	64-pin LQFP		69	
	80-pin LQFP		60	
Thermal resistance Four-layer board				
	48-pin QFN	θ_{JA}	26	°C/W
	64-pin LQFP		50	
	80-pin LQFP		47	

1 Depending on device.

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad \textit{Eqn. 1}$$

where:

T_A = Ambient temperature, °C
θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W
$P_D = P_{int} + P_{I/O}$
$P_{int} = I_{DD} \times V_{DD}$, Watts — chip internal power
$P_{I/O}$ = Power dissipation on input and output pins — user determined

For most applications, $P_{I/O} << P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad \textit{Eqn. 2}$$

Solving Equation 1 and Equation 2 for K gives:

$$K = P_D \times (T_A + 273°C) + \theta_{JA} \times (P_D)^2 \quad \textit{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

3.5 ESD Protection and Latch-Up Immunity

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, normal handling precautions should be used to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits. During the device qualification ESD stresses were performed for the human body model (HBM), the machine model (MM) and the charge device model (CDM).

A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 6. ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human Body	Series resistance	R1	1500	Ω
	Storage capacitance	C	100	pF
	Number of pulses per pin	—	3	
Machine	Series resistance	R1	0	Ω
	Storage capacitance	C	200	pF
	Number of pulses per pin	—	3	
Latch-up	Minimum input voltage limit	—	– 2.5	V
	Maximum input voltage limit	—	7.5	V

Table 7. ESD and Latch-Up Protection Characteristics

No.	Rating[1]	Symbol	Min	Max	Unit
1	Human body model (HBM)	V_{HBM}	± 2000	—	V
2	Machine model (MM)	V_{MM}	± 200	—	V
3	Charge device model (CDM)	V_{CDM}	± 500	—	V
4	Latch-up current at T_A = 85°C	I_{LAT}	± 100	—	mA

1 Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

3.6 DC Characteristics

This section includes information about power supply requirements and I/O pin characteristics.

Table 8. DC Characteristics

Num	C	Characteristic		Symbol	Condition	Min	Typ[1]	Max	Unit
1	—	Operating Voltage[2]		—	—	1.8[3]	—	3.6	V
2	C	Output high voltage	All I/O pins, low-drive strength	V_{OH}	1.8 V, I_{Load} = –2 mA	V_{DD} – 0.5	—	—	V
	P		All I/O pins, high-drive strength		2.7 V, I_{Load} = –10 mA	V_{DD} – 0.5	—	—	
	T				2.3 V, I_{Load} = –6 mA	V_{DD} – 0.5	—	—	
	C				1.8V, I_{Load} = –3 mA	V_{DD} – 0.5	—	—	
3	D	Output high current	Max total I_{OH} for all ports	I_{OHT}	—	—	—	100	mA
4	C	Output low voltage	All I/O pins, low-drive strength	V_{OL}	1.8 V, I_{Load} = 2 mA	—	—	0.5	V
	P		All I/O pins, high-drive strength		2.7 V, I_{Load} = 10 mA	—	—	0.5	
	T				2.3 V, I_{Load} = 6 mA	—	—	0.5	
	C				1.8 V, I_{Load} = 3 mA	—	—	0.5	
5	D	Output low current	Max total I_{OL} for all ports	I_{OLT}	—	—	—	100	mA
6	P	Input high voltage	all digital inputs	V_{IH}	V_{DD} > 2.7 V	0.70 x V_{DD}	—	—	V
	C				V_{DD} > 1.8 V	0.85 x V_{DD}	—	—	
7	P	Input low voltage	all digital inputs	V_{IL}	V_{DD} > 2.7 V	—	—	0.35 x V_{DD}	
	C				V_{DD} >1.8 V	—	—	0.30 x V_{DD}	
8	C	Input hysteresis	all digital inputs	V_{hys}	—	0.06 x V_{DD}	—	—	mV
9	P	Input leakage current	all input only pins (Per pin)	$\lvert I_{In} \rvert$	V_{In} = V_{DD} or V_{SS}	—	0.1	1	µA
10	P	Hi-Z (off-state) leakage current	all input/output (per pin)	$\lvert I_{OZ} \rvert$	V_{In} = V_{DD} or V_{SS}	—	0.1	1	µA
11	P	Pull resistors	all digital inputs, when enabled	R_P	—	17.5	—	52.5	kΩ
12	D	DC injection current [4, 5, 6]	Single pin limit	I_{IC}	V_{IN} < V_{SS}, V_{IN} > V_{DD}	–0.2	—	0.2	mA
			Total MCU limit, includes sum of all stressed pins			–5	—	5	mA
13	C	Input Capacitance, all pins		C_{In}		—	—	8	pF
14	C	POR re-arm voltage[7]		V_{POR}		0.9	1.4	1.79	V
15	D	POR re-arm time		t_{POR}		10	—	—	µs
16	P	Low-voltage detection threshold — high range[8]		V_{LVDH}[9]	V_{DD} falling V_{DD} rising	2.15 2.24	2.32 2.39	2.45 2.49	V

Table 8. DC Characteristics (continued)

Num	C	Characteristic	Symbol	Condition	Min	Typ[1]	Max	Unit
17	P	Low-voltage detection threshold — low range[8]	V_{LVDL}	V_{DD} falling V_{DD} rising	1.70 1.80	1.83 1.89	1.95 2.00	V
18	P	Low-voltage warning threshold — high range[8]	V_{LVWH}	V_{DD} falling V_{DD} rising	2.50 2.50	2.62 2.62	2.70 2.70	V
19	P	Low-voltage warning threshold — low range[8]	V_{LVWL}	V_{DD} falling V_{DD} rising	2.25 2.29	2.32 2.39	2.45 2.49	V
20	P	Bandgap Voltage Reference[10]	V_{BG}	—	1.15	1.17	1.18	V

1 Typical values are measured at 25 °C. Characterized, not tested

2 As an exception, the Fast Ethernet Controller (FEC) is only operational above the operating voltage of 3 V.

3 As the supply voltage rises, the LVD circuit will hold the MCU in reset until the supply has risen above V_{LVDL}.

4 All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

5 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

6 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

7 Maximum is highest voltage that POR is guaranteed.

8 Low voltage detection and warning limits measured at 1 MHz bus frequency.

9 Run at 1 MHz bus frequency

10 Factory trimmed at V_{DD} = 3.3 V, Temp = 25 °C

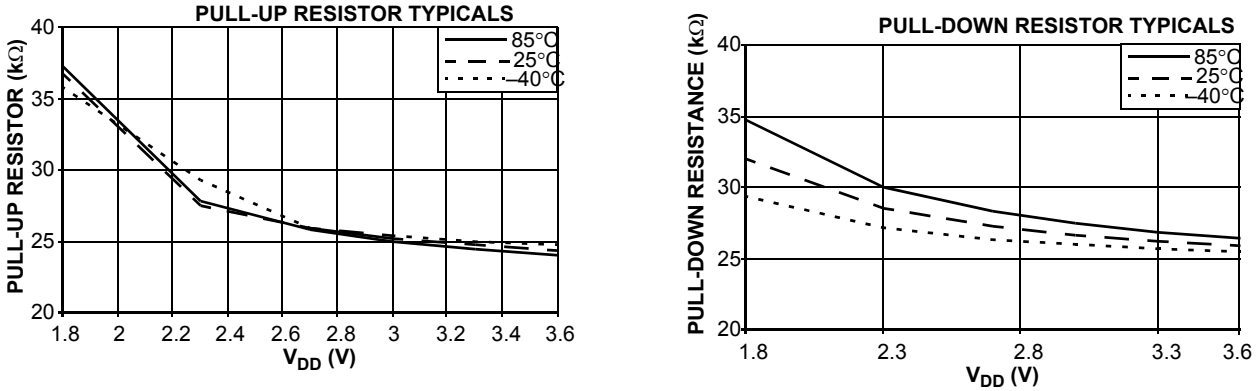


Figure 5. Pull-up and Pull-down Typical Resistor Values

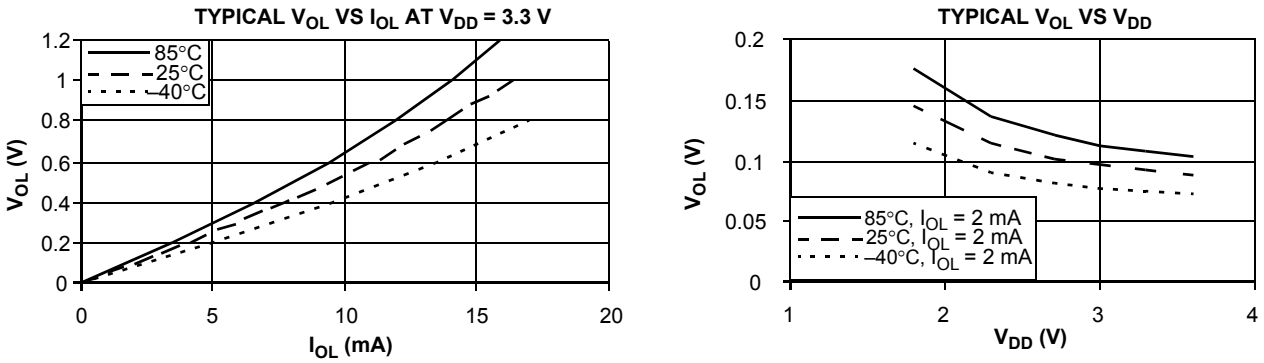


Figure 6. Typical Low-Side Driver (Sink) Characteristics — Low Drive (PTxDSn = 0)

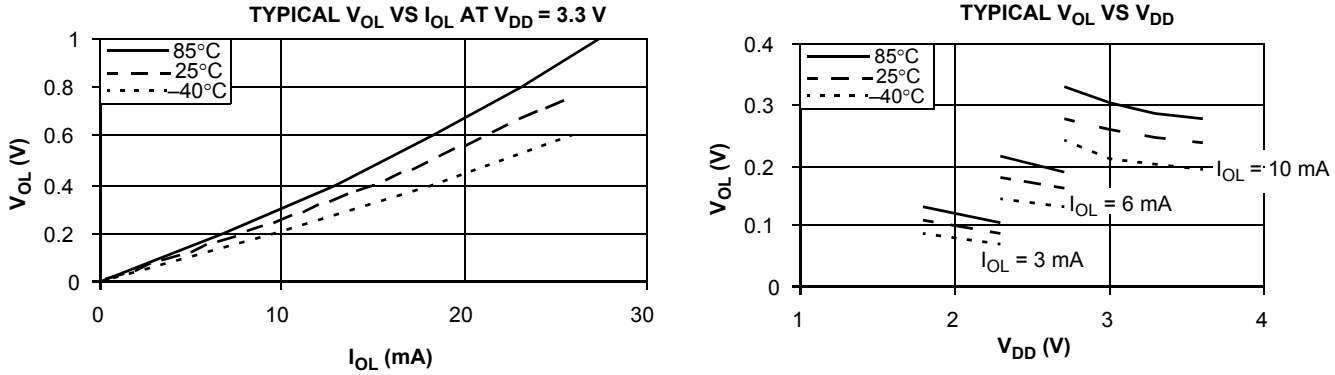


Figure 7. Typical Low-Side Driver (Sink) Characteristics — High Drive (PTxDSn = 1)

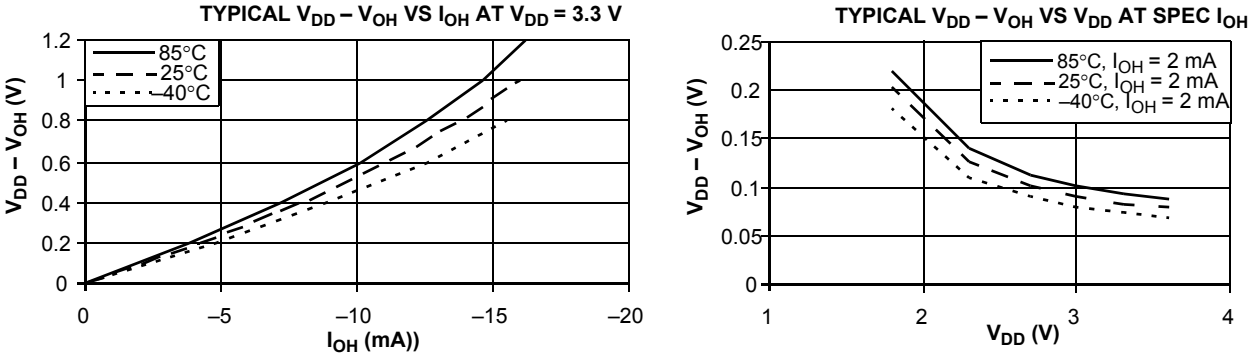


Figure 8. Typical High-Side (Source) Characteristics — Low Drive (PTxDSn = 0)

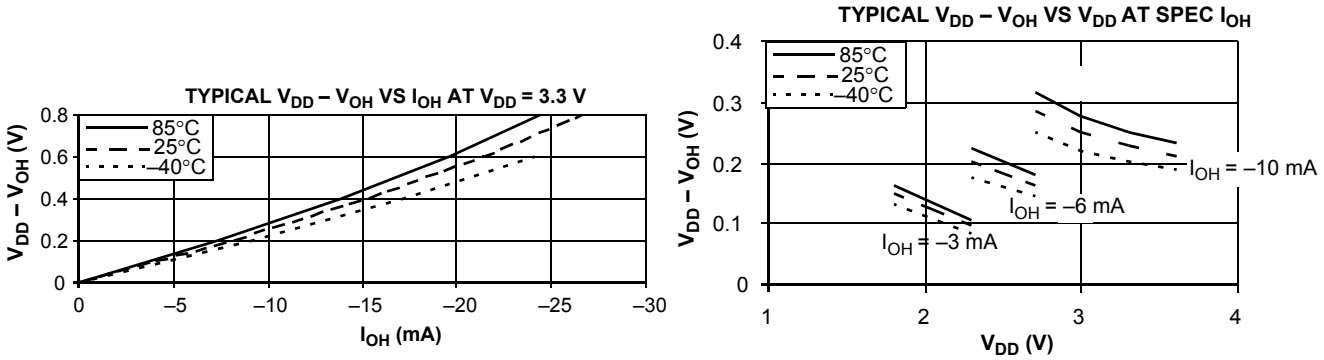


Figure 9. Typical High-Side (Source) Characteristics — High Drive (PTxDSn = 1)

3.7 Supply Current Characteristics

This section includes information about power supply current in various operating modes.

Table 9. Supply Current Characteristics

Num	C	Parameter	Symbol	Bus Freq	V_{DD} (V)	Typ[1]	Max	Unit	Temp (°C)
1	P	Run supply current FEI mode, all modules on	RI_{DD}	25 MHz	3.3	60	75	mA	–40 to 85 °C
	T			20 MHz		49	—		
	T			8 MHz		21	—		
	T			1 MHz		4.6	—		
2	C	Run supply current FEI mode, all modules off	RI_{DD}	25 MHz	3.3	44	47	mA	–40 to 85 °C
	T			20 MHz		36	—		
	T			8 MHz		15.5	—		
	T			1 MHz		3.9	—		
3	T	Run supply current LPRS=0, all modules off	RI_{DD}	16 kHz FBILP	3.3	203	—	µA	–40 to 85 °C
	T			16 kHz FBELP		154	—		
4	T	Run supply current LPRS=1, all modules off, running from Flash	RI_{DD}	16 kHz FBELP	3.3	50	—	µA	–40 to 85 °C
5	C	Wait mode supply current FEI mode, all modules off	WI_{DD}	25 MHz	3.3	11	13.7	µA	–-40 to 85 °C
	T			20 MHz		4.57	—		
	T			8 MHz		2	—		
	T			1 MHz		0.73	—		
6	C	Stop2 mode supply current	$S2I_{DD}$	n/a	3.3	0.35	11	µA	0 to 70 °C
	P						45		–40 to 85 °C
	C				1.8	0.35	12		0 to 70 °C
	C						16.2		–40 to 85 °C

Table 9. Supply Current Characteristics (continued)

Num	C	Parameter		Symbol	Bus Freq	V_{DD} (V)	Typ[1]	Max	Unit	Temp (°C)
7	C	Stop3 mode supply current No clocks active		$S3I_{DD}$	n/a	3.3	0.52	14	µA	0 to 70 °C
	P							55		–40 to 85 °C
	C					1.8	0.52	15		0 to 70 °C
	C							32.4		–40 to 85 °C
8	T	Low power mode adders:	EREFSTEN=1	—	32 kHz	3.3	500	—	nA	–40 to 85 °C
9	T		IREFSTEN=1		32 kHz		70	—	µA	–40 to 85 °C
10	T		TPM PWM		100 Hz		12	—	µA	–40 to 85 °C
11	T		SCI, SPI, or IIC		300 bps		15	—	µA	–40 to 85 °C
12	T		RTC using LPO		1 kHz		200	—	nA	–40 to 85 °C
13	T		RTC using ICSERCLK		32 kHz		1	—	µA	–40 to 85 °C
14	T		LVD		n/a		100	—	µA	–40 to 85 °C

[1] Data in Typical column was characterized at 3.3 V, 25 °C or is typical recommended value.

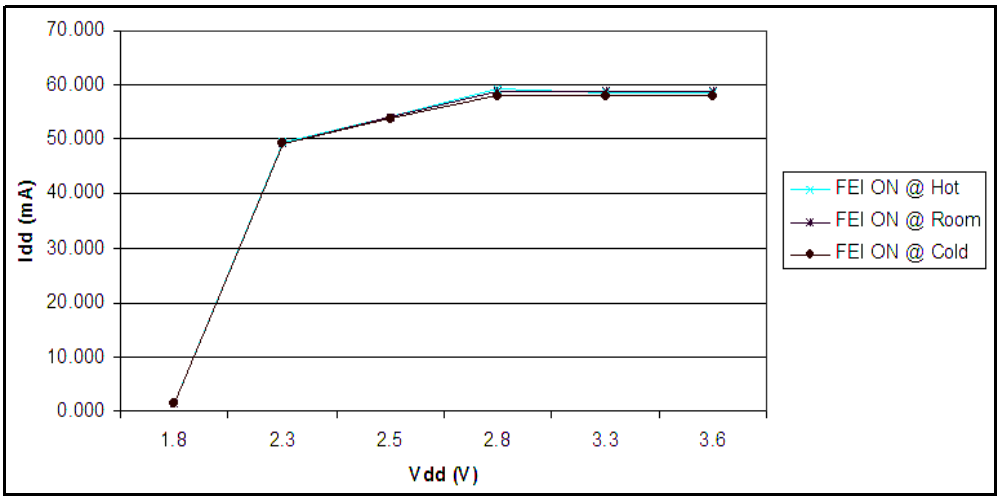


Figure 10. Typical Run I_{DD} for FBE and FEI, I_{DD} vs. V_{DD} (ADC off, All Other Modules Enabled)

3.8 External Oscillator (XOSC) Characteristics

Reference Figure 11 and Figure 12 for crystal or resonator circuits.

Table 10. XOSC and ICS Specifications (Temperature Range = –40 to 85 °C Ambient)

Num	C	Characteristic	Symbol	Min	Typ[1]	Max	Unit
1	C	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1) Low range (RANGE = 0) High range (RANGE = 1), high gain (HGO = 1) High range (RANGE = 1), low power (HGO = 0)	 f_{lo} f_{hi} f_{hi}	 32 1 1	 — — —	 38.4 25 8	 kHz MHz MHz
2	D	Load capacitors Low range (RANGE=0), low power (HGO=0) Other oscillator settings	C_1,C_2	See Note[2] See Note[3]			
3	D	Feedback resistor Low range, low power (RANGE=0, HGO=0)[2] Low range, High Gain (RANGE=0, HGO=1) High range (RANGE=1, HGO=X)	R_F	 — — —	 — 10 1	 — — —	MΩ
4	D	Series resistor — Low range, low power (RANGE = 0, HGO = 0)[2] Low range, high gain (RANGE = 0, HGO = 1) High range, low power (RANGE = 1, HGO = 0) High range, high gain (RANGE = 1, HGO = 1) ≥ 8 MHz 4 MHz 1 MHz	R_S	 — — — — — —	 — 0 100 0 0 0	 — — — 0 10 20	 Ω KΩ
5	C	Crystal start-up time [4] Low range, low power Low range, high power High range, low power High range, high power	 t_{CSTL} t_{CSTH} 	 — — — —	 200 400 5 15	 — — — —	 ms
6	D	Square wave input clock frequency (EREFS = 0, ERCLKEN = 1) External with FLL / PLL enabled (FEE / PEE) External with bypass (FBE.FBELP,PBE, PBELP)	f_{extal}	 0.03125 0	 — —	 50.33 50.33	 MHz MHz

1 Data in Typical column was characterized at 3.3 V, 25 °C or is typical recommended value.

2 Load capacitors (C_1,C_2), feedback resistor (R_F) and series resistor (R_S) are incorporated internally when RANGE=HGO=0.

3 See crystal or resonator manufacturer's recommendation.

4 Proper PC board layout procedures must be followed to achieve specifications.

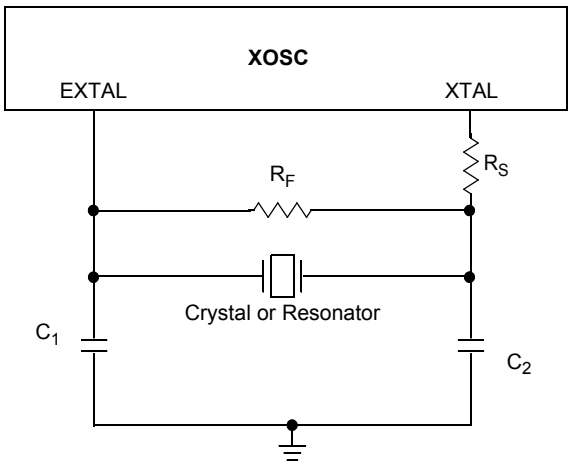


Figure 11. Typical Crystal or Resonator Circuit: High Range and Low Range/High Gain

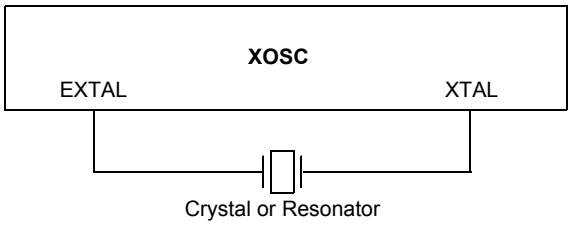


Figure 12. Typical Crystal or Resonator Circuit: Low Range/Low Gain

3.9 Multipurpose Clock Generator (MCG) Specifications

Table 11. MCG Frequency Specifications (Temperature Range = –40 to 125 °C Ambient)

Num	C	Rating	Symbol	Min	Typical	Max	Unit
1	P	Internal reference frequency - factory trimmed at V_{DD} = and temperature = 25 °C	f_{int_ft}	—	32.768	—	kHz
2	P	Average internal reference frequency - untrimmed [1]	f_{int_ut}	25	—	41.66	kHz
3	P	Average internal reference frequency - user trimmed	f_{int_t}	31.25	—	39.06	kHz
4	D	Internal reference startup time	t_{irefst}	—	60	100	us
5	—	DCO output frequency range - untrimmed [1] value provided for reference: f_{dco_ut} = 1024 X f_{int_ut}	f_{dco_ut}	25.6	33.48	42.66	MHz
6	P	DCO output frequency range - trimmed	f_{dco_t}	32	—	40	MHz
7	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (using FTRIM)	$\Delta f_{dco\_res\_t}$	—	± 0.1	± 0.2	$\%f_{dco}$

Table 11. MCG Frequency Specifications (continued)(Temperature Range = –40 to 125 °C Ambient)

Num	C	Rating	Symbol	Min	Typical	Max	Unit
8	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (not using FTRIM)	$\Delta f_{dco\_res\_t}$	—	± 0.2	± 0.4	$\%f_{dco}$
9	P	Total deviation of trimmed DCO output frequency over voltage and temperature	Δf_{dco_t}	—	+ 0.5 -1.0	± 2	$\%f_{dco}$
10	C	Total deviation of trimmed DCO output frequency over fixed voltage and temperature range of 0 - 70 °C	Δf_{dco_t}	—	± 0.5	± 1	$\%f_{dco}$
11	C	FLL acquisition time [2]	$t_{fll\_acquire}$	—	—	1	ms
12	D	PLL acquisition time [3]	$t_{pll\_acquire}$	—	—	1	ms
13	C	Long term Jitter of DCO output clock (averaged over 2ms interval) [4]	C_{Jitter}	—	0.02	0.2	$\%f_{dco}$
14	D	VCO operating frequency	f_{vco}	7.0	—	55.0	MHz
15	D	Lock entry frequency tolerance[5]	D_{lock}	± 1.49	—	± 2.98	%
16	D	Lock exit frequency tolerance[6]	D_{unl}	± 4.47	—	± 5.97	%
17	D	Lock time - FLL	t_{fll_lock}	—	—	$t_{fll\_acquire}$+ 1075(1/f_{int_t})	s
18	D	Lock time - PLL	t_{pll_lock}	—	—	$t_{pll\_acquire}$+ 1075(1/f_{pll_ref})	s
19	D	Loss of external clock minimum frequency - RANGE = 0	f_{loc_low}	(3/5) x f_{int}	—	—	kHz

1 TRIM register at default value (0x80) and FTRIM control bit at default value (0x0).

2 This specification applies to any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

3 This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

4 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{BUS}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

5 Below D_{lock} minimum, the MCG is guaranteed to enter lock. Above D_{lock} maximum, the MCG does not enter lock. But if the MCG is already in lock, then the MCG may stay in lock.

6 Below D_{unl} minimum, the MCG does not exit lock if already in lock. Above D_{unl} maximum, the MCG is guaranteed to exit lock.

3.10 Mini-FlexBus Timing Specifications

A multi-function external bus interface called Mini-FlexBus is provided with basic functionality to interface to slave-only devices up to a maximum bus frequency of 25.1666 MHz. It can be directly connected to asynchronous or synchronous devices such as external boot ROMs, flash memories, gate-array logic, or other simple target (slave) devices with little or no additional circuitry. For asynchronous devices a simple chip-select based interface can be used.

All processor bus timings are synchronous; that is, input setup/hold and output delay are given in respect to the rising edge of a reference clock, MB_CLK. The MB_CLK frequency is half the internal system bus frequency.

The following timing numbers indicate when data is latched or driven onto the external bus, relative to the Mini-FlexBus output clock (MB_CLK). All other timing relationships can be derived from these values.

Table 12. Mini-FlexBus AC Timing Specifications

Num	C	Characteristic	Min	Max	Unit	Notes
—	—	Frequency of Operation	—	25.1666	MHz	—
MB1	D	Clock Period	39.73	—	ns	—
MB2	P	Output Valid	—	20	ns	1
MB3	D	Output Hold	1.0	—	ns	1
MB4	P	Input Setup	22	—	ns	2
MB5	D	Input Hold	10	—	ns	2

1 Specification is valid for all MB_A[19:0], MB_D[7:0], $\overline{\text{MB\_CS}}$[1:0], $\overline{\text{MB\_OE}}$, MB_R/$\overline{\text{W}}$, and MB_ALE.

2 Specification is valid for all MB_D[7:0].

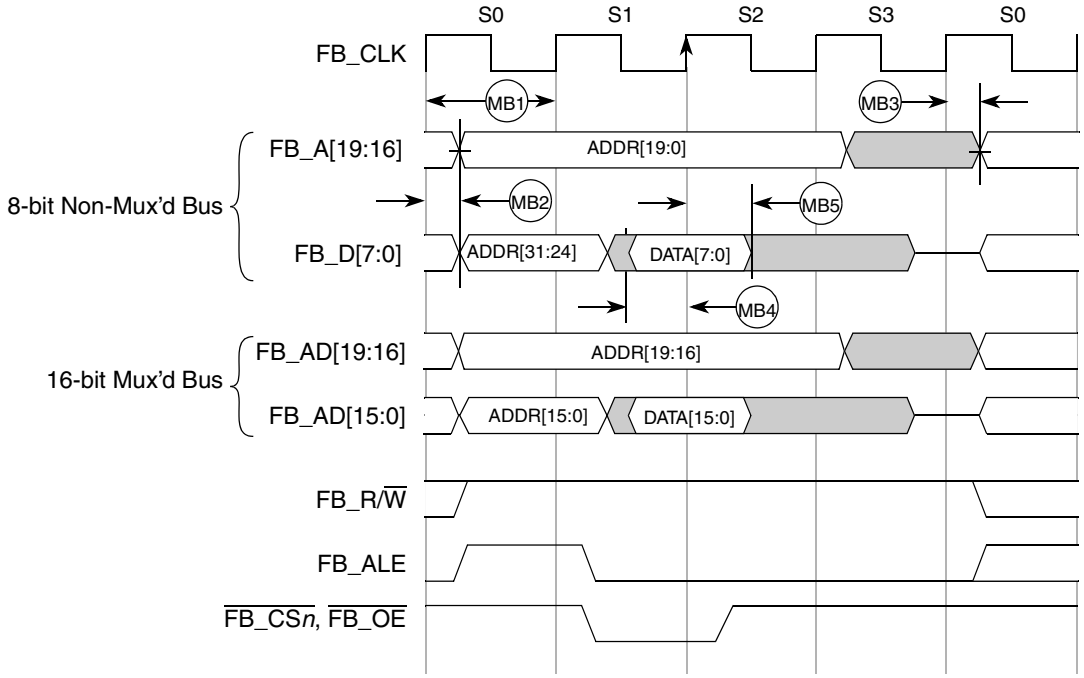


Figure 13. Mini-FlexBus Read Timing

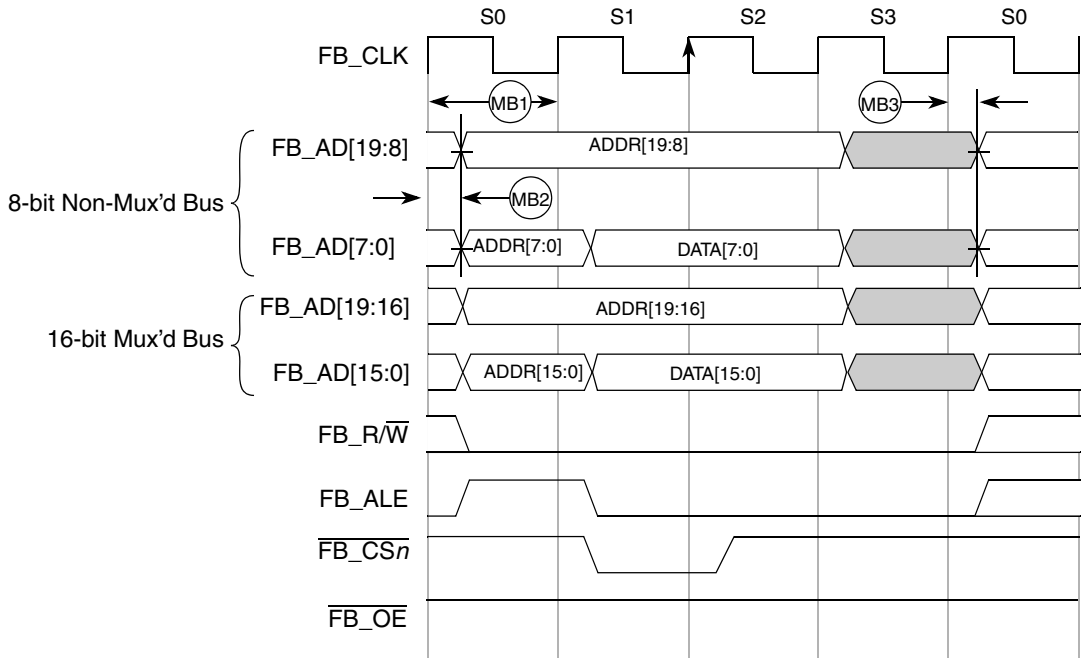


Figure 14. Mini-FlexBus Write Timing

3.11 Fast Ethernet Timing Specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

3.11.1 Receive Signal Timing Specifications

The following timing specs meet the requirements for MII and 7-Wire style interfaces for a range of transceiver devices.

Table 13. Receive Signal Timing

Num	C	Characteristic	MII Mode		Unit
			Min	Max	
—	—	RXCLK frequency	—	25	MHz
E1	P	RXD[3:0], RXDV, RXER to RXCLK setup	5	—	ns
E2	D	RXCLK to RXD[3:0], RXDV, RXER hold	5	—	ns
E3	D	RXCLK pulse width high	35%	65%	RXCLK period
E4	D	RXCLK pulse width low	35%	65%	RXCLK period

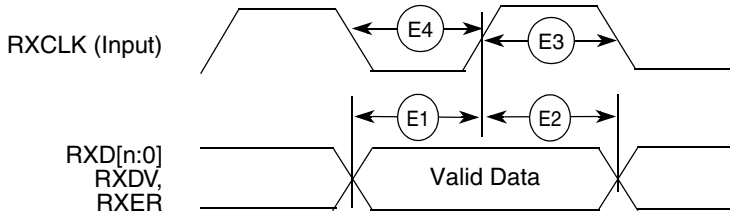


Figure 15. MII Receive Signal Timing Diagram

3.11.2 Transmit Signal Timing Specifications

Table 14. Transmit Signal Timing

Num	C	Characteristic	MII Mode		Unit
			Min	Max	
—	—	TXCLK frequency	—	25	MHz
E5	D	TXCLK to TXD[3:0], TXEN, TXER invalid	5	—	ns
E6	P	TXCLK to TXD[3:0], TXEN, TXER valid	—	25	ns
E7	D	TXCLK pulse width high	35%	65%	t_{TXCLK}
E8	D	TXCLK pulse width low	35%	65%	t_{TXCLK}

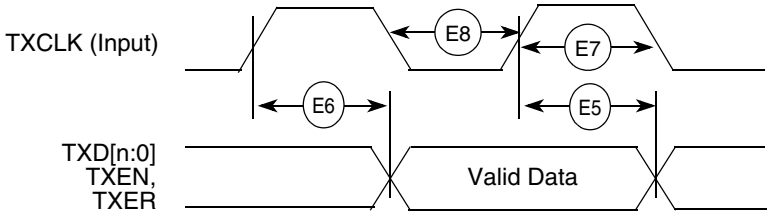


Figure 16. MII Transmit Signal Timing Diagram

3.11.3 Asynchronous Input Signal Timing Specifications

Table 15. MII Transmit Signal Timing

Num	C	Characteristic	Min	Max	Unit
E9	D	CRS, COL minimum pulse width	1.5	—	TXCLK period

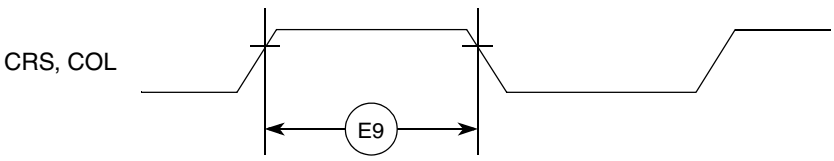


Figure 17. MII Async Inputs Timing Diagram

3.11.4 MII Serial Management Timing Specifications

Table 16. MII Serial Management Channel Signal Timing

Num	C	Characteristic	Symbol	Min	Max	Unit
E10	D	MDC cycle time	t_{MDC}	400	—	ns
E11	D	MDC pulse width	—	40	60	% t_{MDC}
E12	D	MDC to MDIO output valid	—	—	375	ns
E13	D	MDC to MDIO output invalid	—	30	—	ns
E14	D	MDIO input to MDC setup	—	5	—	ns
E15	D	MDIO input to MDC hold	—	15	—	ns

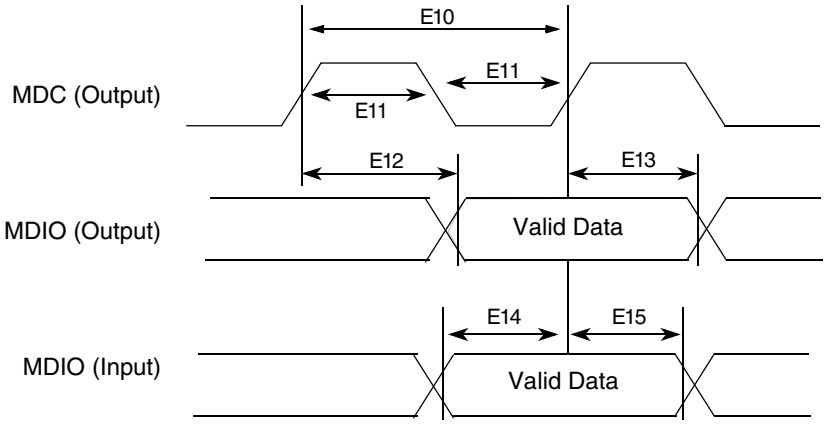


Figure 18. MII Serial Management Channel TIming Diagram

3.12 AC Characteristics

This section describes timing characteristics for each peripheral system.

3.12.1 Control Timing

Table 17. Control Timing

Num	C	Rating	Symbol	Min	Typ[1]	Max	Unit
1	D	Bus frequency (t_{cyc} = 1/f_{Bus}) V_{DD} > 2.7 V 2.7 V > V_{DD} > 2.1 V 2.1 V > V_{DD} > 1.8 V	f_{Bus}	 dc dc dc	 — — —	 50.33 40 20	MHz
2	D	Internal low power oscillator period	t_{LPO}	700	—	1300	µs
3	D	External reset pulse width[2]	t_{extrst}	100	—	—	ns
4	D	Reset low drive	t_{rstdrv}	34 x t_{cyc}	—	—	ns
5	D	BKGD/MS setup time after issuing background debug force reset to enter user or BDM modes	t_{MSSU}	500	—	—	ns

Table 17. Control Timing (continued)

Num	C	Rating	Symbol	Min	Typ[1]	Max	Unit
6	D	BKGD/MS hold time after issuing background debug force reset to enter user or BDM modes [3]	t_{MSH}	100	—	—	µs
7	D	IRQ pulse width Asynchronous path[2] Synchronous path[4]	t_{ILIH}, t_{IHIL}	100 2 x t_{cyc}	— —	— —	ns
8	D	Keyboard interrupt pulse width Asynchronous path[2] Synchronous path[4]	t_{ILIH}, t_{IHIL}	100 2 x t_{cyc}	— —	— —	ns
9	C	Port rise and fall time — Low output drive (PTxDS = 0) (load = 50 pF)[5] Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	— —	16 23	— —	ns
		Port rise and fall time — High output drive (PTxDS = 1) (load = 50 pF) Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	— —	5 9	— —	ns
10	C	Stop3 recovery time, from interrupt event to vector fetch	t_{STPREC}	—	6	10	µs

1 Typical values are based on characterization data at V_{DD} = 3.3 V, 25 °C unless otherwise stated.

2 This is the shortest pulse that is guaranteed to be recognized as a reset or interrupt pin request. Shorter pulses are not guaranteed to override reset requests from internal sources.

3 To enter BDM mode following a POR, BKGD/MS should be held low during the power-up and for a hold time of t_{MSH} after V_{DD} rises above V_{LVD}.

4 This is the minimum assertion time in which the interrupt may be recognized. The correct protocol is to assert the interrupt request until it is explicitly negated by the interrupt service routine.

5 Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range –40 °C to 85 °C.

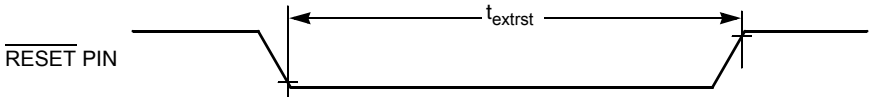


Figure 19. Reset Timing

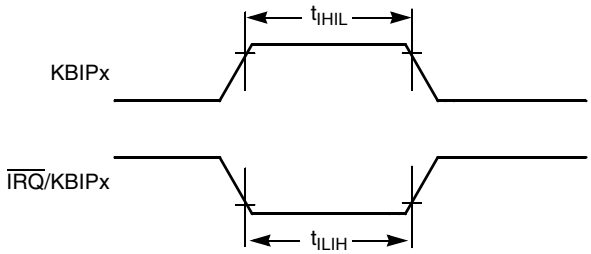


Figure 20. IRQ/KBIPx Timing

3.12.2 TPM Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 18. TPM Input Timing

No.	C	Function	Symbol	Min	Max	Unit
1	D	External clock frequency	f_{TCLK}	0	$f_{Bus}/4$	Hz
2	D	External clock period	t_{TCLK}	4	—	t_{cyc}
3	D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
4	D	External clock low time	t_{clkl}	1.5	—	t_{cyc}
5	D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

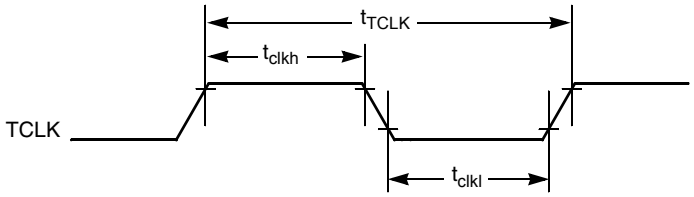


Figure 21. Timer External Clock

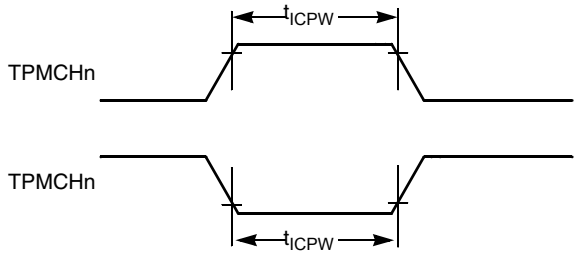


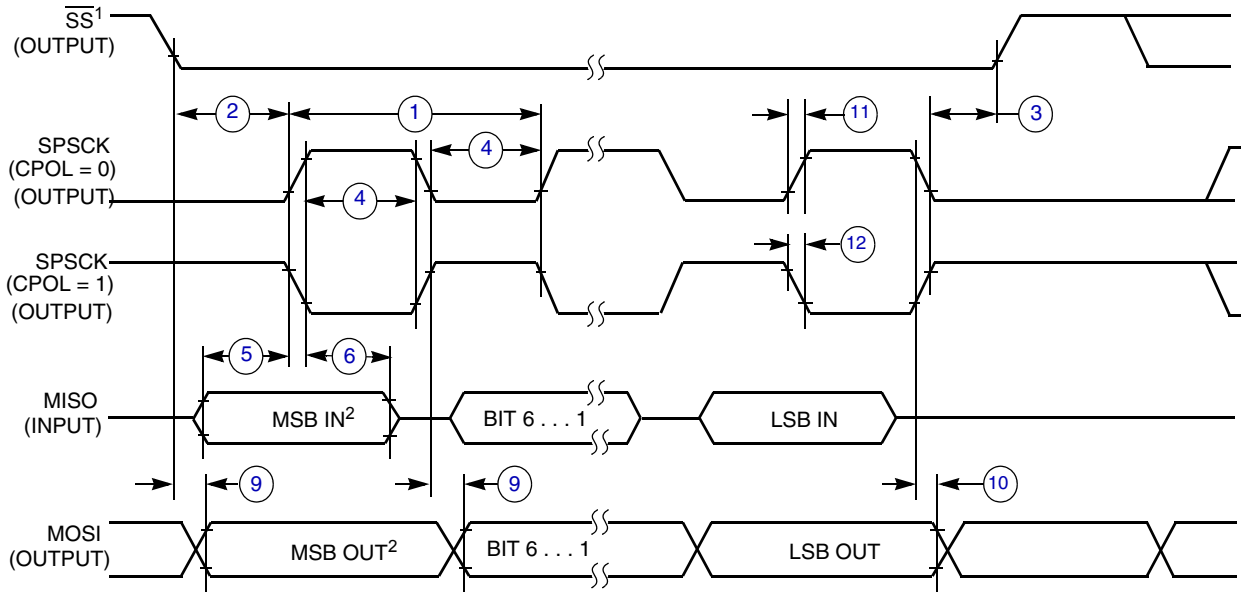
Figure 22. Timer Input Capture Pulse

3.12.3 SPI Timing

Table 19 and Figure 23 through Figure 26 describe the timing requirements for the SPI system.

Table 19. SPI Timing

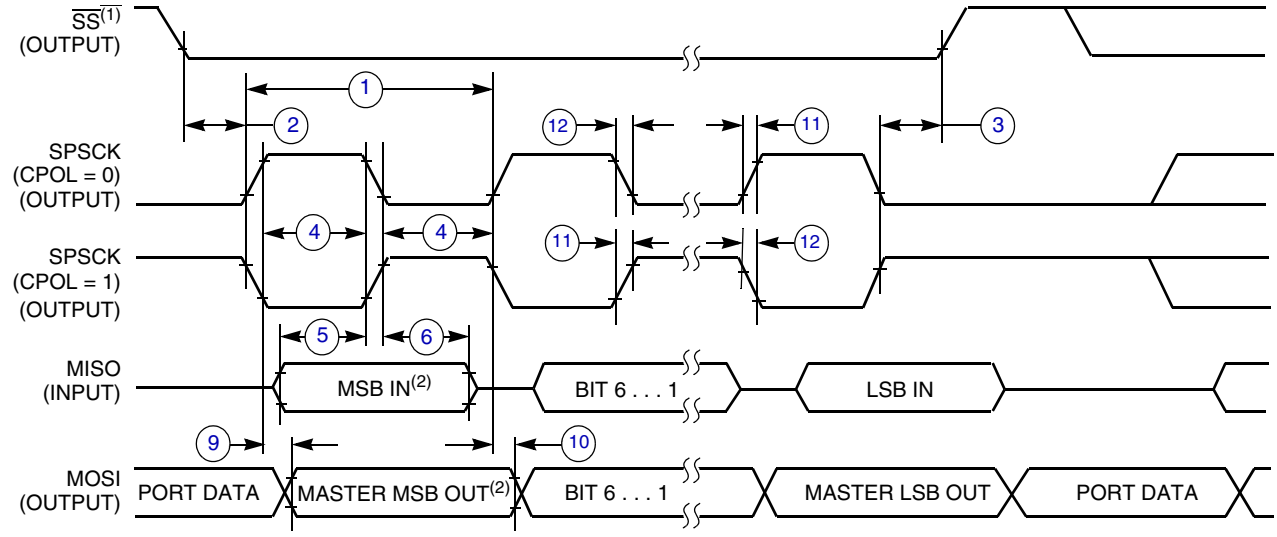
No.	C	Function	Symbol	Min	Max	Unit
—	D	Operating frequency Master Slave	f_{op}	 $f_{Bus}/2048$ 0	 $f_{Bus}/2$ $f_{Bus}/4$	 Hz Hz
1	D	SPSCK period Master Slave	t_{SPSCK}	 2 4	 2048 —	 t_{cyc} t_{cyc}
2	D	Enable lead time Master Slave	t_{Lead}	 1/2 1	 — —	 t_{SPSCK} t_{cyc}
3	D	Enable lag time Master Slave	t_{Lag}	 1/2 1	 — —	 t_{SPSCK} t_{cyc}
4	D	Clock (SPSCK) high or low time Master Slave	t_{WSPSCK}	 $t_{cyc} - 30$ $t_{cyc} - 30$	 1024 t_{cyc} —	 ns ns
5	D	Data setup time (inputs) Master Slave	t_{SU}	 15 15	 — —	 ns ns
6	D	Data hold time (inputs) Master Slave	t_{HI}	 0 25	 — —	 ns ns
7	D	Slave access time	t_a	—	1	t_{cyc}
8	D	Slave MISO disable time	t_{dis}	—	1	t_{cyc}
9	D	Data valid (after SPSCK edge) Master Slave	t_v	 — —	 25 25	 ns ns
10	D	Data hold time (outputs) Master Slave	t_{HO}	 0 0	 — —	 ns ns
11	D	Rise time Input Output	 t_{RI} t_{RO}	 — —	 $t_{cyc} - 25$ 25	 ns ns
12	D	Fall time Input Output	 t_{FI} t_{FO}	 — —	 $t_{cyc} - 25$ 25	 ns ns



NOTES:

1. $\overline{SS}$ output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

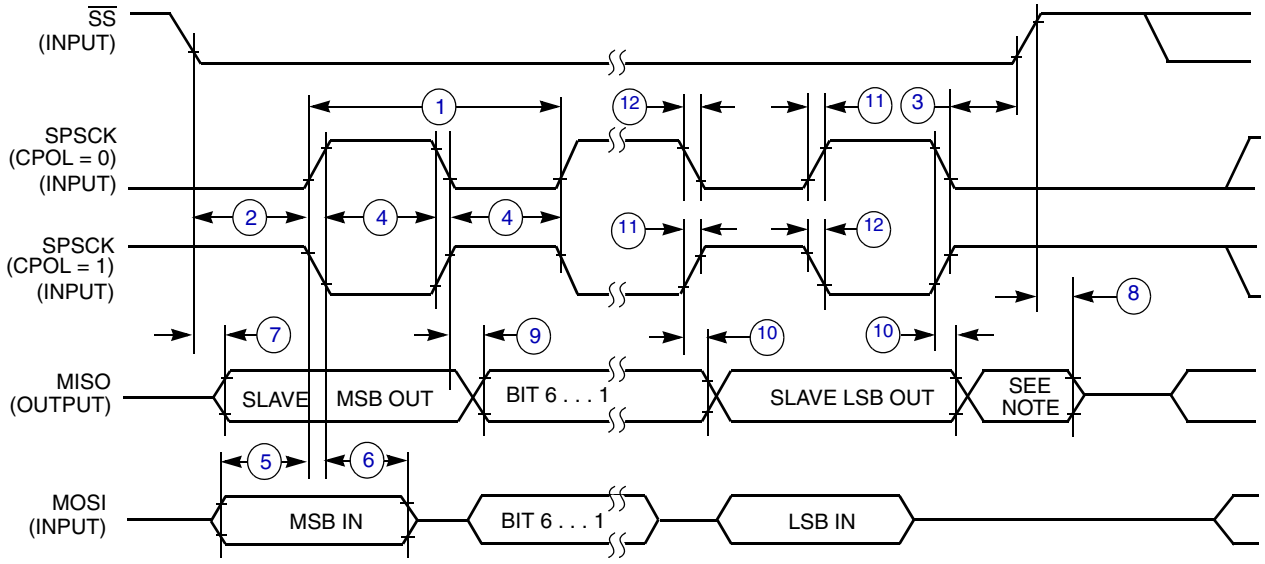
Figure 23. SPI Master Timing (CPHA = 0)



NOTES:

1. $\overline{SS}$ output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

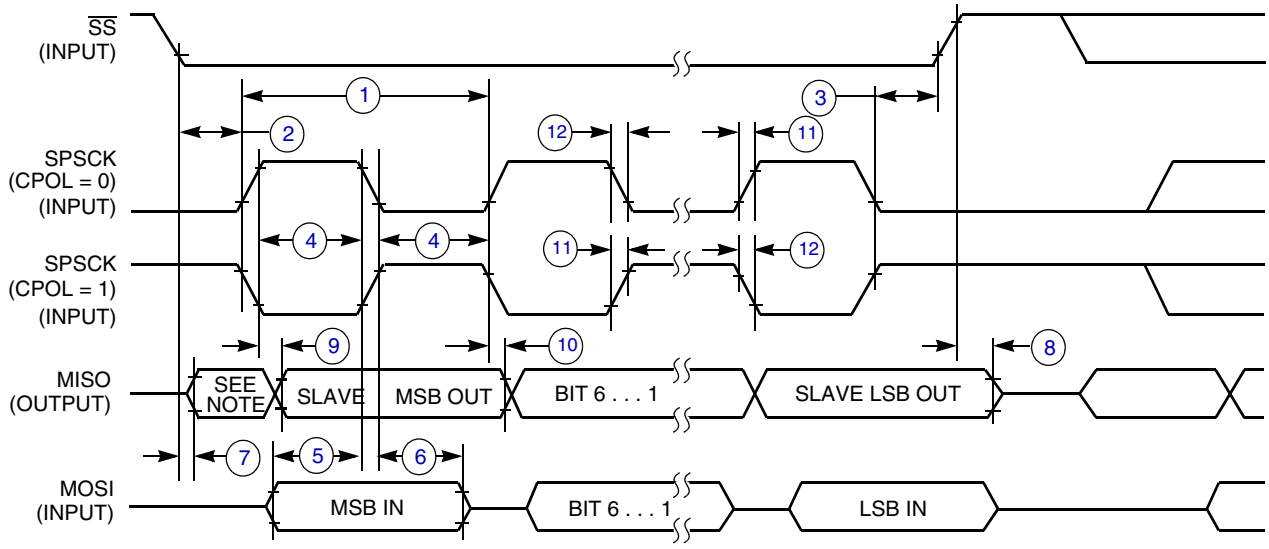
Figure 24. SPI Master Timing (CPHA =1)



NOTE:

1. Not defined but normally MSB of character just received

Figure 25. SPI Slave Timing (CPHA = 0)



NOTE:

1. Not defined but normally LSB of character just received

Figure 26. SPI Slave Timing (CPHA = 1)

3.12.4 ADC Characteristics

Table 20. 12-bit ADC Operating Conditions

C	Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
D	Supply voltage	Absolute	V_{DDAD}	1.8	—	3.6	V	
		Delta to V_{DD} (V_{DD}-V_{DDAD})[2]	ΔV_{DDAD}	-100	0	+100	mV	
D	Ground voltage	Delta to V_{SS} (V_{SS}-V_{SSAD})[2]	ΔV_{SSAD}	-100	0	+100	mV	
D	Ref Voltage High		V_{REFH}	1.8	V_{DDAD}	V_{DDAD}	V	
D	Ref Voltage Low		V_{REFL}	V_{SSAD}	V_{SSAD}	V_{SSAD}	V	
D	Input Voltage		V_{ADIN}	V_{REFL}	—	V_{REFH}	V	
C	Input Capacitance		C_{ADIN}	—	4.5	5.5	pF	
C	Input Resistance		R_{ADIN}	—	5	7	kΩ	
C	Analog Source Resistance	12 bit mode f_{ADCK} > 4MHz f_{ADCK} < 4MHz	R_{AS}	 — —	 — —	 2 5	kΩ	External to MCU
		10 bit mode f_{ADCK} > 4MHz f_{ADCK} < 4MHz		 — —	 — —	 5 10		
		8 bit mode (all valid f_{ADCK})		—	—	10		
D	ADC Conversion Clock Freq.	High Speed (ADLPC=0)	f_{ADCK}	0.4	—	8.0	MHz	
		Low Power (ADLPC=1)		0.4	—	4.0		

1 Typical values assume V_{DDAD} = 3.3 V, Temp = 25 °C, f_{ADCK}=1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 DC potential difference.

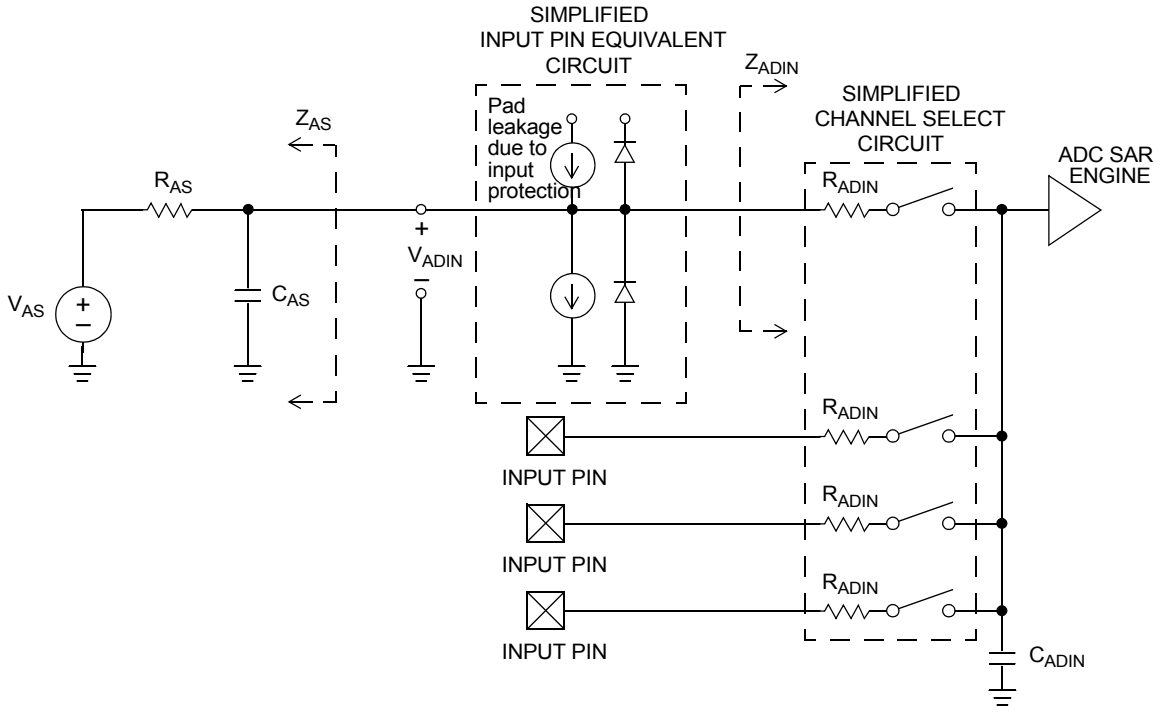


Figure 27. ADC Input Impedance Equivalency Diagram

Table 21. 12-bit ADC Characteristics (V_{REFH} = V_{DDAD}, V_{REFL} = V_{SSAD})

Characteristic	Conditions	C	Symb	Min	Typ[1]	Max	Unit	Comment
Supply Current ADLPC=1 ADLSMP=1 ADCO=1		T	I_{DDAD}	—	120	—	μA	
Supply Current ADLPC=1 ADLSMP=0 ADCO=1		T	I_{DDAD}	—	202	—	μA	
Supply Current ADLPC=0 ADLSMP=1 ADCO=1		T	I_{DDAD}	—	288	—	μA	
Supply Current ADLPC=0 ADLSMP=0 ADCO=1		T	I_{DDAD}	—	0.532	1	mA	
Supply Current	Stop, Reset, Module Off	D	I_{DDAD}	—	0.007	0.8	μA	
ADC Asynchronous Clock Source	High Speed (ADLPC=0)	P	f_{ADACK}	2	3.3	5	MHz	$t_{ADACK} = 1/f_{ADACK}$
	Low Power (ADLPC=1)	C		1.25	2	3.3		

Table 21. 12-bit ADC Characteristics (V_{REFH} = V_{DDAD}, V_{REFL} = V_{SSAD}) (continued)

Characteristic	Conditions	C	Symb	Min	Typ[1]	Max	Unit	Comment
Conversion Time (Including sample time)	Short Sample (ADLSMP=0)	P	t_{ADC}	—	20	—	ADCK cycles	See the ADC chapter in the *MCF51CN128 Reference Manual* for conversion time variances
	Long Sample (ADLSMP=1)	C		—	40	—		
Sample Time	Short Sample (ADLSMP=0)	P	t_{ADS}	—	3.5	—	ADCK cycles	
	Long Sample (ADLSMP=1)	C		—	23.5	—		
Total Unadjusted Error	12 bit mode	T	E_{TUE}	—	±3.0	—	LSB[2]	Includes Quantization
	10 bit mode	P		—	±1	±2.5		
	8 bit mode	T		—	±0.5	±1.0		
Differential Non-Linearity	12 bit mode	T	DNL	—	±1.75	—	LSB[2]	
	10 bit mode[3]	P		—	±0.5	±1.0		
	8 bit mode[3]	T		—	±0.3	±0.5		
Integral Non-Linearity	12 bit mode	T	INL	—	±1.5	—	LSB[2]	
	10 bit mode	P		—	±0.5	±1.0		
	8 bit mode	T		—	±0.3	±0.5		
Zero-Scale Error	12 bit mode	T	E_{ZS}	—	±1.5	—	LSB[2]	V_{ADIN} = V_{SSAD}
	10 bit mode	P		—	±0.5	±1.5		
	8 bit mode	T		—	±0.5	±0.5		
Full-Scale Error	12 bit mode	T	E_{FS}	—	±1.0	—	LSB[2]	V_{ADIN} = V_{DDAD}
	10 bit mode	P		—	±0.5	±1		
	8 bit mode	T		—	±0.5	±0.5		
Quantization Error	12 bit mode	D	E_Q	—	-1 to 0	—	LSB[2]	
	10 bit mode			—	—	±0.5		
	8 bit mode			—	—	±0.5		
Input Leakage Error	12 bit mode	D	E_{IL}	—	±2	—	LSB[2]	Pad leakage[4] * $R_{AS\{test=pad\ leakage\ test\}}$
	10 bit mode			—	±0.2	±4		
	8 bit mode			—	±0.1	±1.2		
Temp Sensor Slope	-40°C to 25°C	D	m	—	1.646	—	mV/°C	
	25°C to 85°C			—	1.769	—		
Temp Sensor Voltage	25°C	D	V_{TEMP25}	—	701.2	—	mV	

1 Typical values assume V_{DDAD} = 3.3 V, Temp = 25 °C, f_{ADCK}=1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 1 LSB = $(V_{REFH} - V_{REFL})/2^N$

3 Monotonicity and No-Missing-Codes guaranteed in 10 bit and 8 bit modes

4 Based on input pad leakage current. Refer to pad electricals.

3.12.5 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the flash memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see the Memory section of the *MCF51CN128 Reference Manual*.

Table 22. Flash Characteristics

C	Characteristic	Symbol	Min	Typical	Max	Unit
D	Supply voltage for program/erase -40 °C to 85 °C	$V_{prog/erase}$	1.8	—	3.6	V
D	Supply voltage for read operation	V_{Read}	1.8	—	3.6	V
D	Internal FCLK frequency[1]	f_{FCLK}	150	—	200	kHz
D	Internal FCLK period (1/FCLK)	t_{Fcyc}	5	—	6.67	µs
P	Longword program time (random location)(2)	t_{prog}	9			t_{Fcyc}
P	Longword program time (burst mode)(2)	t_{Burst}	4			t_{Fcyc}
P	Page erase time[2]	t_{Page}	4000			t_{Fcyc}
P	Mass erase time(2)	t_{Mass}	20,000			t_{Fcyc}
D	Longword program current[3]	R_{IDDBP}	—	9.7	—	mA
D	Page erase current[3]	R_{IDDPE}	—	7.6	—	mA
C	Program/erase endurance[4] T_L to T_H = –40°C to + 85°C T = 25°C		10,000 —	— 100,000	— —	cycles
C	Data retention[5]	t_{D_ret}	15	100	—	years

1 The frequency of this clock is controlled by a software setting.

2 These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.

3 The program and erase currents are additional to the standard run I_{DD}. These values are measured at room temperatures with V_{DD} = 3.3 V, bus frequency = 8.0 MHz.

4 **Typical endurance for flash** was evaluated for this product family on the HC9S12Dx64. For additional information on how Freescale defines typical endurance, please refer to Engineering Bulletin EB619, *Typical Endurance for Nonvolatile Memory.*

5 **Typical data retention** values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25 °C using the Arrhenius equation. For additional information on how Freescale defines typical data retention, refer to Engineering Bulletin EB618, *Typical Data Retention for Nonvolatile Memory.*

3.13 EMC Performance

Electromagnetic compatibility (EMC) performance is highly dependent on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation all play a significant role in EMC performance. The system designer should consult Freescale applications notes such as AN2321, AN1050, AN1263, AN2764, and AN1259 for advice and guidance specifically targeted at optimizing EMC performance.

3.13.1 Radiated Emissions

Microcontroller radiated RF emissions are measured from 150 kHz to 1 GHz using the TEM/GTEM Cell method in accordance with the IEC 61967-2 and SAE J1752/3 standards. The measurement is performed with the microcontroller installed on a custom EMC evaluation board while running specialized EMC test software. The radiated emissions from the microcontroller are measured in a TEM cell in two package orientations (North and East). For more detailed information concerning the evaluation results, conditions and setup, please refer to the EMC Evaluation Report for this device.

4 Ordering Information

This section contains ordering information for MCF51CN128 devices.

Table 23. Ordering Information

Freescale Part Number[1]	Memory		Temperature Range (°C)	Package[2]
	Flash	RAM		
MCF51CN128CLK	128K	24K	–40 to +85	80-pin LQFP
MCF51CN128CLH	128K	24K	–40 to +85	64-pin LQFP
MCF51CN128CGT	128K	24K	–40 to +85	48-pin QFN

1 See the *MCF51CN128 Reference Manual* (document MCF51CN128RM), for a complete description of modules included on each device.

2 See Table 24 for package information.

5 Package Information

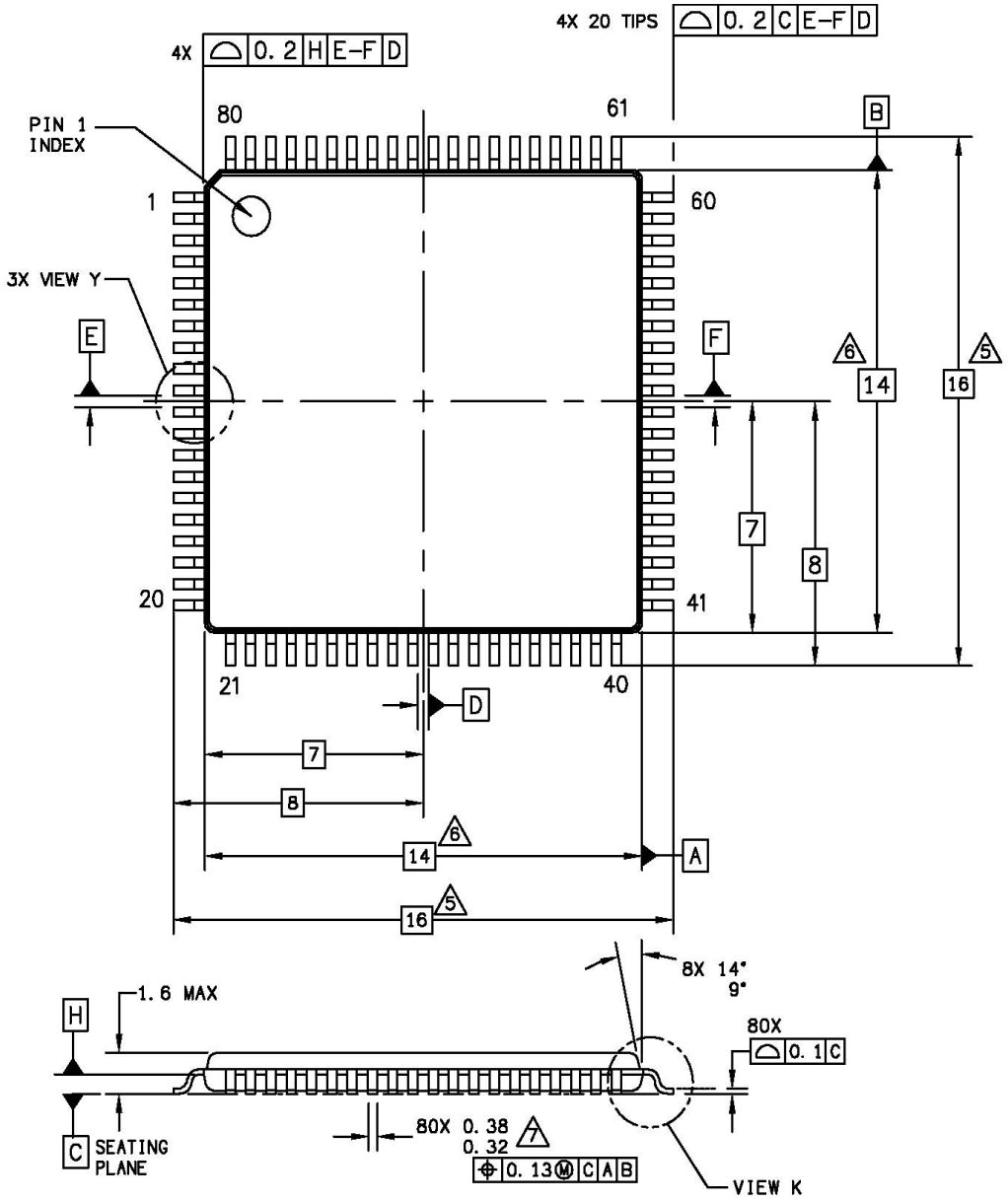
Table 24. Package Descriptions

Pin Count	Package Type	Abbreviation	Designator	Case No.	Document No.
80	Low Quad Flat Package	LQFP	LK	917A	98ASS23237W
64	Low Quad Flat Package	LQFP	LH	840F	98ASS23234W
48	Quad Flat No-Leads	QFN	GT	1314	98ARH99048A

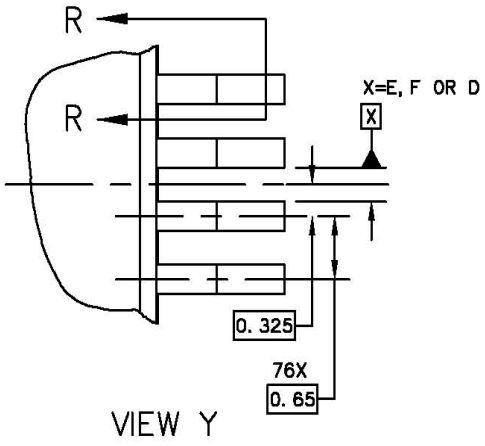
6 Mechanical Outline Drawings

The following pages are mechanical drawings for the packages described in Table 24. For the latest available drawings, visit freescale web site (http://www.freescale.com) and enter the package's document number into the keyword search box.

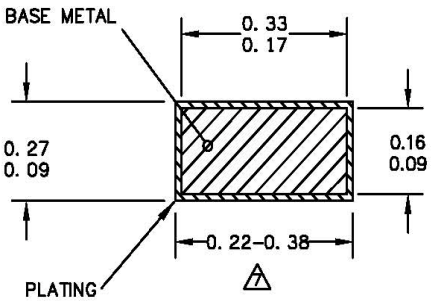
6.1 80-pin LQFP



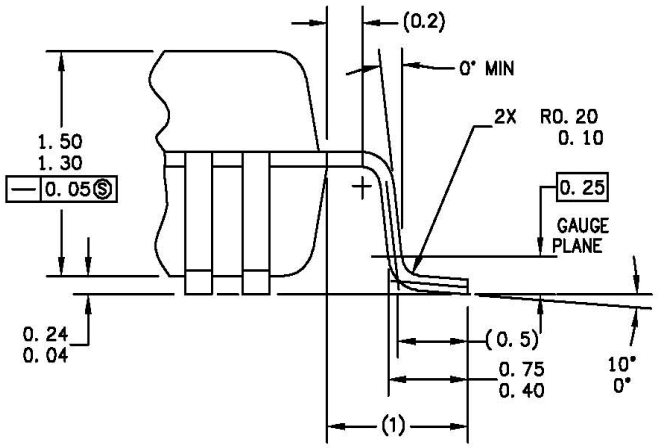
© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: 80 LD LQFP, 14 X 14 PKG, 0.65 MM PITCH, 1.4 THICK	DOCUMENT NO: 98ASS23237W	REV: E
	CASE NUMBER: 917A-03	28 APR 2006
	STANDARD: NON-JEDEC	



VIEW Y



SECTION R–R
ROTATED 90° CW



VIEW K

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TITLE: 80 LD LQFP, 14 X 14 PKG, 0.65 MM PITCH, 1.4 THICK	DOCUMENT NO: 98ASS23237W	REV: E
	CASE NUMBER: 917A-03	28 APR 2006
	STANDARD: NON-JEDEC	

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
2. CONTROLLING DIMENSION : MILIMETER.
3. DATUM PLANE H IS LOCATED AT THE BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUM E, F AND D TO BE DETERMINED AT DATUM PLANE H.
5. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.
6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
7. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.46. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07.

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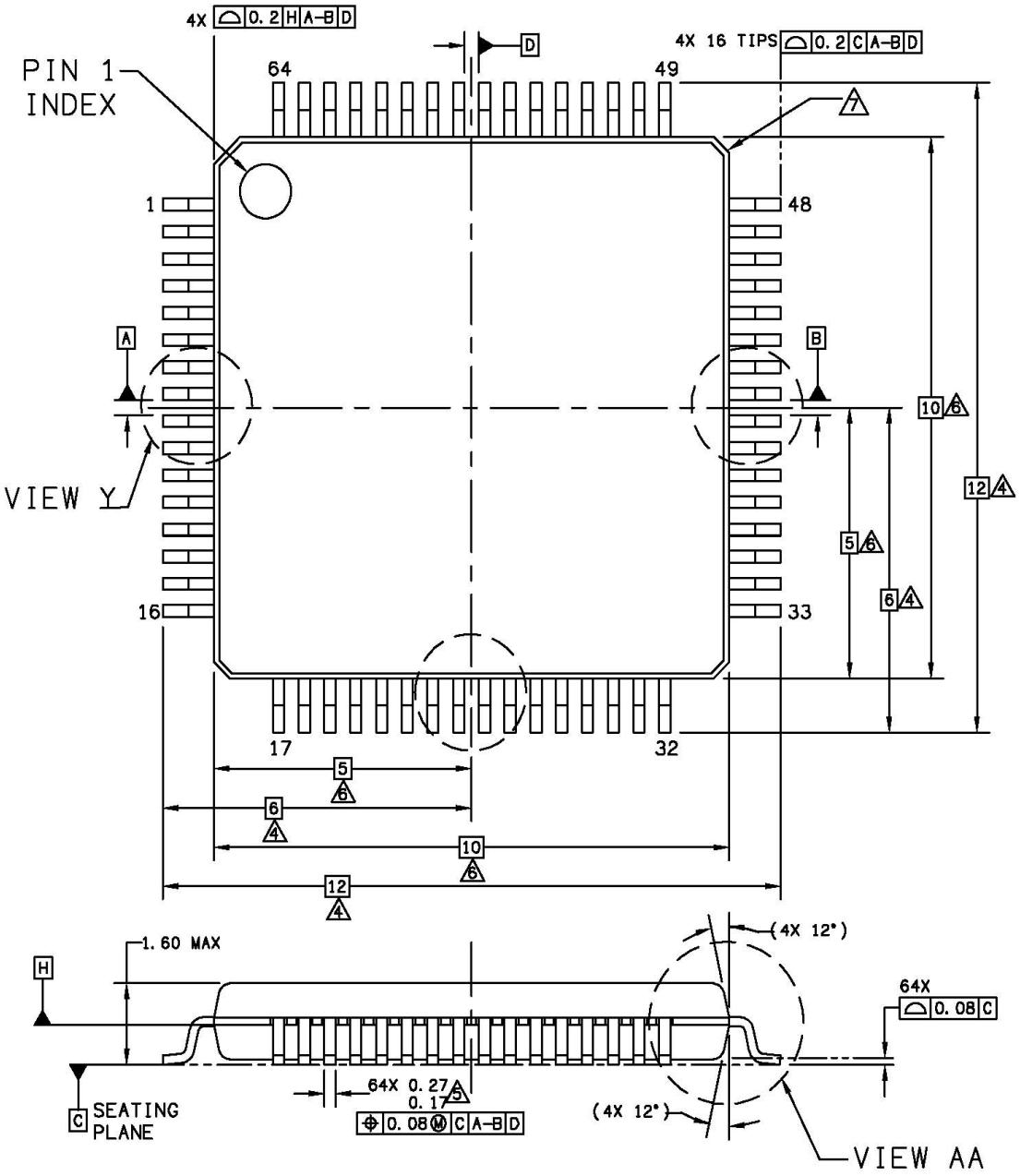
	CASE NUMBER: 917A–03	28 APR 2006
	STANDARD: NON–JEDEC	

6.2 64-pin LQFP



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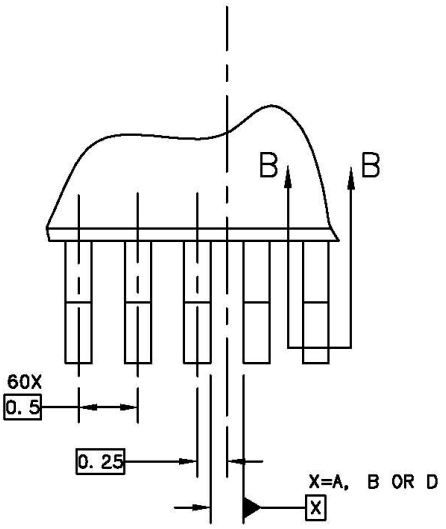
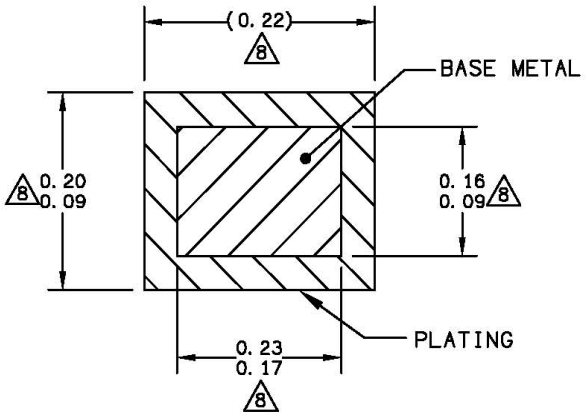
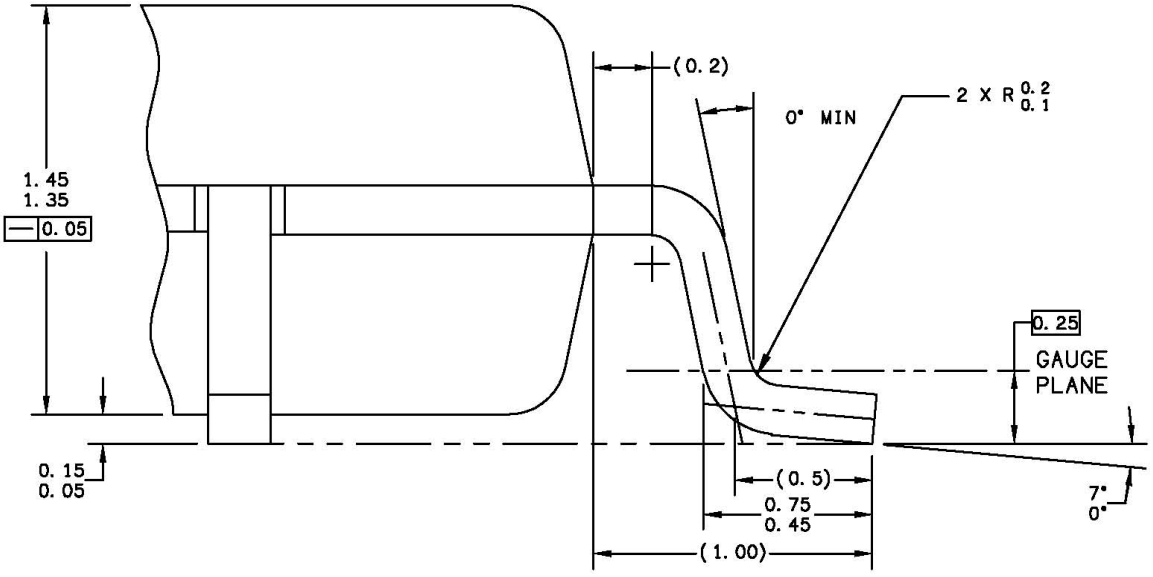
	CASE NUMBER: 840F-02	11 AUG 2006
	STANDARD: JEDEC MS-026 BCD	



VIEW Y



SECTION B–B



VIEW AA

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TITLE: 64LD LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, CASE OUTLINE	DOCUMENT NO: 98ASS23234W	REV: E
	CASE NUMBER: 840F-02	11 AUG 2006
	STANDARD: JEDEC MS-026 BCD	

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.
5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08 mm AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 mm.
6. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 mm AND 0.25 mm FROM THE LEAD TIP.

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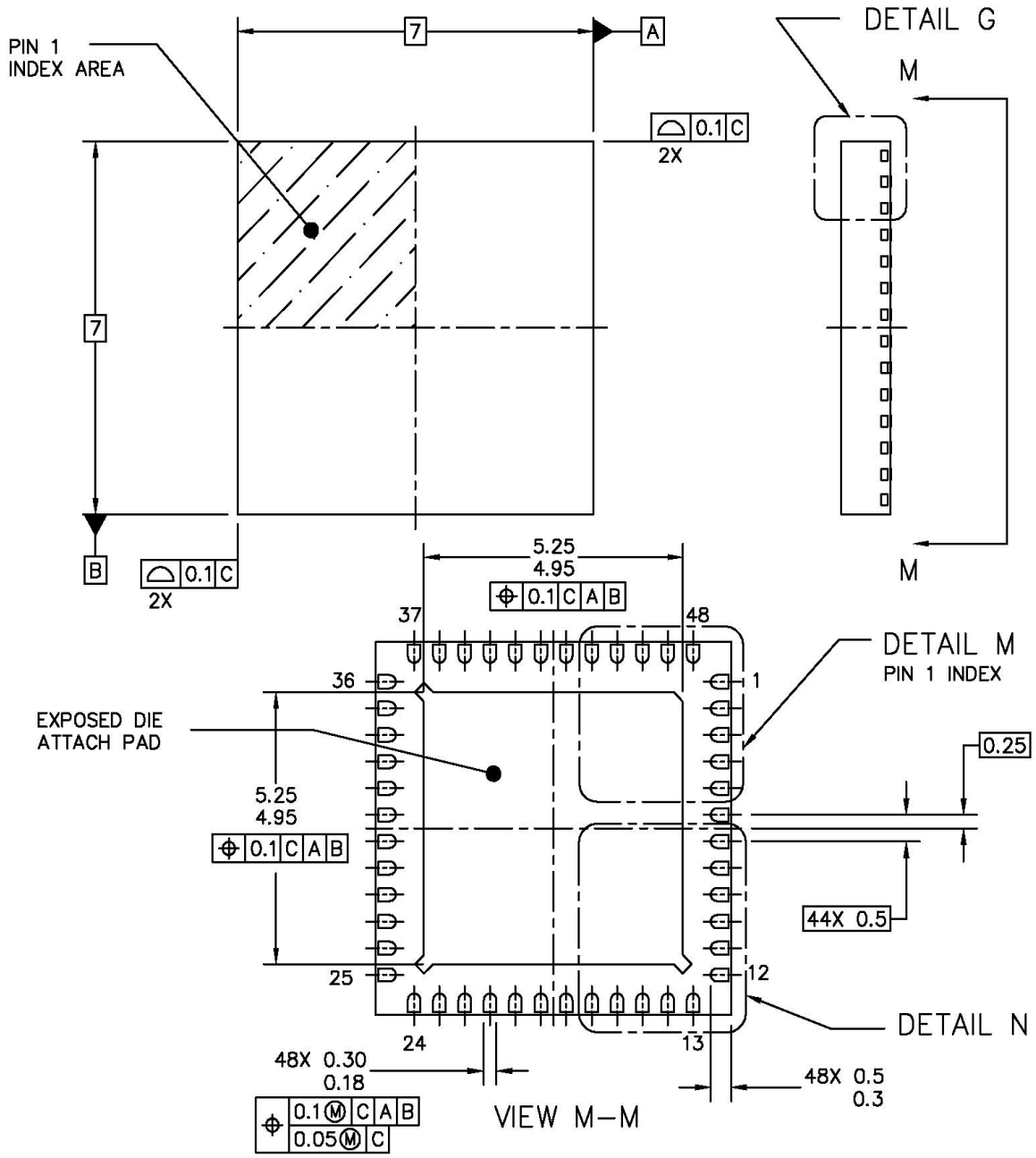
TITLE: 64LD LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, CASE OUTLINE	DOCUMENT NO: 98ASS23234W	REV: E
	CASE NUMBER: 840F-02	11 AUG 2006
	STANDARD: JEDEC MS-026 BCD	

6.3 48-pin QFN



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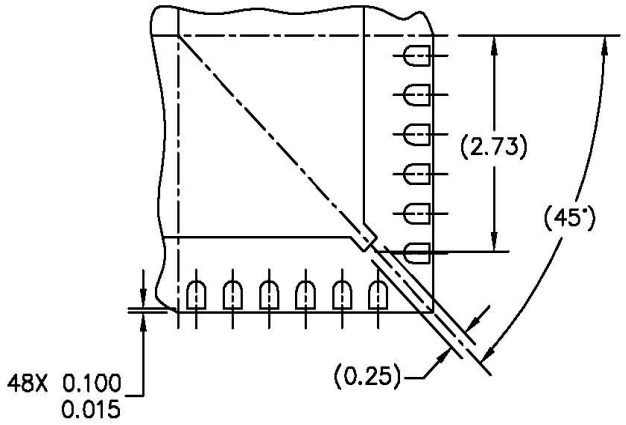
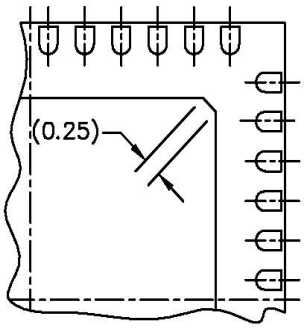
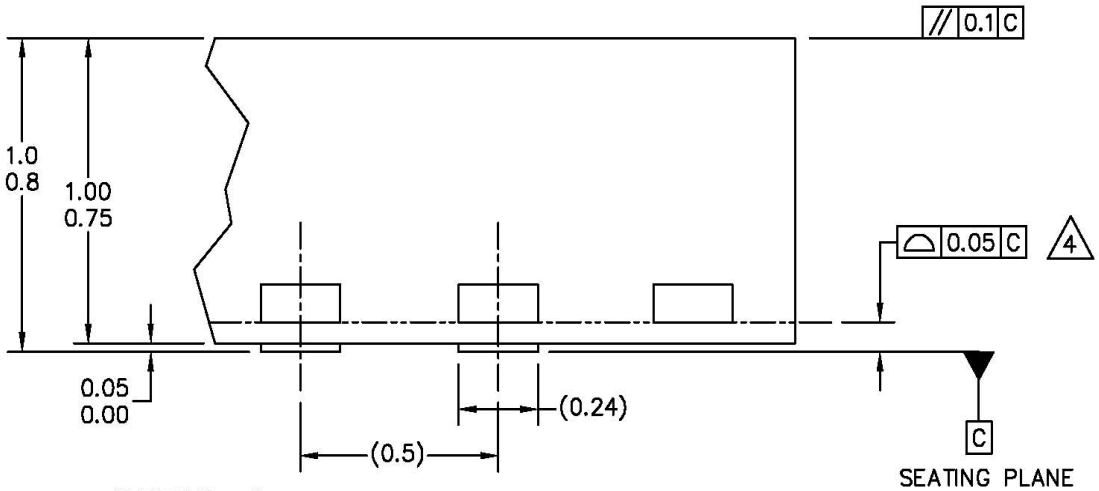
	CASE NUMBER: 1314–05	05 DEC 2005
	STANDARD: JEDEC–MO–220 VKKD–2	



DETAIL N
PREFERRED CORNER CONFIGURATION



DETAIL M
PREFERED PIN 1 BACKSIDE IDENTIFIER



DETAIL G
VIEW ROTATED 90° CW

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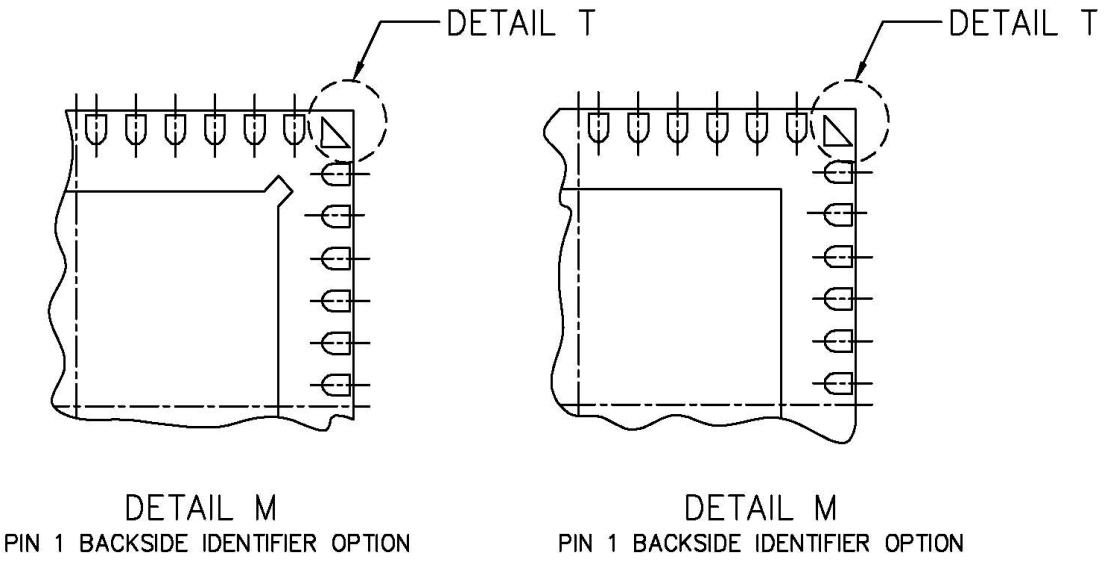
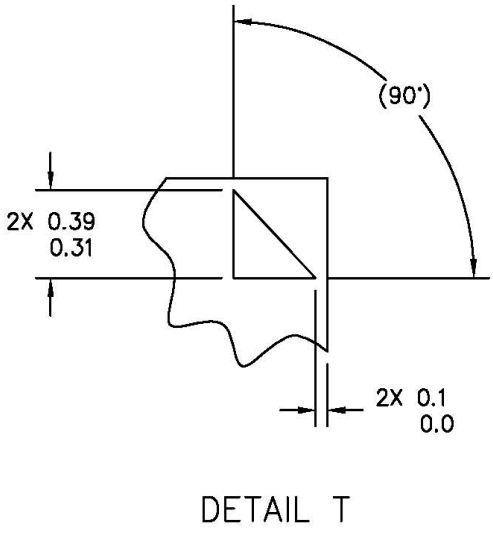
TITLE: THERMALLY ENHANCED QUAD FLAT NON-LEADED PACKAGE (QFN) 48 TERMINAL, 0.5 PITCH (7 X 7 X 1)	DOCUMENT NO: 98ARH99048A	REV: F
	CASE NUMBER: 1314-05	05 DEC 2005
	STANDARD: JEDEC-MO-220 VKKD-2	





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TITLE: THERMALLY ENHANCED QUAD FLAT NON–LEADED PACKAGE (QFN) 48 TERMINAL, 0.5 PITCH (7 X 7 X 1)	DOCUMENT NO: 98ARH99048A	REV: F
	CASE NUMBER: 1314–05	05 DEC 2005
	STANDARD: JEDEC–MO–220 VKKD–2	

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. THE COMPLETE JEDEC DESIGNATOR FOR THIS PACKAGE IS: HF–PQFN.
4. COPLANARITY APPLIES TO LEADS, CORNER LEADS, AND DIE ATTACH PAD.
5. MIN METAL GAP SHOULD BE 0.2MM.

	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: THERMALLY ENHANCED QUAD FLAT NON–LEADED PACKAGE (QFN) 48 TERMINAL, 0.5 PITCH (7 X 7 X 1)	DOCUMENT NO: 98ARH99048A	REV: F
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7 Revision History

This section lists the changes between versions of MCF51CN128 Data Sheet document.

Table 25. Revision History

Revision Number	Date	Description of Changes
1	August 2008	Alpha Customer Release.
2	January 2009	Pre-Launch Release.
3	January 2009	Launch Release.
4	May 2009	• Changed LVDH trip and recovery values in Table 8. • Fixed Mini-FlexBus maximum frequency to 25.1666 MHz in Section 3.10, “Mini-FlexBus Timing Specifications.” • Updated FEC feature list to describe ethernet operation between 3.0 V to 3.6 V. • In Table 8, added a footnote to the operating voltage. It describes an exception to the Fast Ethernet Controller (FEC), because it is only operational above the operating voltage of 3 V. • Corrected Freescale part numbers in Table 23. • In Table 21, changed I_{DDAD} classification to T.

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