Features

- Lead free versions available
- RoHS compliant (lead free version)*
- New Product Development
- Integrated Passive Device
- ESD Protection to IEC61000-4-2 Spec.

BOURNS®

2DAC-C16R Series - Integrated Passive & Active Device using CSP

General Information

This application specific integrated passive component is designed to provide all of the necessary ESD protection on the data port of a portable electronic device. The ESD protection provided by the component enables the data port to withstand ±8 KV Contact / ±15 KV Air Discharge when tested according to the method specified in IEC 61000-4-2. The component incorporates 12 identical ports and is supplied in a 16 pin CSP package which is intended to be mounted directly onto an FR4 printed circuit board. This package is designed to meet typical thermal cycle and bend test specifications without the use of an underfill material.

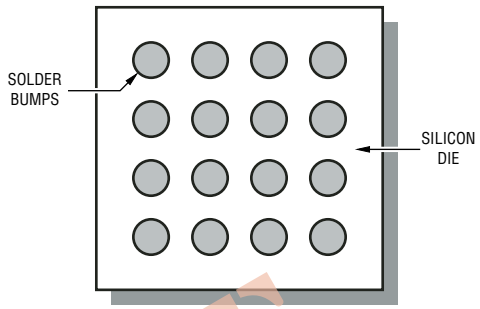

Figure 1 – CSP Format

Electrical & Thermal Characteristics

Electrical Characteristics (T_A = 25 °C unless otherwise noted)	**Symbol**	**Minimum**	**Nominal**	**Maximum**	**Unit**
Zener Diode Breakdown Voltage @ 1 mA	V_{BR}	6	7.2	8	V
Leakage Current @ 3 V	I_R			1	uA
Diode Capacitance @ 1 V & 1 MHz	C_T	8.5	10.5	12.5	pF
ESD Performance (Note 1 & 2) Withstand					
Contact Discharge		±8			kV
Air Discharge		±15			kV
Let Through Contact Discharge				±150	V
Air Discharge				±150	V
Thermal Characteristics (T_A = 25 °C unless otherwise noted)					
Operating Temperature	T_J	-40	25	+85	°C
Storage Temperature	T_{stg}	-60	25	+125	°C
Total Power Dissipation @ 70 °C	P_D			100	mW

Note: 1. *The IEC 61000-4-2 test method will be adapted for component level testing. The device will provide the specified ESD protection performance on the "EXT1 – 12" pins only.*

2. *"Let Through" is a measure of the component of an incident ESD transient that the protection device allows through to the down stream circuitry.*

*RoHS Directive 2002/95/EC Jan 27 2003 including Annex

Specifications are subject to change without notice.
Customers should verify actual device performance in their specific applications.

Mechanical Characteristics

This is a Silicon-based device and is packaged using chip scale packaging technology. Solder bumps, formed on the Silicon die, provide the interconnect medium from die to PCB. The bumps are arranged on the die in a regular grid formation. The grid pitch is 0.5 mm. The dimensions for the CSP packaged device are shown in Fig. 2 below.

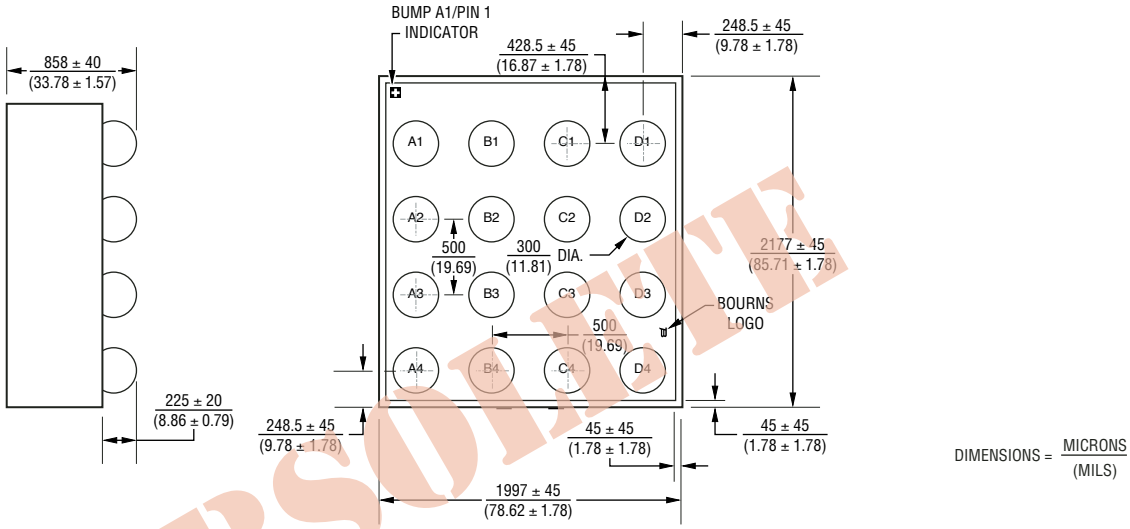

Fig. 2 – Device Mechanical Drawing

Reliability

Reliability data exists and continues to be gathered on an ongoing basis for Bourns Integrated Passive and Active Devices using CSP packaging.

"Package level" testing of the integrity of the solder joint is carried out on an independent Daisy-Chain test device. A 25-Pin Daisy Chain component is available from Bourns for this purpose (part number 2TAD-C25R). This is a 5 x 5 array featuring 0.5 mm pitch solder bumps. The Distance to Neutral Point (DNP) on that component is larger than that of the 2DAC-C16R and is thus deemed a worse case for Thermal Cycle testing.

"Silicon level" reliability performance will be assured by similarity to other Integrated Passive and Active Devices using CSP product from Bourns.

Individual Channel Schematic

This section contains the schematic (See Fig. 3 below) for the single channel in the integrated passive device. Note that the electrical parameter of primary interest is the ESD performance.

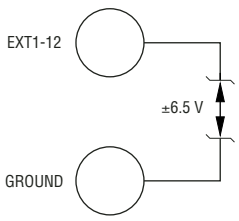

Fig. 3 – Channel Schematic

Key Design Parameters

Zener Diode

V_{BR}: 6 V Min, 8 V Max @ I_{BR} = 1 mA

I_R: 1 uA Max @ V_R = 3 V

C_T: 8.5 pF Min, 10.5 pF Typ, 12.5 pF Max @ V_R = 1 V & F = 1 MHz

Block Diagram

Figure 4 contains a block diagram of the CSP device. This diagram includes the pin names and basic electrical connections associated with each channel.

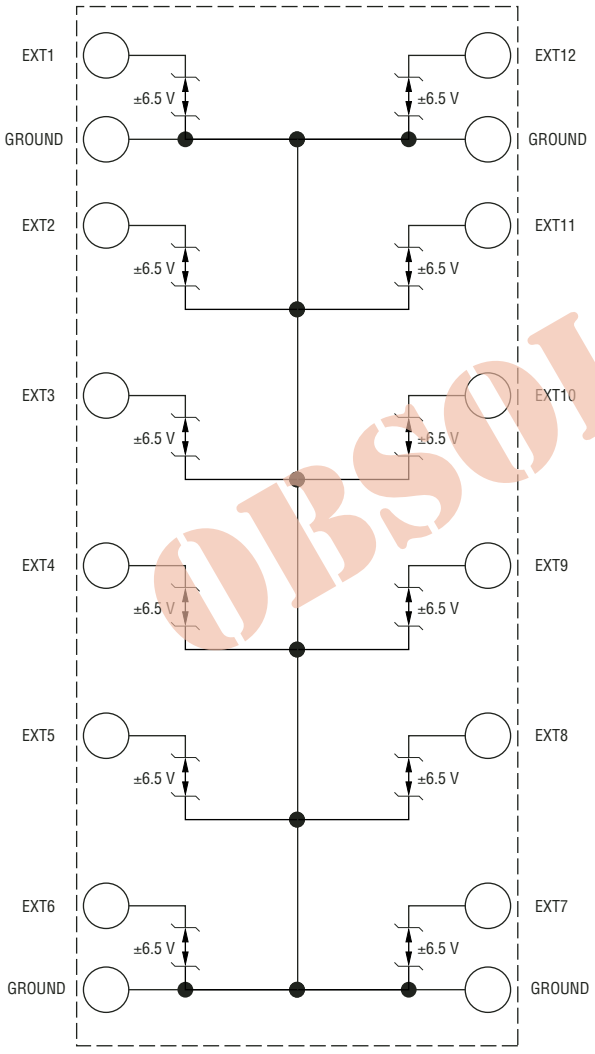

Fig. 4 – Device Block Diagram

Marking

The device will be laser marked on the backside according to the following Fig. 5 scheme below. Position A1, on the Bump Grid is located at the top left of the die when the die is orientated so that the mark is read in the normal fashion.

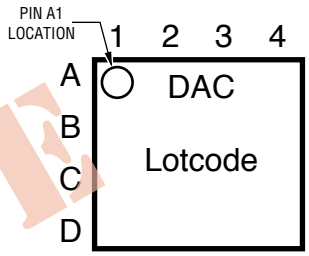

Fig. 5 – Backside Laser Mark

PCB Design and SMT Processing

Please consult Bourns' *Thin Film on Silicon using CSP* Users Guide Application Note for notes on PCB design and SMT processing.

How to Order

2 DAC - C16R __

Thinfilm
Model
Chipscale
No. of Solder Bumps
Packaging Option
R = Tape and Reel
Packaged 3000 pcs. / 7 " reel
Terminations
LF = Sn/Ag/Cu (lead free)
Blank = Sn/Pb

Device Pin Out

The Pin-Out for the device is shown in Fig. 6. Note also that the device is shown with bumps facing up.

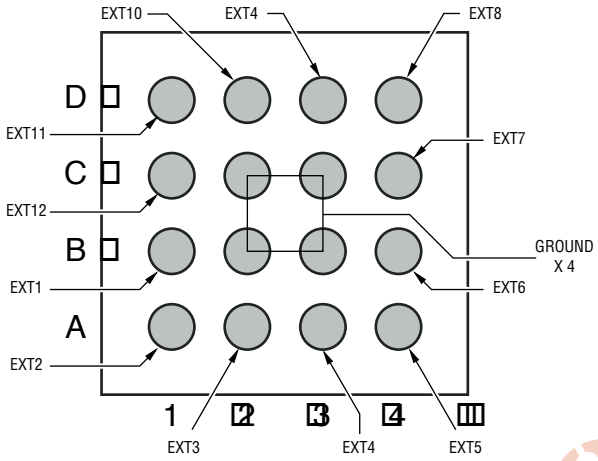

Fig. 6 (a) - Device Pin Out "Bumps Up" View

Pin	Name	Pin	Name
A1	EXT2	C1	EXT12
A2	EXT3	C2	GND
A3	EXT4	C3	GND
A4	EXT5	C4	EXT7
B1	EXT1	D1	EXT11
B2	GND	D2	EXT10
B3	GND	D3	EXT9
B4	EXT6	D4	EXT8

Fig. 6 (b) - Pin Listings

Packaging

The product will be dispensed in an 8mm x 4mm Tape and Reel format - see Fig. 7 diagram below. The Tape and Reel package will conform to customer specification.

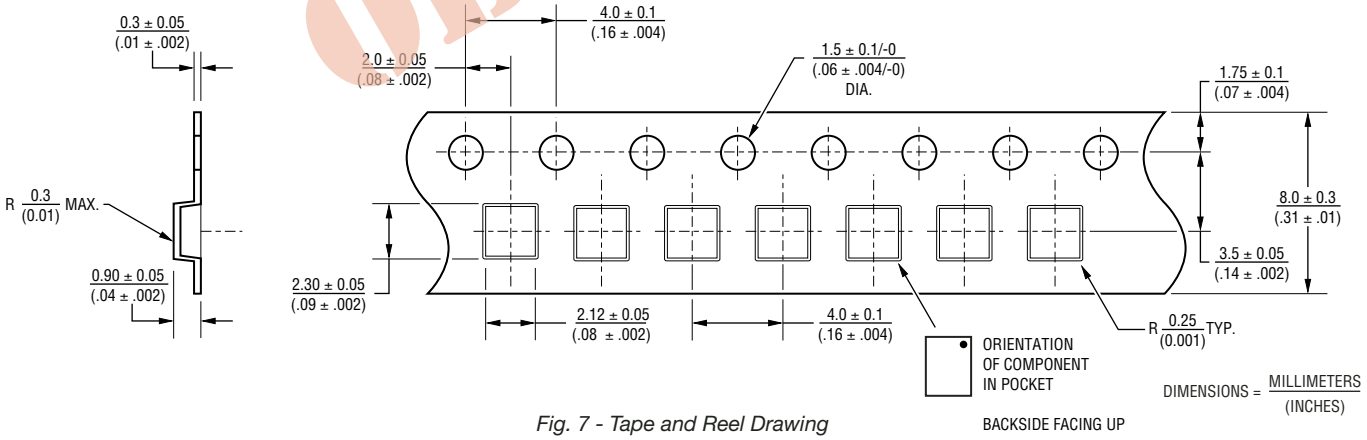

Fig. 7 - Tape and Reel Drawing

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