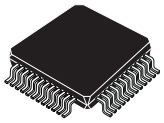
STB5610

GPS RF front-end IC

Not For New Design

Features

- One chip system to interface GPS antenna to GPS microcontroller
- Able to support active and passive antenna
- Minimum external components
- Compatible with GPS L1 SPS signal and Galileo frequencies
- CMOS output levels
- 2.7 V to 3.6 V supply voltage
- Embedded low phase noise PLL
- Active antenna sensor
- Smart chip enable function for power consumption optimization
- ESD protected



LQFP48

Description

The STB5610, using ST RF bipolar technology, implements a global positioning system (GPS) RF front-end.

The chip provides down conversion from the 1575.42 MHz GPS (L1) signal to 4.092 MHz output signal. The integrated PLL with on-chip reference oscillator uses a low cost 16.368 MHz crystal. No TCXO is required.

Table 1. Device summary

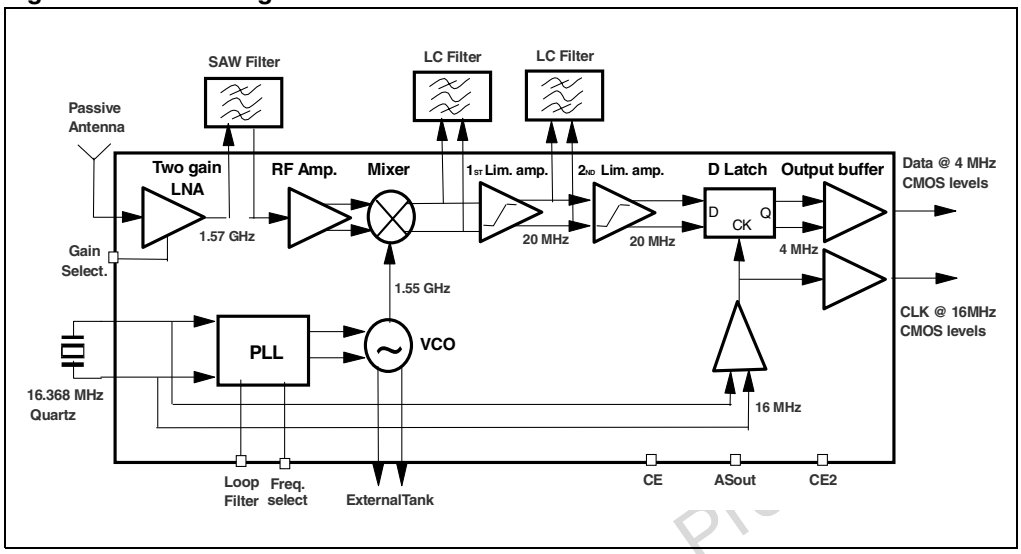
Order code	Package	Packing
STB5610ETR	LQFP48	Tape and reel

Contents

1 Block diagram and functional description

1.1 Block diagram

Figure 1. Block diagram



1.2 Functional description

1.2.1 LNA section

The RF input signal is amplified by two gain levels LNA. Using gain control pin the LNA gain is set to 19 dB to support passive antenna or 10 dB to support active antenna. The LNA output signal is filtered by 1575.42 MHz SAW filter.

1.2.2 RF amplifier plus mixer section

The 1575.42 MHz input signal, amplified by RF amplifier, is mixed with the VCO signal to generate a differential 20.46 MHz IF signal.

1.2.3 IF section

Two LC filters at mixer output and at first limiting output are used to suppress undesirable signals and mixer products. The second stage limiting amplifier is connected to a D-Type latch clocked by 16.368 MHz crystal oscillator signal. The effect of sampling the 20.46MHz signal at 16.368 MHz is to create sub-sampling alias at 4.092 MHz. This is fed to the output level converter.

1.2.4 Output section

The output buffers perform level translation from the internal ECL levels to CMOS output levels referred to ground. The data signal changes during the clock signal negative edge.

1.2.5 Power supplies

The STB5610, has been designed to support from 2.7 V to 3.6 V supply voltage.

1.2.6 VCO and PLL

Using external tank the VCO is able to provide very low phase noise signal. Through the frequency selector pin the VCO signal is set at 1554.96 MHz and at 1571.328 MHz. The on-chip reference oscillator uses a low cost 16.368 MHz crystal.

1.2.7 Antenna sensor circuitry

Integrated sensor circuitry is able to evaluate the antenna current consumption; the Asout pin output provides this info externally. Using external sensing resistor of 10 Ohm if the antenna current consumption is inside the range 10 mA to 40 mA (active antennas typical current consumption) the Asout output logic level is High, if the antenna current consumption is outside the above reported range (passive antenna or problem on antenna connection) the Asout output logic level is low.

1.2.8 Chip enable

Using the CE pin it is possible to switch off all the chip (neither data nor clock available). Using CE2 pin it is possible to disable the analog portion of the chip (no data available) maintaining the digital portion active (Clock available) optimizing the chip current consumption.

2 Pin description

Figure 2. Pin connection (top view)

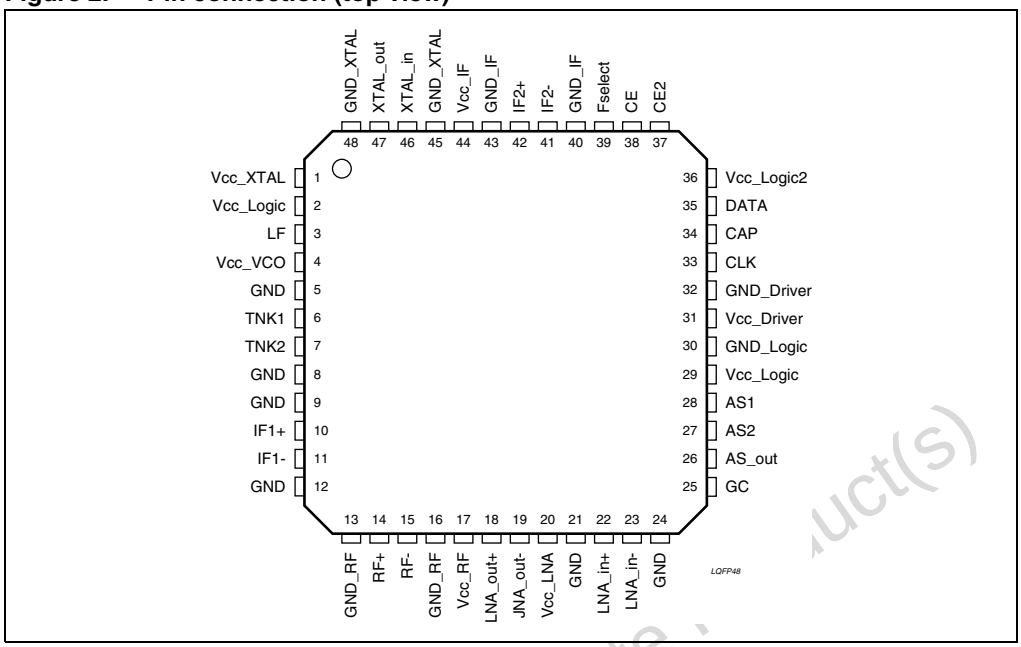


Table 2. Pin description

Pin #	Pin name	Description
1	Vcc_XTAL	Power supply
2	Vcc_Logic	Power supply
3	LF	Loop filter
4	Vcc_VCO	Power supply
5	GND	Ground
6	TNK1	Tank Input
7	TNK2	Tank Input
8	GND	Ground
9	GND	Ground
10	IF1+	Mixer Output
11	IF1-	Mixer Output
12	GND	Ground
13	GND_RF	Ground
14	RF+	RF amp. input
15	RF-	RF amp. input
16	GND_RF	Ground

Table 2. Pin description (continued)

Pin #	Pin name	Description
17	Vcc_ RF	Power supply
18	LNA_Out+	LNA output
19	LNA_Out-	LNA output
20	Vcc_LNA	Power supply
21	GND_LNA	Ground
22	LNA_in+	LNA input
23	LNA_in-	LNA input
24	GND_LNA	Ground
25	GC	LNA Gain control
26	AS_Out	Antenna sensor output
27	AS2	Antenna sensor input
28	AS1	Vcc Antenna Supply
29	Vcc_Logic	Power supply
30	GND_Logic	Ground
31	Vcc_Driver	Supply Voltage
32	GND_Driver	Ground
33	CLK	Clock
34	DATA	Data
35	GND	Ground
36	Vcc_Logic2	Supply Voltage
37	CE2	Chip Enable (no data)
38	CE	Chip Enable
39	Fselect	Frequency Selector
40	GND_IF	Ground
41	IF2-	Lim. Amp. Output
42	IF2+	Lim. Amp. Output
43	GND_IF	Ground
44	Vcc_IF	Supply Voltage
45	GND_XTAL	Ground
46	XTAL_in	Crystal Input
47	XTAL_out	Crystal Output
48	GND_XTAL	Ground

3 Electrical specification

3.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	5.9	V
T_j	Junction operating temperature	-40 to 125	°C

3.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction to case	65	°C/W

3.3 Electrical characteristics

Table 5. Electrical characteristics
(V_{cc} = 3 ±10 %, T_{case} = 25 °C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Supply						
V_{cc}	Supply voltage		2.7	3.3	3.6	V
I_{cc}	Supply current			37		mA
AS1	V_{cc} antenna supply		2.7	3.3 / 5	5.5	V
LNA						
G_p	Power gain	Pin GC at GND Pin GC at V_{cc}		19 10		dB
NF	Noise figure	Pin GC at GND Pin GC at V_{cc}		3 10		dB
IIP3	Input IP3	Pin GC at GND Pin GC at V_{cc}		-20 -5		dBm
VSWRin	Voltage stat. wave ratio	Z_L = 50Ω			2.1	
RF amplifier and mixer chain						
IIP3	Input IP3			-19		dBm
NF	Noise figure			5.5		dB
Z_{IN}	Input impedance			50		Ω

Table 5. Electrical characteristics (continued)
(V_{cc} = 3 ±10 %, T_{case} = 25 °C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Z_{OUT}	Differential output impedance			1.4		KΩ
f_{RF}	Input signal RF			1.575		MHz
G	Voltage convertion gain			30		dB
First limiting amplifier						
G	Voltage gain			60		dB
Z_{OUT}	Differential output impedance			2.4		kΩ
Second limiting amplifier						
G	Voltage Gain			30		dB
VCO (GPS LO frequency 1555 MHz)						
VCO	Phase noise	Df = 1 kHz, SSB (10 kHz PLL closed loop bandwidth)		-60		dBc/Hz
Output buffer (square wave CMOS level)						
V_{OH}	High output voltage		Vcc-0.4		Vcc	V
V_{OL}	Low output voltage		0		0+0.4	V
Phase locked loop						
XTAL	Reference crystal			16.368		MHz

3.4 Input control pins table (the logic levels are TTL compatible)

Table 6. GC Pin (LNA gain control pin)

Logic level	Value
Low	Max gain
High	Min gain

Table 7. CE2 Pin (analog portion enable pin)

Logic level	Value
Low	Switch-off
High	Switch-on

Table 8. CE pin (total chip enable pin)

Logic level	Value
Low	Switch-off
High	Switch-on

Table 9. FSELECT (frequencies Selector Pin)

Logic level	Value
Low	GPS frequency
High	Galileo frequency

3.5 Output control pins table

The Asout pin output provides information on Antenna current consumption.

Table 10. ASout pin (antenna sensor pin)(1)

Logic level	Value
Low(2)	Iant < 10 mA Iant > 40 mA
High(2)	10 mA < Iant < 40 mA

1. It is referred to external sensing resistor of 10 Ohm. Application requiring higher or lower current threshold should adjust the resistor value appropiately.
2. The logic levels are referred to STB5610 supply voltage.

4 Application information

Figure 3. Application board schematic (active antenna)

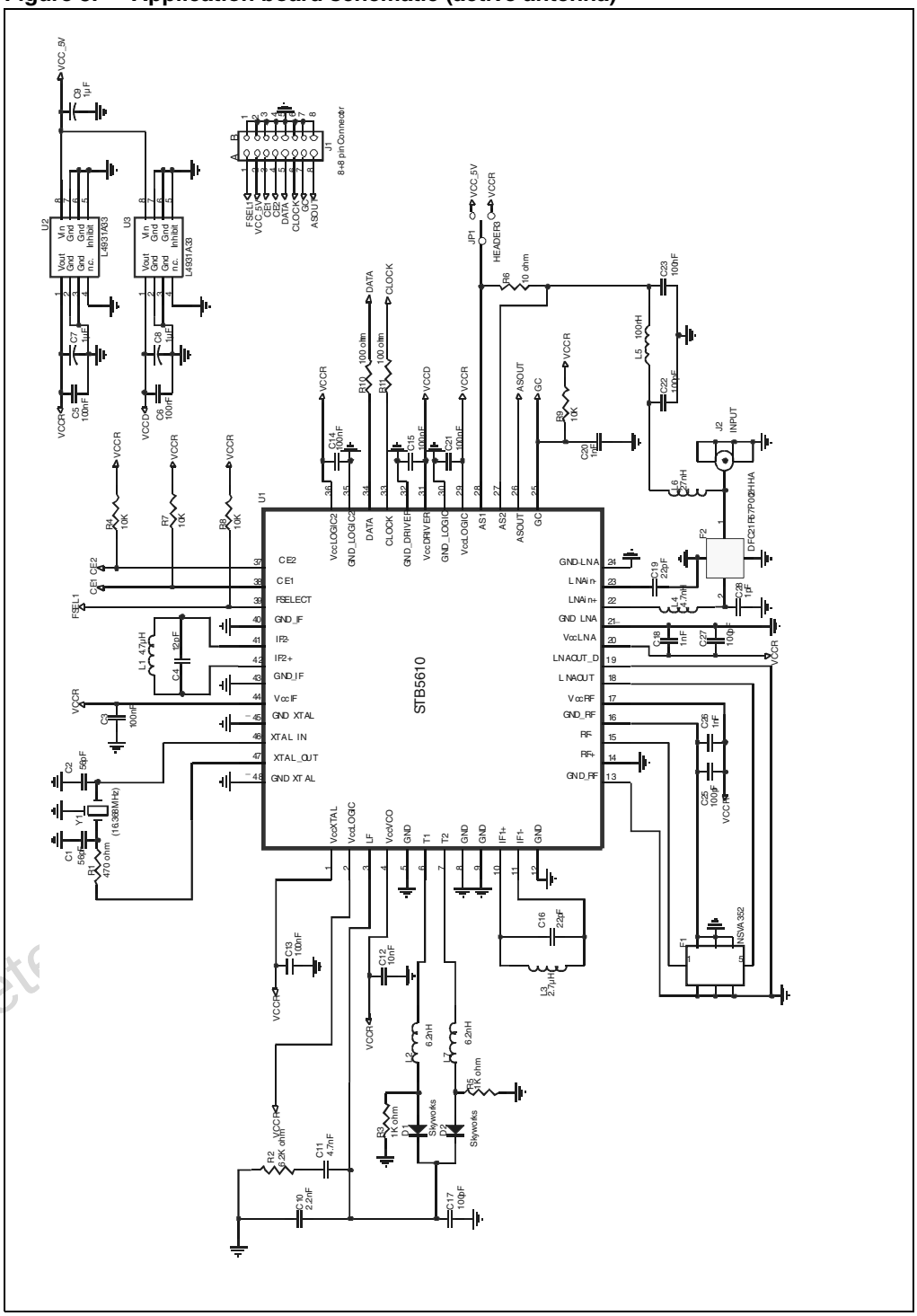


Figure 4. Application board layout (active antenna)

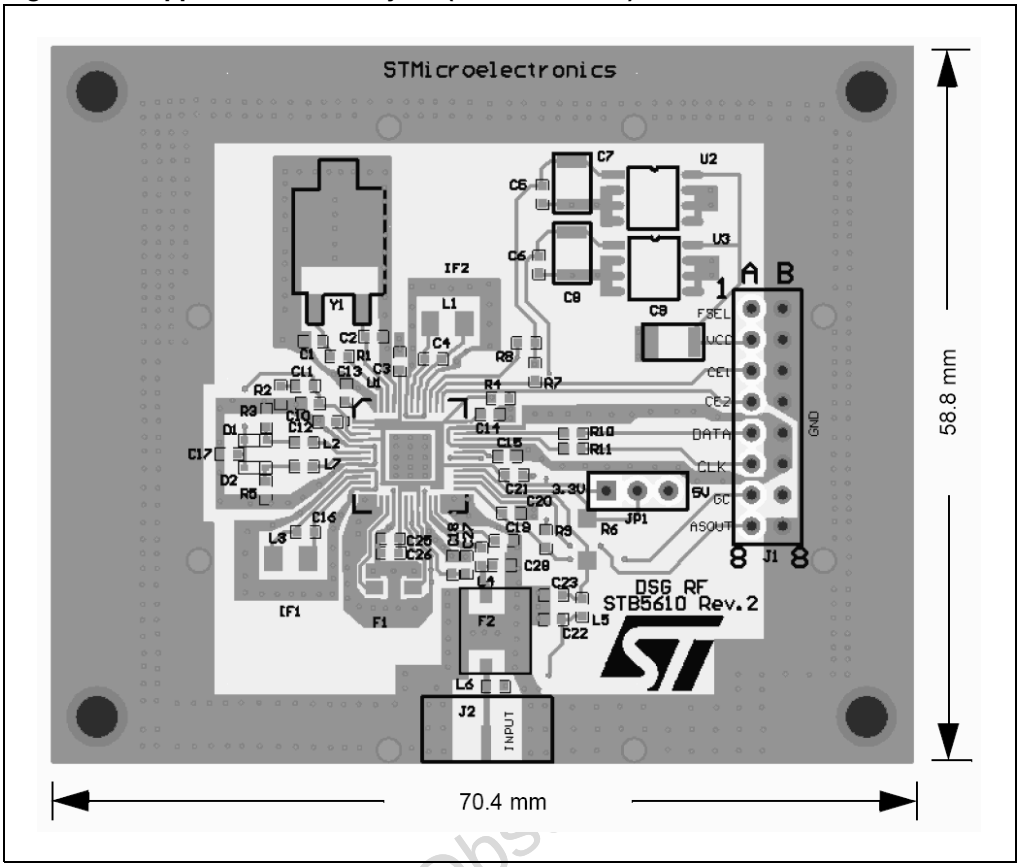


Table 11. Bill of materials

Q.ty	Reference designator	Value	Manufacturer
1	R1	470 ohm	NEOHM (0603)
1	R2	6.2 kohm	NEOHM (0603)
2	R3, R5	1 kohm	NEOHM (0603)
1	R6	10 ohm	NEOHM (0603)
4	R4,R7,R8,R9	10 kohm	NEOHM (0603)
2	R10,R11	100 ohm	NEOHM (0603)
2	C1,C2	56 pF	Murata (series GRM18)
1	C4	12 pF	Murata (series GRM18)
3	C7, C8, C9	1 µF (electrolytic)	Kemet (series T491) Case A
1	C10	2.2 nF	Murata (series GRM18)
1	C11	4.7 nF	Murata (series GRM18)
1	C12	10 nF	Murata (series GRM18)
4	C16,C19	22 pF	Murata (series GRM18)

Table 11. Bill of materials (continued)

Q.ty	Reference designator	Value	Manufacturer
7	C3,C5, C6,C13,C14,C21,C23	100 nF	Murata (series GRM18)
3	C18, C20,C26	1 nF	Murata (series GRM18)
5	C15,C17,C22,C25,C27	100 pF	Murata (series GRM18)
1	C28	1.8 pF	Murata (series GRM18)
1	L1	4.7 µH	Coilcraft (series 1008CS)
1	L2	6.2 nH	Murata (series LQP18M)
1	L3	2.7 µH	Coilcraft (series 1008CS)
1	L4	4.7 nH	Murata (series LQP18M)
1	L5	100 nH	Murata (series LQW18)
1	L6	27 nH	Murata (series LQP18M)
1	L7	6.2 nH	Murata (series LQP18M)
1	U1	STB5610	ST
2	U2, U3	L4931ABD33	ST
1	J1	8+8 pin connector	Various
1	J2	SMA connector (female)	Johnson
1	F1	NSVA352	NJR Corporation
1	F2	DFC21R57P002HHA(1)	Murata
1	D1	SMV1405-079	Skyworks
1	D2	SMV1405-079	Skyworks
1	Y1	DHF32UM-1SJ(16.368 MHz)	Rakon

1. This part number will be changed in DFCB21G57LDJAB-TT1 by MURATA.

5 Package information

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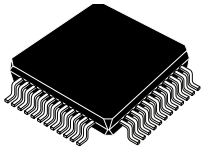
Figure 5. LQFP48 mechanical data and package dimensions

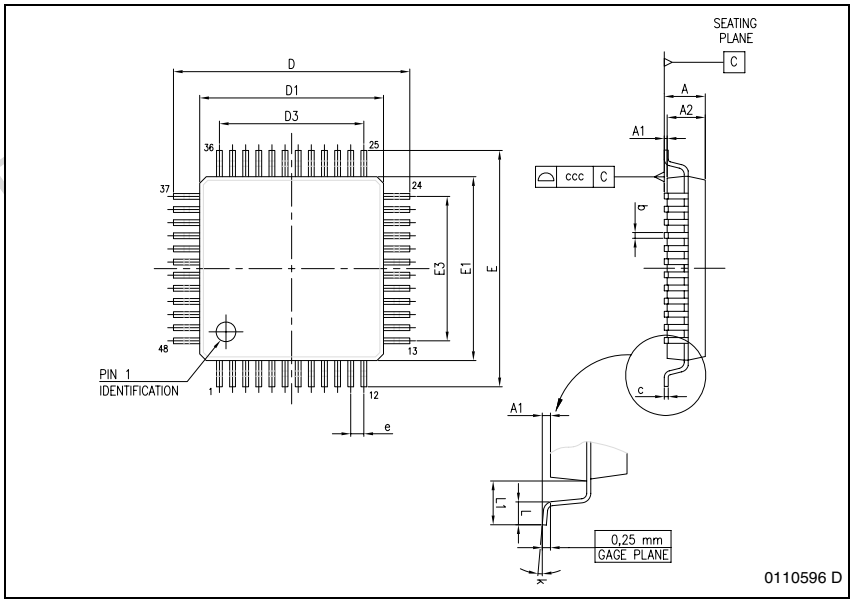
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.006	0.008	0.010
c	0.09		0.20	0.004		0.008
D	8.80	9.00	9.20	0.346	0.354	0.362
D1	6.80	7.00	7.20	0.268	0.276	0.283
D3		5.50			0.217	
E	8.80	9.00	9.20	0.346	0.354	0.362
E1	6.80	7.00	7.20	0.268	0.276	0.283
E3		5.50			0.217	
e		0.50			0.019	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
k	0°(min.), 3.5°(typ.), 7°(max.)					
ccc			0.08			0.0031

OUTLINE AND MECHANICAL DATA



Body: 7 x 7 x 1.4mm

LQFP48



6 Revision history

Table 12. Document revision history

Date	Revision	Changes
20-Dec2003	3	Initial release.
12-Feb-2009	4	Document reformatted. Document status changed from datasheet to not for new design. Updated *Section 5: Package information on page 13*.

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