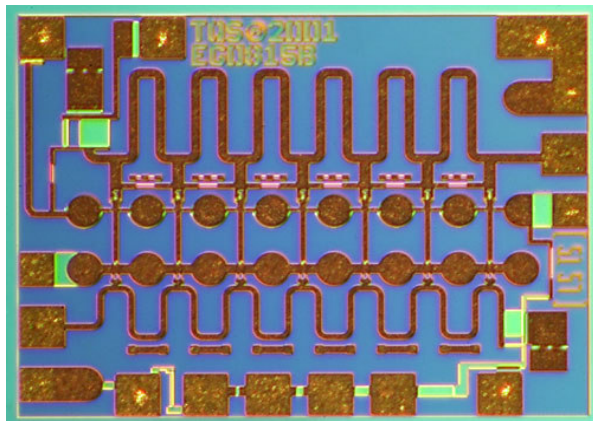


DC - 60 GHz Low Noise Amplifier

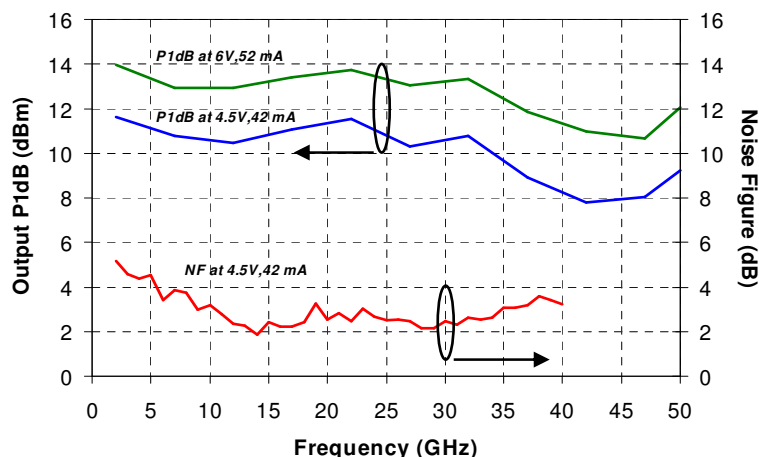
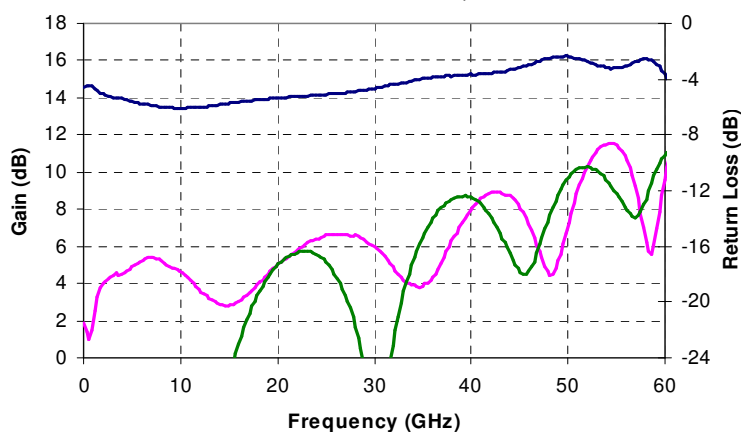


Key Features

- 60 GHz Bandwidth
- 3.0 dB noise figure
- > 15 dB small signal gain
- 13 dBm P1dB
- +/- 7 ps group delay variation
- Bias: 4.5V, 50 mA
- 0.15 um 3MI mHEMT Technology
- Chip Dimensions: 1.30 x 1.06 x 0.1 mm
(0.051 x 0.042 x 0.004) in

Measured Data

Bias Conditions: $V_d = 6\text{ V}$, $I_d = 50\text{ mA}$



Primary Applications

- Wideband LNA / gain block
- Test Equipment
- 40 Gb/s optical networks

Description

The TriQuint TGA4811 is a DC - 60 GHz low noise amplifier that typically provides 15 dB small signal gain and input and output return loss is <10dB. Normal Noise Figure is 3.0 dB from 2 - 40 GHz. P1dB is 13 dBm.

The TGA4811 is an excellent choice for Test Equipment, 40Gb/s optical network applications, and general wideband LNA and Gain Block applications.

The TGA4811 is 100% RF tested to ensure performance compliance.

Lead-Free & RoHS compliant.

Samples are available.

Subject to change without notice.

TABLE I
MAXIMUM RATINGS 1/

SYMBOL	PARAMETER	VALUE	NOTES
V^+	Positive Supply Voltage	6.5 V	<u>2/</u>
V^-	Negative Supply Voltage Range	-2 TO 0 V	
I^+	Positive Supply Current	200m A	
$ I_G $	Gate Supply Current	10 mA	<u>3/</u>
P_{IN}	Input Continuous Wave Power	4 dBm	
P_D	Power Dissipation	0.69 W	<u>2/</u> <u>4/</u>
T_{CH}	Operating Channel Temperature	110 °C	<u>5/</u>
T_M	Mounting Temperature (30 Seconds)	175 °C	
T_{STG}	Storage Temperature	-65 to 110 °C	

- 1/ These ratings represent the maximum operable values for this device.
- 2/ Combinations of resistors voltage and 3V (MAX) on mHEMT.
- 3/ Total current for the entire MMIC.
- 4/ When operated at this bias condition with a base plate temperature of 70 °C, the median life will be reduced.
- 5/ Junction operating temperature will directly affect the device median time to failure (MTTF). For maximum life, it is recommended that junction temperatures be maintained at the lowest possible levels.

TABLE II
ELECTRICAL CHARACTERISTICS
(Ta = 25 °C, Nominal)

PARAMETER	TYPICAL	UNITS
Drain Voltage	6	V
Quiescent Current	50	mA
Small Signal Gain, S21	15	dB
Input Return Loss, S11	10	dB
Output Return Loss, S22	15	dB
Reverse Isolation, S12	-40	dB
Output Power (P1dB)	13	dBm
Power @ saturated, Psat	15	dBm
Noise figure	3.0	dB

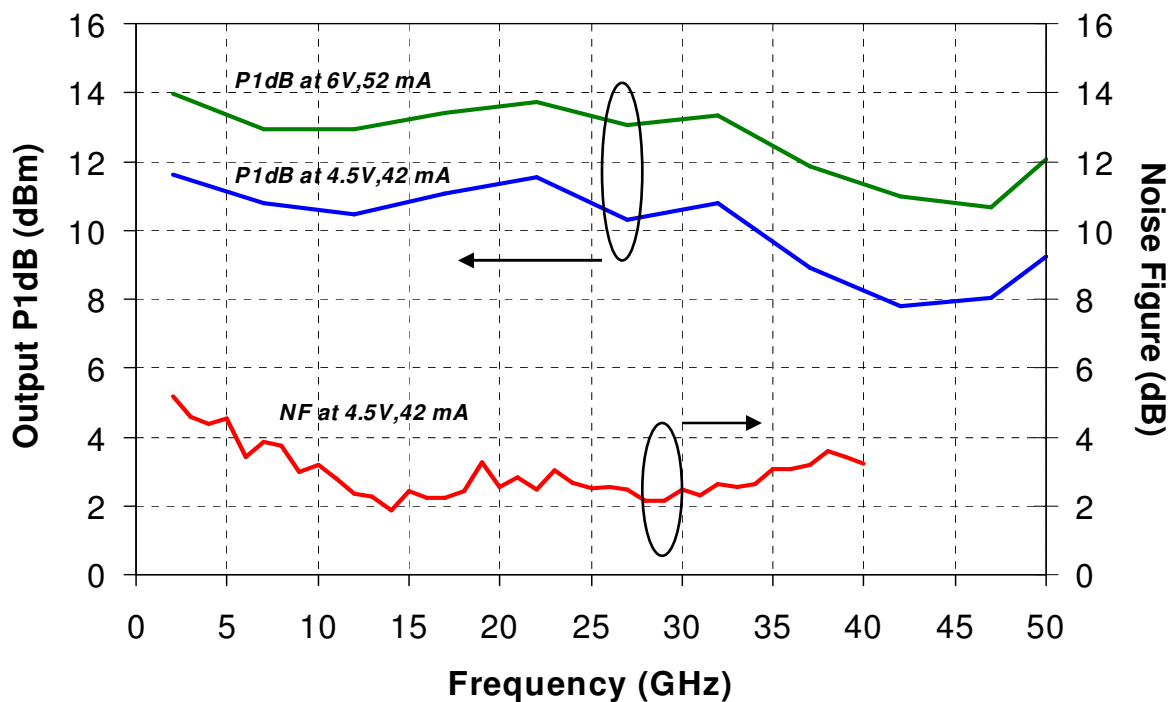
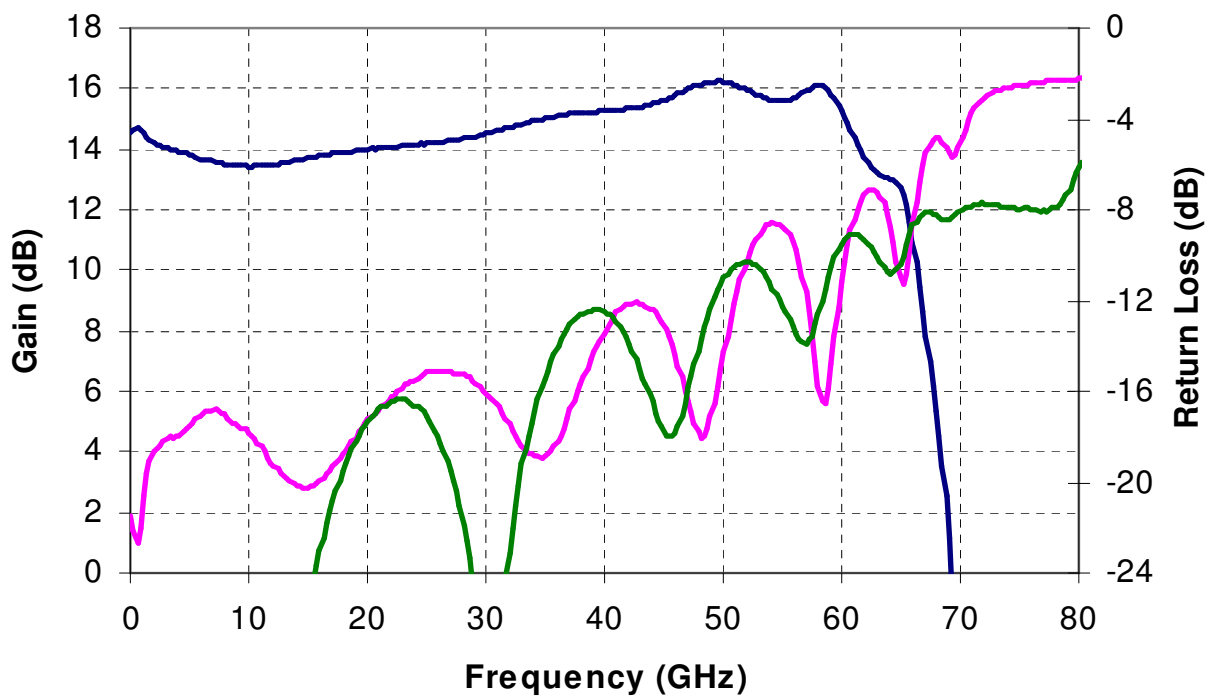
TABLE III
THERMAL INFORMATION

Parameter	Test Conditions	T _{CH} (°C)	R _{θJC} (°C/W)	T _M (HRS)
R _{θJC} Thermal Resistance (channel to backside of package)	Vd = 6 V I _D = 0.05 A P _{diss} = 0.3 W	80	33.3	8.7E8

Note: Die backside epoxy attached to carrier at 70°C baseplate temperature.

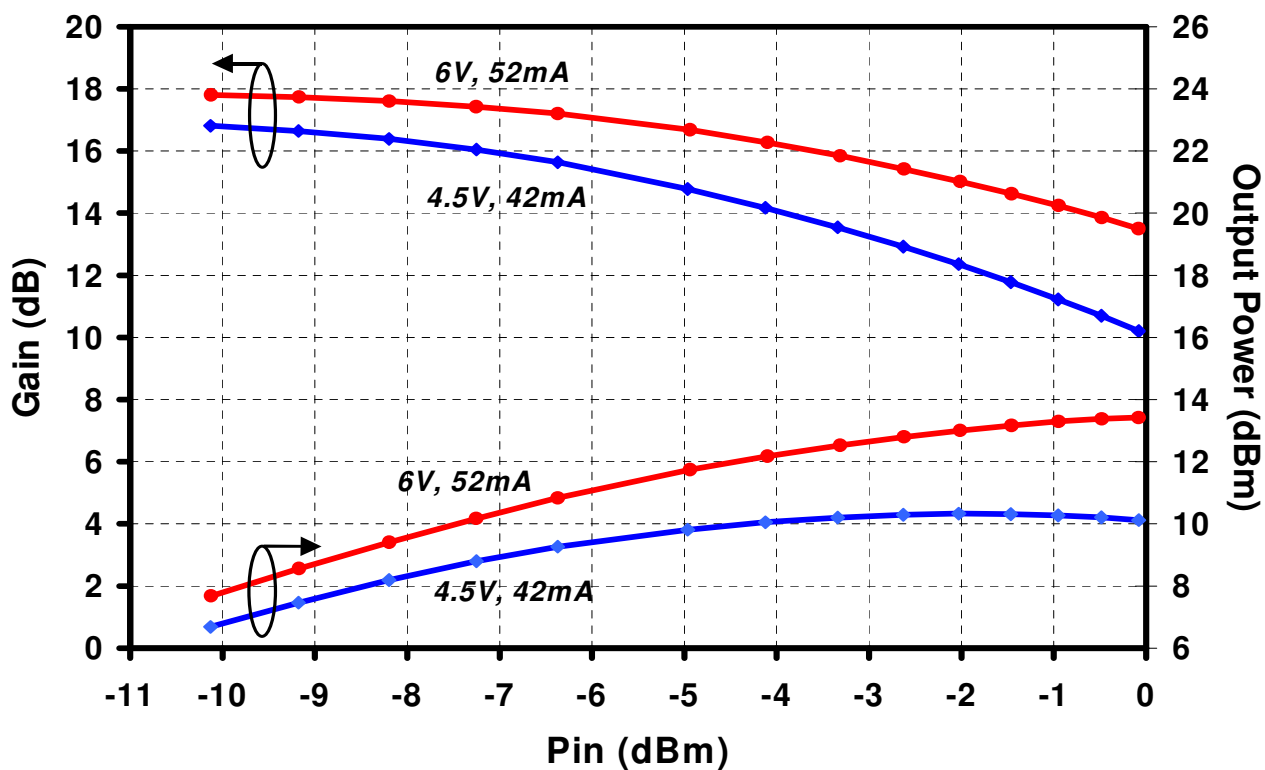
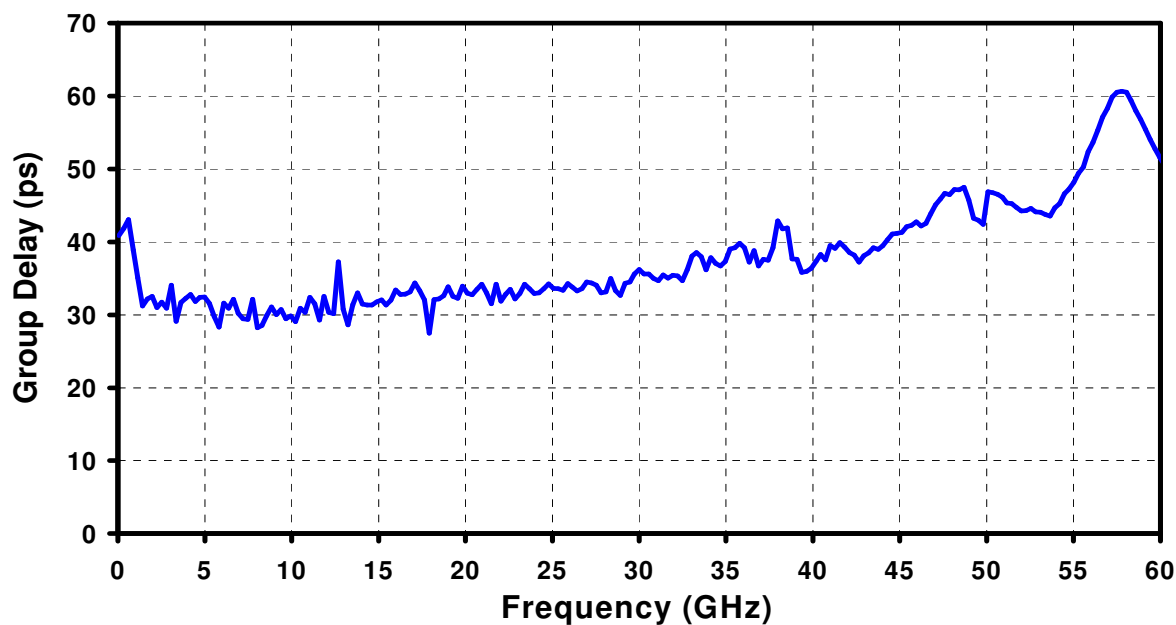
Measured Data

Bias Conditions: $V_d = 6\text{ V}$, $I_d = 50\text{ mA}$

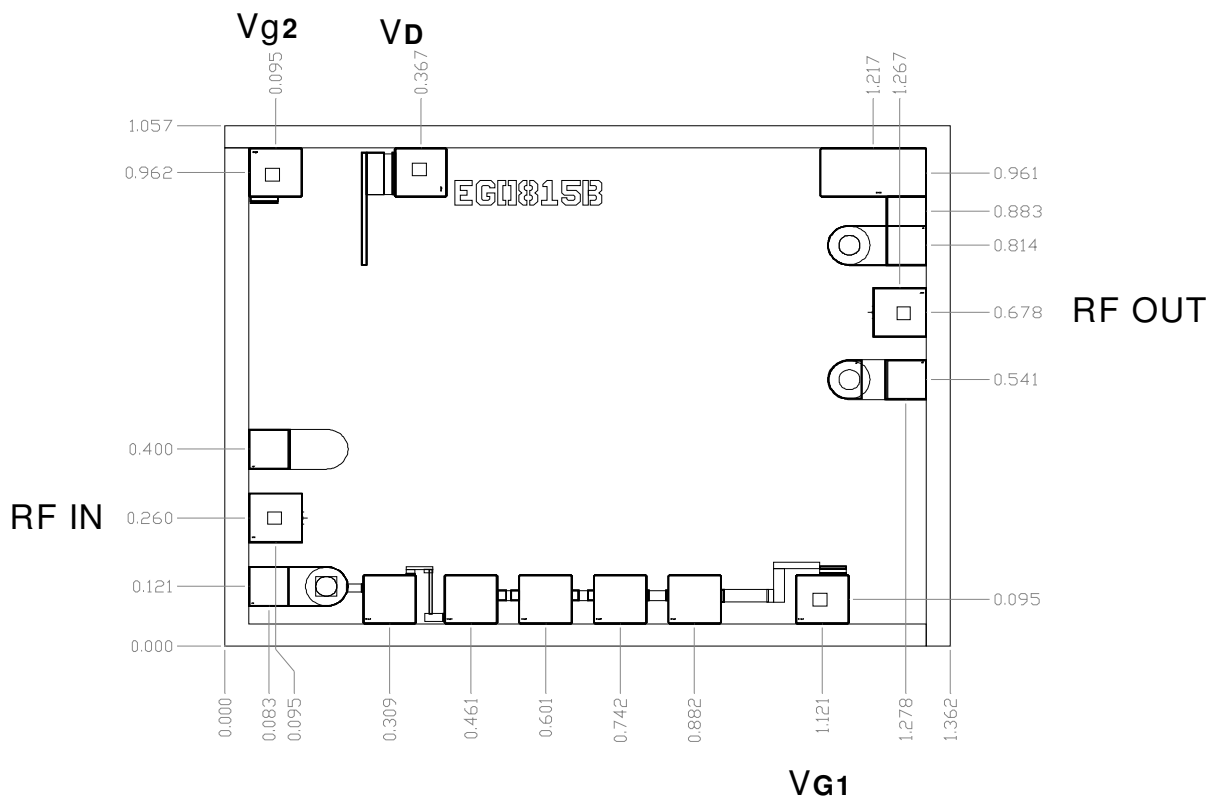


Measured Data

Bias Conditions: $V_d = 6\text{ V}$, $I_d = 50\text{ mA}$



Mechanical Drawing



Units: millimeters

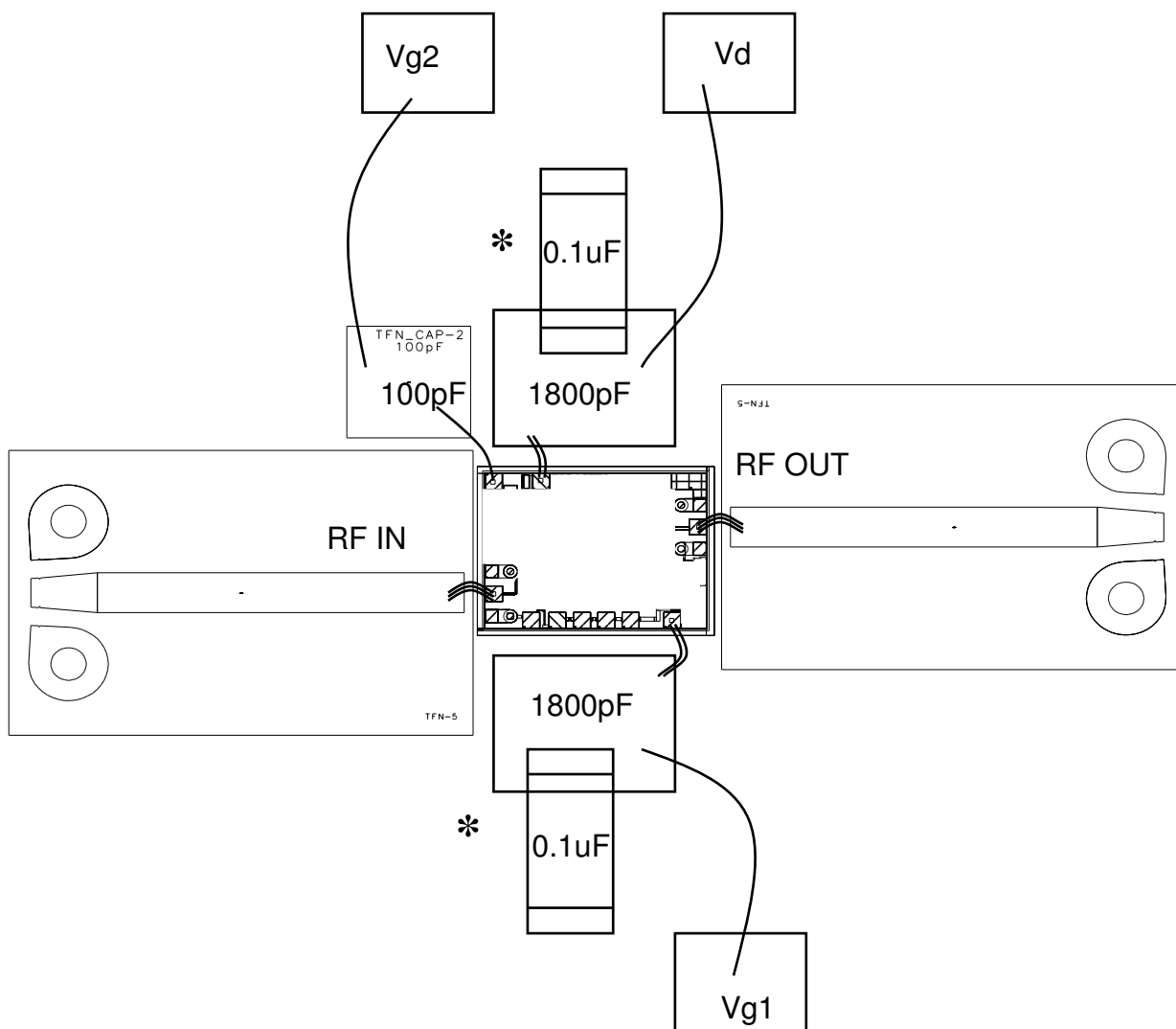
Thickness: 0.1

Chip edge to bond pad dimension are shown to center of bond pad.

Chip size tolerance: ± 0.051

	Pad size (mm)
VD	0.10x0.10
VG1	0.10x0.10
VG2	0.10x0.10
RF IN	0.10x0.10
RF OUT	0.10x0.10

Chip Assembly Diagram

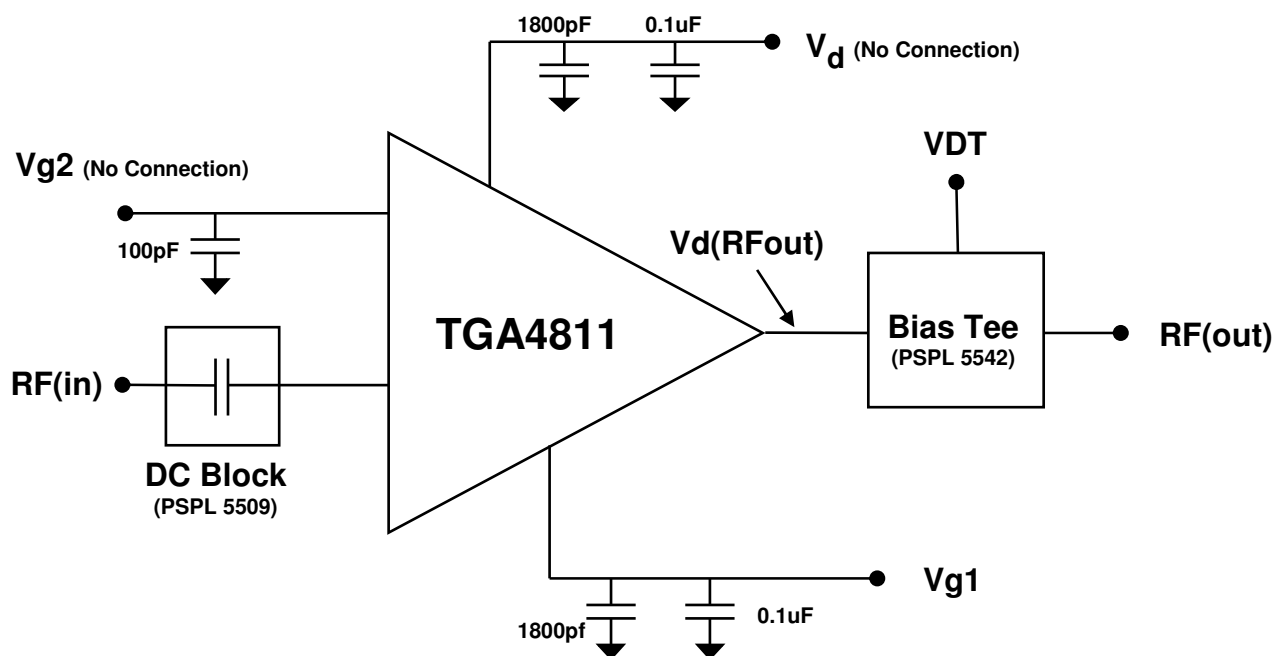


3 (Three) 0.7 mil chisel bond wires at RF IN and RF OUT or 1 (one) 3 mil ribbon at RF IN and RF OUT. Vg2 is optional for the circuit.

* 1800pF & 0.1uF capacitors can be substituted with the following integrated capacitors:

Part Number	Manufacturer
GZ0SYC104KJ8182MAW	AVX
VB4080X7R105Z16VHX182	Presidio

Optional Testing Circuit Schematic



* 1800pF & 0.1uF capacitors can be substituted with the following integrated capacitors:

Part Number	Manufacturer
GZ0SYC104KJ8182MAW	AVX
VB4080X7R105Z16VHX182	Presidio

Recommended Bias-Up Procedure

NOTE: To protect the device, this MMHEMT MMIC will be biased differently than typical PHEMT devices

NOTE: Be sure proper ESD protection is in place

A. If biasing Drain through Vd DC port

1. Leave V_g at 0V
2. Increase V_d to 1 V
3. Adjust V_g to reach 50 mA
4. Increase V_d to 4.5 V
5. Repeat steps 3 and 4 until correct bias is reached (i.e. $V_d = 4.5$ V, $I_d = 50$ mA)

6. To Bias-down device, turn V_g to 0V and decrease V_d to 0V

B. If Biasing Drain through Bias Tee and RF port

1. Leave V_g at 0V
2. Increase V_d to 1 V
3. Adjust V_g to reach 50 mA
4. Increase V_d to 2 V
5. Repeat steps 3 and 4 until correct bias is reached (i.e. $V_d = 2$ V, $I_d = 50$ mA)

6. To Bias-down device, turn V_g to 0V and decrease V_d to 0V

Assembly Process Notes

Reflow process assembly notes:

- Use epoxy with limited exposure to temperatures at 175°C.
- No fluxes should be utilized.
- Coefficient of thermal expansion matching is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.

Component placement and adhesive attachment assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- The force impact is critical during auto placement.
- Organic attachment can be used in low-power applications.
- Curing should be done in a convection oven; proper exhaust is a safety concern.
- Microwave or radiant curing should not be used because of differential heating.
- Coefficient of thermal expansion matching is critical.

Interconnect process assembly notes:

- Thermosonic ball bonding is the preferred interconnect technique.
- Force, time, and ultrasonics are critical parameters.
- Aluminum wire should not be used.
- Maximum stage temperature is 175°C.