

MC100EP140

3.3V ECL Phase-Frequency Detector

Description

The MC100EP140 is a three state phase frequency–detector intended for phase–locked loop applications which require a minimum amount of phase and frequency difference at lock. Since the part is designed with fully differential internal gates, the noise is reduced throughout the circuit, especially at high speeds. The basic operation of a Phase/Frequency Detector (PFD) is to “compare” an incoming signal (feedback) to a set reference signal. When the Reference (R) and Feedback (FB) inputs are unequal in frequency and/or phase, the differential UP (U) and DOWN (D) outputs will provide pulse streams which, when subtracted and integrated, provide an error voltage for control of a VCO. Detector states of operation are shown in the Figure 2 and the State Table.

The typical output amplitude of the EP140 is 400 mV, allowing faster switching time and greater bandwidth. For proper operation, the input edge rate of the R and FB inputs should be less than 5 ns.

More information on Phase Lock Loop operation and application can be found in AND8040.

The pinout is shown in Figure 1, the logic diagram in Figure 3, and the typical termination in Figure 5.

Features

- 500 ps Typical Propagation Delay
- Maximum Frequency > 2.1 GHz Typical
- Fully Differential Internally
- Advanced High Band Output Swing of 400 mV
- Transfer Gain: 1.0 mV/Degree at 1.4 GHz
1.2 mV/Degree at 1.0 GHz
- Rise and Fall Time: 100 ps Typical
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range: $V_{CC} = 3.0\text{ V to }3.6\text{ V}$
with $V_{EE} = 0\text{ V}$
- NECL Mode Operating Range: $V_{CC} = 0\text{ V}$
with $V_{EE} = -3.0\text{ V to }-3.6\text{ V}$
- Open Input Default State
- Pb–Free Packages are Available



ON Semiconductor®

<http://onsemi.com>

MARKING DIAGRAMS*



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb–Free Package

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

MC100EP140

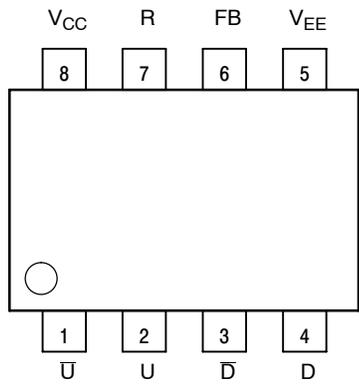


Figure 1. 8-Lead Pinout (Top View)

Table 1. PIN DESCRIPTION

| PIN | FUNCTION |
|-----------------|---------------------------|
| D, \bar{D} | Differential Down Outputs |
| U, \bar{U} | Differential Up Outputs |
| R* | ECL Reference Input |
| FB* | ECL Feedback Input |
| V _{CC} | Positive Supply |
| V _{EE} | Negative Supply |

* Pins will default LOW when left open.

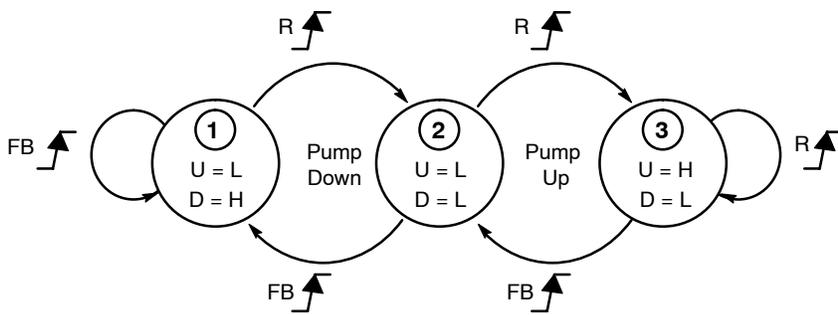


Figure 2. Phase Detector Logic Model

Table 2. STATE TABLE

| PHASE DETECTOR STATE | INPUT | | OUTPUT | |
|----------------------|-------|-----|--------|-----|
| | R | FB | U | D |
| PUMP DOWN 2-1-2 | 2 | L L | L L | L L |
| | 2-1 | L H | L H | L H |
| | 1-2 | H L | L L | L L |
| | 2 | L L | L L | L L |
| PUMP UP 2-3-2 | 2 | L L | L L | L L |
| | 2-3 | H L | H L | L L |
| | 3-2 | H H | L L | L L |
| | 2 | L L | L L | L L |

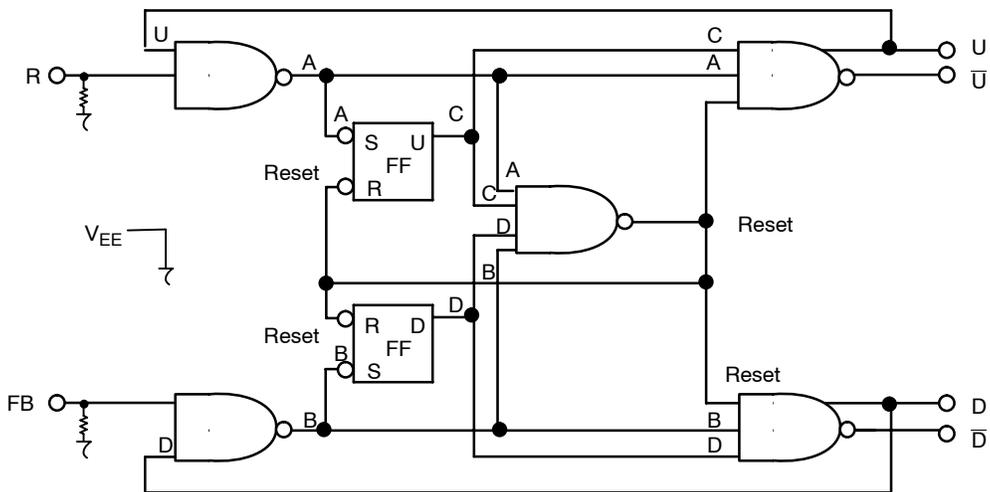


Figure 3. Logic Diagram

MC100EP140

Table 3. ATTRIBUTES

| Characteristics | | Value | |
|---|---|-----------------------------|-------------|
| Internal Input Pulldown Resistor | | 75 kΩ | |
| Internal Input Pullup Resistor | | 37.5 kΩ | |
| ESD Protection | Human Body Model Machine Model Charged Device Model | > 2 kV > 200 V > 2 kV | |
| Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1) | | Pb Pkg | Pb-Free Pkg |
| SOIC-8 | | Level 1 | Level 1 |
| Flammability Rating | Oxygen Index: 28 to 34 | UL 94 V-0 @ 0.125 in | |
| Transistor Count | | 457 Devices | |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test | | | |

1. For additional information, see Application Note AND8003/D.

Table 4. MAXIMUM RATINGS

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Unit |
|------------------|--|--|--|-------------|--------------|
| V _{CC} | PECL Mode Power Supply | V _{EE} = 0 V | | 6 | V |
| V _{EE} | NECL Mode Power Supply | V _{CC} = 0 V | | -6 | V |
| V _I | PECL Mode Input Voltage NECL Mode Input Voltage | V _{EE} = 0 V V _{CC} = 0 V | V _I ≤ V _{CC} V _I ≥ V _{EE} | 6 -6 | V V |
| I _{out} | Output Current | Continuous Surge | | 50 100 | mA mA |
| T _A | Operating Temperature Range | | | -40 to +85 | °C |
| T _{stg} | Storage Temperature Range | | | -65 to +150 | °C |
| θ _{JA} | Thermal Resistance (Junction-to-Ambient) | 0 lfpm 500 lfpm | SOIC-8 SOIC-8 | 190 130 | °C/W °C/W |
| θ _{JC} | Thermal Resistance (Junction-to-Case) | Standard Board | SOIC-8 | 41 to 44 | °C/W |
| T _{sol} | Wave Solder | Pb Pb-Free | | 265 265 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 5. 100EP DC CHARACTERISTICS, PECL V_{CC} = 3.3 V, V_{EE} = 0 V (Note 2)

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|-----------------|-----------------------------------|-------|------|------|------|------|------|------|------|------|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| I _{EE} | Power Supply Current | 45 | 65 | 85 | 50 | 70 | 90 | 53 | 73 | 93 | mA |
| V _{OH} | Output HIGH Voltage (Note 3) | 2155 | 2280 | 2405 | 2155 | 2280 | 2405 | 2155 | 2280 | 2405 | mV |
| V _{OL} | Output LOW Voltage (Note 3) | 1755 | 1880 | 2005 | 1755 | 1880 | 2005 | 1755 | 1880 | 2005 | mV |
| V _{IH} | Input HIGH Voltage (Single-Ended) | 2075 | | 2420 | 2075 | | 2420 | 2075 | | 2420 | mV |
| V _{IL} | Input LOW Voltage (Single-Ended) | 1355 | | 1675 | 1355 | | 1675 | 1355 | | 1675 | mV |
| I _{IH} | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| I _{IL} | Input LOW Current | 0.5 | | | 0.5 | | | 0.5 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

2. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.3 V to -0.3 V.

3. All loading with 50 Ω to V_{CC} - 2.0 V.

MC100EP140

Table 6. 100EP DC CHARACTERISTICS, NECL $V_{CC} = 0\text{ V}$, $V_{EE} = -3.6\text{ V to }-3.0\text{ V}$ (Note 4)

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|----------|-----------------------------------|-------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| I_{EE} | Power Supply Current | 45 | 65 | 85 | 50 | 70 | 90 | 53 | 73 | 93 | mA |
| V_{OH} | Output HIGH Voltage (Note 5) | -1145 | -1020 | -895 | -1145 | -1020 | -895 | -1145 | -1020 | -895 | mV |
| V_{OL} | Output LOW Voltage (Note 5) | -1545 | -1420 | -1295 | -1545 | -1420 | -1295 | -1545 | -1420 | -1295 | mV |
| V_{IH} | Input HIGH Voltage (Single-Ended) | -1225 | | -880 | -1225 | | -880 | -1225 | | -880 | mV |
| V_{IL} | Input LOW Voltage (Single-Ended) | -1945 | | -1625 | -1945 | | -1625 | -1945 | | -1625 | mV |
| I_{IH} | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| I_{IL} | Input LOW Current | 0.5 | | | 0.5 | | | 0.5 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

4. Input and output parameters vary 1:1 with V_{CC} .
 5. All loading with $50\ \Omega$ to $V_{CC} - 2.0\text{ V}$.

Table 7. AC CHARACTERISTICS $V_{CC} = 0\text{ V}$; $V_{EE} = -3.0\text{ V to }-3.6\text{ V}$ or $V_{CC} = 3.0\text{ V to }3.6\text{ V}$; $V_{EE} = 0\text{ V}$ (Note 6)

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit | |
|--------------------------|--|--------------|------------|------------|------------|------------|------------|------------|------------|------------|------|----|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | | |
| f_{max} | Maximum Frequency (Figure 4) | | > 2 | | | > 2 | | | > 2 | | GHz | |
| t_{PLH} , t_{PHL} | Propagation Delay to Output Differential R to U, FB to D FB to U, R to D | 300 400 | 450 600 | 600 800 | 325 450 | 475 650 | 625 850 | 350 500 | 500 700 | 650 900 | ps | |
| t_{JITTER} | Cycle-to-Cycle Jitter (Figure 4) | | .2 | < 1 | | .2 | < 1 | | .2 | < 1 | ps | |
| V_{PP} | Input Voltage Swing | 400 | 800 | 1200 | 400 | 800 | 1200 | 400 | 800 | 1200 | mV | |
| t_r , t_f | Output Rise/Fall Times (20% - 80%) | Q, \bar{Q} | 50 | 90 | 180 | 60 | 100 | 200 | 70 | 120 | 220 | ps |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

6. Measured using a 750 mV V_{PP} pk-pk, 50% duty cycle, clock source. All loading with $50\ \Omega$ to $V_{CC} - 2.0\text{ V}$.

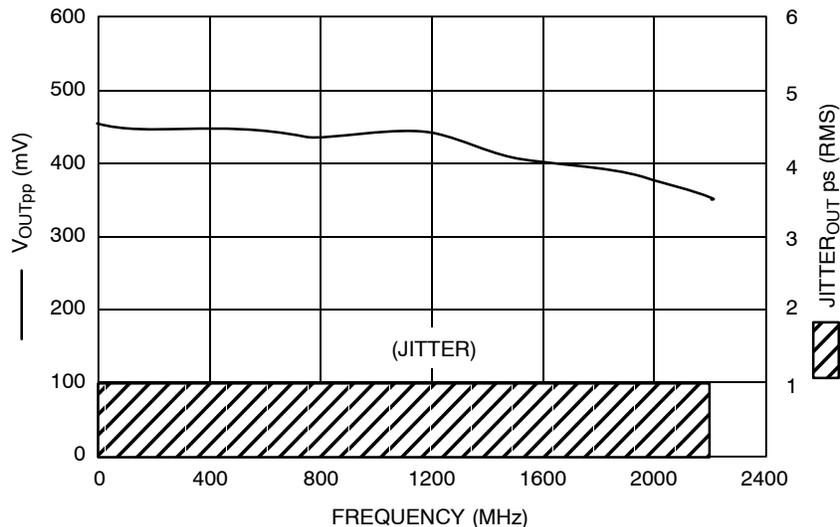
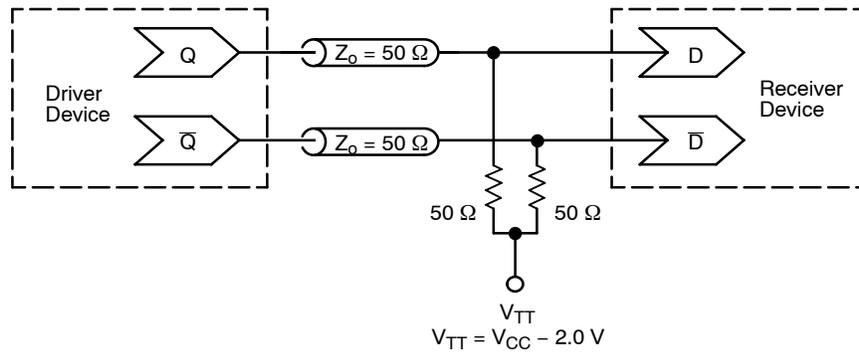


Figure 4. F_{max} /Jitter

MC100EP140



**Figure 5. Typical Termination for Output Driver and Device Evaluation
(See Application Note AND8020/D – Termination of ECL Logic Devices.)**

ORDERING INFORMATION

| Device | Package | Shipping [†] |
|----------------|---------------------|-----------------------|
| MC100EP140D | SOIC-8 | 98 Units / Rail |
| MC100EP140DG | SOIC-8 (Pb-Free) | 98 Units / Rail |
| MC100EP140DR2 | SOIC-8 | 2500 / Tape & Reel |
| MC100EP140DR2G | SOIC-8 (Pb-Free) | 2500 / Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

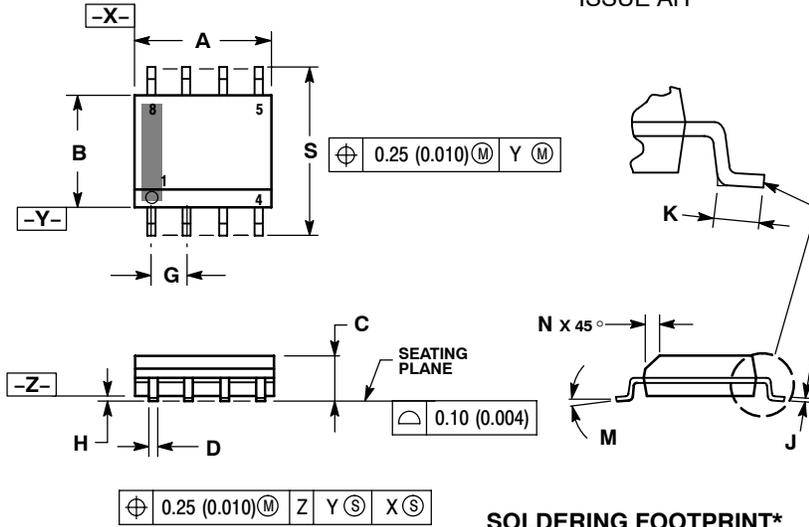
Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPiCE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

MC100EP140

PACKAGE DIMENSIONS

SOIC-8 NB
CASE 751-07
ISSUE AH

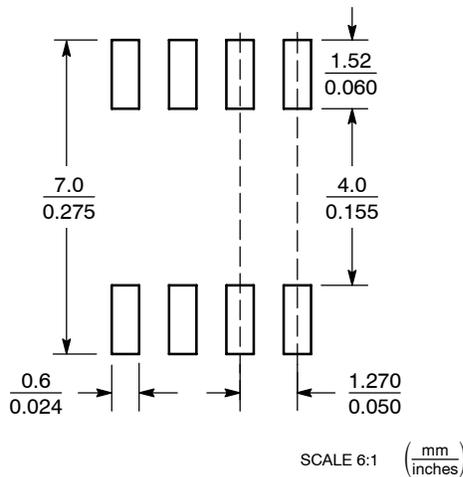


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 4.80 | 5.00 | 0.189 | 0.197 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.053 | 0.069 |
| D | 0.33 | 0.51 | 0.013 | 0.020 |
| G | 1.27 BSC | | 0.050 BSC | |
| H | 0.10 | 0.25 | 0.004 | 0.010 |
| J | 0.19 | 0.25 | 0.007 | 0.010 |
| K | 0.40 | 1.27 | 0.016 | 0.050 |
| M | 0° | 8° | 0° | 8° |
| N | 0.25 | 0.50 | 0.010 | 0.020 |
| S | 5.80 | 6.20 | 0.228 | 0.244 |

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ECLinPS is a trademark of Semiconductor Components Industries, LLC (SCILLC).

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5773-3850

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative

MC100EP140/D