RoHS

CMOS Audio/Video RF Modulators

MC44CC373CA
MC44CC373CAS
MC44CC374CA
MC44CC374T1A

CMOS AUDIO/VIDEO RF MODULATORS

The MC44CC373 / MC44CC374 CMOS family of RF modulators is the latest generation of the legacy MC44BS373/4 family of devices.

The MC44CC373/MC44CC374 RF modulators are designed for use in VCRs, set-top boxes, and similar devices.They support multiple standards, and can be programmed to support PAL, SECAM, or NTSC formats.

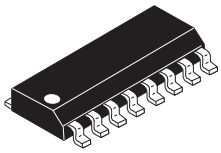
The devices are programmed by a high-speed I^2C Bus.

A programmable, internal PLL, with on-chip LC tank covers the full UHF range. The modulators incorporate a programmable, on-chip, sound subcarrier oscillator that covers all broadcast standards. No external tank circuit components are required, reducing PCB complexity and the need for external adjustments. The PLL obtains its reference from a low cost 4 MHz crystal oscillator.

The devices are available in a 16-pin SOIC, Pb-free package. These parts are functionally equivalent to the MC44BS373/4 series, but are not direct drop-in replacements.

All devices now include the AUX_{IN} found previously only on the 20-pin package option of the MC44BS373. This is a direct input for a modulated subcarrier and is useful in BTSC or NICAM stereo sound or other subcarrier applications.

The MC44CC373CASEF has a secondary I^2C address for applications using two modulators on one I^2C Bus.



EF SUFFIX
SOIC-16 PACKAGE
CASE 751B-05

Features

- Multi-TV standard support: NTSC, PAL, SECAM (B/G, I, D/K, L, M/N).
- UHF operation (460MHz to 880MHz)
- Programmable UHF oscillator and sound subcarrier oscillator.
- On-chip tank circuits. No external varicaps inductors or tuned components required.
- Program control via 800 kHz high-speed I^2C-bus.
- Programmable Sound reference frequency (31.25 kHz or 62.5 kHz)
- Direct sound modulator input (FM and AM).
- Auxiliary input bypasses AM/FM modulators for NICAM or BTSC applications.
- Video modulation depth (96% typ. in system L and 85% typ. in the other standards)
- Programmable Peak White Clip levels
- On-chip video test pattern generator with sound test signal (1 kHz)
- Low-power standby mode
- Output inhibit during PLL Lock-up at power-ON
- Logical output port controlled by I^2C-bus

ORDERING INFORMATION

Orderable Part Number(1)	Replaces Part Number	Default Frequency (MHz)	RF_{OUT}(2) ($dB\mu V$)	I^2C Write Address	PAL or NTSC Capability	SECAM (system L) Capability	AUX_{IN}
MC44CC373CAEF, R2	MC44BS373CAD	591.25	89	0xCA	Yes	Yes	Yes
	MC44BS373CAEF						
	MC44BS373CAFC						
MC44CC373CASEF, R2	MC44BS373CAFC	591.25	89	0xCE	Yes	Yes	Yes
MC44CC374CAEF, R2	MC44BS374CAD	591.25	89	0xCA	Yes	No	Yes
	MC44BS374CAEF						
MC44CC374T1AEF, R2	MC44BS374T1D	871.25	89	0xCA	Yes	No	Yes
	MC44BS374T1EF						
	MC44BS374T1AD	871.25	89	0xCA	Yes	No	Yes
	MC44BS374T1AEF						

1. All orderable parts are in a 16-pin SOIC, with temperature range of 0°C to +70°C ambient. For tape and reel, add the R2 suffix.
2. Refer to application note to obtain 82 $dB\mu V$ or other RF levels.

This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

freescale semiconductor

PIN DESCRIPTIONS

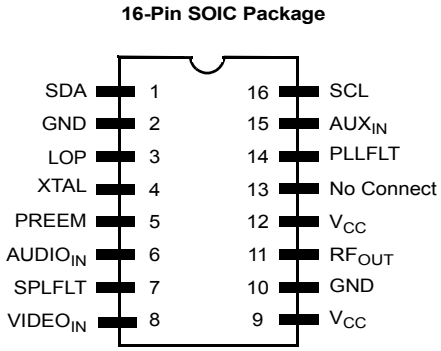


Figure 1. Pin Connections

Table 1. SO16 Package Pin Descriptions

Pin Number	Pin Name	Description	Comments
1	SDA	I^2C data	Bidirectional serial data I/O port for setting configuration. Compatible with 0-5 V and 0-3.3 V I^2C-bus.
2	GND	Ground	
3	LOP	Logical output port controlled by I^2C bus	Open collector output. Controlled by a single bit in the control register.
4	XTAL	Crystal	4 MHz crystal.
5	PREEMP	Pre-emphasis capacitor	
6	$AUDIO_{IN}$	Audio input	> 20 kΩ input impedance.
7	SPLFLT	Sound PLL loop filter	
8	$VIDEO_{IN}$	Video input	1 Volt peak-to-peak baseband video input
9	V_{CC}	Supply voltage	3.3 volt power input.
10	GND	Ground	
11	RF_{OUT}	TV output signal	A 75 Ω composite video output signal
12	V_{CC}	Supply voltage	3.3 Volt power input.
13	NC	No Connection	Do not make any connection to this pin.
14	PLLFLT	RF PLL loop filter	
15	AUX_{IN}	Auxiliary Input	Subcarrier input for stereo and NICAM applications
16	SCL	I^2C clock	Serial control port data clock. Compatible with 0-5 V and 0-3.3 V I^2C bus.

FUNCTIONAL OVERVIEW

Figure 2 shows a simplified block diagram of the MC44CC373CA and MC44CC374CA modulators.

There are three main sections:

1. A high speed I²C-compatible bus section for control and programming.
2. A PLL section to synthesize the UHF output channel frequency.
3. A modulator section, which accepts audio and video inputs and modulates the RF carrier

An on-chip simple video test pattern generator with an audio test signal is included, but is not shown in the block diagram.

The MC44CC373/4CA operates as a multi-standard modulator and can handle the following systems using the same external circuit components: B/G, I, D/K, L, M/N.

The different orderable part numbers provide: a choice in the pre-programmed power-up default channel frequency, the output power level and a pre-programmed secondary I²C address.

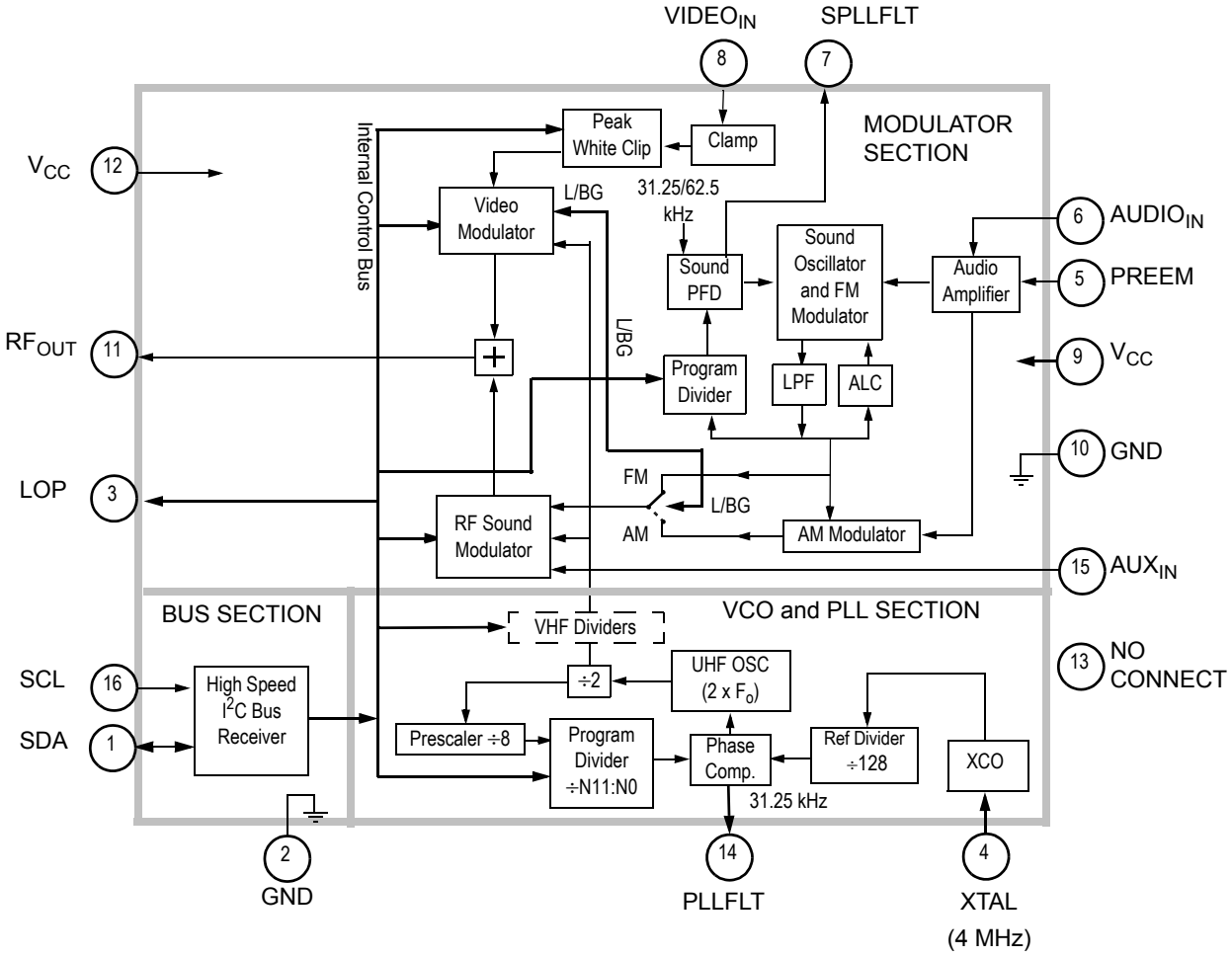


Figure 2. MC44CC373/374 Simplified Block Diagram

MODES OF OPERATION AND FUNCTIONAL DESCRIPTION

POWER ON SETTINGS

At power-on, the modulators are configured with pre-programmed default settings as listed in Table 2.

Table 2. Power On Default Settings

Operating Mode	Default Values			
Part Number	**MC44CC373CA**	**MC44CC373CAS**	**MC44CC374CA**	**MC44CC374T1A**
UHF oscillator frequency (MHz)	591.25	591.25	591.25	871.25
RF_{OUT} power (dBμV)(1)	89	89	89	89
Sound frequency (MHz)	5.5	5.5	5.5	5.5
Sound reference frequency (kHz)	31.25	31.25	31.25	31.25
Logic Output Port (logic level)	Low	Low	Low	Low
Picture to sound ratio (dB)	12	12	12	12
Peak White Clip (state)	On	On	On	On
System Standards	B/G	B/G	B/G	B/G

1. Refer to application note to obtain 82 dBμV or other RF levels.

POWER ON RESET

A power-on reset circuit holds the digital portion in reset until the power supply has stabilized. Additionally a delay of approximately 2 seconds allows the crystal oscillator to stabilize before the digital section begins normal operation.

TRANSIENT OUTPUT INHIBIT

To minimize the risk of interference to other channels while the UHF PLL is acquiring a lock on the desired frequency, the Sound and Video modulators are turned OFF during a time out period in two cases: Power On and UHF oscillator power On (**OSC** bit switched from OFF to normal operation). There is a time out of 262 ms until the output is enabled. This lets the UHF PLL settle to its programmed frequency.

STANDBY MODES

During standby mode, the modulator is switched to low power consumption. The sound oscillator, UHF oscillator, and the video and sound modulator section's bias are internally turned OFF. The I^2C bus section remains active.

The standby mode is set with a combination of 3 bits:
OSC=1, **SO**=1 and **ATT**=1 for MC44CC373/374CAxxx
OSC=0, **SO**=1 and **ATT**=1 for MC44CC374T1Axx

Programming of the Frequency Registers or the Optional Control Registers is not allowed in Standby Mode.

SYSTEM L OR B/G SELECTION

The **SYSL** enable control bit internally switches the following functions:

- **SYSL** = 0 enables B/G system
  - — Video modulation polarity: Negative
  - — Sound modulation: FM
- **SYSL** = 1 enables L system
  - — Video modulation polarity: Positive
  - — Sound modulation AM

CRYSTAL REFERENCE OSCILLATOR

The reference crystal frequency is 4.0 MHz, the same as for the legacy modulators.

The reference crystal oscillator if followed by a fixed divide-by-128, resulting in a reference frequency of 31.25 kHz for the phase detector.

UHF PLL SECTION

The UHF VCO runs at twice the desired RF frequency and is divided by 2 before it is sent to the divide-by-8 prescaler and then the programmable divider.

The programmable divider division-ratio is controlled by the state of control bits **N0** to **N11** and is the binary number for the number of 250 kHz steps in the desired RF_{OUT} frequency. The divider-ratio N for a desired frequency F (in MHz) is given by:

$$N = \frac{(2 \times F)}{16} \times \frac{128}{4}$$

with:

$$N = 2048 \times N11 + 1024 \times N10 + \ldots\ldots + 4 \times N2 + 2 \times N1 + N0$$

NOTE:

Programming a division-ratio N = 0 is not allowed.
Programming of the N value must be performed while the modulator is in normal mode, not standby mode.

UHF OSCILLATOR-VHF RANGE

For VHF range operation, the UHF oscillator can be internally divided by: 2, 4, 8, or 16. This is accomplished via the special test mode bits, **X2:X0**.

NOTE:

The MC44CC373/374 modulators are intended for UHF operation. Using the digital dividers for VHF operation will cause additional spurious content in the RF_{OUT}. Performance specifications for VHF operation are not provided. The user must provide external filtering on RF_{OUT} to meet their VHF spurious requirements.

SOUND SECTION

The sound oscillator is fully integrated and does not require any external components. An internal low-pass filter and matched structure provide very low harmonics levels.

The sound modulator system consists of an FM modulator incorporating the sound subcarrier oscillator. An AM modulator is also included in the MC44CC373/374xxxx devices and is enabled by the **SYSL** control bit for use in system L applications. The audio input signal is AC-coupled into the amplifier, which then drives the modulators.

The sound reference divider is programmed by control bit **SRF,** resulting in a reference frequency of 31.25 kHz or 62.5 kHz. The sound subcarrier frequency is selected by control bits **SFD1:SFD0**. The subcarrier frequencies are 4.5, 5.5, 6.0 or 6.5 MHz. The power-up default value is 5.5 MHz.

A capacitor is connected to the external pin, **PREEM**, to set the pre-emphasis time constant for the application. Information on the selection of this filter may be found later in this document under applications information.

LOGIC OUTPUT PORT (LOP)

The **LOP** pin controls any logic function. The primary applications for the **LOP** are to control an external attenuator or an external switch, between the antenna input and TV output. A typical attenuator application with PIN diode is shown in Figure 3. The **LOP** pin switches the PIN attenuator depending on the signal strength of the Antenna Input. This reduces the risks of intermodulation in certain areas. The **LOP** can also be used as an OFF position bypass switch or for other logic functions in the application.

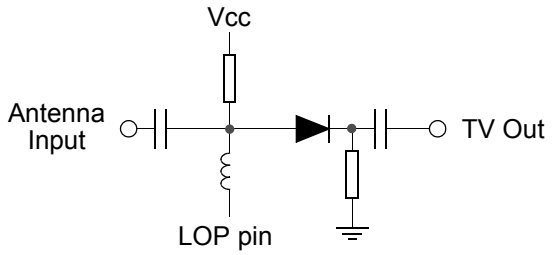


Figure 3. Typical Attenuator Application with Pin Diode

VIDEO SECTION - PEAK WHITE CLIP

The modulators require the following for proper video functionality:

- A composite video input with negative going sync pulses
- A nominal video level of < 1.14 V

This signal is AC-coupled to the video input where the sync tip level is clamped.

The video signal is then passed to a Peak White Clip (PWC) circuit. The PWC circuit function soft-clips the top of the video waveform, if the sync tip amplitude to peak white clip goes too high. This avoids carrier over-modulation by the video.

The Peak White Clip level may be set via the Option Control Register 2, bits **PW1:PW0**. Clipping can be disabled by software via bit **PWC** in the Control register.

TEST PATTERN GENERATOR

The modulators have a simple test pattern generator, that may be enabled under I^2C bus control, to permit a TV receiver to easily tune to the modulator output. The pattern consists of two white vertical bars on a black background and a 1 kHz audio test signal.

The video test pattern consists of two signals generated by the Digital section. One controls the sync pulse circuitry, and the other controls the luminance circuitry. These signals are logic levels that drive the video circuitry which creates a composite signal with the proper levels for sync pulses and luminance as shown in Figure 4.

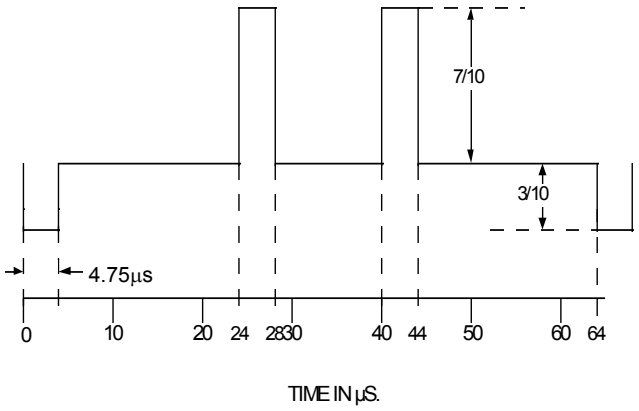


Figure 4. Test Pattern Generator

ELECTRICAL SPECIFICATIONS

Table 3. Absolute Maximum Ratings

Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Characteristic	Symbol	Min	Max	Units
Supply Voltage	V_{CC}	–0.3	+3.6	V
I^2C Input Voltage (SCL and SDA pins)	V_{INI^2C}	–0.3	+5.5	
Any Other Input Voltage	V_{IN}	–0.3	V_{CC} + 0.3	V
Storage Temperature Range	T_{stg}	–65	+150	°C
Junction Temperature	T_J	—	+105	°C

Table 4. General Specifications

Characteristic	Symbol	Min	Typ	Max	Units
ESD Protection (Charge Device Model)	CDM	500	—	—	V
ESD Protection (Human Body Model)(1)	HBM	2000	—	—	V
Latch-Up Immunity	LU	200	—	—	mA
Thermal Resistance from Junction to Ambient	$R_{\Theta JA}$	—	102	—	°C/W

1. JEDEC JESD22-A114D.

Table 5. Recommended Operating Conditions

Characteristic		Symbol	Min	Typ	Max	Units
Supply Voltage		V_{CC}	+3.0	+3.3	+3.6	V
Total supply current (all sections active)		I_{CC}	65	85	98	mA
Total standby mode supply current		I_{CC}	15	22	30	mA
Test pattern sync pulse width		—	3	4.7	6.5	µS
Sound comparator charge pump current	While locking When locked	— —	1 —	3.9 1	7 1.5	µA µA
RF comparator charge pump current		—	1.2	1.6	2	mA
Logic Output Port Saturation voltage at I_{OL}=2 mA Leakage current		 V_{OL} I_{OH}	 — —	 160 —	 300 1	 mV µA
Ambient Temperature		T_A	0	—	+70	°C

NOTE: Crystal specification reference information
Frequency = 4 MHz
Mode = Parallel Resonance
Load Capacitance = 27 pF
Motional Resistance = 10 Ohms Typical (100 Ohms Maximum Starting)

PERFORMANCE CHARACTERISTICS

Unless otherwise stated, all performance characteristics are for:

- Power Supply, V_{CC} = 3.3 V
- Ambient Temperature, T_A = 25°C
- Video Input 1.0 $V_{(pp)}$ 10-step grayscale.
- RF inputs/outputs into 75 Ω load.

NOTE:

Specifications only valid for envelope demodulation.

The parameters listed are based on the type of test conditions found in the column **Type**.

- A = 100% tested
- B = 100% Correlation tested
- C = Characterized on samples
- D = Design parameter

See "Characterization Measurement Conditions" on page 18 for each C type parameter.

Table 6. High Frequency Characteristics

Parameter	Test Conditions[1]	Device	Min	Typ	Max	Unit	Type
RF_{OUT} output level[2]	Output signal from modulator section	MC44CC373CA MC44CC374CA MC44CC374T1A	83	89	93	dBμV	B
UHF oscillator frequency			460	—	880	MHz	A
VHF range	UHF oscillator internally divided		45	—	460	MHz	B
RF_{OUT} output attenuation	During transient output inhibit, or when ATT bit is set to 1.		50	60	—	dBc	B
Sound subcarrier harmonics (Fp+n*Fs)	Reference picture carrier.		—	–63	–40	dBc	C
Second harmonic of chroma subcarrier	Using red EBU bar.		—	–54	—	dBc	C
Chroma/Sound intermodulation: Fp+(Fsnd–Fchr)	Using red EBU bar.		—	–65	—	dBc	C
Out-of-band (UHF picture carrier) spurious (Fo = 460 - 880MHz)	1/4*Fo, 1/2*Fo, 3/4*Fo, 3/2*Fo Output measured from 40 MHz to 1 GHz.		—	12	30	dBμV	C
Fo (picture carrier) harmonics[2][3]	2nd harmonic 3rd harmonic		— —	66 69	74 78	dBμV	C
In band spurious (Fo@5MHz)	No video/sound modulation.		—	—	–65	dBc	C

1. See Performance Measurement Test Set-ups, Table 9.
2. Refer to application note to obtain 82 dBμV or other RF levels and to reduce picture carrier harmonics.
3. Picture carrier harmonics are highly dependent on PCB layout and decoupling capacitors.

Table 7. Video Performance Characteristics

Parameter	Test Conditions[1]	Min	Typ	Max	Unit	Type
Video bandwidth	Reference 0 dB at 100 kHz, measured at 5 MHz.	–0.5	0.1	0.5	dB	C
Video input level	75Ω load	—	1.0	1.5	V_{CVBS}	D
Video input current		8	10	12	µA	A
Video input impedance		75	92	110	KΩ	A
Peak White Clip	Video Modulation depth for video=1.4 V_{CVBS} at default (01) PWC level	90.5	94	97.5	%	B
Video S/N	No sound modulation,100% white video. Using CCIR Rec.567 weighting filter.	53	55	—	dB	C
Differential Phase		+5	—	–5	deg	C
Differential Gain	PWC bit set to 0. CCIR Test Line 310, worst of first 4 out of 5 steps.	–5	—	5	%	C
Luma/Sync ratio	Input ratio 7.0:3.0	6.8/3.2	—	7.2/2.8	—	B
PAL video modulation depth (SYSL = 0)	1.0 Volt Peak-to-Peak input.	75	83	88	%	B
SECAM video modulation depth (SYSL = 1)	Gain set to default	90	96	99	%	B

1. See Performance Measurement Test Set-ups, Table 22.

Table 8. Audio Performance Characteristics

Parameter	Test Conditions[1]	Min	Typ	Max	Unit	Type
Picture-to-Sound ratio	PS bit 0 setting	9	—	19	dB	A
Audio modulation index	Using specific pre-emphasis circuit, audio input level=200 mV_{rms}-audio frequency=1 kHz					
	AM modulation: SECAM Fs=6.5MHz	76	80	86	%	A
	FM modulation: Fs=5.5, 6 or 6.5MHz 100% modulation=±50 kHz FM deviation	95	100	104	%	A
	FM modulation: NTSC Fs=4.5MHz 100% modulation=±25 kHz FM deviation	95	100	104	%	A
Audio input impedance		60	71	80	KΩ	A
Audio Frequency response	Reference 0dB at 1 kHz, using specified pre-emphasis circuit, measure from 50 Hz to 15 kHz	–2.5	—	+2.0	dB	C
Audio Frequency response	No pre-emphasis. Measure from 50 Hz to 50 kHz	±0.5	—	+2.0	dB	C
Audio Distortion FM (THD only)	At 1 kHz, 100% modulation (±50 kHz). Pre-emphasis. No video.	—	0.5	1	%	C
Audio Distortion AM (THD only)	At 1 kHz, 100% modulation Pre-emphasis. No video	—	1.5	2.5	%	C
Audio S/N with Sync Buzz FM	Ref 1 kHz, 50% modulation (±25 kHz) EBU color bars Video signal, using CCIR 468.2 weighting filter. Pre-emphasis.	50	54	—	dB	C
Audio S/N with Sync Buzz AM	Reference 1 kHz, 85% modulation Video input EBU color bar 75% Audio BW 40 Hz - 15 kHz Weighting filter CCIR 468-2. Pre-emphasis.	45	50	—	dB	C
Total Harmonic Distortion (THD)	No Pre-emphasis	—	—	0.1	%	C
Signal-to-Noise Ratio (SNR)	No Pre-emphasis. 50 Hz to 50 kHz BW	58	—	—	dB	C

1. See Performance Measurement Test Set-ups, Table 22.

HIGH SPEED I²C CONTROL INTERFACE OPERATION

The modulator chip's digital control interface is compatible with the I²C bus standard. The two pins used for the I²C bus are the clock (SCL) and data (SDA). The data pin is bidirectional.

The I²C interface lines are 5 Volt tolerant. Therefore, they can be pulled up to 5 Volts, if required, to interface with the microprocessor in a given application.

NOTE:

If the MC44CC373/4 modulator is powered down, it will load the I²C bus by means of leakage current passing through the stacked ESD protection diodes on the SCL and SDA pins.

The input control data stream is clocked in on the rising edge of SCL, with the most significant bit, MSB, first. The seven-bit IC Address and R/W bit are in the first byte sent. This allows the IC to determine if it is the device that is being communicated with. After that, an even number of control data bytes, 8-bits each, sent to configure the IC. The data stored in the input control register is loaded into the appropriate device registers during the acknowledge, ACK, bit time.

The Master controls the clock line, whether writing to the part or reading from it. After each byte that is sent, the device that receives it, sends an acknowledge bit back to the master. After the last data byte and ACK, the master sends a Stop Condition to terminate the write cycle.

Status data can be read back from the modulator chip. The output status data is clocked out on the falling edge of SCL and is valid on the rising edge, with the MSB first.

IC Device Address

Since the I²C bus is a two-wire bus that does not have a separate chip-select line, each IC on the bus has a unique address. This address must be sent each time an IC is communicated with. The address is the first seven bits that are sent to the IC as shown in Table 9. The eighth bit sent is the R/W bit, it determines whether the master will read from or write to the IC.

Table 9. IC Address Byte Format

7	6	5	4	3	2	1	0
IC Address							**Read/ Write**
A6	A5	A4	A3	A2	A1	A0	R/W
1	1	0	0	1	X	1	X

Address bit **A1** selects one of two possible addresses. The chip address is defined by the orderable part number as listed in Table 10. The **RW** bit determines if the master is requesting a read or write. **RW** = 0 = write and **RW** = 1 = read.

Table 10. Chip Address by Orderable Part Number

Orderable Part Number	IC Address Byte				
	A1	RW	Mode	Binary	Hex
MC44CC373CA, MC44CC374CA, MC44CC374T1A	0	0	Write	1100_1010	0xCA
	0	1	Read	1100_1011	0xCB
MC44CC373CAS	1	0	Write	1100_1110	0xCE
	1	1	Read	1100_1111	0xCF

I²C Write Mode Format

In the write mode, each ninth data bit is an acknowledge bit (ACK) as shown in Figure 5. During this time, the Master lets go of the bus, the external pull-up resistor pulls the signal high and sends a logic 1 and the Modulator circuit (slave) answers on the data line by pulling it low.

Besides the first byte with the chip address, the circuit needs two or more data bytes for operation.

The programming of the MC44CC37xxxxx devices is similar to the legacy devices. That is, they may be programmed with either two or four data bytes, after the chip address.

Table 11 shows the permitted data bytes, and the order in which they can be sent, to program the MC44CC373/374 devices. Examples 1 and 2 are the same as the legacy modulators.

The control data bytes all contain an address function bit (the MSB) which lets the IC distinguish between the frequency information and control information. If the address function bit is a logic 1, the following bytes contain control information. The frequency information has the address function bit that is set to a logic 0. This allows the frequency or the control information to be sent first as shown inn Examples 3,and 4.

The MC44BS373/4 legacy family of RF modulators required only two words of data (four bytes) for full configuration. The new CMOS devices have two additional (optional) control words that can be used to access some new features. These features include changing the output power, using a different frequency crystal, and adjusting the peak white clip levels. These new Option Control words do not need to be sent unless access to these new features is desired. The default values for these functions will allow the device to work the same way as the MC44BS373/4 devices did.

Example 5 shows how the new Option Control words are to be sent. OC1 follows the Control word and OC2 follows OC1.

Example 6 shows the Frequency word being sent first followed by the Control bytes.

The following rules apply for the sequences of data bytes for incoming (write) information:

- If an odd number of data bytes are received, the last one is ignored.
- If nine data bytes are received, the ninth and following ones are ignored, and the last ACK pulse is sent at the end of the eighth data byte.
- The optional control register one, most significant and least significant bytes, OC1M, OC1L, data must always be sent after the C1,C0 control data without a stop condition in between.
- The optional control register two, most significant and least significant bytes, OC2M, OC2L, data must be sent directly after the OC1M, OC1L data without a stop condition in between.
- The Control and Frequency information may be sent as separate I2C write sequences. (Example 1 or Example 5 followed/preceeded by Example 2).

Table 11. MC44CC373/4 Programming Sequence (Incoming Information)

Legacy Devices Data Bytes											
Example 1	STA	CA	C1	C0	STO						
Example 2	STA	CA	FM	FL	STO						
Example 3	STA	CA	C1	C0	FM	FL	STO				
Example 4	STA	CA	FM	FL	C1	C0	STO				
MC44CC37xxxxxx Devices using the Option Control Bytes											
Example 5	STA	CA	C1	C0	OC1M	OC1L	OC2M	OC2L	STO		
Example 6	STA	CA	FM	FL	C1	C0	OC1M	OC1L	OC2M	OC2L	STO

Abbreviations:

STA = Start condition

CA = Chip Address

FM = Frequency information, most significant (high order) bits

FL = Frequency information, least significant (low order) bits

C1 = Control information, most significant (high order) bits

CO = Control information, least significant (low order) bits

OC1M = Optional Control 1 information, most significant (high order) bits

OC1L= Optional Control 1 information, least significant (low order) bits

OC2M = Optional Control 2 information, most significant (high order) bits

OC2L = Optional Control 2 information, least significant (low order) bits

STO = Stop condition

I^2C Read Mode Format

To read back the status data, the read address shown in Table 10 is sent by the master. The modulator then responds with an ACK followed by a byte containing status information on the RF oscillator out-of-frequency range.

I²C BIT MAPPING SUMMARY

WRITE MODE	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	ACK
CA-CHIP ADDRESS	1	1	0	0	1	see Table 9	1	0	ACK
FM-High Order Bits	0	TPEN	N11	N10	N9	N8	N7	N6	ACK
FL-Low Order Bits	N5	N4	N3	N2	N1	N0	X1	X0	ACK
C1-High Order Bits	1	AUX	SO	LOP	PS	X3	X2	SYSL	ACK
C0-Low Order Bits	PWC	OSC	ATT	SFD1	SFD0	SREF	X5	X4	ACK
OC1M-High Order Bits	1	0	0	0	0	0	0	0	ACK
OC1L-Low Order Bits	0	0	0	0	0	0	0	0	ACK
OC2M-High Order Bits	1	0	0	0	0	0	0	0	ACK
OC2L-Low Order Bits	0	0	0	0	0	0	PW1	PW0	ACK

READ MODE	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	ACK
CHIP ADDRESS	1	1	0	0	1	see Table 9	1	1	ACK
R-Status Byte	—	—	—	—	—	Y2	Y1	OOR	—

Bit Name	Description
AUX	Auxiliary sound input enable/disable.
ATT	Modulator output attenuated-sound and video modulators ON/OFF
LOP	Logic Output Port
N0…N11	UHF frequency programming bits, in steps of 250 kHz
OSC	UHF oscillator ON/OFF
OOR	RF oscillator out-of-frequency range information
PS	Picture-to-sound carrier ratio
PWC	Peak White Clip enable/disable
SFD0, 1	Sound subcarrier frequency control bits
PW0, PW1	Peak White Clip Level. (see Table 20)
SO	Sound Oscillator ON/OFF
SREF	Sound PLL Reference frequency
SYSL	System L enable-selects AM sound and positive video modulation. (MC44CC373/374xxxx only)
TPEN	Test pattern enable-picture and sound
X5…X0	Test mode bits-All bits are 0 for normal operation. (see Table 18)
Y1, Y2	RF oscillator operating range information

I²C PROGRAMMING SUMMARY TABLES

Sound

SFD1	SFD0	Sound Subcarrier Freq (MHz)
0	0	4.5
0	1	5.5
1	0	6.0
1	1	6.5

PS	Picture-to-Sound Ratio (dB)
0	12
1	16

SO	Sound Oscillator
0	Sound oscillator ON (Normal mode)
1	Sound oscillation disabled (oscillator and PLL section bias turned OFF)

AUX	Auxiliary Audio Input
0	AUX input disabled (normal mode)
1	AUX input enabled

Video

SYSL	System L/BG Selection
	SYSL only applies to MC44CC373/374xxxx
0	System B/G enabled, System L disabled (FM sound and negative video modulation)
1	System L enabled, System B/G disabled (AM sound and positive video modulation)

PWC	Peak White Clip
0	Peak White Clip ON (System B/G)
1	Peak White Clip OFF (System L)

PW1	PW0	Peak White Clip Level
0	0	
0	1	1.0 Volt - Default
1	0	
1	1	

TPEN	Test Pattern Signal
0	Test pattern signal OFF (normal operation)
1	Test pattern signal ON (picture and sound)

UHF

OSC	UHF Oscillator	
	MC44CC373/ 374CAxxx	MC44CC374T1Axx
0	Normal operation.	UHF oscillator disabled.
1	UHF oscillator disabled.	Normal operation.

When UHF oscillator is disabled, do not program the frequency register N; also writing to Option Control Registers 1 and 2 is not allowed.

ATT	Modulator Output Attenuation
0	Normal operation
1	Modulator output attenuation (sound and video modulators sections bias turned OFF.

Sound PLL

SREF	Description
0	Sound Reference frequency = 31.25 kHz
1	Sound Reference frequency = 62.5 kHz

Standby Mode

OSC	SO	ATT	Combination of 3-bits
1	1	1	Modulator standby mode **(MC44CC373/374CAxx)**
0	1	1	Modulator standby mode **(MC44CC374T1Axx)**

Do not program the frequency register N value and Optional Control Registers during standby mode.

Logic Output Port

LOP	Description
0	Pin 3 is low voltage
1	Pin 3 is high impedance

INTER-IC (I^2C) INTERFACE TIMING

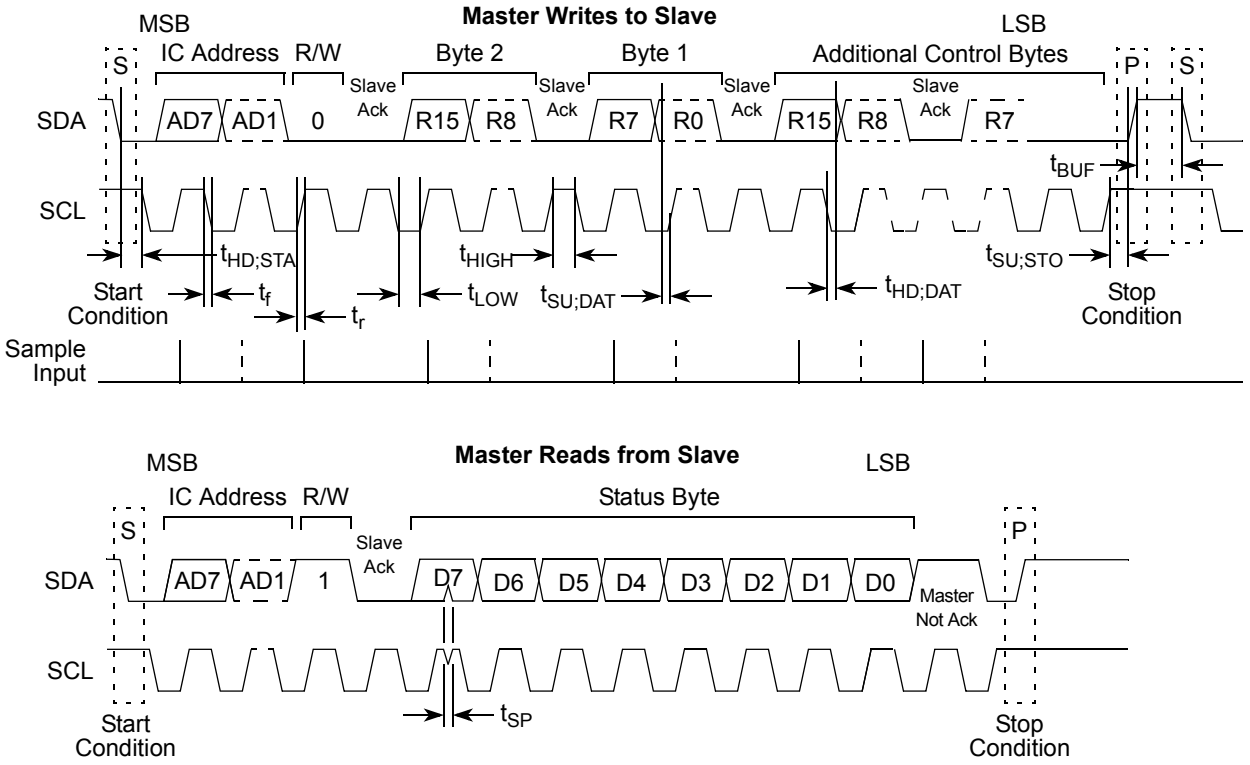


Figure 5. I^2C Timing Diagram

Table 12. I^2C Interface Bus Specifications

Parameter	Symbol	Min.	Max.	Units
Low Level Output Voltage	V_{OL}	0	0.4	V
High Level Input Voltage	V_{IH}	$0.7V_{CC}$	V_{CCmax}+0.5	V
Low Level Input Voltage	V_{IL}	–0.5	$0.3\ V_{CC}$	V
Absolute Max Input Voltage	—	—	5.5	V
Hysteresis of Schmitt trigger inputs	V_{hys}	$0.05V_{CC}$	—	V
Capacitance for each I/O pin(1)	C_{IN}	—	10	pF
Pulse width of spikes filtered out	t_{SP}	0	50	nS
SCL Frequency	f_{SCLK}	0	800	kHz
Hold time Start condition	$t_{HD;STA}$	500	—	nS
Set-up time for repeated start	$t_{SU;STA}$	500	—	nS
Data Set-up time	$t_{SU;DAT}$	100	—	nS
Data Hold time	$t_{HD;DAT}$	0	—	nS
Set-up time for Stop condition	$t_{SU;STO}$	500	—	nS
Low period of the SCL clock	t_{LOW}	0.6	—	uS
High period of the SCL clock	t_{HIGH}	0.6	—	uS
Rise time of both SDA and SCL	t_r	$20+ 0.1C_b$	300	nS
Fall time of both SDA and SCL	t_f	$20+ 0.1C_b$	300	nS
Bus free time between Stop and Start	t_{BUF}	200	—	nS

1. C_b = total capacitance of one bus line in pF.

CONTROL AND DATA REGISTER - DEFINITIONS

The legacy MC44BS373/4 modulators had two 16-bit control registers (Control and Frequency) and one data/status register. The new MC44CC373/374 family has the same register configuration and may be programmed with the same program software as the legacy devices. This backward compatibility allows a faster migration to new product redesigns. There are some additional control features that may be used in new designs. However, it is not necessary to program these bits when upgrading a legacy system with the new modulator family.

CONTROL REGISTER FORMAT

The control register format is shown in Figure 6 and the descriptions for the High-order and Low-order bits (bytes) are listed in Table 13 and Table 14 respectively.

MSB															**LSB**	
R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	
1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	Reset State
1	AUX	SO	LOP	PS	X3	X2	SYSL	PWC	OSC	ATT	SFD1	SFD0	SREF	X5	X4	
Adr					TEST MODE									TEST MODE		

Figure 6. Control Register Format

Table 13. Control Register (High-order) Bit Description

Bit	Name	Description	
15	Adr	Address Function bit. Must be set to a logic 1.	
14	AUX	Gates the AUX_{IN} pin	
		0	Disable AUX_{IN} pin.
		1	Enable AUX_{IN} pin.
13	SO	Sound Oscillator On/Off	
		0	Sound oscillator is on (normal mode).
		1	Sound oscillator is disabled (osc and PLL section bias is turned off).
12	LOP	Logic Output Port	
		0	LOP pin is low voltage.
		1	LOP pin is high impedance.
11	PS	Picture-to-sound carrier ratio	
		0	Picture-to-sound carrier ratio is 12 dB.
		1	Picture-to-sound carrier ratio is 16 dB.
10	X3	Test Mode bits, must be set to logic 0 for normal operation.	
9	X2	Test Mode bit. May be used for VHF divider	
8	SYSL	System L Enable - Selects AM sound and positive video modulation. *(Applies to MC44CC373xxx devices only. For the MC44CC374xxx devices this bit is set to 0 and may not be modified).*	
		0	System B/G enabled (FM sound and negative video modulation).
		1	System L enabled (AM sound and positive video modulation).

Table 14. Control Register (Low-order) Bit Description

Bit	Name	Description		
7	PWC	Peak White Clip enable/disable		
		0	Peak White Clip on (system B/G).	
		1	Peak White Clip off (system L).	
6	OSC	UHF oscillator On/Off		
			MC44CC373/ 374CAxxx	MC44CC374T1Axx
		0	Normal operation.	UHF oscillator disabled.
		1	UHF oscillator disabled.	Normal operation.
5	ATT	Modulator output attenuated.		
		0	Normal operation.	
		1	Modulator output attenuation (sound and video modulator sections bias is turned off).	
4	SFD1	Sound subcarrier frequency control bits.		
			SFD1	**SFD0**	**Frequency**
			0	0	4.5 MHz
3	SFD0		0	1	5.5 MHz
			1	0	6.0 MHz
			1	1	6.5 MHz
2	SREF	Sound PLL reference frequency		
		0	Sound reference frequency = 31.25 kHz	
		1	Sound reference frequency = 62.5 kHz	
1	X5	Test Mode bits, must be set to logic 0 for normal operation.		
0	X4			

FREQUENCY REGISTER FORMAT

The format for the frequency register is shown in Figure 7. The descriptions for the High-order and Low-order bits (bytes) are listed in Table 15 and Table 16 respectively.

MSB															LSB	
R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	
0	0	See Table 17 for the default (reset) value.												0	0	Reset State
0	TPEN	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	N0	X1	X0	
Adr	Test Ptrn	N Counter												TEST MODE		

Figure 7. Frequency Register Format

Table 15. Frequency Register (High-order) Bit Description

Bit	Name	Description	
15	Adr	Address Function bit. Must be set to a logic 0.	
14	TPEN	Test Pattern Enable.	
		0	Test pattern signal off (normal operation).
		1	Test pattern signal on (picture and sound).
13	N11	N Counter program bits, N11:N6.	
12	N10		
11	N9		
10	N8		
9	N7		
8	N6		

Table 16. Frequency Register (Low-order) Bit Description

Bit	Name	Description
7	N5	N Counter program bits, N5:N0.
6	N4	
5	N3	
4	N2	
3	N1	
2	N0	
1	X5	Test Mode bits, must be set to logic 0 for normal operation. May be used for VHF divider.
0	X4	

The **N Counter** bits determine what UHF frequency is used. **N11:N0** is the binary number of 250 kHz steps in the desired RF_{OUT} frequency F. With:

$$N = 2048 \times \mathbf{N11} + 1024 \times \mathbf{N10} + \ldots\ldots + 4 \times \mathbf{N2} + 2 \times \mathbf{N1} + \mathbf{N0}$$

NOTE:

Programming a division-ratio N = 0 is not allowed.

At power up the modulator will assume a default value for the **N Counter**. The default is determined at time of manufacture and is listed in Table 17 by the orderable part number.

Table 17. Power-On Default Values for N Counter by Orderable Part Number

Orderable Part Number	Frequency	N Counter Value		
		Decimal	Hex	Binary
MC44CC373CAEF, MC44CC373CASEF, MC44CC374CAEF	591.25	2365	0x93D	1001 0011 1101
MC44CC374T1AEF	871.25	3485	0xD9D	1101 1001 1101

The Test Mode bits, **X5:X0**, found in the frequency and control registers, control 15 different test mode states. Only four of these states have an application use. All other states are intended for manufacturing test purposes only.

The test mode states defined by **X2:X0** in Table 18 may be used to operate the modulator in the in VHF range.

It should be noted that operation in the VHF range has a high spurious content due to the digital dividers. Filtering of the RF_{OUT} signal may be required to meet desired performance specifications. Performance data is not provided for VHF operation.

Table 18. Test Modes usable for VHF operation

X5	X4	X3	X2	X1	X0	Description
0	0	0	0	0	0	Normal Operation
0	0	0	0	0	1	RF/2
0	0	0	0	1	0	RF4
0	0	0	0	1	1	RF/8
0	0	0	1	0	0	RF/16
x	x	x	1	x	x	The 11 other test mode states are reserved for manufacturing test purposes.

OPTION CONTROL REGISTER 1 FORMAT

The format for the Optional Control Register 1, OCR1, is shown in Figure 8. Bits **R14:R0** are not defined for system applications. They are for manufacturing test only. **For normal operation these bits must be set to a logic 0.** When UHF oscillator is disabled, do not write to Option Control Register 1 and 2. Any other time, writing to Option Control Registers 1 and 2 is allowed.

MSB															**LSB**	
R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Reset State
1	Reserved for manufacturing test purposes only							Reserved for manufacturing test purposes only								
Adr																

Figure 8. Option Control Register 1 Format

Table 19. Option Control Register 1, Bit Description

Bit	Name	Description
15	Adr	Address Function bit. Must be set to a logic 1.
14-8	—	Reserved for manufacturing test.
7-0	—	Reserved for manufacturing test.

OPTION CONTROL REGISTER 2 FORMAT

The format for the Optional Control Register 2, OCR2, is shown in Figure 9. Bits **R14:R2** are not defined for system applications. They are for manufacturing test only. **For normal operation these bits must be set as defined by the reset state.**

MSB															**LSB**	
R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	
1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	Reset State
1	Reserved for manufacturing test purposes only													PW1	PW0	
Adr														Peak White clip level		

Figure 9. Option Control Register 2 Format

The Peak White Clip level may be set by setting bit PW1 and PW0 as listed in Table 20. The default (power-up) setting is 1.0 volts.

When UHF oscillator is disabled, do not write to Option Control Registers 1 and 2. Any other time, writing to Option Control Registers 1 and 2 is allowed.

Table 20. Option Control Register 2, Bit Description

Bit	Name	Description		
15	Adr	Address Function bit. Must be set to a logic 1.		
14-2	—	Reserved for manufacturing test.		
1	PW1	Peak White Clip level		
		PW1	PW0	Video Modulation Depth for video = 1.4 V_{CVBS}
		0	0	90%
0	PW0	0	1	94%
		1	0	91%
		1	1	92.5%

DATA/STATUS REGISTER FORMAT

The data/status read back format is shown in Figure 10. The first byte contains the status information on the RF oscillator out-of-frequency range and is the same format used by the legacy devices. Therefore, current legacy software will be unaffected as it will only read back this most significant byte.

During manufacturing test, additional two byte registers are read back without sending a stop condition. This read back data has no significance to end system applications. Therefore if it is read by a master, it should be ignored.

The bit description for the status byte is listed in Table 21.

MSB							**LSB**
R7	R6	R5	R4	R3	R2	R1	R0
-	-	-	-	-	Y2	Y1	OOR
Reserved					OSC Status		

Figure 10. Status/Data Register Format

Table 21. Status Byte Bit Description

Bit	Name	Description
R7:R3	-	Reserved
R2	Y1	Frequency Too High / Too Low 0 VCO out of range, frequency too low, only valid if OOR=1 1 VCO out of range, frequency too high, only valid if OOR=1
R1	Y2	Low/High VCO Active 0 High VCO is active 1 Low VCO is active
R0	OOR	UHF Osc Out of Freq. Range 0 Normal operation, VCO in range 1 VCO out of range

CHARACTERIZATION MEASUREMENT CONDITIONS

The default configuration unless otherwise specified:

- Peak White Clip enabled
- UHF oscillator ON
- Sound and video modulators ON
- Sound subcarrier frequency = 5.5 MHz
- Sound Oscillator ON
- Sound PLL reference frequency = 31.25 kHz
- Logic Output Port LOW
- Picture-to-sound carrier ratio = 12 dB
- System L disabled
- Test pattern disabled
- All test mode bits are '0'
- Frequency from channel 21 to 69
- RF Inputs / Output into 75Ω Load using a 75 to 50 Ω transformation.
- Video Input 1Vpp.
- Audio pre-emphasis circuit enabled.

Table 22. Performance Measurement Test Set-ups

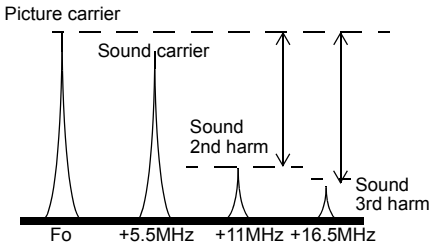
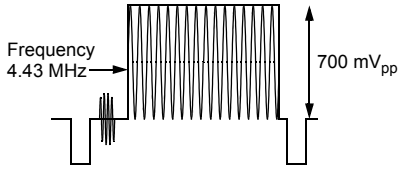
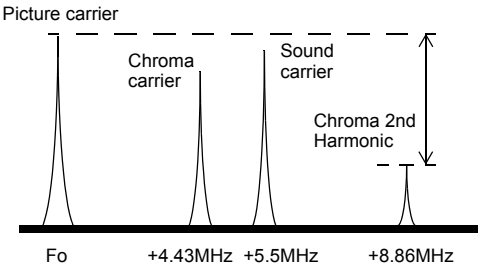
Device and Signals Set-up	Measurement Set-up
RF_{OUT} Output Level	
Video: 10 steps grey scale No audio	Measured picture carrier in dBμV with a Spectrum Analyzer using a 75 to 50 Ω transformation, all cables losses and transformation pads having been calibrated. Measurement used as a reference for other tests: RFout_Ref
RF_{OUT} Output Attenuation	
ATT bit = 1 No Video signal No Audio signal	Measure in dBc picture carrier at **ATT**=1 with reference to picture carrier at **ATT**=0
Sound Subcarrier Harmonics	
Video: 10 steps grey scale No Audio signal	Measure in dBc second and third sound harmonics levels in reference to picture carrier (RFout_Ref). 
Second Harmonics of Chroma Subcarrier	
No audio Video: a 700m $V_{(PP)}$ 4.43 MHz sinusoidal signal is inserted on the black level of active video area. 	Measure in dBc, in reference to picture carrier (RFout_Ref), second harmonic of chroma at channel frequency plus 2 times chroma frequency, resulting in the following spectrum. 

Table 22. Performance Measurement Test Set-ups (continued)

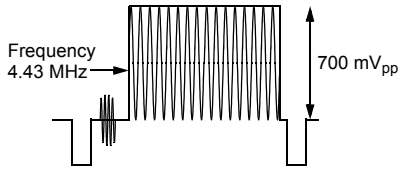
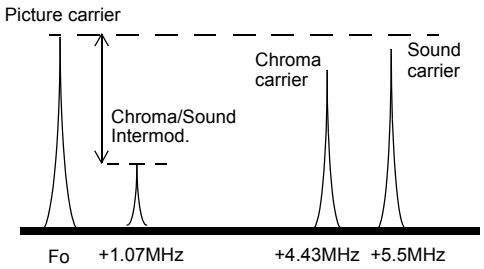
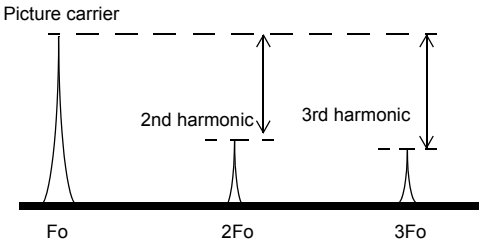
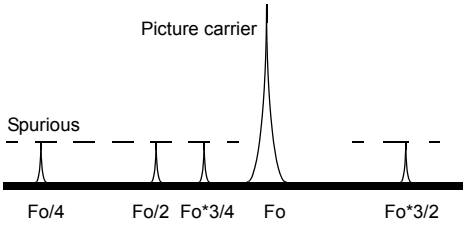
Device and Signals Set-up	Measurement Set-up
Chroma/Sound Intermodulation	
No audio signal Video: 700 $mV_{(PP)}$ 4.43 MHz sinusoidal signal inserted on the black level of active video area.This is generated using a Video Generator and inserting the required frequency from a RF Signal generator. 	Measure in dBc, in reference to picture carrier (RFout_Ref), intermodulation product at channel frequency plus the sound carrier frequency (+5.5 MHz) minus the chroma frequency (–4.43 MHz), resulting in the following spectrum. Intermodulation product is at the channel frequency +1.07 MHz. 
Picture Carrier Harmonics	
No Video signal No Audio signal	Measure in dBc, in reference to picture carrier (RFout_Ref), second and third harmonic of channel frequency, resulting in the following spectrum. 
Out of Band Spurious	
No Video signal No Audio signal	Measure in dBµV spurious levels at 0.25, 0.5, 0.75 and 1.5 times channel frequency, resulting in the following spectrum Measure from 40 MHz to 1 GHz (Fo = 460 - 880 MHz). 

Table 22. Performance Measurement Test Set-ups (continued)

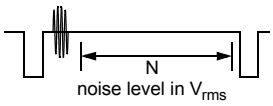
Device and Signals Set-up	Measurement Set-up
In Band Spurious	
No Video signal No Audio signal	Measure in dBc, in reference to picture carrier (RFout_Ref), spurious levels falling into video bandwidth starting from ±100 kHz from the picture carrier up to ±5 MHz.
Video Bandwidth	
No audio Video: 600m $V_{(PP)}$ sinusoidal signal inserted on the black level of active video area.	The Video signal is demodulated on the spectrum analyzer, and the peak level of the 100 kHz signal is measured as a reference. The frequency is then swept from 100 kHz to 5 MHz, and then the difference in dB from the 100 kHz reference level is measured.
Weighted Video Signal to Noise	
Video: 100% White video signal - 1 $V_{(PP)}$. No Audio signal This is measured using a Demodulator in B/G (using a CCIR Rec. 567 weighting network, 100 kHz to 5 MHz band with sound trap and envelope detection, and a Video Analyzer.	The Video Analyzer measures the ratio between the amplitude of the active area of the video signal (700mV) and the noise level in Vrms on a video black level which is show below. Video S/N is calculated as 20 x log(700 /N) in dB. 
Unweighted Video Signal to Noise	
Same as above with CCIR filter disabled.	Same as above.
Video Differential Phase	
Video: 5 step Grey Scale- 1 $V_{(PP)}$. No Audio signal This is measured using a Demodulator in B/G (using a CCIR Rec. 567 weighting network, 100 kHz to 5 MHz band with sound trap, and envelope detection, and a Analyzer.	On line CCIR 330, the video analyzer DP measure consists of calculating the difference of the Chroma phase at the black level and the different chroma subcarrier phase angles at each step of the greyscale. The largest positive or negative difference indicates the distortion. $\text{DIFF PHASE} = \frac{\text{the largest positive or negative difference}}{\text{the phase at position 0}} * 100\%$ The video analyzer method takes the worst step from the first 4 steps.

Table 22. Performance Measurement Test Set-ups (continued)

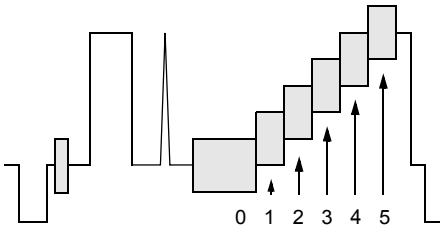
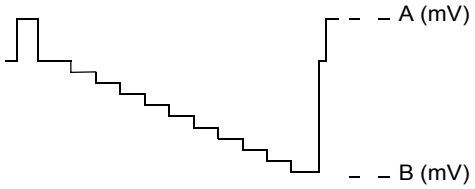
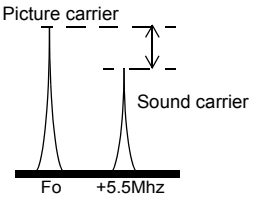
Device and Signals Set-up	Measurement Set-up
Video Differential Gain	
Video: 5 step Grey Scale- 1 $V_{(PP)}$. No Audio signal This is measured using a Demodulator in B/G (using a CCIR Rec. 567 weighting network, 100 kHz to 5 MHz band with sound trap and envelope detection, and a Video Analyzer.	On line CCIR 330 shown below, the video analyzer DG measure consists of calculating the difference of the Chroma amplitude at the black level and the different amplitudes at each step of the greyscale. The largest positive or negative difference indicates the distortion.  5-step greyscale with Chroma, line CCIR330 $\text{DIFF GAIN} = \frac{\text{the largest positive or negative difference}}{\text{the amplitude at position 0}} * 100\%$ The video analyzer method takes the worst step from the first 4 steps.
Video Modulation Depth	
No Audio signal Video: 10 step grey scale	This is measured using a Spectrum Analyzer with a TV Trigger option, allowing demodulation and triggering on any specified TV Line. The analyzer is centred on the maximum peak of the Video signal and reduced to zero Hertz span in Linear mode to demodulate the Video carrier.  TV Line Demodulated by Spectrum Analyzer-BG standard The Modulation Depth is calculated as (A – B) / A x 100 in % Same measurement method for L standard, with inverted video.
Picture to Sound ratio	
No Video signal No Audio Signal **PS** bit set to 0 and 1	Measure in dBc sound carrier in reference to picture carrier (RFout_Ref) for **PS** bit = 0 (PS = 12 dB typical) and for **PS** bit = 1 (PS = 16dB). 

Table 22. Performance Measurement Test Set-ups (continued)

Device and Signals Set-up	Measurement Set-up
Audio Modulation Index - FM Modulation	
Video: Black Sync Audio signal: 1 kHz, 205 mV_{rms}. This is measured using a Demodulator in B/G and an Audio Analyzer at 1 kHz	The audio signal 205 mV at 1 kHz is supplied by the Audio Analyzer, and the FM demodulated signal deviation is indicated on the Demodulator in kHz peak. This value is then converted in % of FM deviation, based on specified standards.
Audio Frequency Response	
Video: Black Sync Audio signal: 50 Hz to 15 kHz, 100 mV_{rms} This is measured using a Demodulator in B/G and an Audio Analyzer.	The audio signal 1 kHz 100 mV_{rms} is supplied by the Audio Analyzer, demodulated by the Demodulator and the audio analyzer measures the AC amplitude of this demodulated audio signal: this value is taken as a reference (0 dB). The audio signal is then swept from 50 Hz to 15 kHz, and demodulated AC amplitude is measured in dB relative to the 1 kHz reference. Audio pre-emphasis and de-emphasis circuits are engaged, all audio analyzer filters are switched OFF.
Audio Distortion FM	
Audio: 1 kHz, adjustable level Video: Black Sync This is measured using a UHF Demodulator in B/G and an Audio Analyzer at 1 kHz. The output level of the audio analyzer is varied to obtain a deviation of 50 kHz indicated on the Demodulator.	The input arms detector of the Audio Analyzer converts the ac level of the combined signal + noise + distortion to dc. It then removes the fundamental signal (1 kHz) after having measured the frequency. The output rms detector converts the residual noise + distortion to dc. The dc voltmeter measures both dc signals and calculates the ratio in% of the two signals. $ADist = (Distortion + Noise)/(Distortion + Noise + Signal)$
Audio Signal to Noise	
Audio: 1 kHz, adjustable level Video: EBU Color Bars This is measured using a Demodulator in B/G and an Audio Analyzer at 1 kHz. The output level of the Audio analyzer is varied to obtain a Modulation Deviation of 25 kHz indicated on the Demodulator.	The Audio Analyzer alternately turns ON and OFF its internal audio source to make a measure of the Audio signal plus noise and then another measure of only the noise. The measurement is made using the internal CCIR468-2 Filter of the Audio Analyzer together with the internal 30 +/–2 kHz (60 dB/decade) Lowpass filters. The demodulator uses a quasi-parallel demodulation as is the case in a normal TV set. In this mode the Nyquist filter is bypassed and the video carrier is used without added delay to effectuate intercarrier conversion. In this mode the phase noise information fully cancels out and the true S/N can be measured. $ASN(dB) = 20 \times \log(Signal + Noise)/(Noise)$

PIN CIRCUIT SCHEMATICS

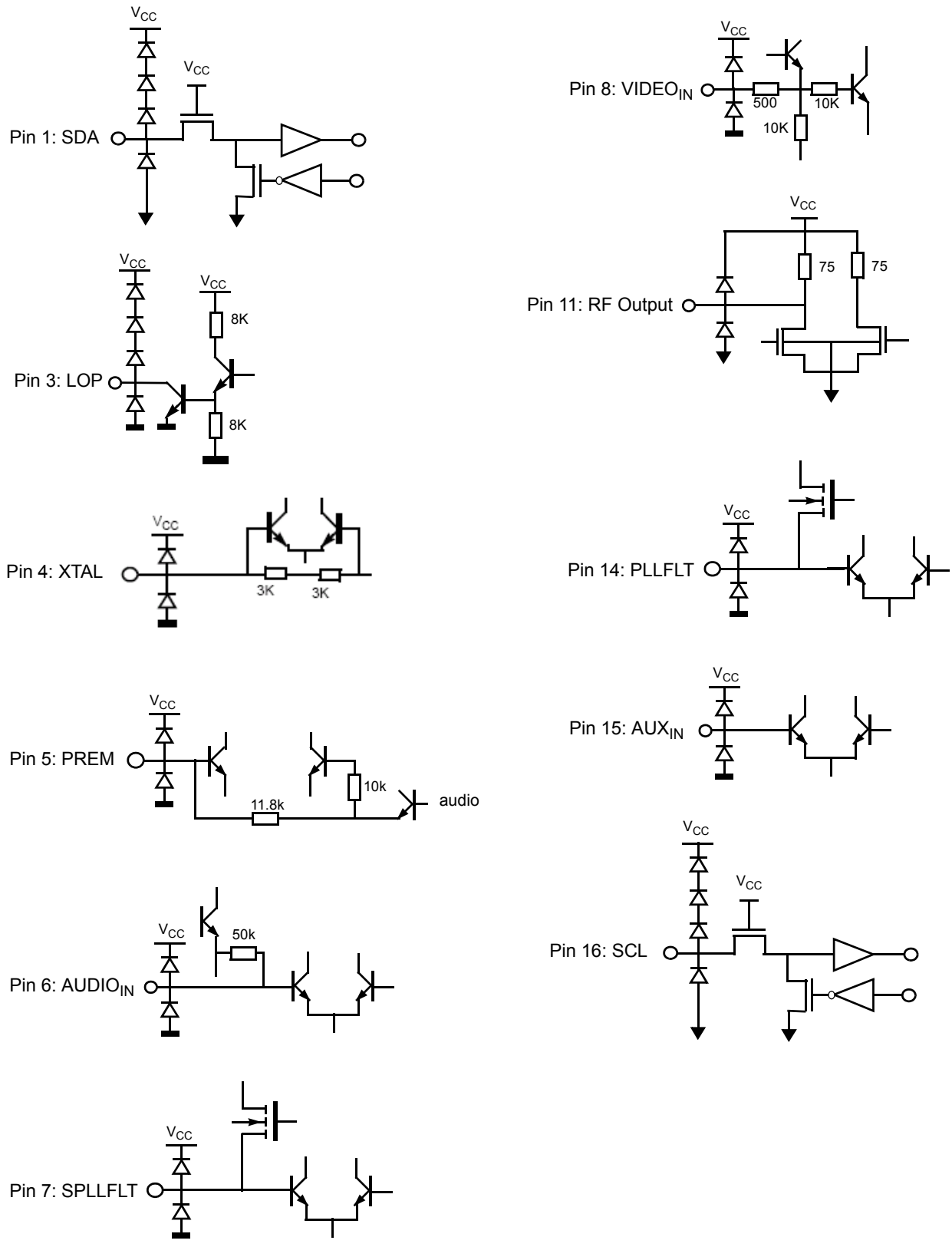


Figure 11. Pin Circuit Schematics

EVALUATION BOARD SCHEMATIC

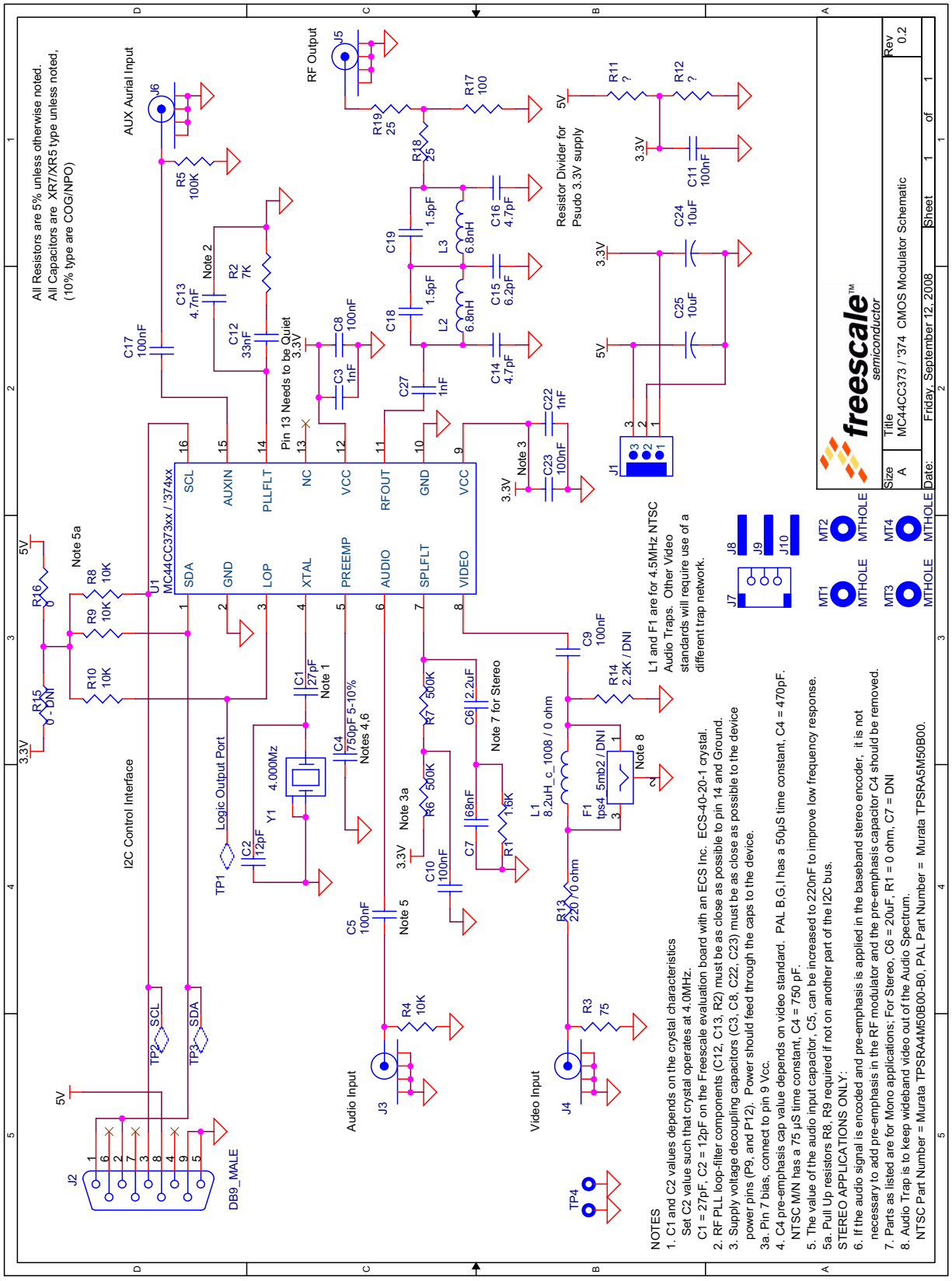
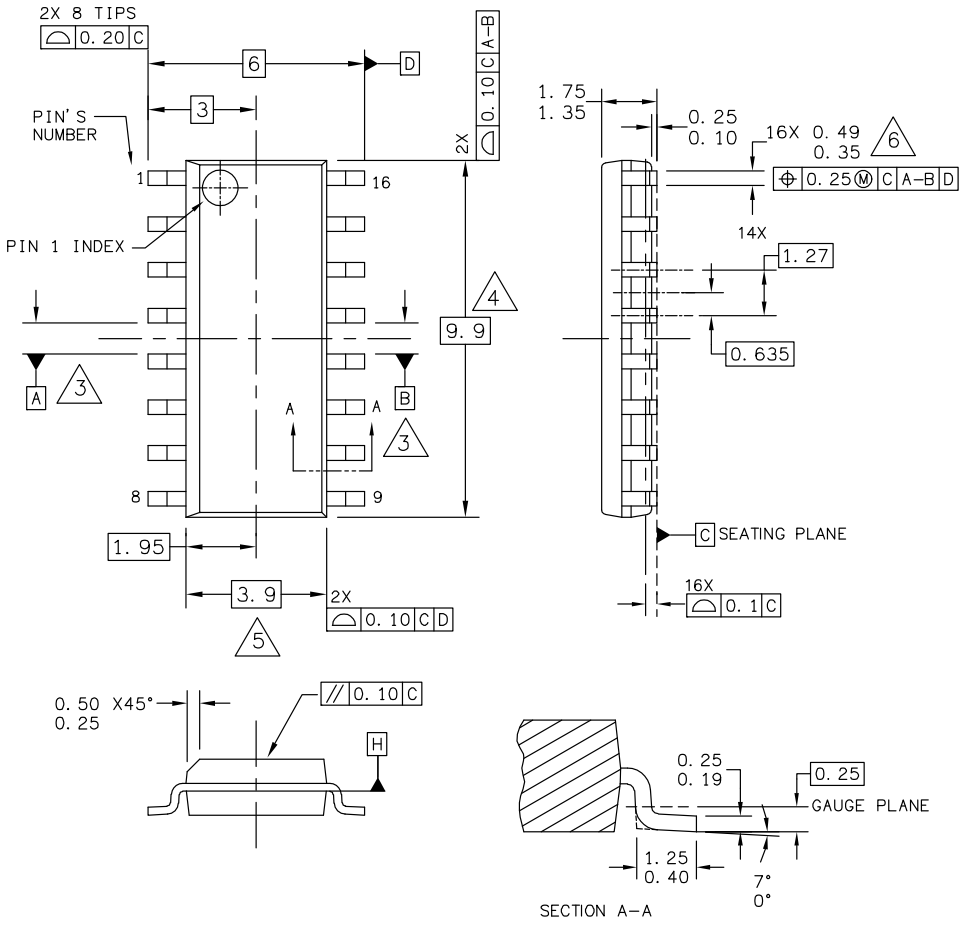


Figure 12. Evaluation Board Schematic

PACKAGE DIMENSIONS



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	CASE NUMBER: 751B-05	06 FEB 2006
	STANDARD: JEDEC MS-012AC	

Figure 13. SOIC-16 Package Dimensions

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.

2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.

3. DATUMS A & B TO BE DETERMINED AT DATUM H.

4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE.

5. THIS DIMENSION DOES NOT INCLUDE INTER–LEAD FLASH OR PROTRUSIONS. INTER–LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.

6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.62 mm.

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	CASE NUMBER: 751B–05	06 FEB 2006
	STANDARD: JEDEC MS–012AC	

Figure 14. SOIC-16 Package Dimensions - continued

PRODUCT DOCUMENTATION

Refer to the following documents to aid your design process.

Application Notes

- To be updated.

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