Features

- **Backscatter-based UHF RFID IC (860 MHz to 960 MHz) Supporting Current and Future Radio Regulations**
- **Support for All Data Structures Defined in ISO/IEC 18000-6, ISO/IEC 15961, ISO/IEC 15963, GS1**
- **Passive Backscatter-communication–based Data Carrier IC**
  - **12 µW RF Power Required for Minimum Communication Feasibility**
- **Memory Programming Possible in Atomic and Global Mode**
- **Programmable Trigger Functionality**
- **PR-ASK/ASK Modulation Combined with Pulse Interval Encoding (PIE) Style in the Forward Direction to Enable Maximum Power Transport Combined with High Blocking Resistance**
- **Short, Long, and Temporary Commands**
- **Synchronous Return Link to Achieve Highest SNR**
- **2PSK for the Backscatter Data Stream to Achieve Highest SNR**
- **Full-duplex and Half-duplex Communication Modes**
- **Several Closed-loop Possibilities to Enable**
  - **Adaptive Speed During Read and Anticollision Procedures**
  - **Fast Programming**
- **Communication Speed 5 Kbits/s to 60 Kbits/s, Fully Controlled by the Reader**
  - **Different Speed Factors Possible in Forward and Return Link**
- **Two Kinds of Anticollision Procedures Implemented**
  - **Deterministic and Slotted Aloha Anticollision Procedure**
  - **Group_selection Commands Supporting =, <, and > Comparisons**
  - **Wake-up Commands**
  - **All Procedures Support 16-bit Random Values for Access Control Mechanisms**
- **No Unique Data Structures are Needed to Enable Both Anticollision Procedures**
  - **Parallel Handling of Different Structures, and Opening of Migration Paths for Private Structures**
  - **Applications in Open Data Systems as well as in Closed Systems**
  - **Maximum ID is Limited Only by the User Memory Space (1024 Bits + 256 Bits)**
- **Both Procedures Also Support Virgin-tag Initialization During Anticollision**
- **High-efficiency Commands to Increase and Adapt Anticollision Speed**

1. Description

ATA5590 is a wireless data carrier IC. The IC is powered by the RF field transmitted by a reader. The carrier frequency is typically in the UHF region. The functionality of the IC is controlled by the reader. The IC returns the required information back to the reader using a backscatter modulation technique; it is a passive UHF transponder device based on the experience of the EU-funded project Palomar (IST1999-10339).

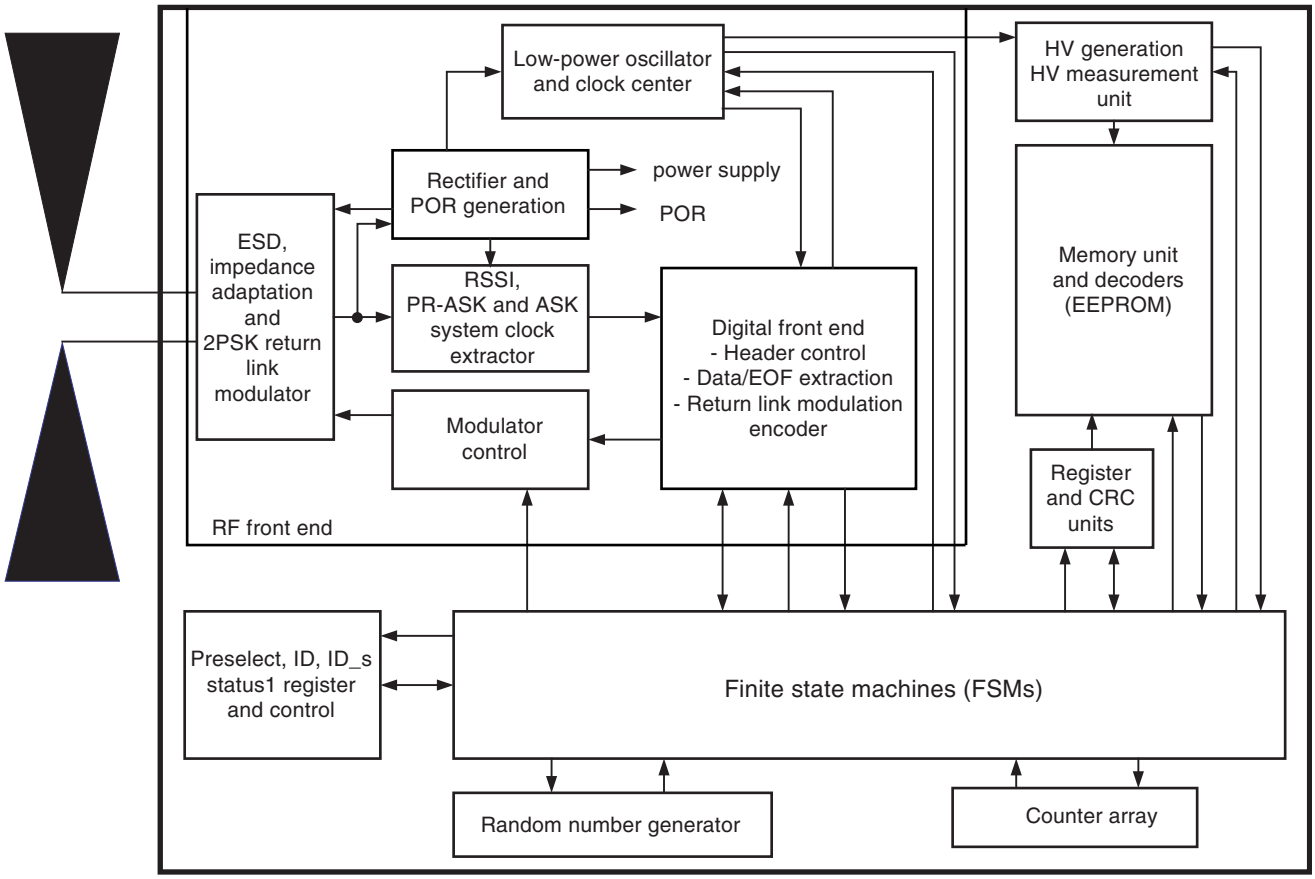
The main challenge for ATA5590 was to enable applications for open data management systems while considering legacy data systems.

1.3-kbit UHF R/W IDIC® with Anti-collision Function

ATA5590 TAGIDU™

4817C–RFID–03/07

Figure 1-1. Block Diagram of the ATA5590



1.1 Parameters of the Link

Table 1-1. Parameters of the RF Link

Parameter	Parameter Value	Comment
Forward link encoding	Pulse interval modulated code	To generate the boundaries between the bits and symbols
Forward link modulation	PR-ASK and ASK	
Forward modulation index m	PR-ASK: 100% ASK: > 80%	
Forward link data rate	5 Kbits/s to 60 Kbits/s	
Forward link bit ordering	MSB first	
Type of communication	Half duplex or full duplex	
Type of command	Short commands Long commands Temporary commands	
Return link data rate	5 Kbits/s to 60 Kbits/s	Independent from forward data rate
Return link modulation	2PSK	To achieve higher SNR and lower BER values than ASK To achieve longer communication distances
Return link encoding for data encoding	FM0 3phase1 NRZI Soft NRZI	Spectrum and edge management during the return link header section controlled by the reader
Error and ready signalling	Sub-carrier OSC / 4 Sub-carrier OSC / 8	Sub-carrier modulation used for error and ready signalling
Return link bit ordering	MSB first	
Return link transmission mode	Synchronous	Including loop functions

Table 1-2. Error Detection and Signalling

Parameter	Description	Comment
Error detection forward link	Header plausibility check 2-bit CRC for command frame 16-bit CRC over the whole frame Bit length check Loop function for CRC Once received, a decoded bit is backscattered in full duplex mode	To be synchronized to the reader, the header_ok check and the command CRC have to be received successfully; then the tag can communicate with the reader
Error detection return link	16-bit CRC CRC length is adaptive, also in loop mode	
Error code during return link	Inside the 8-bit status2 transfer	Data CRC wrong Bit length coding wrong Page locked (for programming)
Error coding if forward CRC was correct but command unknown	Disabling full duplex in the forward direction and sub-carrier (OSC / 4) during the first symbol after EOF1	No error code (status2) is backscattered Tag is silent during return link, and becomes asynchronous to the reader
Error coding if memory address is unknown but command was known.	Sub-carrier modulation (OSC / 4) during the first header symbol of the return link	No error code (status2) is backscattered Tag is silent during the rest of the return link
Error coding if program procedure is failed	Sub-carrier: OSC / 8	Sub-carrier modulation is active until the return link header
Address overflow during deterministic arbitration	Sub-carrier modulation OSC / 4	Sub-carrier is active if the arbitration was started and the arbitration pointer (one bit before the contents is backscattered) is outside the memory

Table 1-3. Anticollision and Memory Parameters

Parameter	Description	Comment
Group management	System supports several group commands incluldingg = ≤ ≥ decisions	The following commands are able to consider group command results
Collision arbitration	Deterministic modified binary tree Aloha	All support non-unique data structures; Deterministic procedures can point to any memory location
Collision management	Deterministic: full duplex communication Aloha: slot based	Single selection of a procedure or a mixture is possible
Slots for Aloha	32 Main slots + Deterministic sub-slots	
Collision arbitration linearity (deterministic)	>> 2^{1286}	
Maximum tag inventory capability		The deterministic-based algorithm is not limited
Maximum size of the memory	1344 bits	
Memory addressing	Blocks of 32 bits Pages of 128 bits	
Protection against overprogramming	Lock bit	One lock bit per page located within the page itself
Tag identifier (Tag_ID)	Default: 96 bits Maximum size: 1270 bits	The memory size is limited only by the max. ID size

1.2 Abbreviations

2PSK	2-state phase-shift keying
AFI	Application family identifier
Ant	Antenna (pad)
ASK	Amplitude shift keying
Clk	Clock
CRC	Cyclic redundancy check
CW	Continuous wave
DSF	Data storage format
DSFID	Data storage format identifier
EEPROM	Electrically erasable programmable memory
EOF	End of frame
EOT	End of transmission
ESD	Electrostatic discharge
Forward link	Reader to tag communication, to transport the command and the parameters
GND	Ground (potential on-chip)
ID	Identifier
ID_s	Identified and silent (internal status information of the tag)
I/O	Input and output (pad)
HBM	Human body model (ESD characteristic)
LSB	Least significant bit
MHz	Megahertz
MSB	Most significant bit
NRZ	No return to zero
NRZI	No return to zero inverted
PR-ASK	Phase reversal–Amplitude-shift keying
	The phase of the carrier is switched by 180° to generate a boundary signal for a symbol
Pre	Pre_select (status information)
PIE	Pulse interval encoding
Return link	The time after the tag has received a command and its parameters
RF	Radio frequency
RFID	Radio frequency identification device
RFU	Reserved for further use
RTF	Reader talks first
Trigger	Trigger signalling
TTF	Tag talks first
VDD	Supply voltage (on-chip)

2. Overview

2.1 Pinning

Figure 2-1. Pinning TSSOP10

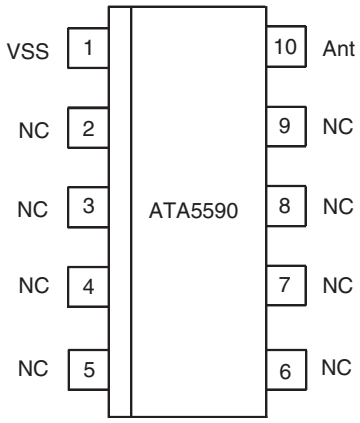


Table 2-1. Pin Description

Pin	Symbol	Function
1	VSS	Antenna_gnd
2	NC	Not connected
3	NC	Not connected
4	NC	Not connected
5	NC	Not connected
6	NC	Not connected
7	NC	Not connected
8	NC	Not connected
9	NC	Not connected
10	Ant	Antenna

Figure 2-2. Pin Configuration of ATA5590 at Die Level

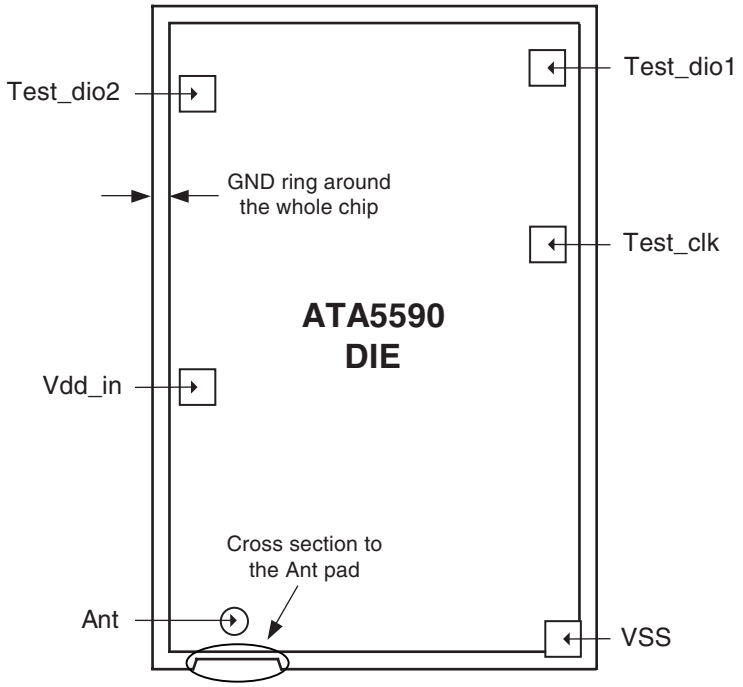
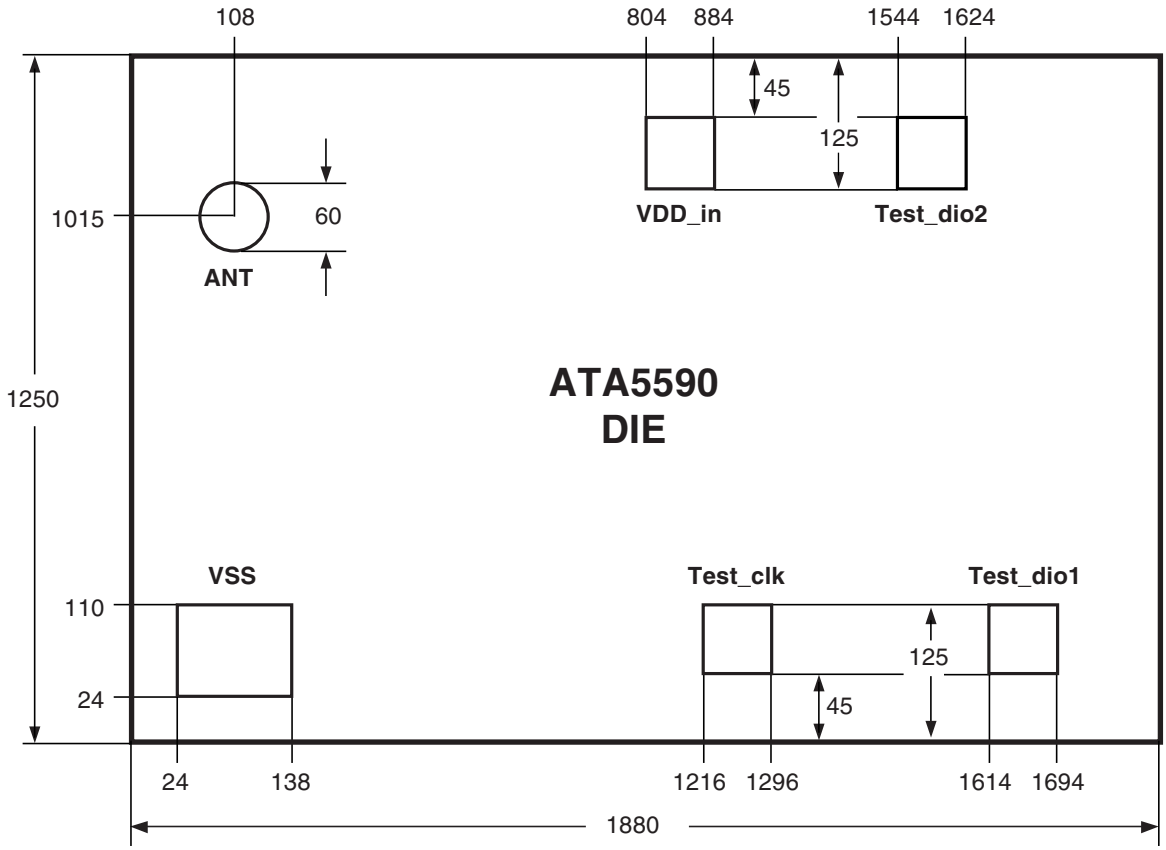


Table 2-2. Pads at Die Level

Pad	Function	Physical Construction	Comment
Ant	Antenna	RF in	Diameter of opening 60 µm
VSS	Antenna_gnd	RF Ground	
VDD_in	Test pad	Output	VDD after the rectifier
Test_Clk	Test clock in	Input	Notch input
Test_dio1	Test pad	In/out open drain	For control and observation
Test_dio2	Test pad	In/out open drain	For control and observation

Figure 2-3. The Pad Coordinates



2.2 Main Parameters of the Die

Table 2-3. Main Frequency-independent Parameters at 25°C

Parameter	Condition/Comment	Typical	Value
Shortest PIE time	To define a “0”	8 + notch time	µs
Longest PIE time	To define EOF	88 + notch time	ms
Storage time of status bits: pre_select, ID, ID_s	Without external power, 1.3V, 25°C	8	s
Programming time[1]	2V VDD, 32 bits t = 0 for this special case	9 + t	ms

Note: 1. Timing calculation is based on an oscillator frequency of 420 kHz. The timing value of t depends on the RF field strength, and will be dynamically adjusted.

Table 2-4. Main Frequency-dependent Parameters at 25°C and 868 MHz

Parameter	Condition/Comment	Typical	Value
Input impedance[1, 2]	11 µW RF power, modulation state 1	6.7 – j216 (6970 – j216)	Ω
	Modulation state 2	6.1 – j202 (6695 – j202)	Ω
Input impedance[1, 2]	25 µW RF power, programming	12.3 – j217 (3840 – j217)	Ω

Notes: 1. For packaged parts, the imaginary part decreases as a function of the housing and bonding technology.

2. Impedance is calculated as a series impedance of R and C. Values in () are the values for an equivalent parallel circuit.

Table 2-5. Main Frequency-dependent Parameters at 25°C and 915 MHz

Parameter	Condition/Comment	Typical	Value
Input impedance[1, 2]	12 µW RF power, no modulation state 1	6.9 – j205 (6097 – j205)	Ω
	Modulation state 2	6.4 – j191 (5706 – j191)	Ω
Input impedance[1, 2]	26 µW RF power, programming	10.3 – j191 (3552 – j191)	Ω

Notes: 1. For packaged parts, the imaginary part decreases as a function of the housing and bonding technology.

2. Impedance is calculated as a series impedance of R and C. Values in () are the values for an equivalent parallel circuit.

Table 2-6. Main Frequency-dependent Parameters at 25°C and 960 MHz

Parameter	Condition/Comment	Typical	Value
Input impedance[1, 2]	13 µW RF power, modulation state 1	6.6 – j196 (5827 – j196)	Ω
	Modulation state 2	6.1 – j182 (5436 – j182)	Ω
Input impedance[1, 2]	27 µW RF power, programming	9.7 – j182 (3424 – j182)	Ω

Notes: 1. For packaged parts, the imaginary part decreases as a function of the housing and bonding technology.
2. Impedance is calculated as a series impedance of R and C. Values in () are the values for an equivalent parallel circuit.

Table 2-7. Main Frequency-dependent Parameters at 25°C and 2450 MHz

Parameter	Conditions/Comment	Typical	Value
Input impedance[1, 2]	49 µW RF power, modulation state 1	4.0 – j84.8	Ω
	Modulation state 2	3.8 – j79.2	Ω
Input impedance[1, 2]	85 µW RF power, programming	4.6 – j85	Ω

Notes: 1. For packaged parts, the imaginary part decreases as a function of the housing and bonding technology.
2. Impedance is calculated as a series impedance of R and C. Values in () are the values for an equivalent parallel circuit.

2.3 Functional Changes and New Features Relative to ATA5590 Version 1

Table 2-8. ATA5590 Version 1 Errata Fixed in this Version

Function Level	Short Description
Modulation coding FM0	The modulation now changes at each bit boundary.
Selected access mode during deterministic anticollision	If the tag is selected by a group select command which was sent before an anticollision command, the anticollision command will now based on this selection. The read and program commands which follow will not; they wil be based only on the selection of the arbitration result.
Test pads' behavior	Both I/O pads are now usable in both directions.

3. Memory

ATA5590 is a wireless data carrier IC with a UHF carrier and backscatter-based link mechanism. Data is stored in an EEPROM, and the content is under the control of manufacturers and the end user.

ATA5590 contains an EEPROM to store a Tag_ID, system-related information, and user-controllable data. The memory access is controlled by commands transmitted by the reader. Additionally, the manufacturer area is controlled by a security mechanism which is destroyed after sawing.

The memory itself is split in 2 parts:

- The user memory (1 Kbit)
- The control memory (320 bits) containing the Tag_ID and other sequences such as AFI, DSFID, etc.

ATA5590 does not protect data against reading but does protect against overwriting. To protect data against reading, the user should use encryption. For decryption, the user could use, for example, the user-controlled system information page (control memory) to store a pointer to an external device or memory to retrieve the key and the information regarding the algorithm used over a secure connection.

The memory is organized in pages of 128 bits. Each page is organized in blocks of 32 bits. For programming, each block must be programmed separately. The page is protected against overwriting by a lock bit which is located at the MSB position (bit 31 of page 3). Therefore, the lock bit should be set in an additional step or as the last command during the programming of a page.

The system memory supports:

- A Tag_ID page, which can also be related to an object to which the tag is attached
- A user system-information page
- Two manufacturer system-information blocks

3.1 Tag_ID Page

Some short commands address the Tag_ID page automatically. In the default configuration, the Tag_ID is used to create a link between the tag and, for example, an item. Nevertheless, the user is free to store such an ID at other locations of the memory as well. The following description applies to the default configuration.

The Tag_ID and the type of the ID construction shall be programmed before using the tag in the application. During programming, it can be locked against over-programming. After locking, the Tag_ID is a fixed value. Nevertheless, it is also possible to program virgin tags one by one out of a bulk arrangement by using the separation ability of the anticollision procedure.

The length of the ID depends on the type (structure definition) of the ID. By default, a 96-bit field is reserved (ID page) plus an 8-bit value to define the structure of the ID (DSFID).

The Tag_ID is located in the system memory area, and can be addressed directly (control memory page address 0) or via the symbolic address 0h.

If more than 96 bits are needed, the user is free to store the rest of the structure in the user memory, because deterministic anticollision and group-selection routines are able to include the neighbor pages of the ID page (user memory) in the arbitration frame.

3.1.1 AFI Identifier

The Application Family Identifier (AFI) supports a common group-selection mechanism. It is an 8-bit value. The structure and the function are described in ISO 18000-6, and based on ISO/IEC 15962.

The AFI frame shall be used as a low-level hierarchical selection mechanism to separate RF tags. ATA5590 supports this mechanism as a first group-selection mechanism, including a joker mechanism. Therefore, the reader can select a tag using this special family structure code. The joker mechanism is based on the value 00h. If this code is received by the tag, it is selected automatically.

3.1.2 DSF Information

The data storage format is defined within an 8-bit value. The structure is defined in ISO/IEC 15962 section 7.2.5.

Table 3-1. Storage Schema of the DSF Information

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Access method		RFU	Data format				

Numbering of the access method is defined in ISO/IEC 15961, section 7.1.2.4. The data structure describes a method, whether or not there is a directory structure on-chip, or how the data is organized.

The first 13 values for the data format are described in ISO/IEC 15961, section 7.1.2.5.
The DSFID is a special output of this common definition, describing only the Tag_ID structure.

The DSFID information links the data format on a one-to-one basis with the AFI structure, which enables higher-level and lower-level selection processes.

3.1.3 DSFID

ATA5590 supports a DSF mechanism according to ISO/IEC 15962 and ISO/IEC 15961 to define the structure of the ID (DSFID). The 8-bit value is stored by default in the lower byte of the upper block of the Tag_ID page.

3.1.4 Default Storage Scheme for the Tag_ID Page

Different Tag_ID structures are supported by ATA5590. These structures can be defined by the DSFID information. Arbitration, non-unique and private structures are also supported.

ATA5590 supports anticollision procedures which are based on this Tag_ID, whereas the default anticollision procedure starts with the DSFID information.

The Tag_ID is stored in a 128-bit page of the control memory at page address 00h. It can also be addressed by a symbolic addressing mechanism (symbolic address 0h). The MSB of the Tag_ID is located at the MSByte of block 2. In some cases, it contains the header information of the Tag_ID.

The Tag_ID, the AFI, and the DSFID values have to be set via the system provider or in cooperation with the label or IC manufacturer, and can be protected by a lock bit. The default structure of the ID page is shown in Table 3-2 on page 14:

Table 3-2. Default Construction of the Tag_ID Page

Block/Bit	31:24	23:16	15:8	7:0
3	Administration	7:0 RFU	7:0 AFI	7:0 DSFID
2	Upper byte of ID			
1				
0				Lowest byte of ID

For private structures or for structures of closed data systems, the structure can be changed. It is also possible to use other sizes for the ID.

Notes:
1. When using Aloha commands, only this ID page is supported.
2. Deterministic-arbitration commands can point to any memory address. Also, it is possible to support an expanded size of the ID for arbitration
3. In the case of large ID values (for example, license plate applications), it is recommended to start the ID within the ID page. The other values are stored then in the user memory (page address 7, 6, 5, etc.), because the addressing mechanism during deterministic arbitration is based on an auto-increment function. Then, only the lock bit function of each page must be considered.

The administration byte is defined as:

Table 3-3. Recommended Construction of the Administration Byte of the Tag_ID Page

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Lock_ID page	Private	DSFID_nAC	DSFID_ISO	AFI	DSFID	LID	CRC

- Lock_ID page: Locks the whole page. No change of the page is possible after setting this bit to 1.
- Private: If set to “1”, custom structure and flags will be used. If set to “0”, the flags defined here will be used.
- DSFID_nAC: If set to “1”, DSFID information is stored at byte 0 of block 3. If set to “0”, the Allocation Class information is stored at byte 0 of block 3.
- DSFID_ISO: If set to “1”, the DSFID coding structure is not in line with ISO15962 regulations (only 00 to 0B are currently defined by ISO)
- DSFID: Indicates if the DSFID information is stored in the Tag_ID page. The contents are stored at byte 0 or byte 2, depending on DSFID_nAC.
- AFI: Indicates that the AFI is stored in the Tag_ID page. The construction of AFI corresponds with ISO 18000-6 FDIS
- LID: Indicates that a Tag_ID has a size longer than 96 bits. The other bits are stored in page 7,6, etc. of the user memory, as required.
- CRC: Indicates that a CRC value is supported. The CRC value can be stored after the administration part (byte 2) if the location is not used for storing the DSFID value.

Notes:
1. The anticollision and group-selection procedures of ATA5590 support AFI as well as the ID_type (DSFID) information.
2. The tag manufacturer can program and lock the Tag_ID page.
3. The lock bit function is hard-wired in ATA5590. All of the other bits are recommended.

3.1.5 ID_type Coding

The ID_type is an 8-bit value defined according to the DSF information in ISO/IEC 15962. Therefore, the ID is defined by the lower 5 bits of the DSFID information. The codes for the different ID structures are defined as:

- 00 to 0B reserved by ISO/IEC 15961 (see section 7.1.2.5 of ISO/IEC 15961 and 7.2 of ISO/IEC 15962)
- 0C to 1F: RFU

Code 00 enables migration paths for private or closed-system numbering systems.

Note: As the anticollision commands support an auto decrement function of the memory address, the ID can have more then 96 bits. The other information may then be located at address 1F, 1E, etc.

3.2 User System Information Block

The second page of the system memory is available for private system management indication. This page is in the system memory at page address 1. The symbolic address is 1h.

After sawing, the MSByte of the upper block can be programmed using an OTP mechanism. The MSB is the lock bit of the three lower blocks of the page. The MSBlock of this page will not be locked against programming (except the upper byte of this block, which is OTP). Therefore, the user can use the three lower bytes of the upper block for changeable data such as the packaging level information, a CRC, etc.

To protect the three lower blocks of the page against over programming, the lock bit must be set. The user system information can be read out by read32c or read128c commands, or by using the get_system informational command.

3.3 Manufacturer System Information

Information regarding the functionality of the chip and other reference data is stored in the manufacturer system information blocks.

This information is stored in the system memory area of the EEPROM, and can be read out directly by a get_system command. Programming is possible during wafer test. After sawing, only the 8th byte can be reprogrammed by using a sequence of arbitration and prognbyte commands. The physical page address is 2h, as is the symbolic address.

The system information is split in 8 bytes (64 bits)

3.3.1 Manufacturer System Information Byte 8

Table 3-4. Manufacturer System Information, 8th Byte

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Trigger_en	Trigger(0)	RFU	RFU	RFU	RFU	RFU	RFU
0	0	0	0	0	0	0	0

Trigger_en = “1” indicates that the trigger function is selected

Trigger(0) defines the frequency of the sub-carrier:
“0” = OSC / 4
“1” = OSC / 8

The definition of the following bytes is reserved for further use, based on the described protocol mechanism.

3.4 Memory Organization Summary

Table 3-5. System Memory

Logical Address	Block Address	Byte3 31	30	29	28	27	26	25	24	Byte2 23	22	21	20	19	18	17	16	Byte1 15	14	13	12	11	10	9	8	Byte0 7	6	5	4	3	2	1	0
2	1	Manufacturer System Info – 8th byte								Manufacturer System Info – 7th byte								Traceability Data Structure – 6th byte								Traceability Data Structure – 5th byte							
		Trigger_en	Trigger(0)	RFU	RFU	RFU	RFU	RFU	RFU	TAG TYPE	TAG TYPE	TUNE	IC Rev. Nr.	IC Rev. Nr.	LotID Character	LotID Character	LotID Character	LotID Character	LotID Character	LotID Number	LotID Number	LotID Number	LotID Number	LotID Number	LotID Number	LotID Number	LotID Number	LotID Number	LotID Number	LotID Number	LotID Number	LotID Number	LotID Number
										0h		0	0h		LC#			LC#		LotID #						LotID #							
	0	Traceability Data Structure – 4th byte								Traceability Data Structure – 3rd byte								Traceability Data Structure – 2nd byte								Traceability Data Structure – 1st byte							
		RFU	RFU	TUNE	CRC5	CRC5	CRC5	CRC5	CRC5	LotID Number	LotID Number	LotID Number	Wafer Number	Wafer Number	Wafer Number	Wafer Number	Wafer Number	Die Number	Die Number	Die Number	Die Number	Die Number	Die Number	Die Number	Die Number	Die Number	Die Number	Die Number	Die Number	Die Number	Die Number	Die Number	Die Number
		0h		0	Crc5#					LotID #			Wafer #					die on wafer #								die on wafer #							
1	3	User System Info - Admin								User System Info								User System Info								User System Info							
		Lock Bit (User sys.)																															
	2	User System Info								User System Info								User System Info								User System Info							
	1	User System Info								User System Info								User System Info								User System Info							
	0	User System Info								User System Info								User System Info								User System Info							
0	3	ADMIN								RFU								AFI (ISO/IEC15962) [1]								DSFID (ISO/IEC15962)							
		LOCK ID PAGE	PRIVATE	DSFID_nAc	DSFID_ISO	AFI	DSFID	LID	CRC									ApplicationFamily	ApplicationFamily	ApplicationFamily	ApplicationFamily	ApplicationFamily	ApplicationFamily	ApplicationFamily	ApplicationFamily	AccessMethod	AccessMethod	RFU	DataFormat	DataFormat	DataFormat	DataFormat	DataFormat
	2	Upper Byte ID																															
		ID	ID	ID	ID	ID	ID	ID	ID	ID	ID	ID	ID	ID	ID	ID	ID	ID	ID	ID	ID	ID	ID	ID	ID	ID	ID	ID	ID	ID	ID	ID	ID
	1	ID	ID	ID	ID	ID	ID	ID	ID	ID	ID	ID	ID	ID	ID	ID	ID	ID	ID	ID	ID	ID	ID	ID	ID	ID	ID	ID	ID	ID	ID	ID	ID
	0																									Lower Byte ID							
		ID	ID	ID	ID	ID	ID	ID	ID	ID	ID	ID	ID	ID	ID	ID	ID	ID	ID	ID	ID	ID	ID	ID	ID	ID	ID	ID	ID	ID	ID	ID	ID

ProgNbyte (tag must be selected)
Blocked after sawing
Can be locked (when locked it can't be reprogrammed) - OTP mechanism

[1]: List of Application Family Identifiers are defined in ISO/IEC 15961.

Table 3-6. User Memory

Logical Address	Block Address	Byte3						Byte2						Byte1						Byte0											
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
7	3	Lock Bit(1)																															
	2																																
	1																																
	0																																
:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
0	3	Lock Bit(1)																															
	2																																
	1																																
	0																																

Notes: 1. Page can be locked (when locked it can't be reprogrammed) - OTP mechanism

2. Whole page usable for expanded ID

4. Communication

4.1 Default Operation Basics

Communication between the reader and the tag is based on the reader talks first (RTF) principle. When a tag receives modulation ticks from the reader, the stream is checked by several mechanisms. If they all result in a valid status, the tag becomes synchronous to the stream and the tag is ready to communicate.

Communication always starts with a forward message (reader to tag). ATA5590 supports full duplex communication during the forward link after becoming synchronous to the reader. Therefore, the reader can check on-the-fly whether the tags have received the right values.

The tag answers by backscattering a message back to the reader (return link).

The messages are covered by a CRC.

The backscatter mechanism is based on 2PSK modulation, which means that the tag changes the imaginary part of the input impedance as a function of the data stream and the selected encoding. This modulation type offers maximum robustness against noise combined with minimum influence on supply voltage generation.

4.2 Status Registers

ATA5590 has two status registers.

- Status1, which represents the selection status and
- Status2, which represents the communication status

Status1 contains the result of the arbitration procedure (Aloha-based or anticollision and group-selection status), and status2 contains the communication results.

4.2.1 Status1 Register

Status1 is a special register; the contents of the register are persistent for 8 seconds at 25°C after RF power is lost. The register will be refreshed by the POR mechanism.

Note: The persistence time is a function of the temperature. A common attribute of CMOS technologies is that the leakage current changes by a factor of 2 for every 9°C. The leakage current is the main influence on the storage time.

- Pre_select: A “1” indicates that the tag was previously selected by a group-selection command. It can be set and reset by group-selection commands. A reset is also possible using the reset command.
- ID: A “1” indicates that the tag has currently won a deterministic arbitration via deterministic anticollision commands. It can be reset by group-selection commands (group condition is no longer true) or by the reset command.
- ID_s: A “1” indicates that the tag, which has won arbitration before, will now be silent because it was detected, or, in the case of a deterministic selection procedure, it has received a new anticollision command. The bit can be reset by the reset command.

Table 4-1. Contents of Status 1 Register

GENERALLY	Indicates or stores the selection status of the IC (ALOHA, deterministic anticollision or group select)
Pre-select	“1b” indicates that the reader was detected before by a group select command
ID	“1b” indicates that the tag has won the arbitration (deterministic anticollision)
ID_s	“1b” indicates that the tag which has won the arbitration and detected before, shall now be silent (during deterministic- and ALOHA arbitration the flag is set after detecting and by following of a new arbitration command - ALOHA- or a deterministic arbitration command).

Table 4-2. Typical Storage Time of a Logical “1” in Status1 Register at Different Temperatures

Temperature	**–47°C**	**–29°C**	**–11°C**	**7°C**	**25°C**	**43°C**	**61°C**
Storage time [s]	2048	512	128	32	8	2	0.5

4.2.2 Status2 Register

Register status2 gives an overview of the status of communication. It is part of a backscattered message during program commands and read commands.

Table 4-3. Contents of Status2 Register

Index	Read Commands	Program Commands
7	Pre_select	Pre_select
6	ID	ID
5	Lock protected	Lock protected
4	1	1
3	Bit length not ok	Program_ok
2	Aloha	Aloha
1	CRC wrong	CRC wrong
0	0	0

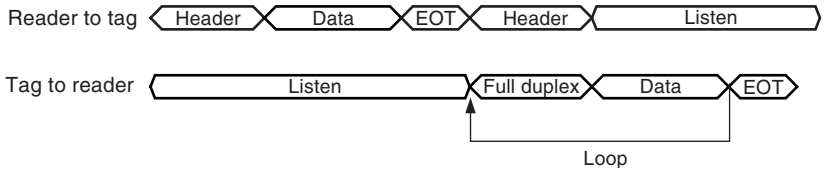
4.3 Frame Concept

Communication is based on the following frames:

- A header frame for timing adjustments
- A data frame to transport the data (Forward: reader to tag, and Return: tag to reader)
  - In the forward direction, the data frame contains the command, the parameters, the CRC value, and, if necessary, the address vectors and the data for programming. The length of the data frame depends on the command and the selected addressing mechanism.
- In the return link, the data frame contains the required data, if possible, and, as a function of the command, the status2 information. A CRC is also part of the data frame.
- An end of transmission (EOT) frame to mark the end of the forward or return link.

These three frames are elementary parts of the forward and return links.

Figure 4-1. Frame Ordering During the Default Communication



During the header it is possible to work in full duplex mode to optimize the link. Under control of the reader, the return link can operate in a loop until the reader sends an EOT frame.

The return link is arranged as a synchronous link. The reader transmits the boundaries of the bit by sending notches to achieve higher SNR. The maximum time for this bit as well as the spectrum of the backscattered bit shall be adjusted by the reader by tuning the return link header.

4.4 OSI1 Layer Concept

To enable communication in even the worst environments, ATA5590 supports the following options:

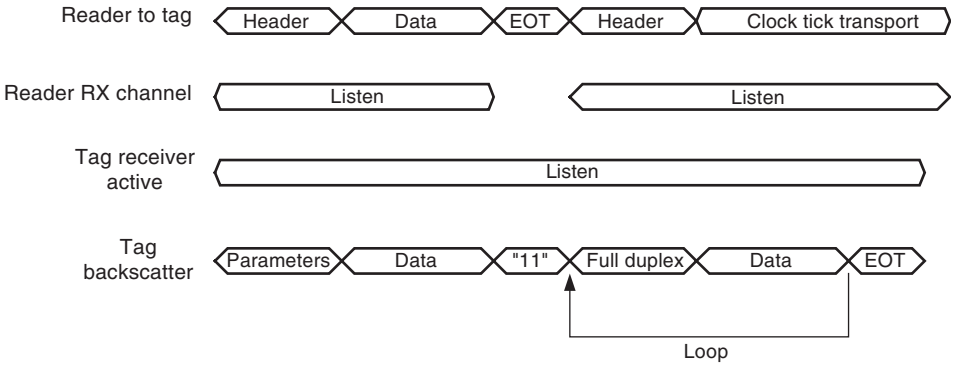
- The reader transmits clock ticks to the tags in the RF field. The clock tick receiver circuit tolerates ticks generated by PR-ASK or ASK (m > 0.8) mechanisms. PR-ASK combines high SNR, a good power transport mechanism, and a lower frequency spectrum compared to ASK ticks. Therefore, PR-ASK guarantees robustness against noise and blocking from other RF sources, as well as reliability.
- The time for a notch is not part of any timing calculation, enabling power savings and guaranteeing flexibility with regards to different spectrum requirements.
- The forward coding is based on a Pulse Interval Encoding (PIE) style.
- The forward baud rate and the rules to distinguish between “0”, “1”, and EOF symbols are transmitted during a header section by the reader.
- The return link operates synchronously. As the reader can control the speed and the modulation ticks of the synchronous return link, this link type has a higher SNR than an asynchronous link.
- The return link is based on a 2PSK modulation, which means that the imaginary part of the input impedance changes mainly. This has a positive influence on supply voltage for the tag IC, and also on the tolerated noise floor of the system.
- The timings of the return link are based on a header section in the beginning of the return link. During this header section, the reader transports timing information, which is used in the return link.
- ATA5590 supports static and dynamic modulation coding techniques to backscatter data. The dynamic coding style is able to shift the modulation edges to get a better spectrum or to shift the edge away from the synchronization tick.
  - Static modulation coding: NRZI coding
  - Dynamic modulation coding:
    - Soft NRZI coding
    - FM0 coding
    - 3phase1 coding

The baud rate is fully controlled by the reader by adjusting the timings in the header section of the forward and the return header. The baud rate can be adjusted between 5 Kbits/s and 60 Kbits/s.

ATA5590 operates in the following communication modes

- Half duplex communication
  - During the forward link if the synchronous condition is not valid
- Full duplex communication
  - During the forward link if the synchronous condition is valid
  - During the deterministic-arbitration process
  - During the return link

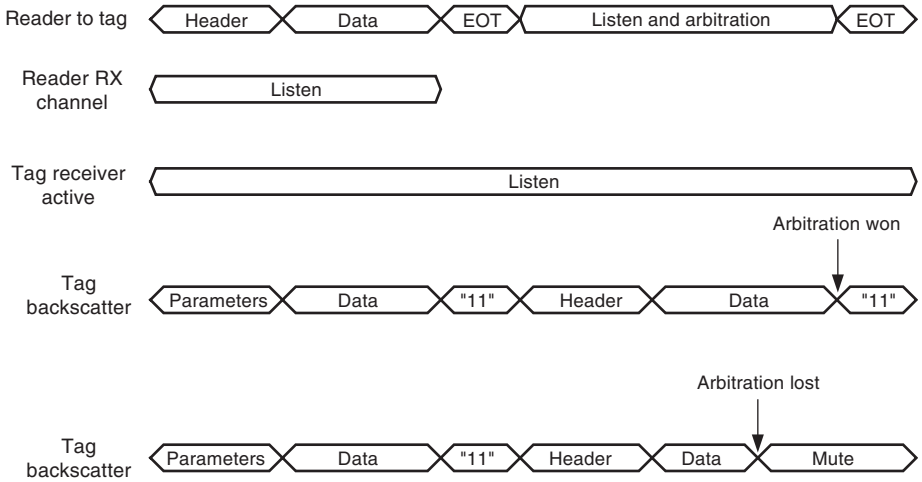
Figure 4-2. Default Full Duplex Communication Principle



During the data section of the forward stream, the tag backscatters the decoded value of the received data back to the reader.

This enables the reader to control the quality of the link. It also enables the reader to check if the tag has received the right message. If the reader detects an error, it stops the transmission directly by sending the stop code or by remaining silent for a specific time (programmable watchdog). Then the tag becomes asynchronous to the link, and the reader can tune the link by tuning the transport parameters via the header section of the forward link.

Figure 4-3. Communication During Deterministic Arbitration



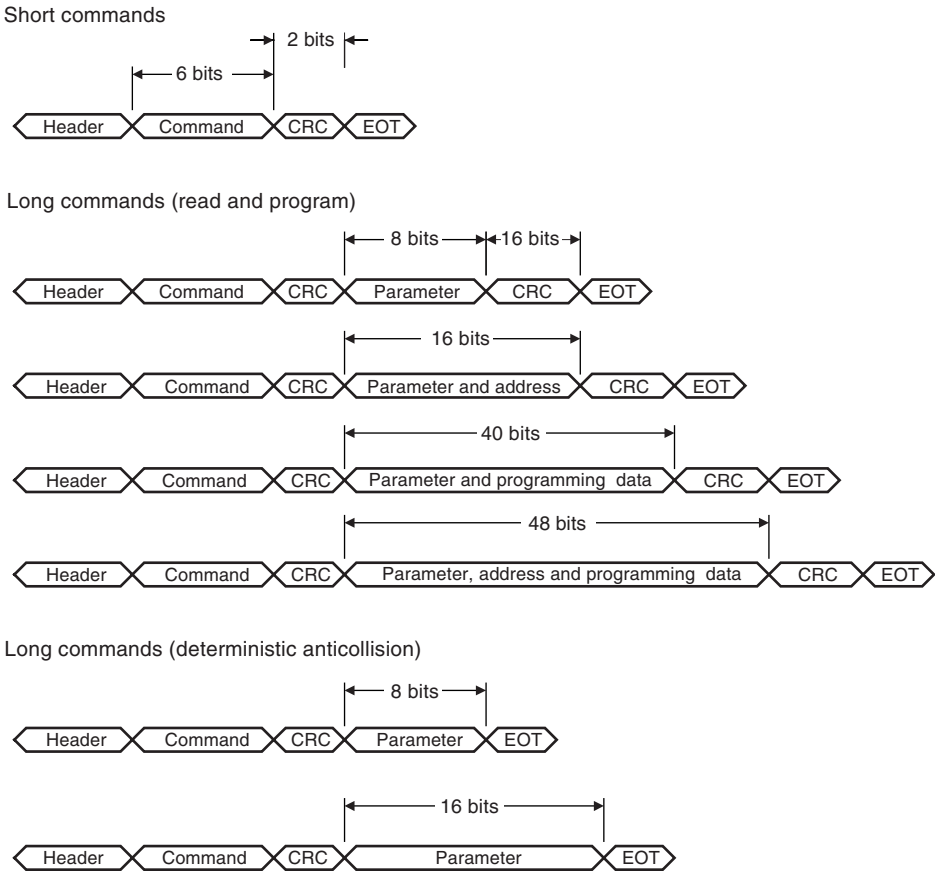
During the deterministic anticollision procedure, full duplex communication is used.

4.5 Default Frames of the Forward Link Stream

The basic protocol contains the following elements:

- A forward header to define the boundaries of the data encoding transmitted by the reader.
- A data frame containing the command and its CRC, data setting parameters, address information, and data for programming. The encoding of the data frame is based on the boundary setting made during the header.
  - Short commands are based only on the 6-bit command code and its 2-bit CRC.
  - Temporary commands are short commands which are not stored in an on-chip command register. They are only used to repeat the former command if possible.
  - Long commands consist, at least, of the command frame, its CRC, and the parameter field.
- A 16-bit CRC frame if a long command was transmitted. In the case of deterministic anticollision commands, the 16-bit CRC field is not part of the forward link because the CRC result is the start value for the CRC of the return link.
- An EOT frame which is based on 2 EOF (end of file) symbols.

Figure 4-4. Default Forward Frames



Note: The speed of the deterministic anticollision procedure can be increased by combining the long commands with the short repeat_arb command.

4.6 Use of the Random Number Generator

ATA5590 supports several commands where the execution or the return link contents is based on random effects. Therefore, a random number generator is implemented on the ATA5590 chip.

Random effects are used

- To calculate a 5-bit slot number and/or an 8-bit random value, which is backscattered during the Aloha-based arbitration
- To calculate a 4-bit slot number for the answering mechanism triggered by the wake-up commands
- To calculate an 8-bit random value for the deterministic arbitration, if required

Therefore, ATA5590 supports non-unique data structures for each arbitration procedure.

4.7 Default Frames of the Return Link Stream

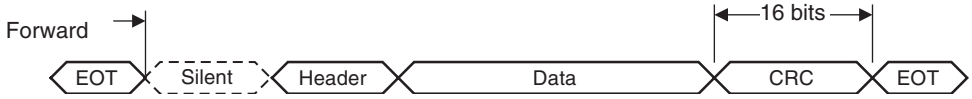
The return link is built by

- A return link header to get reference symbols, adjust modulation timing, adjust timing windows for anticollision, and set the EOF timing
- A data frame which can be based (depending on the command) on
  - The 8-bit status2 register
  - The 8-bit random value (arbitration commands)
  - The 16-bit slot information (wake-up commands)
  - The contents of the EEPROM (n bits)
- A 16-bit CRC frame (the bit count can be adjusted by the reader, if required)
- An EOT frame

During the synchronous return link, it is possible to operate in a loop mode which increases the SNR for the whole communication. There is no need for new command sequences.

Synchronous operation mode enables some adaptive mechanisms such as quasi-continuous bit rates or adaptive CRC.

Figure 4-5. Return Link Frame



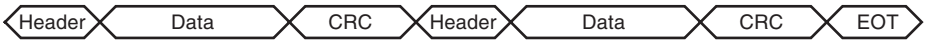
During programming the return link contains a silent time, during which the reader does not send any messages to the tag. During this time the reader sends a continuous wave (CW). The length of the silent time depends on the field strength of the received RF signal.

For all other commands, the silent time is zero.

The length of the data frame depends on the command and the reader. The reader is able to close the return link by transmitting an EOT frame.

If the reader wants to increase the robustness of the link, the reader may restart the message by sending a new header instead of the EOT frame.

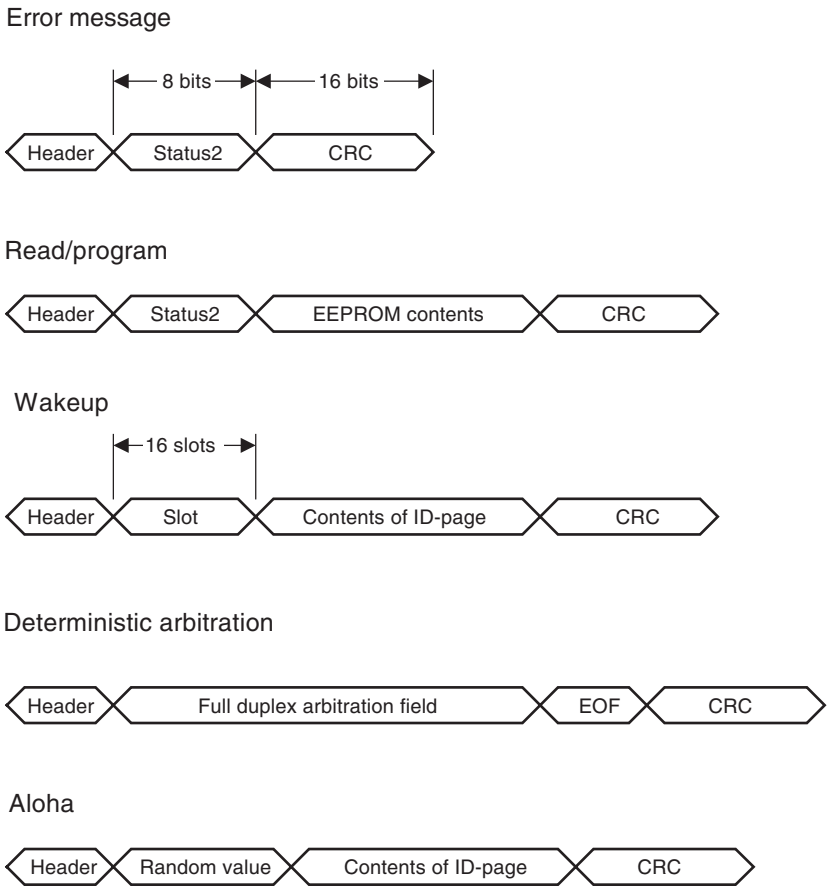
Figure 4-6. The Loop Function



The construction of the data frame itself depends on the command. It can contain

- A status (status2) message (read, program commands, error)
- An 8-bit random field (wake-up, and some arbitration commands)
- A data field which is the output of the EEPROM
- A 16-bit CRC field

Figure 4-7. Construction of the Default Return Link in Detail



During deterministic arbitration (deterministic selection procedures), the data field works in full duplex mode. The tag backscatters the value of its EEPROM value bit by bit, and the reader transfers (as a reaction to this information) a bit by bit decision. This decision then controls the next bit operation of the tag. If the reader has transmitted a decision which corresponds with the content of the selected bit of the EEPROM, the tag backscatters the next bit. Otherwise it is silent until the next deterministic-arbitration command.

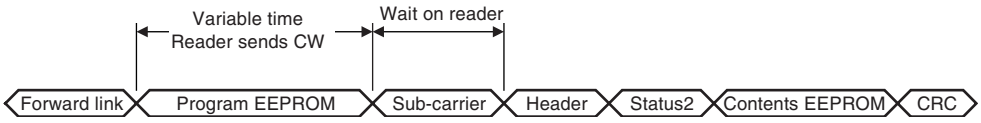
If the reader then marks the end of the arbitration by sending an EOT sequence,

- The reader knows the (item level linked) ID or a part of it for the selected tag, and
- The reader is free to send new commands to this selected tag. The tags which are not selected listen, but are not active

During programming, the tag is silent. When the programming is finished or if the tag has detected an error, the tag backscatters a sub-carrier, until the reader transmits a header to start the return link.

Notes: 1. Due to 2PSK backscatter modulation, ATA5590 is able to detect a notch until it backscatters a message.
2. When the RF field strength is low, the programming time is longer. The programming time depends on the field strength of the received RF signal.

Figure 4-8. Frame Construction During Programming



The time required to program the EEPROM is a function of the RF field strength, and the status of the block to which the address pointer points. If the block is locked against over programming, the tag starts immediately to backscatter a sub-carrier back.

4.8 Principal Communication Flow

Figure 4-9. Principal Flow of the Communication

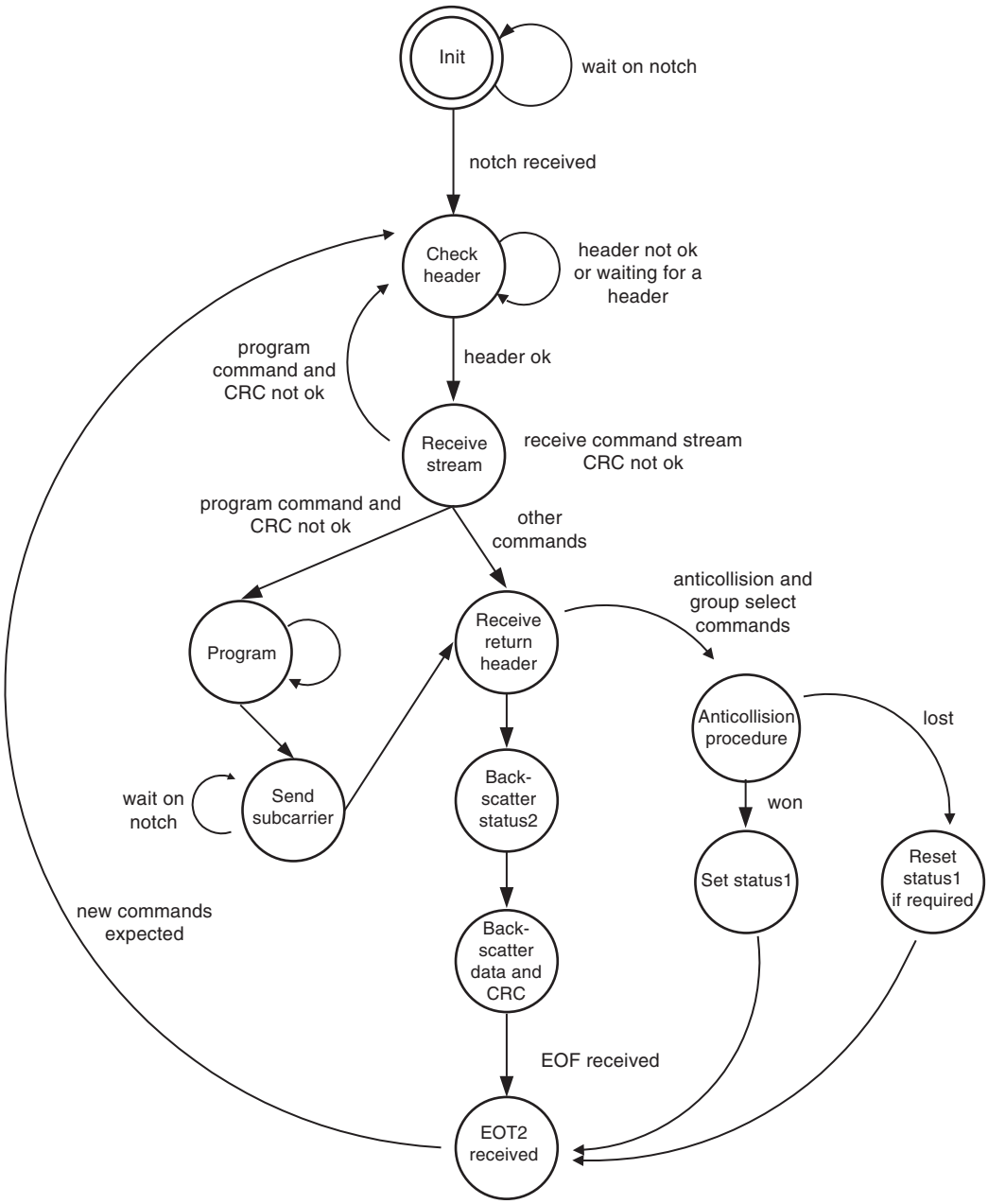


Figure 4-9 shows the flows for read, program, and deterministic anticollision commands. ATA5590 also supports other types of commands; in which case the flow can be slightly different.

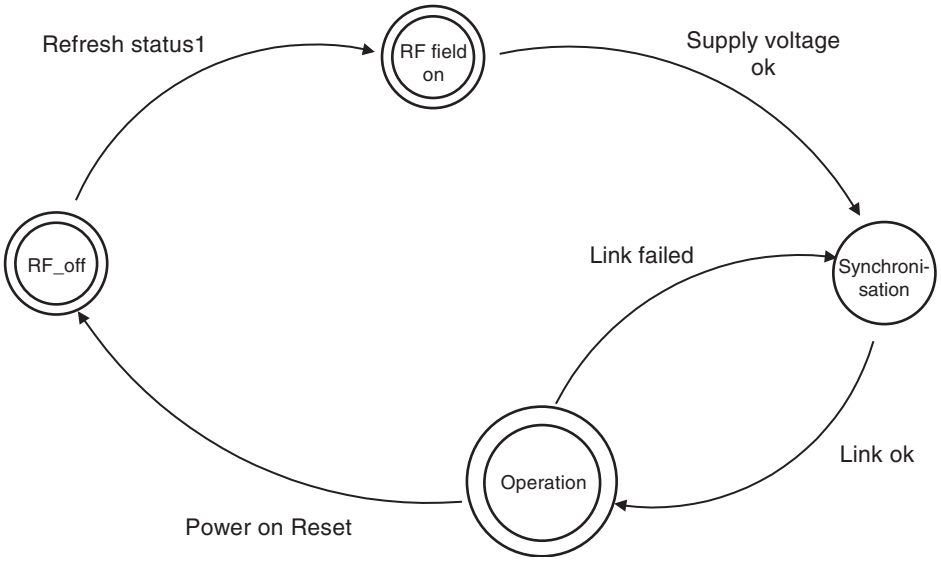
To be able to control such flows, ATA5590 implements several state machines, which work in parallel or sequentially.

4.9 States of the Tag

To minimize communication problems, the tag has to first become synchronous to the RF stream transmitted by a reader; after this the tag is ready for communication.

Additionally, most of the operations are controlled by select conditions which are fully controlled by the reader, and are based on the status1 register contents.

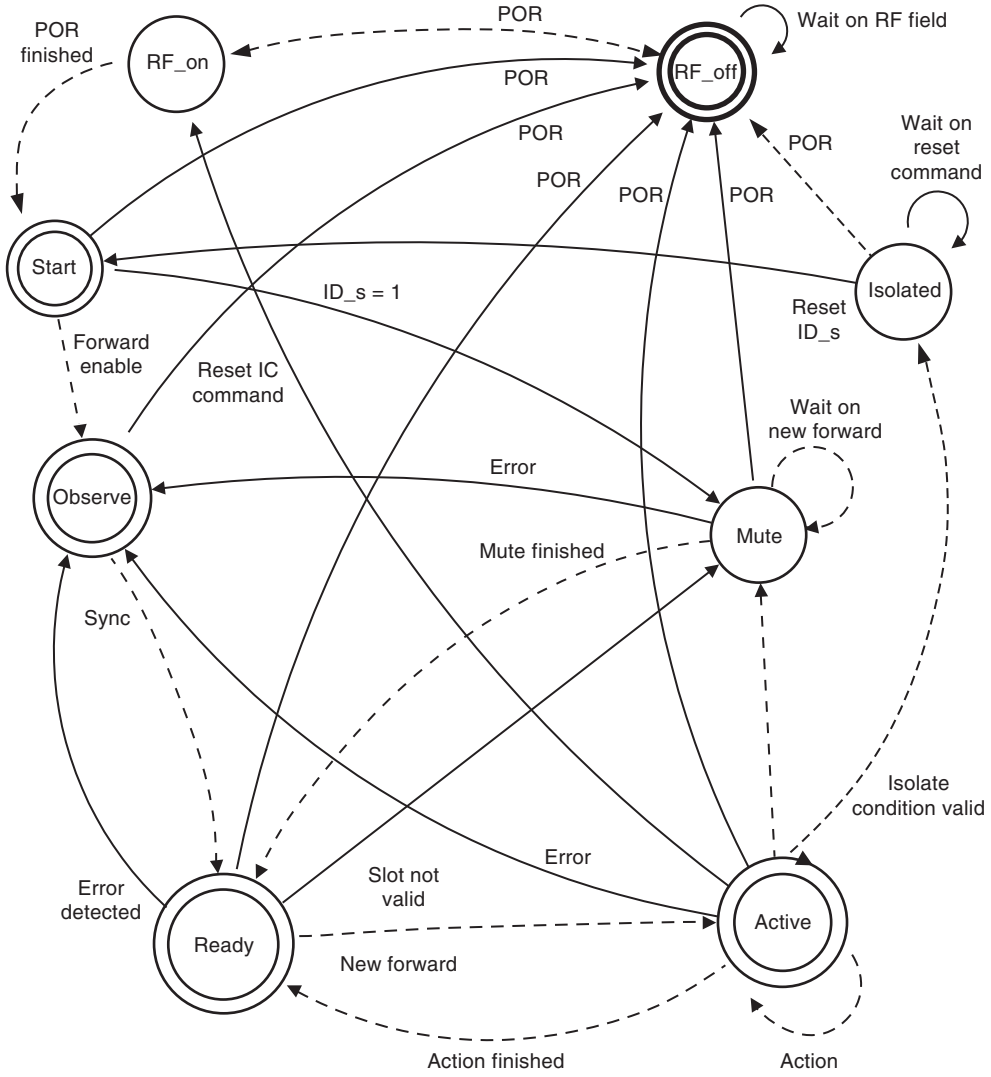
Figure 4-10. Operation Flow



To enable this operation flow, the tag must be in one of the following top view states:

- RF field off
- RF field on
- Start state
- Observe state
- Ready state
- Active state
- Mute state
- Isolated state

Figure 4-11. Top Level State Diagram (Starting Point is RF_off, Main Path is Represented by a Dashed Line)



4.9.1 Starting Point: RF Field Off

As long as the tag is not powered, the tag is not able to operate.

The tag stores the information of the status1 register (pre_select, ID, ID_s) for a defined time without any external power (8 seconds at 25°C). The storage time is a function of the temperature. The storage time increases as the temperature drops. As the time depends on temperature, the contents of the register after this time is no longer defined.

Note: Only a logical “1” can be stored over time. If the register was “0”, the contents is still defined after this persistence time; it will still be “0”.

4.9.2 RF Field On

When a tag enters an RF field, and the RF field strength (in respect to the resonant frequency of the antenna and its bandwidth) is above a certain value, the reset circuit generates a power-on reset (POR). After POR the on-chip oscillator is switched on.

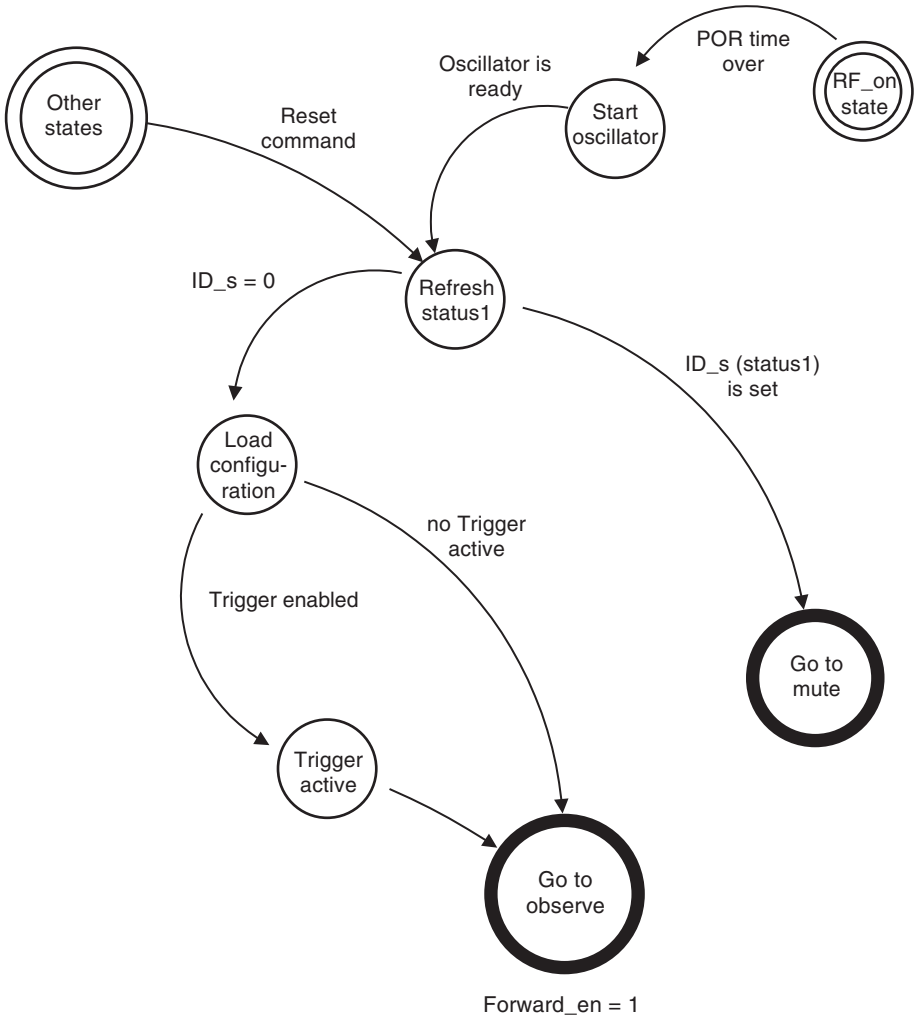
If the RF field has reached a minimum power level, and the power-on reset is finished, the tag IC changes to the start state.

4.9.3 Start State

After POR, the circuit generates a refresh procedure for the status1 register (pre_select, ID, ID_s). Then it reads the configuration of the chip out of memory. Based on the configuration, it enables or disables the trigger function. The detection of a first modulation tick (RSSI circuit) is enabled after configuration.

After enabling the RSSI circuit, the tag waits for a first modulation dip. The trigger function stops after receiving a first modulation dip.

Figure 4-12. Start State

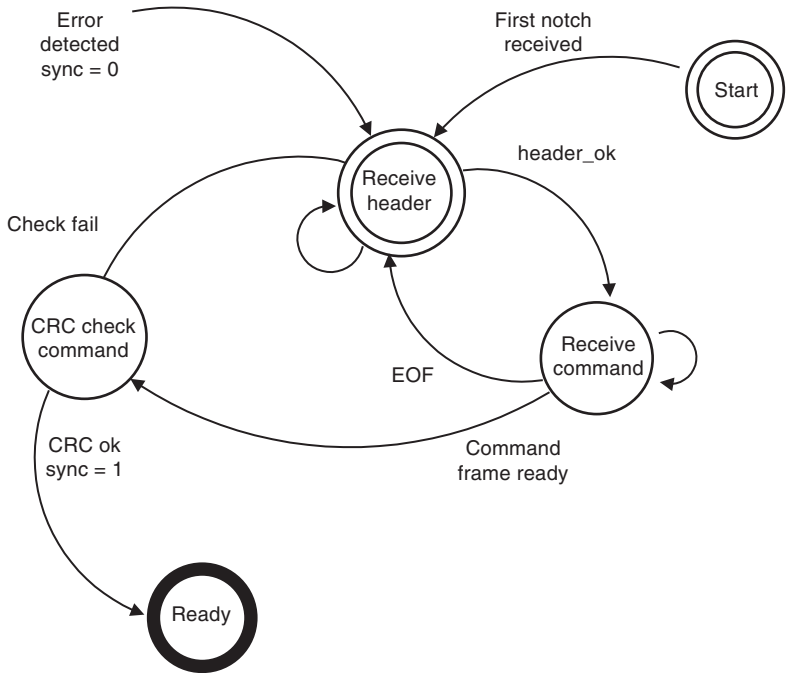


4.9.4 Observe State

To enable further actions, such as programming, the chip must be synchronous to the reader. Therefore, some checks have to be made over the stream which is received by the tag (timing of the forward header must be valid, the command must be known, and the first command CRC must be valid).

If these checks pass, the tag is synchronous to the modulated stream transmitted by the reader.

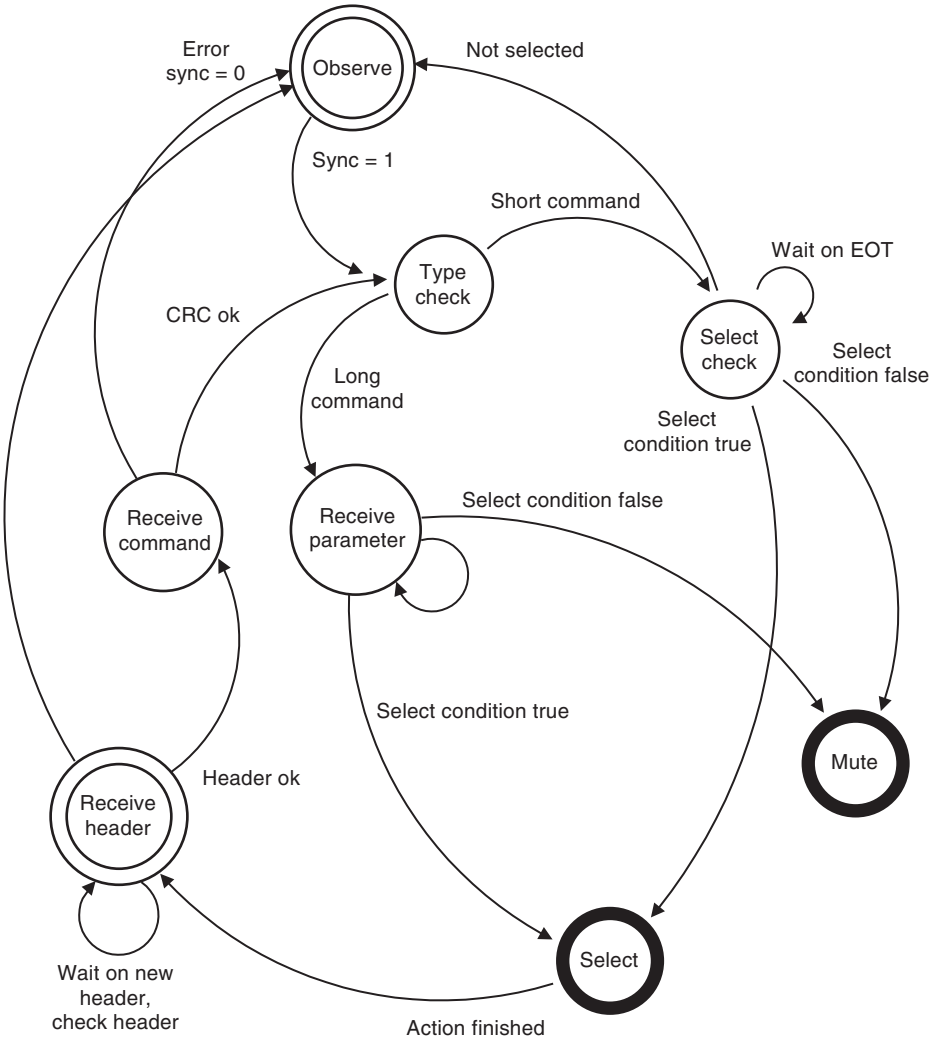
Figure 4-13. Observe State



4.9.5 Ready State

In this state, the enabling conditions are checked. If the conditions are true, the tag changes to the selected state, otherwise to the mute state.

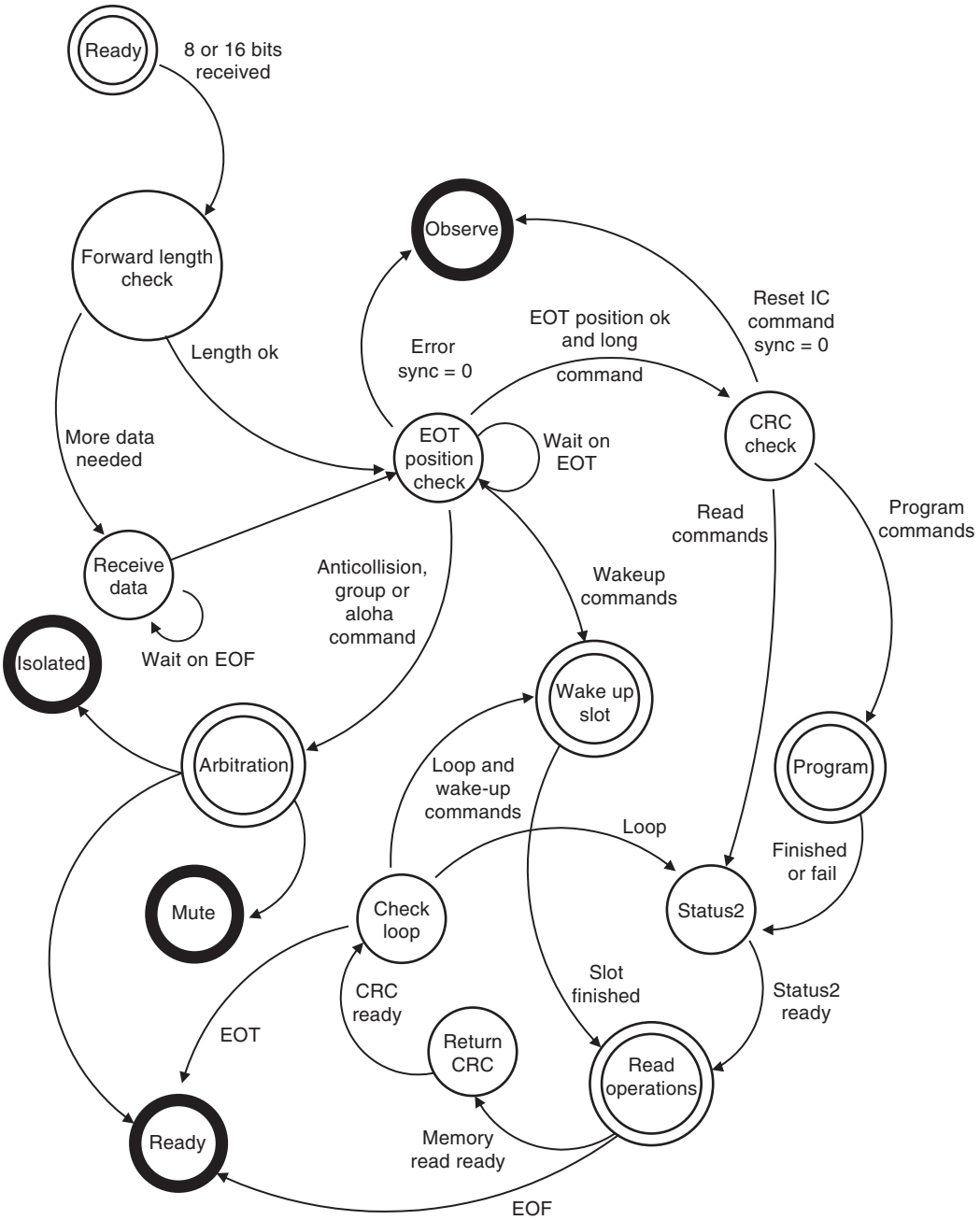
Figure 4-14. Ready State



4.9.6 Active State

If necessary, the rest of the forward frame (address, data, or both) must be received. Then the tag can carry out the required operation (program, arbitration, or starting the return link).

Figure 4-15. Active State



4.9.7 Mute State

The mute state is quite similar to the select state. However, as the select condition was false, the tag remains silent, and no operation (such as programming, arbitration or backscattering data) is done.

4.9.8 Isolate State

The isolate state is also quite similar to the select state. The tag is isolated and waits on a power-on reset or a reset command, which will reset the ID_s flag of the status1 register.

4.10 Summary of the Supported Arbitration Possibilities

If more than one tag is in the RF field and ready to operate, the system must support an arbitration procedure to be able to select one or a group of tags for further operations (for example, program or read), or to identify them.

The system must also be able to isolate a tag after an operation to be sure that this tag does not disturb the following communications. The flag which indicates this silent mode is ID_s, one of the status1 register bits.

Furthermore, in some applications it is helpful to get a first impression of whether there are several tags in the field or not. Therefore, the ATA5590 supports wake-up commands. After the return link header, the protocol supports a slot zone containing 16 bits. A tag modulates one of the 16 slots (the select mechanism for the slot is based on a random value calculated on-chip).

ATA5590 supports two kinds of principal arbitration mechanisms:

- A deterministic-arbitration procedure which is able to handle hierarchical processes, and
- An Aloha-based procedure which is time-slot-based. The size (time and bit count) of such a slot is under control of the reader

ATA5590 can mix these procedures, yielding a two-level arbitration mechanism.

The deterministic procedure can be combined with a random approach to be able to handle data structures in the arbitration process which are not unique. This random approach is not Aloha-based, and, therefore, strongly deterministic.

The result of each procedure is stored in the register status1.

Aloha-based procedures also influence the ID_s flag, and are able to consider the flags pre_select and ID.

Aloha is controlled by slot commands. The close slot command finishes the Aloha arbitration.

After POR, the tag starts to calculate a random value. The calculation continues as long as the tag receives power.

After a tag has received a slot command

- It takes a random number from the random number generator, which points to a slot number between 0 and 31 on-chip.
- After receiving the start command, all tags backscatter their information back to the reader during the first slot, independently from the chosen random value. If the tag's calculated random value matches the first slot number, it calculates a new one during this slot. Therefore, the tags in Aloha are always able to backscatter their information two times.
- If this random slot value matches the slot number which is under control of the reader, the tag becomes active, enabling the reader to communicate with the tag. If the slot value doesn't match, the tag does not answer to any command (mute state). The other operations (changing status1 or programming) are also blocked.

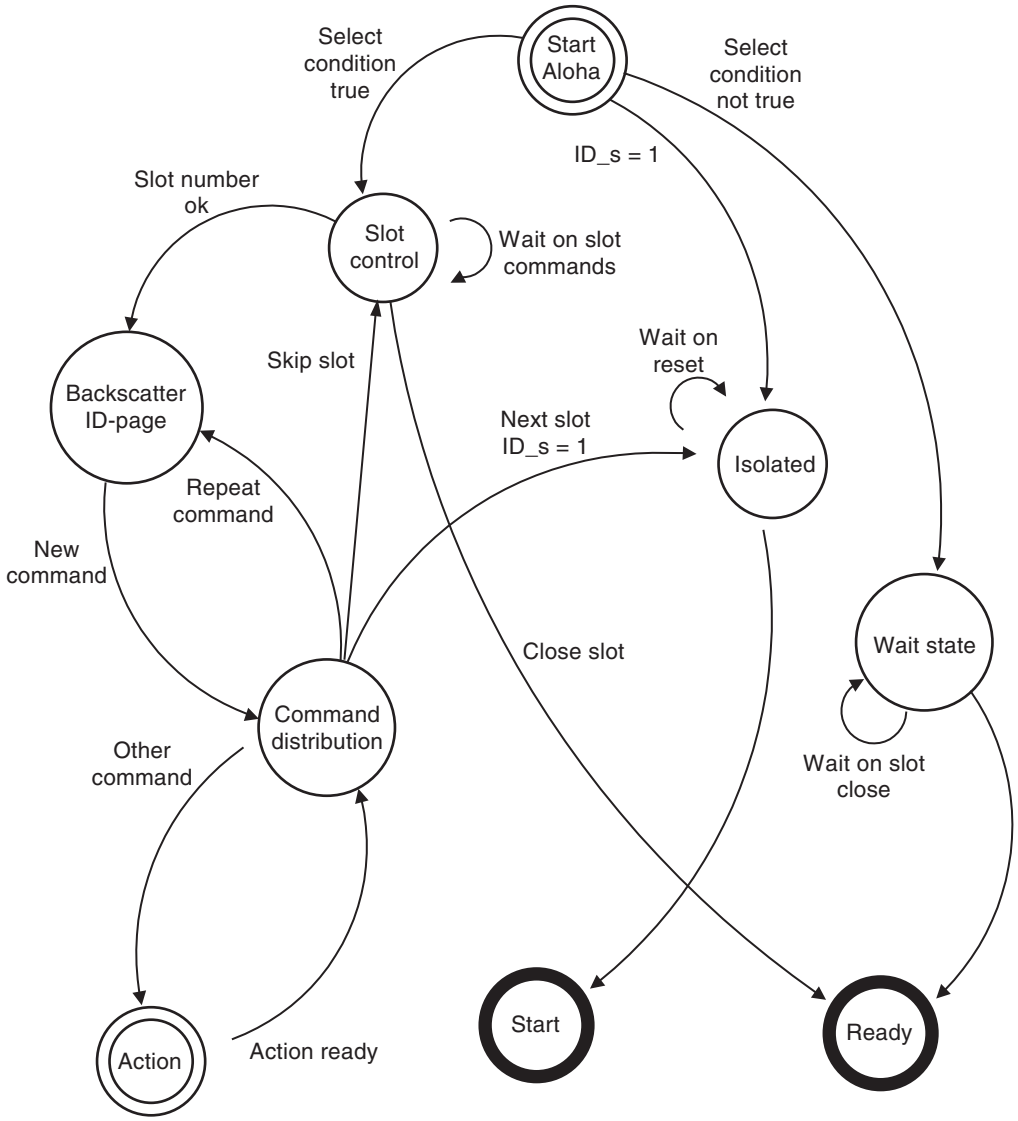
If the tag receives a new slot command (without the slot repeat, skip slot or slot close command) the tag calculates if it is now to be active or not.

If the reader detects a collision, it can skip the slot directly by sending a skip slot command. Then the formerly selected tags calculate a new slot value, rather than set the ID_s flag.

To increase the number of slots, the ATA5590 is able to change to a second arbitration level which is based on deterministic procedures. Therefore, the ATA5590 is able to operate with second level slots without changing the slot number.

The information which is backscattered by the tags is an 8-bit random number, and the contents of the ID page. Therefore, if the tags are virgin or if the ID is not unique, the reader is able to identify a collision between tags by observing the random number.

Figure 4-16. Aloha in Principle



Most of the commands supported by the ATA5590 consider the status1 contents. Therefore, it is possible to communicate with a group, with a single tag, or with all tags in the RF field. Some commands (short commands) directly consider the status1 flags. Long commands support a selection condition inside their streams; if the select condition flag is set to “1”, all tags with the pre_select or the ID flag set, and the ID_s flag not set, are addressed. For all commands except the reset command, if the selection flag is set to “0”, all tags in the RF field with ID_s flag set to “0” are selected.

Note: If the pre_select flag is set, and then the reader sends a deterministic anticollision command combined with the select condition
- The anticollision procedure is based only on the pre_select flag
- The subsequent commands (read or program), combined with the select condition, are based only on the result of the arbitration procedure. The pre_select status bit no longer influences the commands

ATA5590 supports several commands to solve collision problems deterministically. ATA5590 distinguishes between deterministic anticollision and the group-selection mechanism. The deterministic anticollision procedure of ATA5590 is based on a flexible binary tree algorithm which is characterized by:

- A modified deterministic binary tree algorithm, and
- Full duplex communication

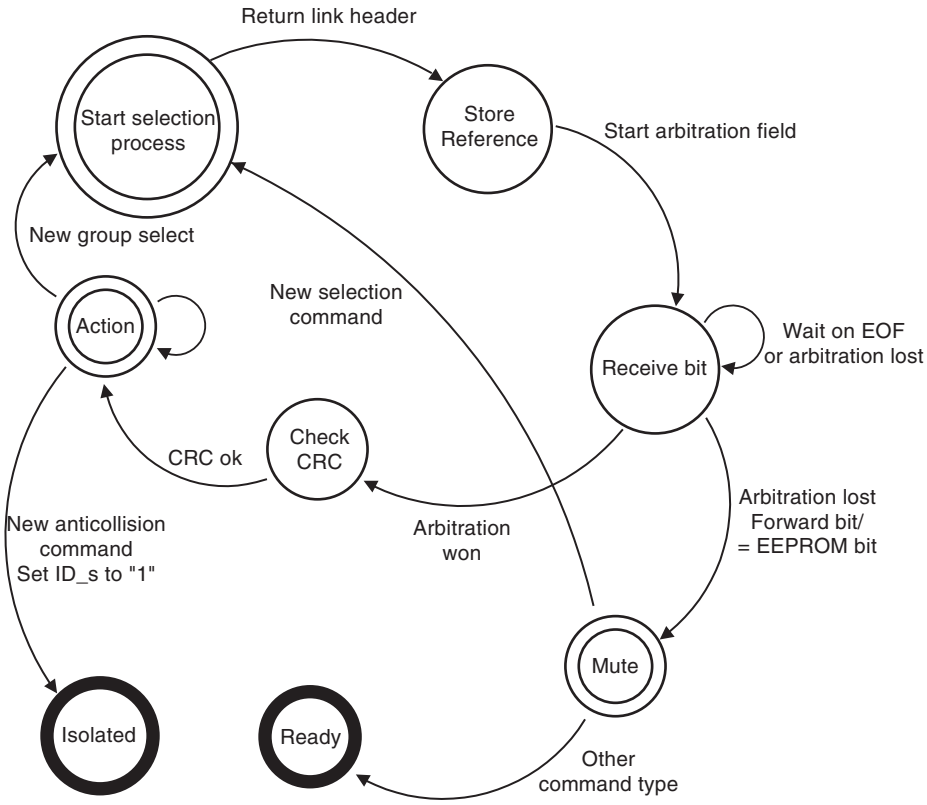
During arbitration, the procedure is based on full duplex communication to enable closed loop arbitration. Therefore, during arbitration the reader is able to control and to change priority bit-by-bit.

If the CRC condition is true, at the end of each arbitration procedure a group of tags or a single tag is automatically selected. The contents of the memory which was part of the arbitration is also known. There is no need for an additional acknowledgement to the tag. The reader can communicate immediately with the selected tags.

The deterministic anticollision procedure which is implemented in ATA5590 does not expect unique data structures, such as an ID, for arbitration, because ATA5590 also supports random frames during arbitration.

The arbitration process itself is also based on a PIE style. The reader transmits a reference time first (return link header section). Then, during arbitration, the tag compares the time between two bits with this reference. If the bit time is less than the reference time, a “0” was transmitted, otherwise a “1”. This value will be compared against the internal bit value of the EEPROM. If the values are the same, the tag has won the arbitration for this bit, and is enabled for further steps. If not, the tag has lost the arbitration, and waits on a new arbitration command. Up to this time, the tag is silent, and not available for programming or reading.

Figure 4-17. Arbitration Process



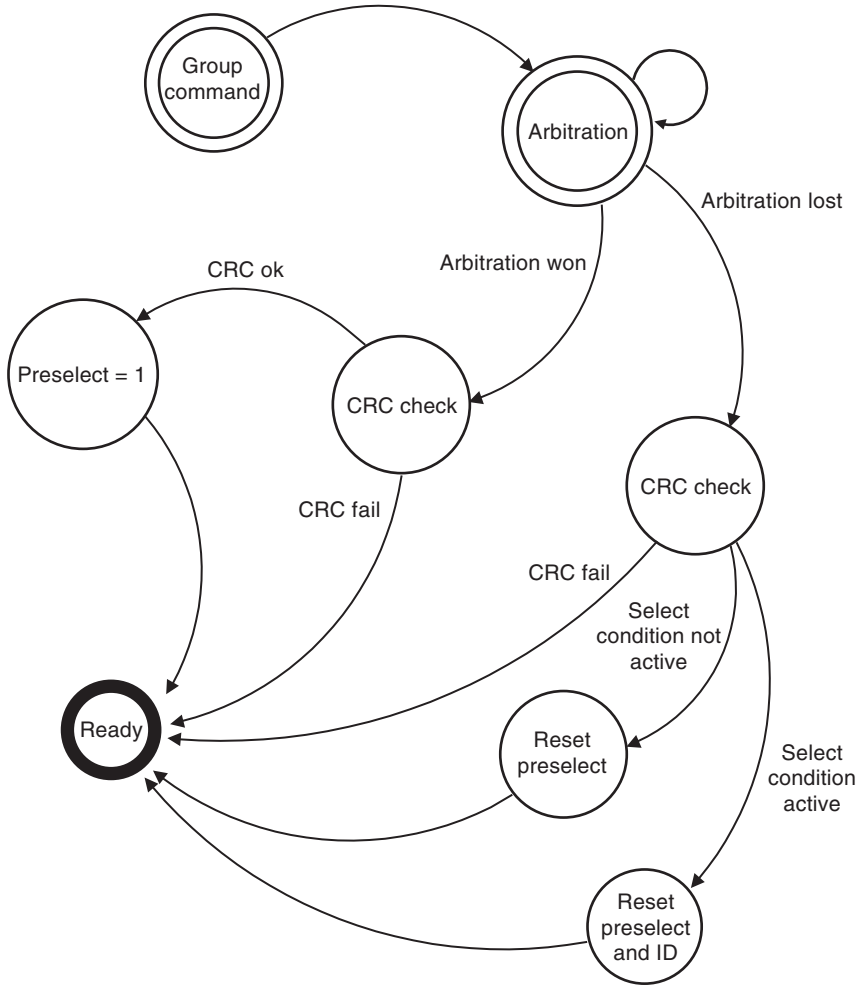
The pre_select flag of status1 can be set and reset by group-selection commands. Therefore, it is possible to select a group or a single tag with these command types. ATA5590 offers full duplex operation during group-selection commands.

The pre_select flag can also be reset by the reset command.

ATA5590 supports several kinds of group-selection commands addressing the ID or the AFI and DSFID mechanism. Additionally, a pointer-based group-selection mechanism is supported. Decisions can be made based on =, ≥, and ≤ comparisons.

After a group or a single tag is selected, the reader is immediately free to communicate with the tag(s).

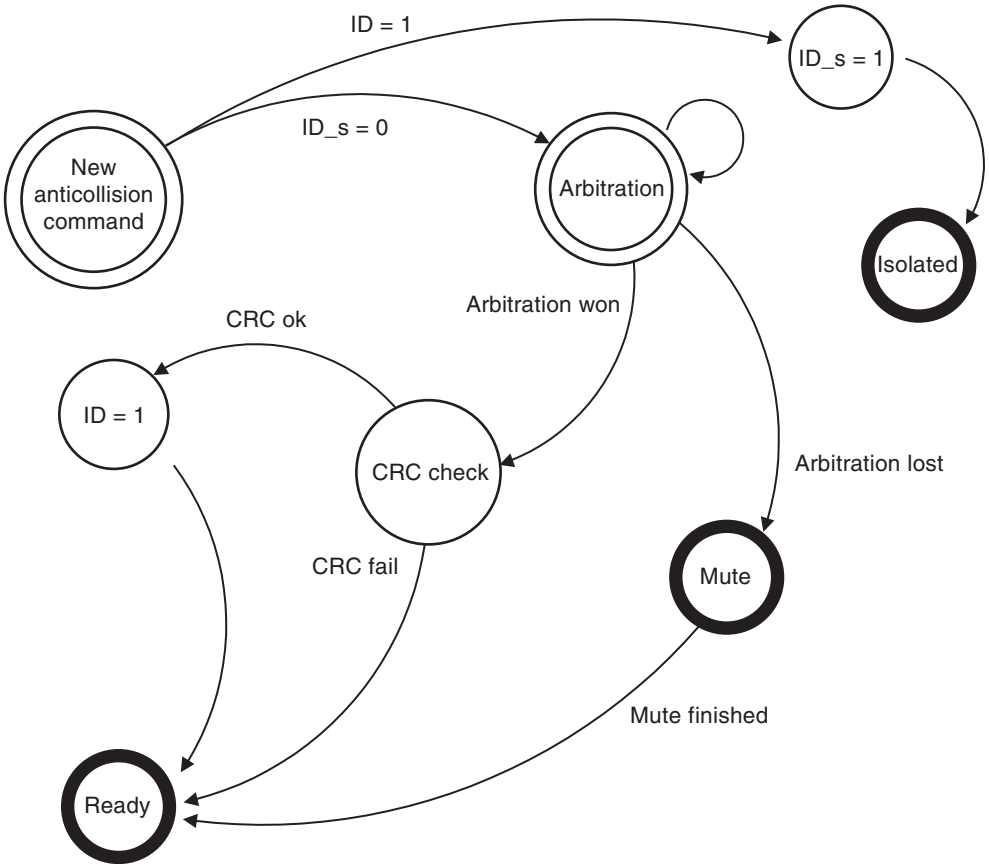
Figure 4-18. Pre_select Flow



During the deterministic-arbitration procedure, ID and ID_s flags can be set. The ID and ID_s flags are based on full duplex communication results.

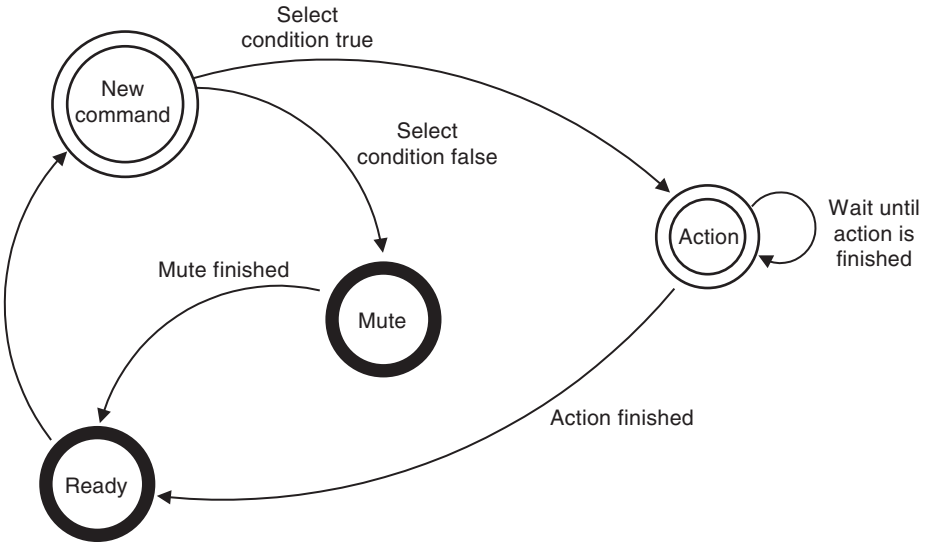
The ID flag is set to “1” if the tag wins an arbitration frame, and if the CRC is correct. The ID flag can be reset by a reset command, or, if the select flag is set, by a group-selection command (arbitration was lost)

Figure 4-19. ID and ID_s Flow (Deterministic Arbitration) in Principle



Deterministic procedures are able to influence the pre_select, the ID, and the ID_s flags.

Figure 4-20. Selection Process in Principle



The default anticollision procedure is based principally on a Tag_ID. The deterministic anticollision procedure itself is based on an adaptable binary search. The adaptation is fully controlled by the reader, and allows a priority change on the fly.

The deterministic anticollision is based principally on full duplex communication.

The IC stores the status of anticollision in 2 bits (ID and ID_s) in the status1 register (8 seconds storage time without power at 25°C).

ATA5590 also supports variable pointer-based anticollision commands, and a command which considers a random value. These commands are able to address the whole system and user memory.

After a group or a single tag is selected, the reader is free to communicate with them immediately.

The length of the arbitration fields is under the control of the reader. After receiving an EOF symbol, the CRC section starts.

A combination of the long deterministic commands and the short repeat_arb command is possible, which results in a faster arbitration.

4.11 Combination of Different Deterministic Selection Procedures

Anticollision and group-selection commands can be combined to achieve a hierarchical selection algorithm.

4.12 Combination of Aloha-based and Deterministic-based Selection Procedures

As ATA5590 supports Aloha and deterministic-based selection procedures, the user can mix them to implement a second selection level.

Figure 4-21. Flow to Implement a Second Selection Level in Aloha

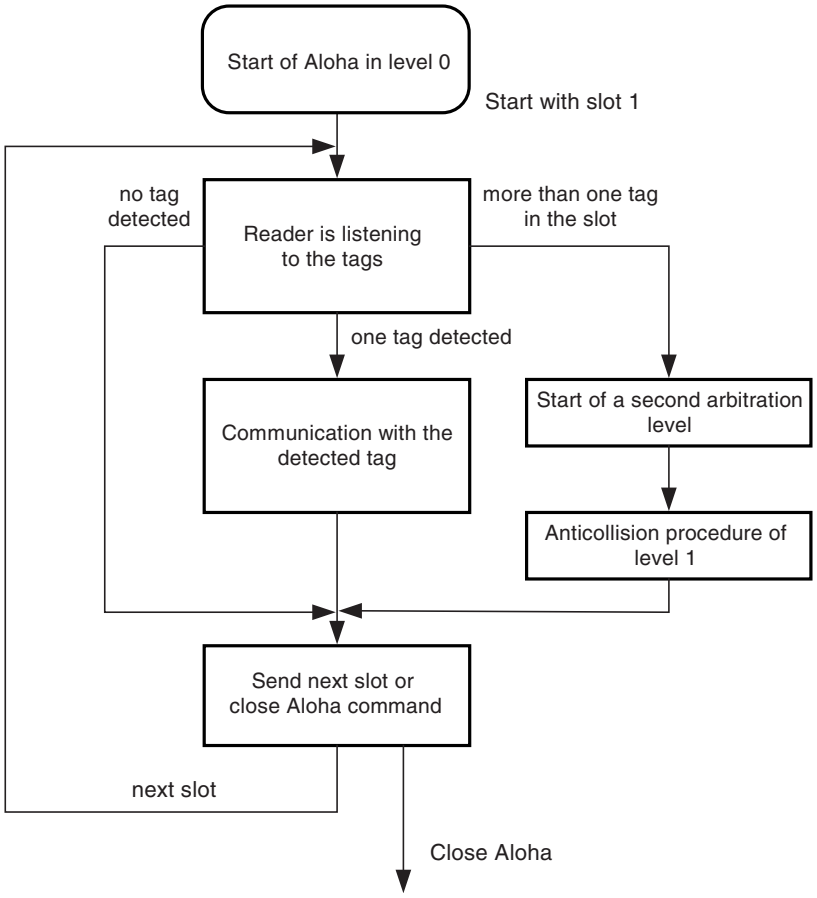
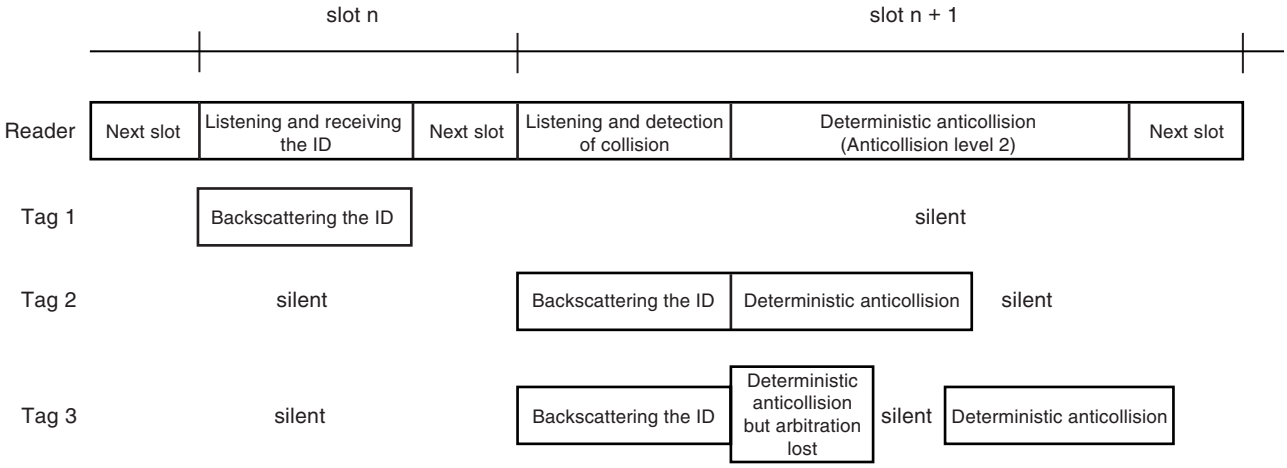


Figure 4-22. Example for a Two-level Selection Process Over Time



4.13 Application-specific Selection Procedures

4.13.1 Initialization of Virgin Tags Out of a Group of Tags

ATA5590 supports two possibilities for communication with virgin tags. During Aloha, the tags calculate a slot number which is independent from the memory contents. If only one tag back-scatters during a slot, this tag can be programmed.

In the case of deterministic procedures, the reader shall send a command which enables an arbitration over a random value. Based on this random value, the reader can isolate each tag.

After separation, the reader is able to program the tags with a unique number (Tag_ID or item-linked information).

4.13.2 One Tag is in the RF Field

Once the tag IC is ready for operation, the reader can send a first command to the tag to start communication.

4.13.3 Several Tags are in the RF Field

If the situation is stable (the tags are not moving), the reader can send a wake-up command first to get an initial impression of how many tags are in the field.

Then the reader determines which kind of selection procedure it wants to use, or it can decide that there is a need first for a pre-selection.

Pre-selection can be based on an AFI mechanism or can be based on some portion of the memory contents. Each anticollision mechanism supports the feasibility of operating with or without pre-selection, as does each read or program command.

The reader is also free to chose to operate using anticollision commands, a combination of Aloha and deterministic procedures, or a combination of both.

Notes:
1. The deterministic selection process supported by ATA5590 is able to address each bit position of the EEPROM during the arbitration process.
2. Deterministic arbitration is not limited by block or page borders of the EEPROM.

4.13.4 Moving Tags in the Field

If there is a possibility of tags arriving in the field (because the tags are moving), then it is recommended to operate with pre-selection. At the end of the communication (with the selected tags), the reader can send a wake-up command to all tags not pre-selected to be sure that it has identified all tags in the RF field which can participate (ID_s = 0).

5. Trigger Functionality

After each POR or global reset command, the start state becomes active. In this state, ATA5590 reads the trigger configuration out of the EEPROM. If the trigger function is enabled (trigger configuration(1)), the second bit is read out to configure the sub-carrier frequency.

Table 5-1. Trigger Configuration

Trigger Configuration(1:0)	Function
00	Trigger not active
01	Trigger not active
10	Sub-carrier frequency is OSC / 4
11	Sub-carrier frequency is OSC / 8

The sub-carrier modulates the field as long as the tag does not receive a notch tick. After detection of the start of the forward stream, the trigger function is switched off.

The trigger function becomes active again after receiving a global reset command.

The trigger function can be controlled by a special programming sequence.

6. Commands

ATA5590 supports long and short commands.

6.1 Long Commands

Table 6-1. IC Control Command

Command	Short Description	Comment
Reset	Reset of the circuit or parts of the status1 register	Affects the whole circuit or just the status1 register

Table 6-2. Group-selection Commands

Command	Short Description	Comment
Group_ID	Group select targeting ID	Affects only the pre_select flag
Group_AFI	Group select targeting AFI	Affects only the pre_select flag
Group_p	Group select supporting address and bit pointer	Affects only the pre_select flag
Group_p_leeq	Group select supporting address and bit pointer	Affects only the pre_select flag
Group_p_greq	Group select supporting address and bit pointer	Affects only the pre_select flag

Table 6-3. Full-duplex Anticollision Commands

Command	Short Description	Comment
Anticollision_ID	Full-duplex anticollision command targeting ID	Affects ID and ID_s
Anticollision_p	Full duplex anticollision command, supporting address and bit pointer	Affects ID and ID_s
Anticollision_p _random	Full duplex anticollision command, supporting address, bit pointer, and random methods	Affects ID and ID_s

Table 6-4. Read Commands

Command	Short Description	Comment
Read32	Read 32 bits in loop	Pointing to memory
Read32c	Read 32 bits in loop	Pointing to control memory
Read128	Read 128 bits in loop	Pointing to memory
Read128c	Read 128 bits in loop	Pointing to control memory

Table 6-5. Program Commands

Command	Short Description	Comment
Program4byte	32-bit programming at once	Pointing to memory
Program4bytec	32-bit programming at once	Pointing to control memory
Programnbyte	Up to 32-bit programming at once A portion of 8 bits can be selected	1 byte to 4 bytes are selectable

6.2 Short Commands

Table 6-6. Short Read Commands

Command	Short Description	Comment
Get_ID_page		Corresponds with read128c(0)
GET_system	Manufacturer system information to ID page	8-bit status2 + 320-bit EEPROM contents

Table 6-7. Short Anticollision Commands

Command	Short Description	Comment
Wakeup_s	Each selected tag answers in one of 16 slots, and backscatters the ID plus 8-bit DSFID	
Wakeup_sb	Tags which are not selected answer as described for Wakeup_s	
Repeat_arb	Repeats the long-arbitration or group_selection command which was previously received The return header and the following frames are the same as for the last command	Used to shorten the anticollision timing Repeat_arb is a temporary command All switching and tuning possibilities are enabled
Slot	Aloha	Affects ID_s
Slot_selected	Aloha	(ID or pre_select) and not ID_s Affects ID_s
Slot_not_selected	Aloha	Not ID and not ID_s and not pre_select Affects ID_s
Slot_repeat	Aloha	ID_s is not affected
Skip_slot	Aloha	ID_s is not affected Skip_slot is a temporary command
Slot_close	Aloha	Affects ID_s

The table above also contains temporary commands which are specified in Table 6-8. These commands are based on the command which was previously received by the tag. If the function is not enabled, an error code is backscattered.

Note: In the case of an invalid command (CRC was received correctly), the following communication stream will not be disturbed, and therefore no blocking situation can occur.

Table 6-8. Temporary Commands

Command	Short Description
Repeat_arb	Used to speed up deterministic anticollision procedures.
Skip_slot	Used only in Aloha procedures, if the reader has detected a collision and deterministic anticollision is not supported by the reader. The last Aloha command is repeated. The slot counter is incremented. The ID_s status flag is not influenced.

6.3 Access to Memory

ATA5590 supports several addressing mechanisms to optimize the memory access mechanism.

- Long physical (up to 11 bits) and symbolic addresses (8 bits)
- Short address (3 bits)
- Short symbolic address (3 bits)

7. Elements of the Link

As the tag normally works in a very noisy environment, the link must support techniques to achieve a high signal to noise ratio (SNR), and low bit error rates (BER). Therefore, the default link supports

- PR-ASK for generating a system clock (notch)
  - ASK technique with $m \geq 0.8$ is also supported, but this technique does not support BER and SNR values which are achievable with PR-ASK
- Synchronous return link controlled by notch signals generated by the reader
- Different coding styles for the return link

Additionally, the link is protected by 2 kinds of CRC:

- 2-bit CRC for each command byte
- 16-bit CRC frame over all data

When using classic commands (read, program), the 16-bit CRC is used during the forward and return link. For group and anticollision commands, the 16-bit CRC is used only one time.

Short commands are based only on the 2-bit command CRC plus the 16-bit return link CRC

7.1 Forward Link

The forward link supports long and short commands. If the header was correctly received, ATA5590 is able to receive and to decode the following stream of the reader. After it has received the 8-bit command code, ATA5590

- Stores the 6 bits of the command frame in a command register, and
- Checks the two bits of the command CRC

Additionally, ATA5590 supports two temporary commands (skip_slot and repeat_arb). After receiving these codes, ATA5590 checks the conditions. If the commands are enabled, the storing mechanism of the 6-bit command frame is skipped. Therefore, ATA5590 backscatters an answer based on the command which was received before. Temporary commands have the same length as short commands, also including the 2-bit command CRC.

Short commands are based on the following fields:

- Header for timing definition to be able to extract the following symbols (“0”, “1”, EOF)
- 8-bit command field
- EOT frame

The 8-bit command field contains the 2-bit CRC.

An EOT frame is based on two EOF symbols.

Long commands (read and program) are based on the following fields:

- Header for timing definition to be able to extract the following symbols (“0”, “1”, EOF)
- 8-bit command field
- 8-bit parameter field
- 8-bit address (depends on command and addressing mode)
- 32-bit data field (program commands only)
- CRC frame
- EOT frame

The header, 8-bit command frame, 8-bit parameter frame, 16-bit CRC frame, and EOT frame are default structures of long read and program commands.

Anticollision and group-selection commands are based on the following structure:

- Header for timing definition to be able to extract the following symbols (“0”, “1”, EOF)
- 8-bit command field
- 8-bit parameter field
- 8-bit address (depends on command and addressing mode)
- EOT symbol to close the command
- Header for timing initialization
- N-bit arbitration data field
- EOF symbol
- CRC frame
- EOT frame

The EOF symbol is used to close the arbitration.

The length and the mechanism included in the CRC field transmitted after the command section depends on the internal communication status of the tag, and the control sequences transmitted by the reader during the forward link.

In default mode (no additional action of the reader), the CRC field has a length of 16 bits.

After the tag becomes synchronous to the stream of the reader, the reader can change the bit count as well as the communication style of the CRC field.

7.2 Return Link

The return link depends on the command. After receiving a read command, it is based on:

- Header section to define different timings and spectra
- Status byte
- Data section
- CRC section
- End of frame (EOT) section

If ATA5590 has received a program command, the reader has to send a continuous wave until the tag backscatters a ready signal (sub-carrier), because ATA5590 supports an adaptive programming algorithm to enable short-distance and long-distance programming routines. After receiving this acknowledge signal, the reader starts transmitting the sequence as just described.

Anticollision, group-selection, and wake-up commands are based on different return link structures; only the headers are the same. The return links of the anticollision and group-selection commands look the same as the forward links.

In the case of wake-up commands, the 8-bit status information is replaced by a 16-bit slot zone.

The mode of the return link is the synchronous communication mode; the reader transmits the header sequence to adjust timings, and transmits notches to mark the boundaries of the link.

In synchronous operation mode, the reader is able to get the message in a loop by transmitting a new header sequence instead of the EOT frame.

It is also possible to send only the CRC in a loop (adaptive CRC) by inserting an EOF symbol at the position of the last data bit (LSB). The reader can also shorten the CRC zone.

7.3 Handover Timing

7.3.1 Forward Link to Return Link

As the handover mechanism from the forward link to the return link is synchronous, there is no wait cycle between the link mechanisms. The forward link is closed by the EOT stream. Then the tag expects the return link header for further control settings.

7.3.2 Return Link to Forward Link

After the return link header is passed, the reader is free to stop the return link at any point by sending the EOT sequence. If the adaptive CRC field is selected, the reader has to send the EOT sequence as well.

The tag decodes the first clock tick of the return link after the EOT sequence (the symbol must be closed) as the start of the forward header. The time between this first notch (forward header) and the end of the EOT sequence is therefore limited by the RF regulation.

7.4 Robustness of the Link

The robustness of the link depends on the likelihood of detecting an error. Therefore, the link is based on several mechanisms to control the robustness level.

- The forward symbol definition is based on a pulse interval encoding (PIE) concept to define “0”, “1”, and EOF symbols. The boundary for detection is controlled by the reader. The timing and the timing differences between the symbols are defined by the header, which allows flexible, and therefore user-controlled, robustness.
- After the header has defined the boundaries of the symbol lengths, the reader transmits a command frame which contains the 6-bit command and 2-bit CRC.
- At the end of long commands in the forward data stream, a 16-bit CRC follows. The length of this CRC frame can be shortened or extended by the reader to increase robustness, or, if the reader is able to interpret the backscattered stream directly, to shorten messages.
- After becoming synchronous to the reader, the tag backscatters the received and decoded bits of the forward stream back to the reader. This enables the possibility of controlling the link on the fly, and, if the reader detects an error, it can close this command directly to avoid misunderstanding, or to shorten the communication time.
- The return link supports different types of coding mechanism to avoid interpretation mistakes by the reader. FM0, NRZI, and 3phase1 coding techniques are supported.
- The return link also supports a 16-bit CRC frame. The length can be shortened or extended by the reader.
- Each anticollision or group-selection procedure is ended by a 16-bit CRC field. The length of this CRC frame, as well as the direction (reader-to-tag or tag-to-reader), is controlled by the reader.
- During the forward header, after the tag is synchronous, the tag transmits internal status information back to the reader.
- During the return link header, ATA5590 also transports status and timing information to the reader, enabling adaptive optimization of the link.
- Additionally, ATA5590 checks the position of EOF symbols and the number of symbols transmitted by the reader.

7.4.1 Command CRC

The command frame contains

- 6 command bits and 2 CRC bits, if it is a default command
- 4 command bits, 2 modulation control bits, plus 2 CRC bits

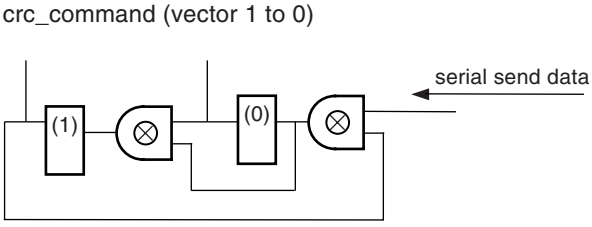
The expected CRC is the inverted value of

$x^2 + x^1 + 1$

Reset and start value is 2h

The remainder is 2h.

Figure 7-1. Schematic of the Command CRC and Initialization Values



Comment: The reset value of the CRC register is 10_B

7.4.2 Sync Condition

To enable the tag for communication it is necessary that the tag is synchronous to the reader. Therefore, the tag checks the timing of the forward header and the command CRC to decide if the tag is synchronous or not. If these conditions are true, the tag becomes synchronous after receiving the EOT sequence. Then the tag supports full duplex during the forward link.

7.4.3 16-bit CRC

The 16-bit CRC calculation (during the forward link and return link, over each section including the command section of the forward link) is based on

$x^{16} + x^{12} + x^5 + 1$

The reset and start value is FFFFh.

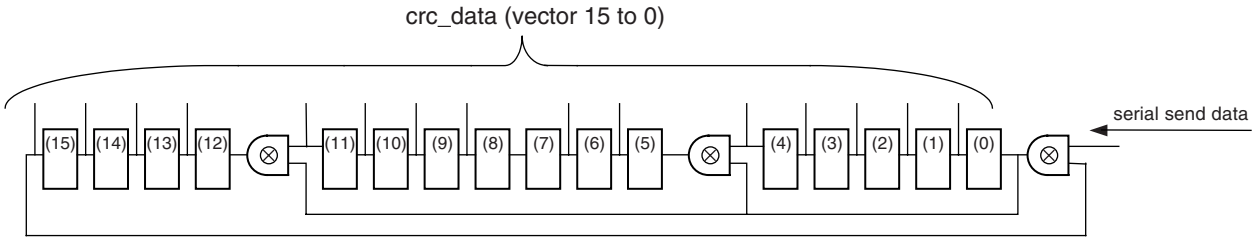
During the forward link,

- The calculation is made over the 8-bit command frame, the parameter frame, and, if present, the address and the data (for programming) frame
- The tag IC expects the inverted value for CRC checking starting from the command

During the return link, the IC backscatters the inverted value back to the reader. The calculation is made over the bits after the return header.

The remainder is: 1D0Fh

Figure 7-2. Schematic of the 16-bit CRC Register



Generator polynomial (CRC-CCITT) = > $x^{16} + x^{12} + x^5 + 1$

x^{16}	x^{15}	x^{14}	x^{13}	x^{12}	x^{11}	x^{10}	x^9	x^8	x^7	x^6	x^5	x^4	x^3	x^2	x^1	x^0
1	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	1

Comments:

The generator polynomial is 17-bit-value
The crc-result is 16-bit value
The reset value of a CRC register is $FFFF_H$

Note: As mentioned earlier, ATA5590 supports adaptive CRC frame constructions for the 16-bit CRC frame; the reader is able to change the length to a minimum value of 1 bit or it can increase the length. In such cases, the tag backscatters the CRC to the reader in a loop mode. The reader can then decide the length.

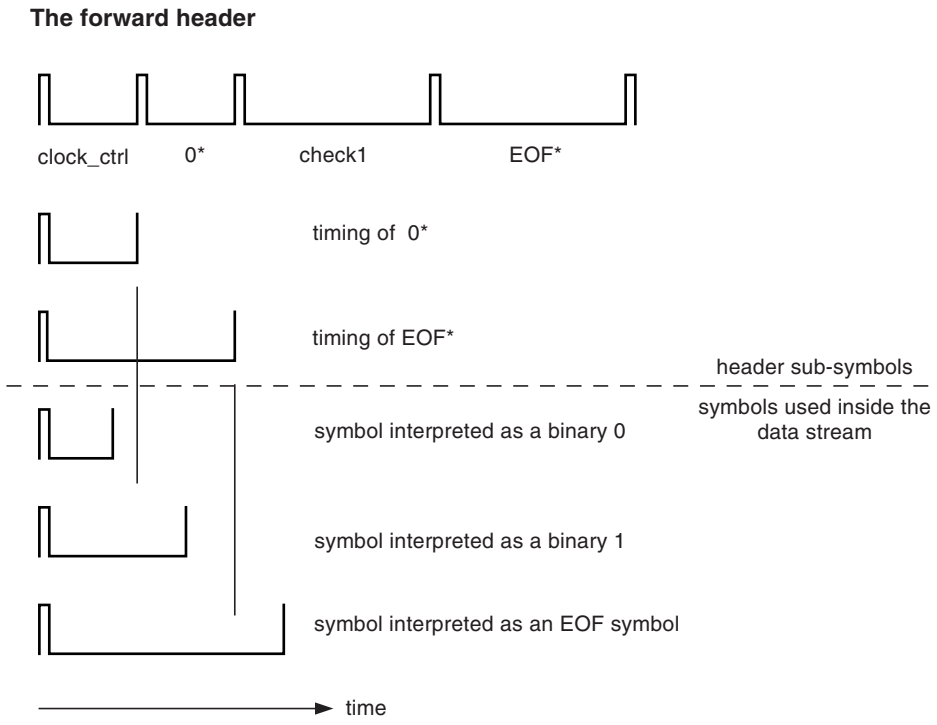
8. Forward Stream

8.1 Forward Header

The forward header consists of 4 symbols. The time between the notches is measured by ATA5590. Some of these timings are the base for PIE of the forward link. The timing relations are also checked by ATA5590. This mechanism is used to find the header, which results in a first pre-synchronization.

The tag itself measures the time between two notches, which means that this measurement is independent from the length of the notch signal.

Figure 8-1. Principal Timing (the Pulses are Generated by Notches)



Note: The EOT symbol at the end of a command or at the end of the synchronous return link is a combination of two EOF symbols.

Figure 8-1 shows

- The link is based on a relative timing, considering the length of the symbols transmitted during the header.
- The boundaries between the symbols are marked by notch signals. The notch signal is generated by the reader by changing the polarity of the modulation (PR-ASK) or by a traditional AM signal.

The header is accepted by the tag if the check1 and the EOF* symbols are longer than the 0* symbol. If the header is not accepted, ATA5590 continues to search for a valid header as long as it receives symbols from a reader.

During the following sections (data and EOF), the tag measures the time between two notch signals. Considering the timing of 0* and EOF*, the tag decides if it has received a binary 0, a binary 1, or an EOF.

- The time for a binary 0 is less than the time for 0*, for example 0.8 times 0*
- The time for a binary 1 is greater than for 0* but less than EOF*, for example 1.2 times 0*
- The time for an excepted EOF is greater than the time for EOF*, for example 1.2 times EOF*

ATA5590 is based on an oscillator-based timing measurement. Therefore, the minimum symbol length between two notches (edge-to-edge) is defined to be 5 oscillator clock cycles. Status2 register bit 3 indicates if the minimum length during the symbol transport was correct.

The oscillator frequency is tuned to 420 kHz (die) –10% to +40% at room temperature.

Based on the length of the first symbol of the header, ATA5590 adjusts the internal clock frequency to save power. Therefore, the internal clock cycle can be half or double the internal oscillator frequency.

Notes:
1. The time for a binary 1 must be less than for EOF*
2. The measurement is based on a timer measurement. The timer is driven by a clock signal. The frequency of this clock signal depends on the adjustment of the first symbol of the header. It is obvious that for comparison the difference between, for example, a logical 0 and 0* shall be more then one clock cycle.

8.1.1 Time-out Mechanism (Adaptive Watchdog Functionality)

After receiving the second notch of the header section, an adaptive time-out mechanism is enabled. During the header, ATA5590 stores the time between two notches. If there is no further notch after 4 times this stored time, the forward link and the synchronous condition will both be reset.

8.1.2 Power Management During Forward Link

ATA5590 starts its timing measurement with the OSC frequency, and measures the time of the first symbol (time between the first and the second notch of the header). If this time is lower than an internal value, ATA5590 switches the internal clock to 2 × OSC. This increases the power consumption.

If the measured value is higher than a second internal value, ATA5590 switches to OSC / 2, which results in lower power consumption.

8.1.3 Resolution and Data Rate Management

The size of the internal timer is 8 bits. As explained before, by changing the timing of the first symbol of the header, the internal frequency is changed. This has an effect on the timing measurement unit which calculates the bits of the stream.

- The resolution for timing checks can be changed under the control of the reader.
- The resolution and accuracy of the backscatter timing can be changed under the control of the reader.
- The data rate can be adapted.

As this offers maximum flexibility, the timing is controlled by a hard-wired watchdog function, which is given by a timer overflow condition (9th bit of the timer = timer overflow). If this occurs, the link and the sync flag are reset. The data rate that is supported by ATA5590 is in the range of 5 Kbits/s to 60 Kbits/s.

8.1.4 Accuracy Aspects of the Timing — Internal Oscillator

The timing of the ATA5590 is based on an on-chip oscillator. The typical frequency is 420 kHz at 25°C at the die level. The tolerance of the oscillator is –10 to +40%.

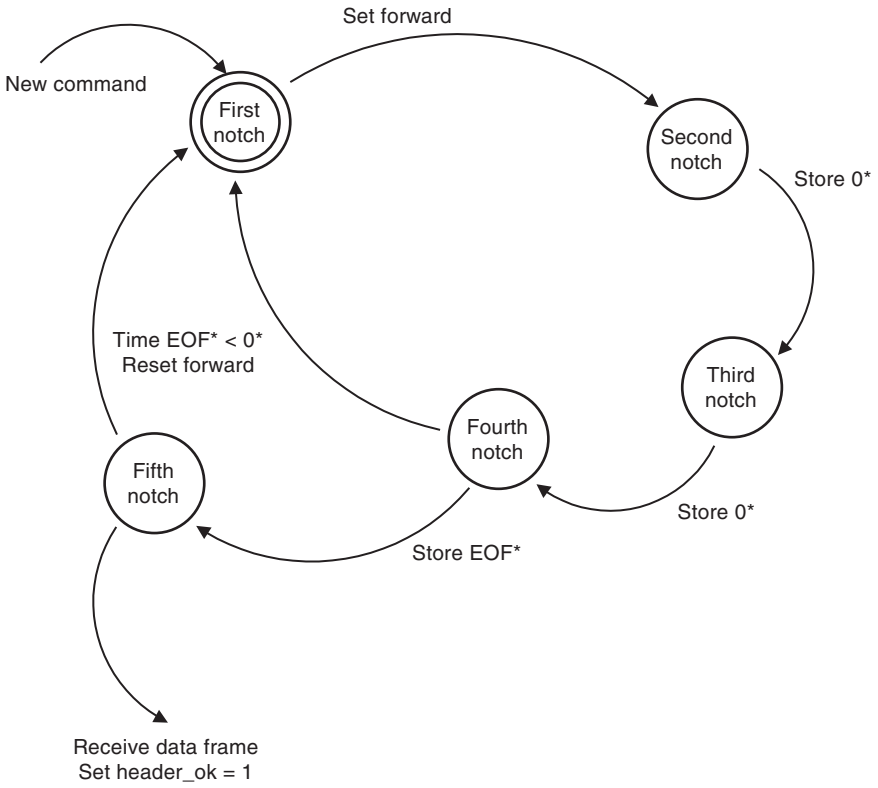
As the oscillator runs asynchronously to the clock ticks coming from the reader, the timing difference between 0* and the following data 0 shall be 2 oscillator clocks at a minimum rectangle modulation in the far field. The same rule applies for data 1's and EOT*.

8.1.5 Header_ok Check

ATA5590 checks the header timing on the fly. If the timing check passes, the tag is able to receive the rest of the stream.

If the header_ok check results in a fail, the tag restarts, in search of a valid header.

Figure 8-2. Header_ok Check



Note: The header_ok result influences the sync condition.

8.1.6 Modulation During the Forward Header

ATA5590 changes the state of modulation during the forward header. The modulator is at state0 for a time1 after notch. Time1 is the time the tag needs for internal calculations, and is therefore also the minimum time for a logical 0.

Note: The tag operates clock synchronous to an internal oscillator. Therefore, the absolute time is the difference from bit to bit.

Figure 8-3. Modulation During the Forward Header (Tag is Synchronous)

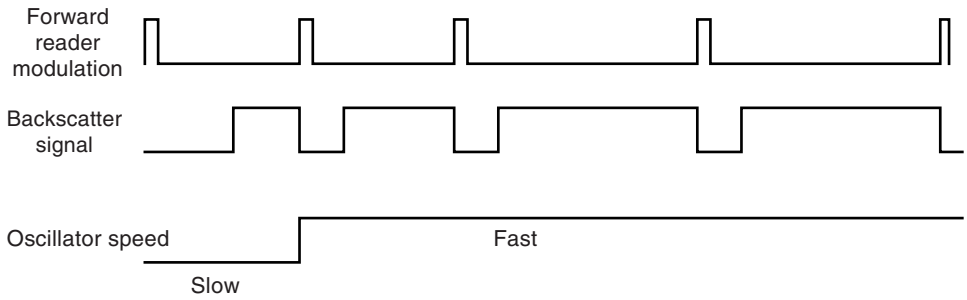


Figure 8-3 on page 55 shows an example of the implemented power management mechanism which selects the internal clock frequency. This mechanism has an influence on the backscattered modulation stream if the dynamic coding mechanism is selected (accuracy of the timing).

8.1.7 Modulation During the Forward Link

After becoming synchronous to the link (ATA5590 has received a full command correctly), ATA5590 backscatters the received data back to the reader.

The modulation coding type is the type which was defined in the previous command. Therefore, the reader is able to control the link on the fly.

The reset value is Soft NRZI

If a timing reference is needed for encoding, ATA5590 uses the time of 0* as a timing reference.

8.2 Command Coding

Commands can control the function of the tag.

8.2.1 Long Command Codes

After getting the timing definition for PIE out of the forward header section, the tag receives a 6-bit command and 2-bit CRC information. ATA5590 checks the CRC after receiving this 8-bit frame. If the CRC check passes and the reader does not send an EOT after this section, the tag interprets the next 8-bit field as a parameter field. An address field, data field, or both can follow the parameter field (depending on the command and the supported addressing mode which is stored in the parameter field). At the end, an end of file (EOT) symbol is expected.

Table 8-1. Command Codes for IC Control Command

Com(7:2)	8-bit Value, Inclusive CRC (hex)	Command	Comment
001010	2B	Reset	Reset of the control logic and/or reset of status1 register contents No answer is backscattered if the whole circuit is reset

8.2.1.1 Group-selection Commands

Group-selection commands can address the whole memory. The start address of the page is only fixed by using Group_afi or Group_ID commands.

The end address is under the control of the reader, because all group-selection commands support an auto-decrement function of the address. This enables arbitration even outside the start page.

Table 8-2. Command Codes for Group-selection Commands

Com(7:2)	8-bit Value, Inclusive CRC (hex)	Command	Comment
000001	06	Group_AFI	Based on the AFI byte of the Tag_ID page Affects pre_select
000011	0F	Group_ID	Affects pre_select
010010	49	Group_pointer	Affects pre_select
010110	5B	Group_pointer_leeq	Forward data ≥ EEPROM data Affects pre_select
010111	5C	Group_pointer_greq	Forward data ≤ EEPROM data Affects pre_select

Note: If there is a need in the application to use such commands several times, there is the possibility of shortening the whole procedure by using the short temporary command repeat_arb

8.2.1.2 Deterministic Full Duplex Anticollision Commands

Anticollision commands can address the whole memory. The Anticollision_ID commands are used to fix the start address of the page.

The end address is under control of the reader, because all anticollision commands support an auto-decrement function of the address. This enables arbitration even outside of the start page.

Table 8-3. Command Codes for Deterministic Anticollision Commands

Com(7:2)	8-bit Value, Inclusive CRC (hex)	Command	Comment
000000	01	Anticollision_ID	Based on page0 (Tag_ID) in the control memory Affects ID and ID_s
010011	4E	Anticollision_pointer	Affects ID and ID_s
010101	55	Anticollision_pointer_random	Affects ID and ID_s

Note: If there is a need in the application for using such commands several times, there is the possibility of shortening the whole procedure by using the short temporary command repeat_arb

8.2.1.3 Read commands

Table 8-4. Command Codes for Read Commands

Com(7:2)	8-bit Value Inclusive CRC (hex)	Command	Comment
000100	13	Read32	Physical addressing: user memory only
100100	91	Read32c	Control memory only
001100	30	Read128	Physical addressing: user memory only
100110	98	Read128c	Control memory only

8.2.1.4 Program commands

Table 8-5. Command Codes for Program Commands

Com(7:2)	8-bit Value Inclusive CRC (hex)	Command	Comment
001000	22	Program4byte	Physical addressing: user memory only
100000	83	Program4bytec	Control memory only
011000	63	Programnbyte	Program up to 4 bytes of a block

8.2.2 Short Command Codes

After getting the length definition out of the header section, the tag receives a 6-bit command and 2-bit CRC information. If this CRC check passes, the tag expects the EOT field.

As no parameter field follows the short commands, the modulation properties are defined by bits (3:2) of the command frame. The CRC is stored in bits 1 and 0 of the frame.

Table 8-6. Command Structure of Short Command Code

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Com(3:0)				Mod(1:0)		CRC(1:0)	

Table 8-7. Command Codes for Short Commands

Com(3:0)	Command	Comment
0001	Wakeup_s	All selected tags answer
0010	Wakeup_sb	All tags in the field answer if not selected by pre_select or ID
0101	Get ID page	The whole page, 128 bits
0110	Get system information	The whole system memory Manufacturer system information + user system information + ID page
0100	Repeat_arb	If the tag has received a long arbitration or group_command before, then this former command will be repeated.
1000	Slot	Aloha addressing all tags Set, start Aloha, and increment slot counter
1001	Slot_selected	Aloha addressing selected tags ((ID or pre_select are 1) and ID_s is 0) Set, start Aloha, and increment slot counter
1010	Slot_not_selected	Aloha addressing unselected tags (ID and pre_select and ID_s is 0) Set, start Aloha, and increment slot counter
1011	Slot_close	Close Aloha
1100	Slot_repeat	Aloha addresses only those tags which are active in a slot
1101	Skip_slot	Increment slot counter. No effect on ID_s

8.2.3 Error handling

If ATA5590 receives a command which is not known by the IC, the tag does not backscatter a specific error code during the return link.

If the received invalid command is interpreted as a long command, the tag stops backscattering the detected data during the forward link.

The following answers are backscattered by the tag:

- The command was known and the command CRC was correct: Normal operation
- The command was known but the CRC is wrong: The tag backscatters the error message (status2 register)
- The command is not known and the CRC is wrong: The tag backscatters the error message (status2 register)
- The command is not known but the CRC is correct:
  - The tag backscatters a sub-carrier during the symbol after EOF1
  - The tag stops backscattering the detected data (parameter field, address field, CRC field)

8.3 Parameter Field

When using long commands, a parameter field transports an 8-bit data field to the tag defining selection mode and return link modulation encoding scheme. Additionally, address information and other command-specific data are defined.

The default structure is defined in the following way:

Table 8-8. Parameter Field in Conjunction with the Defined Commands

Index	Function
7	Addressing_mode(1), if needed
6	Addressing_mode(0), if needed
5	Depends on the command
4	Depends on the command
3	Depends on the command
2:1	Return modulation type: Mod(1:0)
0	Select flag 0: to all (ID_s is “0”) 1: if selected (via group select (pre_select)) before or during anticollision, after ID was set

Depending on the command, no addressing mode bit or only one (addressing_mode(1)) bit is used.

The power-on reset value of the parameter register is 00h.

Table 8-9. Modulation Control Using Default Commands

Mod(1:0)	Type of Modulation
00	NRZI soft locked (1 / 4 of reference time)
01	3Phase1
10	NRZI notch locked
11	FM0

The modulation coding is the same as used during short commands.

ATA5590 supports different addressing modes for read, write, and anticollision operations. The addressing mode(1:0) is stored in bits 7 and 6 of the parameter field.

Table 8-10. Encoding of the Addressing Modes Stored in the Parameter Field

Addressing mode(1:0)	Addressing Mode	Comment
11	Symbolic address, short	The lower three bits of the 4-bit symbolic address are stored in the parameter field. The block address points to the MSBlock of the page. The third bit is emulated as 0.
10	Symbolic address, long	Four bits of the symbolic address are stored in the address field. A block address can be transmitted within the parameter field.
01	Physical address mode, short	Three bits are set in the parameter field. The other address bits are automatically set to “0”. The third bit is emulated as “0”.
00	Physical address, long	The page address is stored in the 8-bit address field. The block address is transmitted within the parameter field.

Additional address information is transmitted via bits (5:3), the 8-bit address field which follows the parameter field, or both.

To shorten the communication time, the system supports a symbolic addressing mechanism. When using the address bits of the parameter fields, only value(2:0) is used.

Table 8-11. Supported Symbolic Addresses

Symbolic Addresses	Value(3:0)
Tag_ID	0000
User system information	0001
Manufacturer system information	0010

The address of page and block can be transmitted by command name or inside the forward stream as a part of the parameter, address field, or both.

8.4 Address Field

The address field is used by long commands in combination with long addressing modes to point to the EEPROM (read and program commands).

The pointer-based anticollision and group-selection commands (Group_p, Group_p_leeq, Group_p_greq, and Anticollision_pointer) use this byte to point to a bit which was addressed by the page address transmitted via the parameter field.

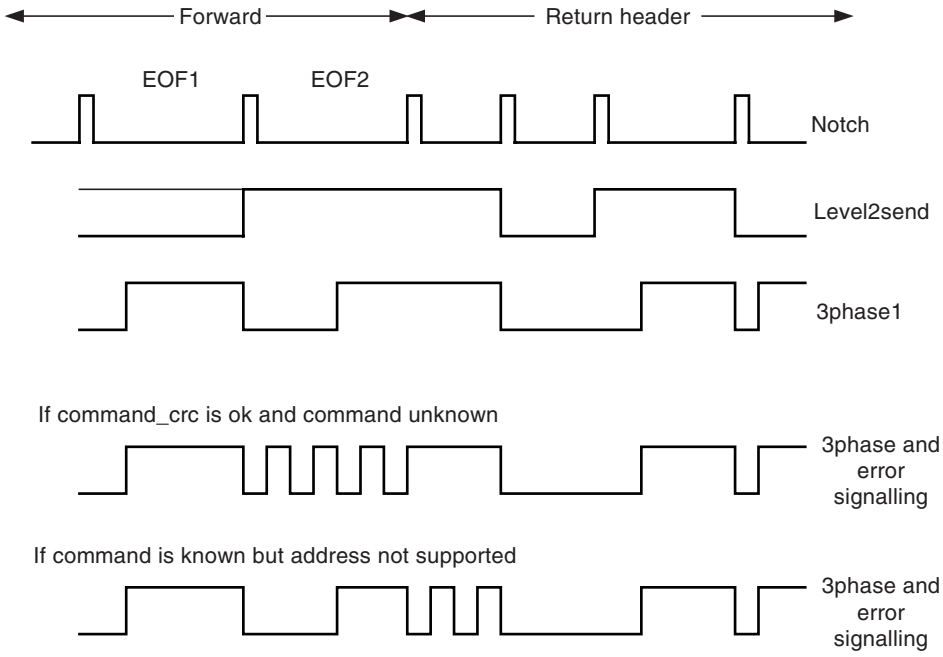
The size of the address field is 8 bits. Therefore, an address space of 32 Kbits of user memory and 32 Kbits of control memory can be addressed via read and program commands. ATA5590 uses only the lower 3 bits to point to page addresses. The other bits are ignored, but it is recommended to set them to “0” for compatibility with future IC derivatives.

8.4.1 Error Handling: Address Unknown

If the command is known and accepted by the tag, but the tag is not able to support the address information, the tag signals this by backscattering a sub-carrier during the first bit of the return link header.

Additionally, it stops backscattering the detected data during the CRC field of the forward link. During the rest of the return link, the tag does not backscatter any other information to the reader.

Figure 8-4. Error Signalling if the Command is Unknown (but CRC is Correct) or the Address is Unknown



8.5 Overview of Addressing Modes

The physical address of a memory cell is given by a block address and a bit address. The physical block address itself is generated out of the transmitted page address plus a 2-bit coded block address which together address only a block of a page. Additionally, the information about user or system memory influences the physical addressing.

To address the whole memory, 6 address bits are needed to address the physical block. Bits 1:0 represent the block address. The block address (4:2) is given by the page information, and block address (5) is given by the user/system memory information.

Group_ID, group_afi, anticollision_ID: No additional addressing information is needed, because the address is encoded in the command itself.

Table 8-12. Address Coding for read32, read32c, read128, read128c, prog4byte, prog4bytec Commands

Parameter(7:6)	Page Address	Block Address	Comment
11 symbolic long	Address(2:0)	Parameter(4:3)	
10 symbolic short	Parameter(5:3)	11	Only the MSBlock is addressed
01 physical short	Parameter(5:3)	11	Only the MSBlock is addressed
00 physical long	Address(2:0)	Parameter(4:3)	

Note: Symbolic addresses currently address only the control memory.

Table 8-13. Address Coding for anticollision_pointer, anticollision_pointer_random, group_p, group_leeq, group_p_greq, read Commands

Parameter(7)	Page Address	Block Address	Bit Pointer
1 symbolic address	Parameter(5:3)	Address(7:6)	Address(4:0)
0 physical address	Parameter(5:3)	Address(7:6)	Address(4:0)

Table 8-14. Address Coding for the Prognbyte Command

Parameter(7)	Page address	Block Address	Binary Byte Select Information
1 symbolic address	Address(2:0)	Address(7:6)	Parameter(6:3)
0 physical address	Address(2:0)	Address(7:6)	Parameter(6:3)

8.6 Data Field

To program the EEPROM, a 32-bit data field is used to transmit the contents of the block.

8.7 CRC Field

The CRC field has a length of 16 bits. The tag expects the inverted CRC value to check against the constant residue. If the residue is also correct, the command is accepted, and the tag is synchronous to the link.

If the tag is synchronous to the reader, it is possible to activate an adaptive CRC mode during the forward link. Then the tag backscatters the calculated inverted CRC value to the reader in a loop, and the reader has to send an acknowledgement. It is also possible to shorten the CRC frame, because the reader has already received the decoded data.

8.8 End of Transmission (EOT) Mechanism During the Forward Link

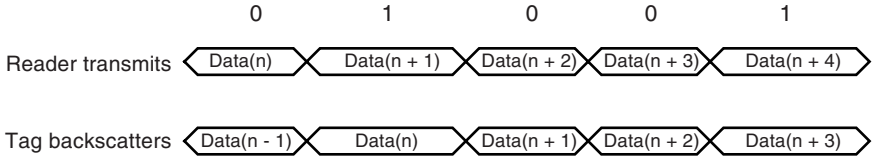
The EOT frame is built by two EOF symbols.

Note: The first symbol after the EOF1 symbol (which can be the EOF2 symbol) is used by the tag to mark the command status. Then the reader knows if the command can be accepted by the tag, or if the command CRC was correct.

8.9 Full Duplex Operation During the Forward Link

After becoming synchronous to the reader stream, ATA5590 backscatters the received and decoded data back to the reader. Therefore, the reader is able to check the link on the fly.

Figure 8-5. Modulation Scheme of the Full-duplex Forward Link



Note: If the tag does not support the command (but the command CRC was correct) or the required address information, the tag stops backscattering the received values back.

The full duplex possibility enables an adaptation possibility of the link by making the length of the CRC frame adaptive (minimum length is one bit). Furthermore, the adaptive CRC link enables longer CRC fields, if needed, because the CRC is backscattered in a loop.

Figure 8-6. Default Full-duplex Communication Flow at the Data-CRC Boundary

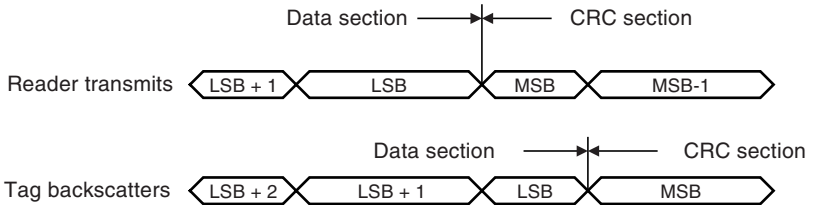


Figure 8-7. Switching Mechanism to Change to the Adaptive Forward Link CRC

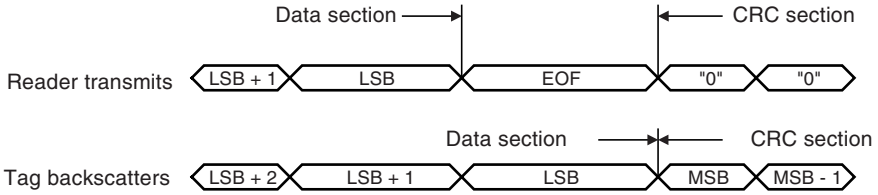
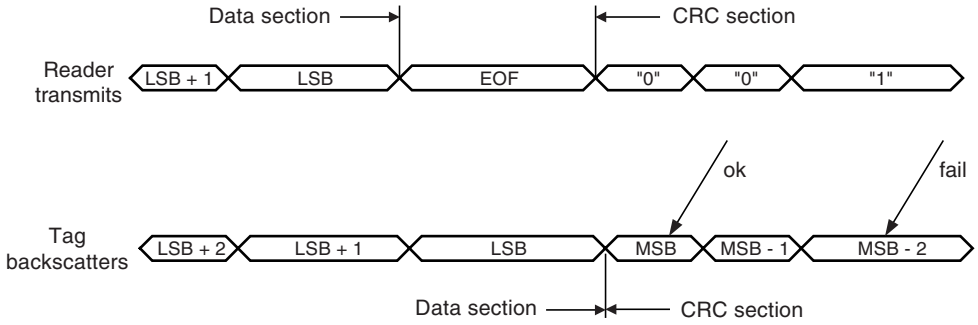


Figure 8-8. Switching Mechanism to Adaptive Forward Link Showing an Error Signalling Condition



If the tag receives a “1” because the reader has detected an error in the backscattered CRC stream, the internal crc_ok flag is set to fail, and the execution of the command is blocked. The reader can send an EOF frame directly after this logical “1”. There is no need to send 16 symbols during the CRC frame.

The CRC field is closed by an EOT sequence.

The backscatter coding style during the CRC field is based on the selected coding style of the command which was sent before.

The timing of the coding is based on the timing of 0*, which was transmitted in the forward header.

The tag expects at least one acknowledge bit. If more then 16 acknowledge bits are received, the CRC value is backscattered in a loop.

Notes:
1. The tag backscatters the inverted internal CRC value.
2. The position of the EOF symbol which is responsible for the switch mechanism has to be at the position of the first CRC bit (default mode).
3. If the position of the EOF symbol is inside the data frame, the command will not be accepted, and the tag will be asynchronous to the reader stream (EOF-wrong_position).

9. Return Link

The return link is based on a synchronous communication style in combination with 2PSK-type modulation to get maximum SNR and minimum BER values.

In synchronous mode, the tag backscatters the information regarding the bit information between two notch signals. The coding style of the return link was determined (mod flags) during the forward link. Therefore, the spectrum to be used can be adjusted by the return header.

As the backscattered signal is always very weak, the reader can tune the quality of the link by observing and analyzing the reference signals backscattered in the return link header section.

9.1 Return Link Header

The return link header is used for return link initialization, and for initialization of the full duplex communication during anticollision and group selection (deterministic-arbitration part).

The return link is controlled by this return header. The return header is used to set the following parameters for the communication style:

- The timing information of the EOF symbol of the return link, plus
- Timing information used as reference timing during the return link modulation

During anticollision and group-selection procedures, the header is additionally used for defining timing references of priority symbols.

If a static modulation scheme (notch-locked NRZI) is used during the return link, the modulation inside the return header can be used as a reference symbol for the modulation. Therefore, the first symbol is modulated, and the second symbol is not modulated. During the 3rd and 4th symbols, the tag backscatters the modulation scheme as received with the modulation control bits.

Different coding styles inside the header section:

The return header contains 4 symbols. The EOF definition which is based on timing information in the return header is mandatory for each tag. The third symbol shall have the same timing as the fourth symbol. The tag stores all length information of the return header so that it can decode EOF.

Table 9-1. Features and Agreements of the Return Header

Symbol/Function	Return Link Modulation Inside the Symbols	Comment
1st symbol Main timing, accuracy, and power management for the return link	NRZ modulation on, or sub-carrier	Can be used by the reader to adapt the baud rate of the return link. The sub-carrier indicates that the tag is not able to support the required address.
2nd symbol Timing reference	Modulation off, or sub-carrier	- 3phase1 control - FM0 control - Deterministic anticollision control symbol Note: there is a timing shift for NRZI soft-locked modulation type, if selected The sub-carrier indicates that the tag is not able to support the transmitted parameter setting.
3rd symbol Same timing as the fourth symbol	Tag backscatters a logical 1 which corresponds to the type of modulation and the timing reference of the 2nd sub_symbol	When using NIRZ, the modulation is on.
4th symbol Timing reference for EOF detection	4th symbol The modulation is like “0”	The value for level2send_old is also set to “0”

Figure 9-1. Modulation During the Return Link Header (No Error Signalling Included)

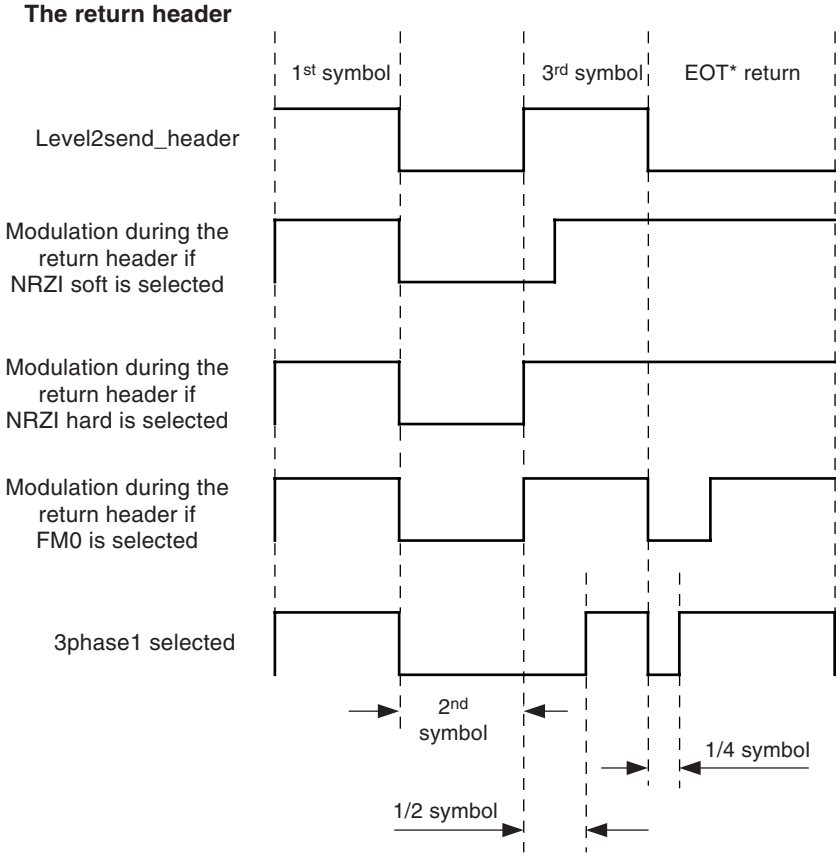
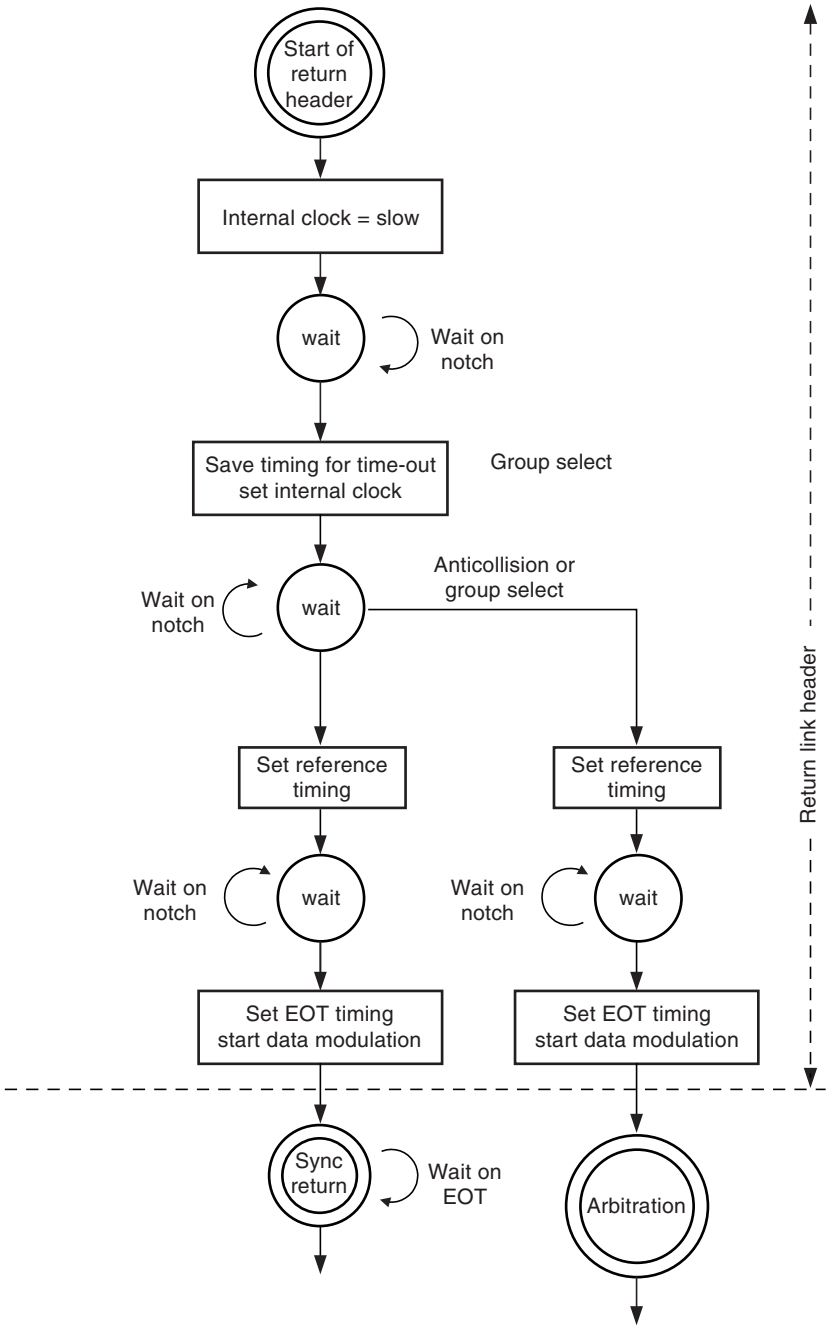


Figure 9-2. Return Link Header Flow (Error Signalling Not Included)



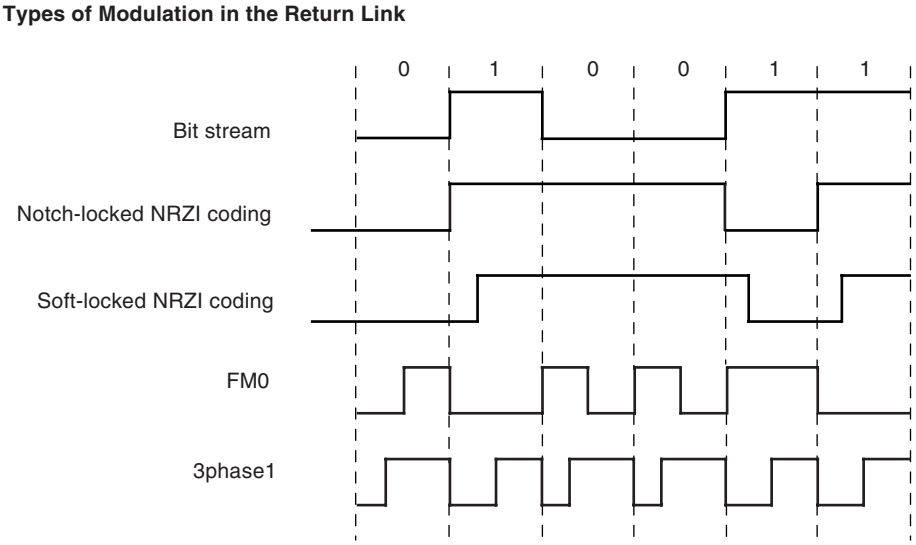
9.2 Loop Function

The synchronous return link supports a loop function. If the tag has transmitted all data and CRC fields, the reader can start the loop function by sending a new header.

The reader is free to change any value of the return link header to optimize the link and its quality.

9.3 Return Link Coding

Figure 9-3. Modulation During the Return Link



Note: In the case of NRZI, the level depends on the status one bit earlier. The last sub-symbol (4th sub-symbol of the return header) is set to high.

Note: Only FM0 and 3phase1 support a bitwise modulation references. For the other coding structures, the reader can use the modulation references of the return header.

9.3.1 Influence of the 2nd Symbol of the Return Header on the Modulation Stream

The second symbol of the return link header is used as a reference symbol which controls the timing for the not–notch-locked modulation coding. The timing is stored in an internal register. If a not-locked modulation coding type is selected, the IC compares the current time with one-quarter and one-half of this stored value. Depending on the data, the modulation switches between the notches.

Note: This feature enables a dynamic sideband management to minimize noise effects or to optimize the baud rate.

When using 3phase1, the best solution will be to shift the changes to one-third and two-thirds of the current length. Then the maximum baud rate can be achieved. During anticollision, this length information is also used as a boundary length.

9.4 Status Information

The tag transfers the information stored in the status2 register back to the reader using read or program commands.

The status2 register contains all the mandatory information and error codes which can be read out by the protocol.

Table 9-2. Contents of the Status2 Register

Index	All Commands Except Program	Program
7	0 (RFU)	0 (RFU)
6	ID	ID
5	Lock protected	Lock protected
4	1 (RFU)	1 (RFU)
3	Bit_length_not_ok	Program ok
2	Aloha	Aloha
1	(16 bits) Data CRC wrong	(16 bits) Data CRC wrong
0	0 (RFU)	0 (RFU)

A “1” in the bit_length_not_ok flag indicates that each received symbol was longer then the minimum length of the bit.

Note: Data CRC is not supported for short commands. If the command CRC is wrong, the sync condition will be reset to “0”.

9.5 Data Field

The data field is backscattered in a loop. The length of the data field is defined by the command.

9.6 CRC Field

The CRC field has a length of 16 bits. The equation is the same as in the forward link. The CRC field is calculated over all data (status and data field), except in the case of anticollision and group-selection commands.

For wake-up commands, the CRC is not calculated over the slot region.

For anticollision and group-selection commands, the CRC of the return link is based on all data fields of the forward and return link.

The tag backscatters the inverted value of the CRC register back to the reader.

The length of the CRC field can be adapted by using advanced communication modes.

9.7 EOT Frame

The EOT frame contains two EOF symbols.

9.8 Adaptive Return Link CRC Field

During return link operation, ATA5590 supports an adaptive CRC field.

In the case of anticollision and group-selection commands, the function must be enabled by a bit in the parameter field. The control bit is called nCRC_adapt. If this bit is set to “0”, the CRC has a fixed length. If the bit is set to “1”, the bit count of the CRC is under the control of the reader.

To activate this mode for all the other commands, the reader has to send an EOF symbol in the LSB position of the data frame. After receiving the EOF symbol, the tag backscatters the CRC value in a loop.

The tag observes the data stream coming from the reader during this adaptive period. The reference for decoding this acknowledgement is the 2nd symbol of the return link header. A time shorter than this reference results in a “0”, otherwise in a “1”.

A timing longer than the 4th symbol (EOF reference) results in an EOF.

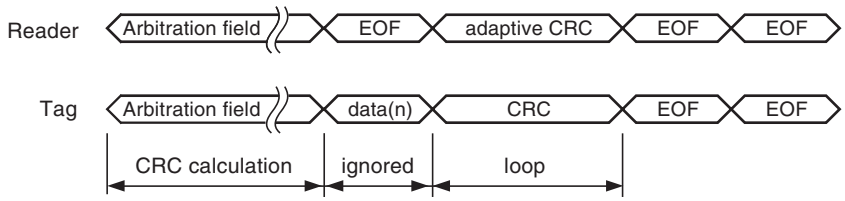
The tag expects at minimum one acknowledge bit; then a new header can follow.

ATA5590 checks the PIE information transmitted by the reader for anticollision and group-selection commands. A “0” is interpreted as a pass, and a “1” is interpreted as a fail. An EOF is interpreted as the end of the CRC field.

After receiving the second EOF symbol, the tag can change the status1 register contents.

Notes: 1. The data information which was backscattered during the EOF symbol is not part of the CRC calculation.
2. The CRC frame has a minimum length of one bit.

Figure 9-4. Adaptive CRC Field During Group-selection and Anticollision Procedures



The CRC field can also be adaptive for commands other than anticollision or group selection. If the reader transfers an EOF symbol instead of the last data bit, the CRC field is also adaptive after reception of this bit.

Note: The data which is backscattered during the EOF field is not part of the CRC calculation.

During the adaptive CRC field, the tag observes the data stream coming from the reader. The loop function is active as long as the tag receives a “0”. If the tag receives a “1”, it expects a new return link header. If an EOF is received, it expects an additional EOF to generate the EOT.

10. Detailed Command Description

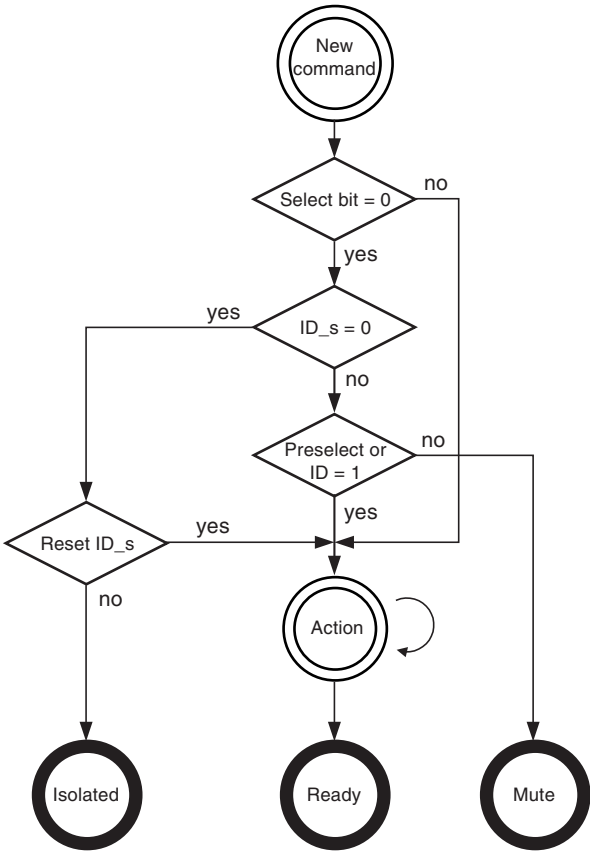
10.1 Common Parameters

All commands are based on common parameter bits:

- Define the encoding schema of the backscatter modulation — mod(1) and mod(0)
- Define if the tag has to consider the results of the arbitration or group_select mechanism stored in status2, the select bit.

Additionally, some commands support pointers to EEPROM addressing.

Figure 10-1. Principle of the Selection Flow



If the select bit is set in the parameter field (parameter(0)) or implemented in the command (short commands), then the ID_s, ID, and pre_select flags (status1) influence the execution flow as shown in Table 10-1.

Notes: 1. All anticollision commands check only the pre_select flag of status2, if required (select bit).
2. If a deterministic arbitration was activated before the following read and write commands, check only the arbitration status bit, otherwise, the pre_select bit.

10.2 Reset Command

After receiving the forward header, the reset command, the parameter, and the 16-bit CRC, the tag generates a complete or a partial soft reset. The command byte is 2Bh including the 2-bit command CRC. The selection mechanism is defined by the parameter field:

Table 10-1. Parameter Field

Index	Function
7	Reset all registers except status1
6	Reset ID_s
5	Reset ID
4	Reset pre_select
3	0 (RFU)
2:1	Return link modulation
0	Select

If parameter(7) is set to “1”, no answer is backscattered to the reader because the tag is asynchronous to the reader. Therefore, the next notch is interpreted as the beginning of the next forward header.

In the case of any other parameter settings in the reset command, the tag backscatters status1 and crc16 back, if the select criterion is valid.

This means that if the select bit (parameter(0)) is “0”, the message will be backscattered. If the select bit is set to “1”, and after the reset neither pre_select nor ID is set, then no answer follows.

Notes:
1. To reset the status1 register, the special bits in the parameter field have to be set separately.
2. Reset ID_s is also possible if the ID or pre_select status bits are set, and the select bit (parameter(0)) is set to “1”.
3. Parameter(3) shall be set to “0” to enable future expansion possibilities (2nd reset address).
4. If the select bit is set to “1”, the tag will not respond in the return link if the reset command has reset the select condition.
5. If the select bit is set to “1”, and the select condition is not valid for the tag, the tag stops backscattering the received symbol in the forward link after it has received the parameter field.

10.3 Read Commands

10.3.1 Read32 and Read32c

The read32 command reads a block (32 bits) of the memory. Read32c reads a block of the control memory. Short, long, and symbolic addressing modes are supported. After receiving the header, the command, the parameters, and, optionally, the address field (long addressing mode), the tag expects the CRC stream (inverted CRC), and then two EOF symbols.

After getting the two EOF symbols, the tag expects the return header. When this is received, the tag returns the status2 register, and the 32-bit + 16-bit CRC data.

After transmitting the last bit, the tag expects two EOF symbols. If it does not receive them, it assumes that the reader is transmitting a new header, and the tag enters loop status.

The command byte is:

- 13h (read32) or
- 91h (read32c)

The above values include the 2-bit CRC value.

Table 10-2. Construction of the Forward Link for Read32 Commands

Short Read User Memory	Header	Command	Parameter	CRC	EOT	
Short Read Control Memory	Header	Command	Parameter	CRC	EOT	
Long Read User Memory	Header	Command	Parameter	Address	CRC	EOT
Long Read Control Memory	Header	Command	Parameter	Address	CRC	EOT

Table 10-3. Parameter Field of the Read Commands

Index	Function
7:6	Addressing mode
5:3	- 3-bit short address (short addressing modes), or - 2-bit (4:3) block address (long addressing mode); index(5) must be “0”
2:1	Return link modulation
0	Select

When using long addressing modes, the page or symbolic page address is stored at address(2:0). To avoid future incompatibility, the other bits in the address field should be set to “0”.

10.3.2 Read128 and Read128c

The read128 command can read the full page of the memory. Read128c addresses a page in the control memory. Short, long, and symbolic addressing modes are supported. After receiving the header, the command, the parameters, and, optionally, the address field, the tag expects the CRC stream (inverted CRC), and then the two EOF symbols.

After getting the two EOF symbols the tag expects the return header. Then the tag transfers the status2 register and the 128-bit + 16-bit CRC data back.

After transmitting the last bit, the tag expects the two EOF symbols. If it does not receive them, it assumes that the reader is transmitting a new header. The tag enters the loop status.

The command byte is

- 30h (read128)
- 98h (read128c), and includes the 2-bit command CRC

Table 10-4. Construction of the Forward Link for prog4byte Commands

Short Read User Memory	Header	Command	Parameter	CRC	EOT	
Short Read Control Memory	Header	Command	Parameter	CRC	EOT	
Long Read User Memory	Header	Command	Parameter	Address	CRC	EOT
Long Read Control Memory	Header	Command	Parameter	Address	CRC	EOT

Table 10-5. Parameter Field of the Read Commands

Index	Function
7:6	Addressing mode
5:3	- Short address (short addressing modes) - (4:3) start block (long addressing mode); index(5) shall be set to “0”
2:1	Return link modulation
0	Select

When using long addressing modes, the page address is stored at address(2:0). The other bits of the address field shall be set to “0”.

The start address of the block is stored at parameter(4:3). Parameter(5) shall be set to “0”.

10.3.3 Get_ID Page

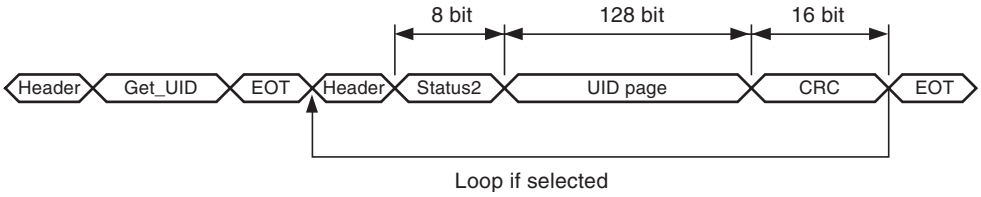
Get_ID page is a short command. After receiving the header, the tag expects only the 8-bit command frame, the EOT frame, and the return header. Then it starts backscattering the status2 information and the expected data (entire ID page).

Table 10-6. Command Frame of the Get_ID Command

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	0	1	Mod(1:0)		CRC(1:0)	

After backscattering the data, the tag inserts the inverted 16-bit CRC into the stream. The information is then backscattered in a loop (synchronous return link).

Figure 10-2. Command Flow of the Get_ID Page



10.3.4 Get_system Information

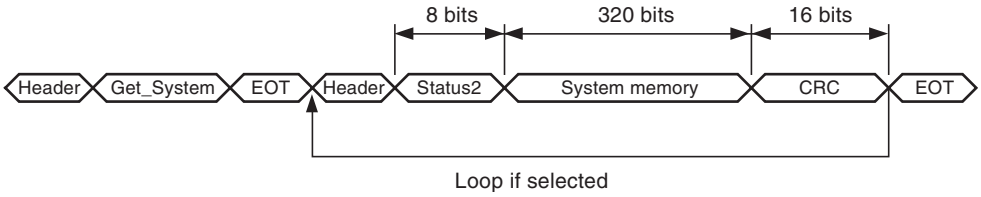
Get_system information backscatters the status, the 64-bit manufacturer system information, the 128-bit user system information, the 128 bits of the ID page, and the 16-bit CRC information back to the reader.

Table 10-7. Command Frame of the Get_system Command

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	0	1	Mod(1:0)		CRC(1:0)	

The information is backscattered in a loop (synchronous return link).

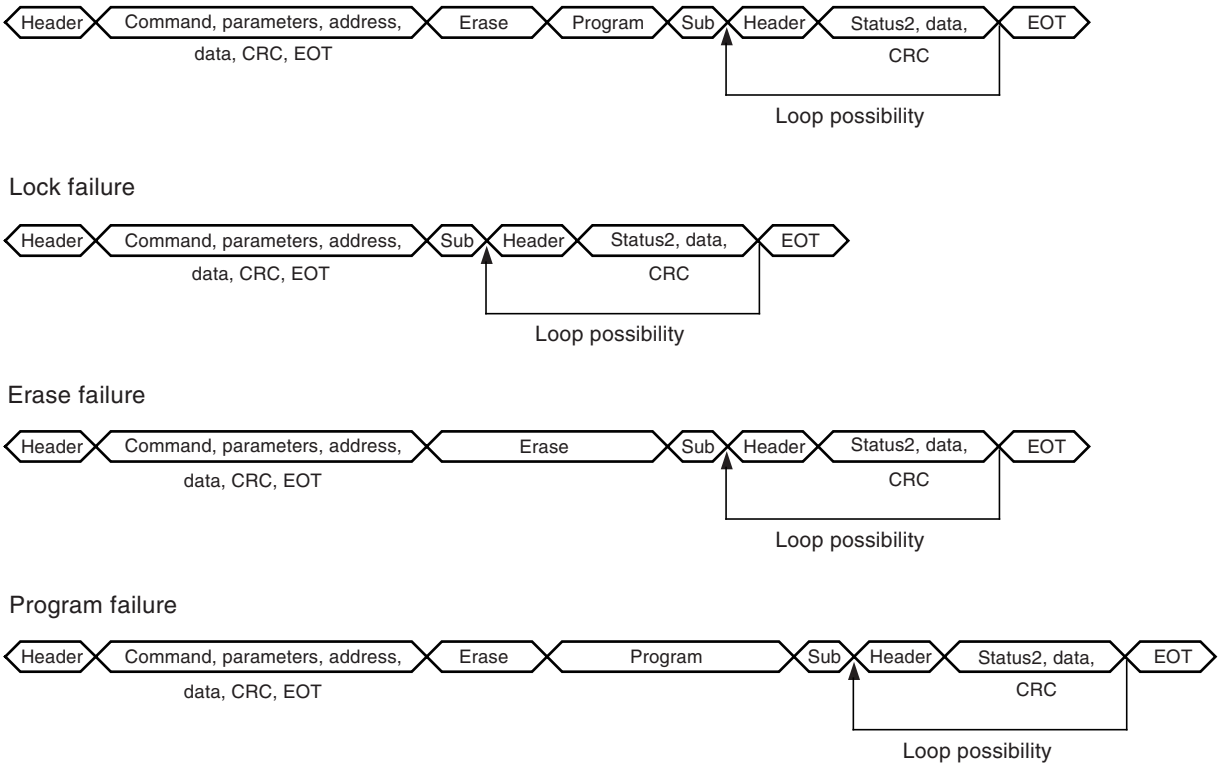
Figure 10-3. Command Flow of the Get_system Information Command



10.4 Program Commands

10.4.1 Programming Sequence

Figure 10-4. Programming Sequence in More Detail



ATA5590 checks the access rules during the forward EOT sequence. The erase phase starts if programming access is allowed. After the erase, the whole block is programmed. When this step is finished, ATA5590 backscatters a sub-carrier back to the reader indicating that the programming sequence was successful.

If the program access is forbidden (lock failure), the tag skips the erase and the program cycle, and backscatters a sub-carrier directly after the EOT sequence of the forward link.

ATA5590 is based on a closed-loop programming time management concept which adjusts the programming time to the RF conditions (field strength). The time for programming is limited. If the maximum time is reached, a time-out occurs, and ATA5590 backscatters a sub-carrier.

If the erase or programming cycle fails, the tag backscatters a sub-carrier frequency.

If programming was successful, the sub-carrier frequency is defined by internal frequency / 4; otherwise, by internal frequency / 8.

Note: The internal frequency is adjusted by the first header sub-symbol.

10.4.2 Prog4byte and Prog4bytec

The prog4byte and prog4bytec commands enable a programming sequence after receiving the complete command successfully. After programming, the tag expects the return header. Then, it transfers the status information and the data (read out of the EEPROM) back. The return link then looks the same as the return link of a read32 command.

Table 10-8. Construction of Forward Link (Prog4byte Command)

Short Program User Memory	Header	22h	Parameter	32-bit data	CRC	EOT	
Short Program Control memory	Header	83h	Parameter	32-bit data	CRC	EOT	
Long Program User Memory	Header	22h	Parameter	Address	32-bit data	CRC	EOT
Long Program Control Memory	Header	83h	Parameter	Address	32-bit data	CRC	EOT

The type of modulation coding after programming is defined in the parameter field. During programming the reader has to transmit a carrier wave.

Table 10-9. Parameter Field of the Prog4byte Command

Index	Function
7:6	Addressing mode
5:3	Page address (short addressing modes) (4:3) block address (long addressing mode); index(5) shall be set to “0”
2:1	Return link modulation
0	Select

Note: Currently, each block of the whole memory can be programmed by using the prog4byte command and the symbolic addressing mechanism.

10.4.3 Prognbyte

Prognbyte is a long command supporting the address field. With this command it is possible to program only a portion of the selected block. The block and the page information are transmitted in the address field.

The program code is 63h, and includes the 2-bit command CRC

If the page is locked, only the upper byte (admin byte) of the upper block is changeable. Then this byte works the same as an OTP memory.

Table 10-10. Parameter Field of the Prognbyte Command

Index	Function
7	Addressing mode 0: physical addresses (page and block) in the address field 1: symbolic address and block address in the address field
6:3	Byte select(6) = MSByte of the block Byte select(3) = LSByte of the block
2:1	Return link modulation
0	Select

Table 10-11. Address Field Supported by the Prognbyte Command

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address field(7:6)		Address field(5:3)			Address field(2:0)		
Block(1:0)		000			Physical page(2:0) or Symbolic address(2:0)		

Special cases regarding

- System memory access
  - The upper byte of the second block of the manufacturer page can still be changed after the sawing step.
  - The upper byte of the user system information is blocked after locking. The three lower bytes of the upper block are still changeable after locking the page. Therefore, the lock bit of the page is not active while prognbyte is programming the upper block of the user system memory.
  - It is possible to change the upper byte of the manufacturer system information (trigger control), but first the chip must be pre-selected, and the select flag in the parameter field must be set to “1”.
- User memory access
  - After locking the page, prognbyte can still change the upper byte of the upper block of each page, but erase is blocked. Then an OTP mode is enabled.

11. Anticollision Procedures

ATA5590 supports an Aloha-based selection procedure, a deterministic selection procedure, and the mixture of deterministic and Aloha.

Additionally, the deterministic anticollision procedure supports non-unique ID structures (migration path).

To get a first impression about the situation, a wake-up command is transmitted. Each addressed tag in the field modulates one of the 16-bit slots which are part of the return link. If the reader has not seen a modulation in more than one slot, then there is the possibility that only one tag is in the field. After the slot window is closed, the tag backscatters the ID information automatically.

A deterministic procedure is based principally on long commands containing the command, the parameter field, and, for special commands, an address field. To minimize the time for deterministic anticollision procedures, ATA5590 supports a short command called repeat_arb. After receiving this command, the last command is repeated if it was received successfully. To solve problems where the ID is not unique, or to solve the problem of virgin tags, ATA5590 can insert a 16-bit random value. Then the ID need not be unique.

Deterministic procedures can set status1 flags (storage time 8 seconds without external power at 25°C). Deterministic anticollision procedures operate in full duplex mode, allowing very fast operation. The data rate is under the control of the reader. After selection, the tag is free for operation (reading, programming, etc.).

ATA5590 also supports an Aloha-based anticollision procedure. The system is based on slot commands (short commands), and a slot value of 32. Each tag calculates a random value at the beginning of Aloha. This random value is then the slot number during which the tag switches to an active state (enabling operation and backscattering).

To get a first impression if there is a tag in the field, each tag operates in two slots

- The first slot, and
- An additional slot (1 out of the next 31 slots).

The user is free to mix the two anticollision modes.

12. Aloha-based Anticollision Procedure

Aloha anticollision is based on a slot mechanism. A tag calculates a slot number by a random counter.

Inside each slot, a tag can communicate with the reader if the calculated slot value is the same as the slot number which is under control of the reader.

ATA5590 generates a slot number between 1 and 31. The first slot is used by each tag. If only one tag is there, the reader has the full access to it during this first slot.

Therefore, the Aloha system is based on 32 slots. The maximum number of slots is fixed.

The Aloha procedure starts with

- Slot, or
- Slot_selected, or
- Slot_not_selected

Therefore, the reader is able to control the participants by group or deterministic anticollision commands. If ID_s was set before, the tag is silent.

After receiving a slot command, the tag backscatters the 16-bit random value, and the contents of the ID page (128 bits) back to the reader. The same ID information is backscattered if the slot number is the same as the slot number given by the reader, and the tag was selected before. The slot counter is incremented by each of the above mentioned slot commands. If the reader wants to have a message repeated, it can transmit the slot_repeat command. The Aloha procedure is closed by the slot_close command. If the reader has detected a collision (for example, during the random value, if the ID was not unique), the reader can skip the slot by sending the command skip_slot.

The reader is also able to use all the other commands during Aloha, including deterministic anticollision and group-selection commands. Therefore, the Aloha procedure which is implemented in ATA5590 does not need an adaptive round mechanism.

The status2 register which is backscattered after long commands also contains the Aloha information (status2(2)).

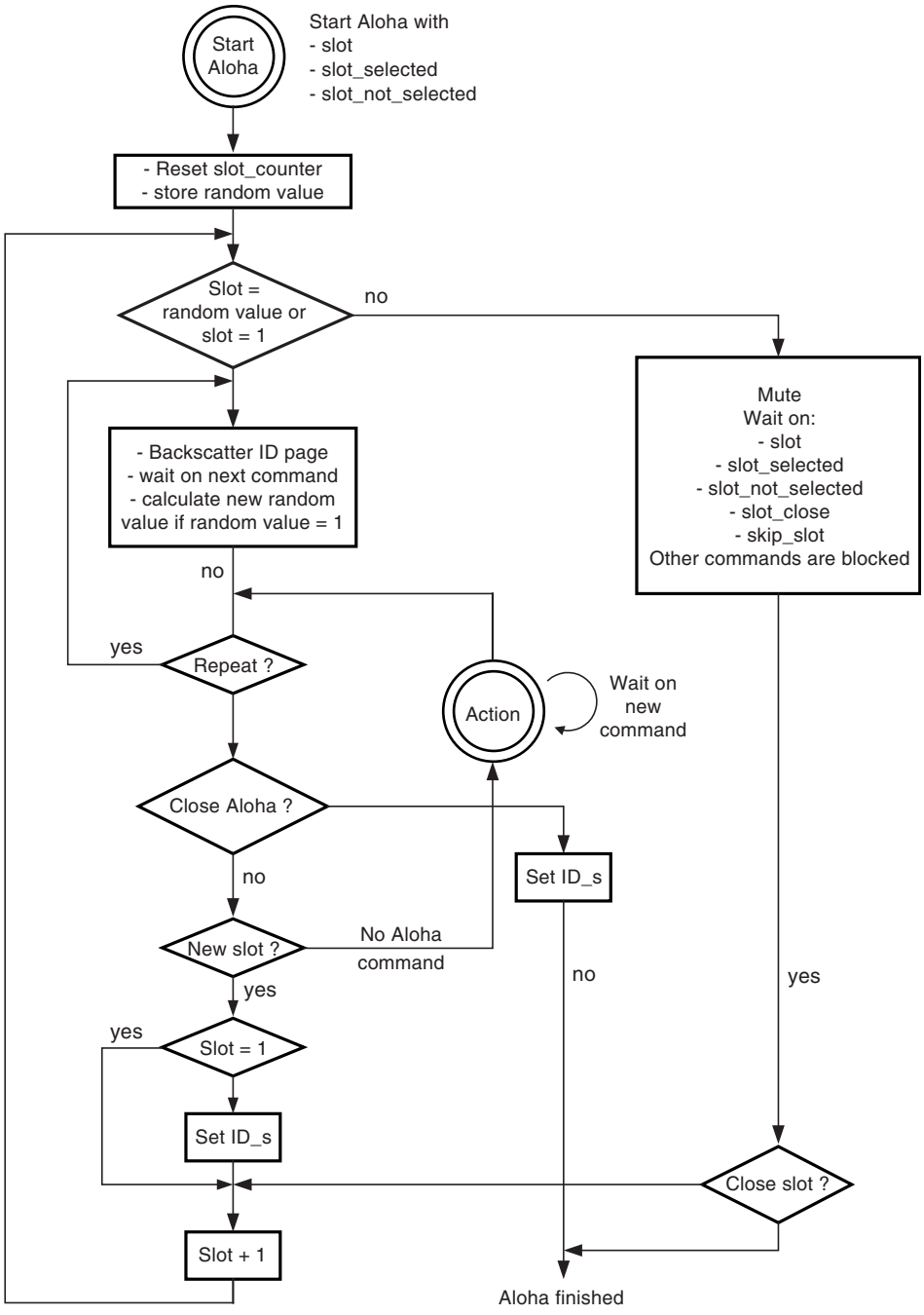
If the communication was started in Aloha mode, the tag enters the isolated state (ID_s is set) when:

- The slot number is equal to the internal slot number (on-chip), and
- When it receives a slot command

ID_s can be reset by the reset command.

If the reader transmits deterministic anticollision commands during an active slot, the ID and the ID_s flags work as described in Figure 12-1 on page 80.

Figure 12-1. Aloha Selection Process



13. Deterministic Arbitration and Group Selection

ATA5590 supports deterministic-based anticollision procedures as well as a group-selection mechanism. After initializing the link, an arbitration procedure follows. During these procedures, the link between the reader and tag is full duplex.

This means that the tag backscatters its internal (memory) value back to the reader, while the reader transmits priority information to the tag. This priority information is used as a confirmation from the reader to indicate the priority decision of the reader. The information is PIE. The reference length of PIE is transmitted by the reader during the return link header.

As opposed to Aloha-based anticollision routines (Aloha-based routines backscatter a stream only if the slot number is equal to the internal (random) number), in deterministic-based routines, the tag backscatters as long as the compare condition is true.

Therefore, it is possible for more than one tag to backscatter its information during one bit.

The deterministic-based anticollision routines are the same as for group-selection commands. The difference is the effect on the register status1.

The differences between group and deterministic anticollision commands are

- During group selection, the tag backscatters its value, but the reader is free to observe the communication. In any case, the reader is able to check if there is a tag which can be addressed by this priority code.
- Group selection supports a hierarchical mechanism
- Group-selection commands only affect the pre_select flag (set and reset mechanism).
- Deterministic anticollision commands work the same as group-selection commands. The reader is free to interpret the backscattered value.
- Deterministic anticollision commands affect the ID flag (set). Deterministic anticollision supports only a set mechanism for ID and ID_s.
- If the tag receives a second anticollision command and ID was set before, the tag will be silent and ID_s will be set.
- A reset of the status1 register flags is possible by a reset command.

Deterministic anticollision procedures are mainly used to select one out of *n* tags. For such applications, ATA5590 supports several commands addressing different application scenarios. A main feature of ATA5590 is that it does not need unique ID structures for arbitration because the arbitration can also be based on random values.

This makes it possible to use this mechanism to program virgin tags, which are in a box, for example, with unique identifiers.

The random value has a maximum size of 16 bits. After each deterministic access, the selected tag is in a mute state. All the other tags calculate a new random number, and if the reader sends either this command again or the repeat_arb command, the reader can fetch the next tag. Then the 16-bit random number that was calculated by the tag which is now in the mute state, can be used again. Therefore, this algorithm is not limited by the size of the random value.

13.1 Anticollision Status Register

The status1 register contains the information of the anticollision procedure. A part of this register can be read out. The value of the status1 register is stored up to 8s (at 25°C) after the supply voltage falls below an internal POR voltage level. The storage time depends on fabrication tolerances and temperature effects, and will increase if the temperature is below 25°C or decrease if the temperature is higher than 25°C.

After getting power back (POR), the status of the register will be refreshed, which means that the IC stores back the load information of a capacitor into the register. Therefore, only logical information will be refreshed. Due to the leakage current of the circuit, the capacitor loses the stored information over time. If this charge is less than a certain value, the contents is interpreted as a logical 0.

To reset the register contents, the carrier must be switched off for a certain amount of time (a function of the temperature as explained above), or the reader has to send a reset command (control bit and selection condition must be true).

The stored values are

- ID_s: The tag was identified (selected) during arbitration, and is in the sleep state now. The tag can receive any stream coming from the reader and analyze it, but the tag will not act unless the reset condition is true.
- ID: The tag was identified (selected) during arbitration, and has not received a new anticollision command. The reader can communicate with all selected tags.
- Pre_select: The tag was identified by a group select command and the result was true. The reader can communicate with all tags which are pre-selected by setting the select bit or choosing the right short command.

Group-selection commands affect only the pre_select bit, whereas anticollision commands are influenced by the ID and the ID_s flags. The reader can use the pre_select and ID flags to control the functionality of the tag.

After releasing an anticollision procedure by the tag, the backscatter link is controlled by the ID and ID_s flags. If an anticollision procedure is started, the tag backscatters information to the reader:

- If it has not won an arbitration during the last arbitration field
- If ID is set and ID_s is “0”
- If the reader sends a short command, the tag answers if ID is set and ID_s is ”0”

If ID_s is set, the tag must receive a reset command before beginning new communication, or the RF power must be switched off for a certain time (> 8s at 25°C)

13.2 Deterministic Anticollision Procedure in Principle

The anticollision procedure is based on the contents of register status1 (ID_s, ID, and pre_select), and the internal signal arbitration lost. The power-on reset (POR) signal does not reset this status1 register, but the contents is refreshed during each POR and general reset. The internal signal arbitration lost is not persistent, meaning that it will be reset if a POR occurs.

Figure 13-1. Flow Inside the Anticollision Procedure (nCRC_adapt is Set to “1”, Therefore, the Inverted CRC is Backscattered to the Reader)

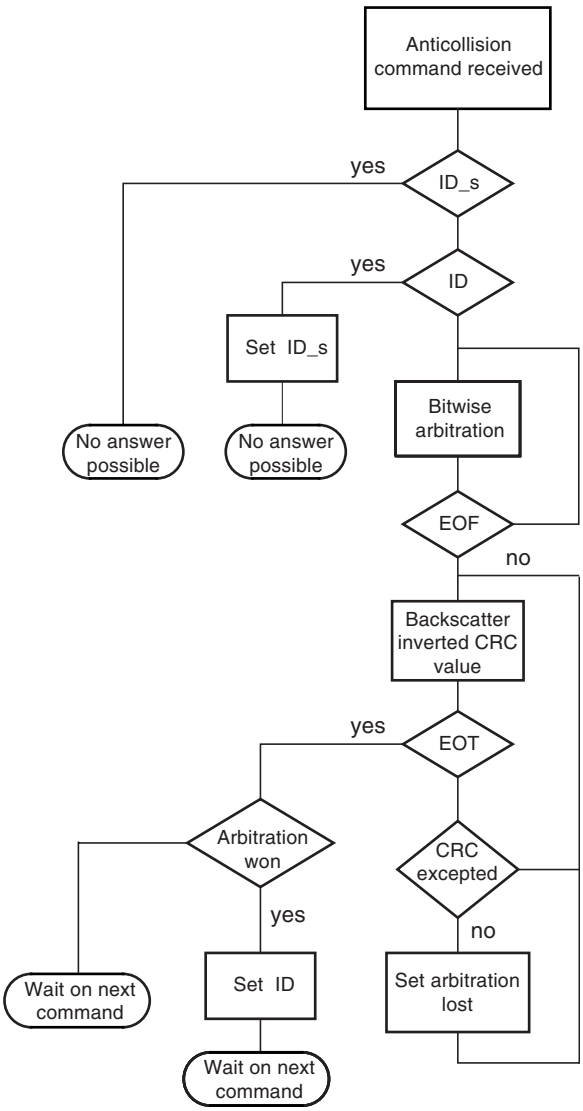
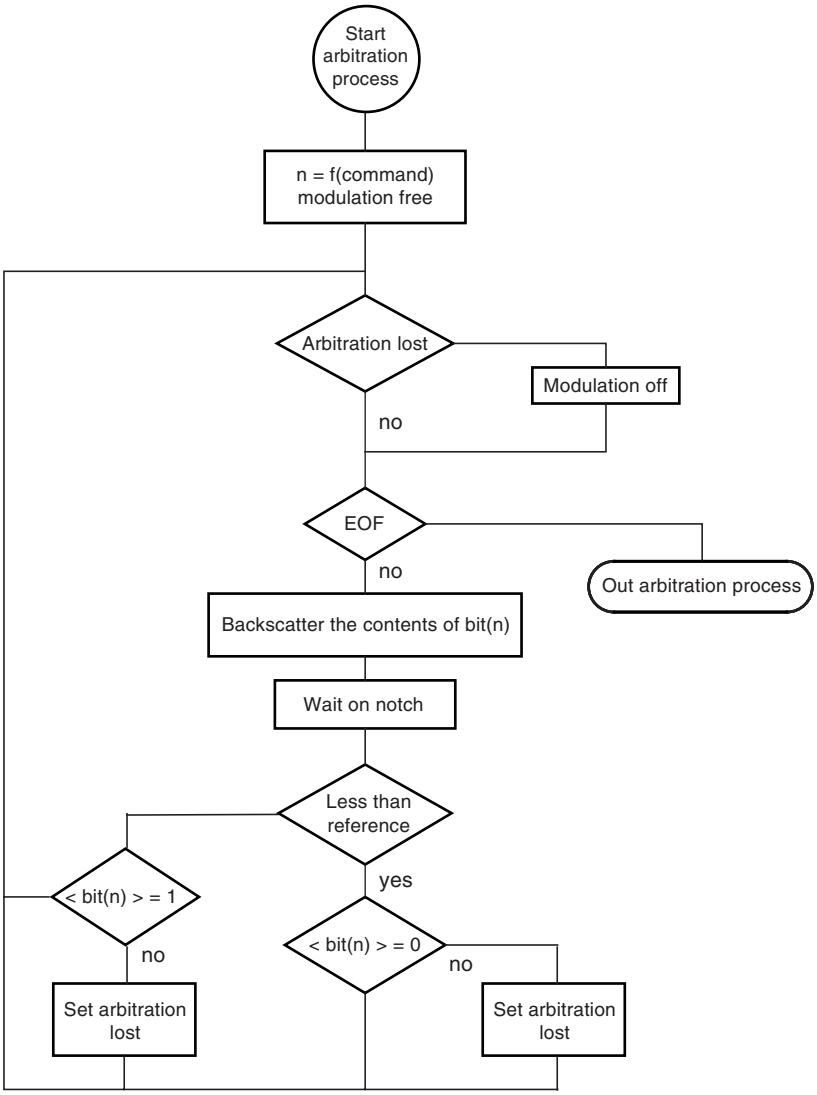


Figure 13-2. Arbitration Flow



The arbitration procedure during anticollision is based on full duplex communication. The tag shares its internal bit value with the reader. The reader then has several options:

- The reader dictates a select stream. Then in reality, a group-selection mechanism is enabled but the pre_select flag is not affected.
- The reader interprets the backscattered signal and decides which priority will go forward. Therefore, during arbitration, a change of priority can be realized any time
- The reader analyzes the level of the backscattered signal and the backscattered value. Then the reader chooses the tag with the highest level.

The arbitration works bit by bit. The reader itself defines the selected priority by the PIE signal during the arbitration. The timing reference is defined in the return link header. After each bit, the tag decides whether the arbitration is won or lost. If the arbitration is lost, the tag does not change the state of the modulator, meaning that it no longer modulates the antenna impedance. The decision is under control of the reader station because the reader observes the backscattered modulation during the bit, and can therefore decide which data is backscattered by the tag. The control mechanism is based on the timing information between two notches and the reference time transmitted during the header. If the time is less than the reference length (2nd symbol of the return header), then the tag which has backscattered a “0” has won the arbitration. If this time is longer, the tag which has backscattered the “1” status has won otherwise lost.

Note: The time for a logical 1 shall be less than the time for the EOF.

13.3 CRC Calculation During Anticollision and Group Selection

The tag calculates a CRC over the command, the parameter, and the arbitration field. The header and the EOT symbols are not part of the calculation. During arbitration, the calculation is based on the internal values of the memory and, if activated, over the random value.

13.4 CRC Condition

The flag nCRC_adapt in the parameter field decides the function of the CRC communication.

If it is set to “1”, the tag expects the inverted 16-bit CRC information from the reader to decide if the result of the arbitration will be accepted.

If it is set to “0”, the tag backscatters the inverted value. The tag backscatters the CRC in a loop (rot_l), and expects from the reader a “0” for each bit (shorter than the second symbol of the return header). If the tag detects a “1”, it sets an arbitration_lost flag internally, and stops backscattering. No status register flag of register status1 will be set.

Note: It is enough to send one logical 1 (nCRC_adapt = 1). Directly following, the reader can send the EOF sequence.

13.5 Set and Reset Conditions of Status1 Register Flags

13.5.1 Common

Set and reset conditions are based on the result of the arbitration over the data field in conjunction with the result of the CRC field. If the tag receives an error during the CRC field, the result of the arbitration over the data field will be ignored.

13.5.2 Set Condition of Pre_select

- If the pre_select flag was set and a power-on reset has occurred (reload function after POR)
- If a group command was in use, the tag has won the arbitration, and the tag did not receive an error during CRC

13.5.3 Reset Condition of Pre_select

- If the pre_select flag was not set, and a power-on reset has occurred (reload function after POR)
- If a group command was in use, and the tag did not win the arbitration (new relative to Palomar)
- Reset command and the pre_select flag inside the parameter field was set (new relative to Palomar)

13.5.4 Set Condition of ID

- If the ID flag was set, and a power-on reset has occurred (reload function after POR)
- If an anticollision command was in use, and the tag won the arbitration

13.5.5 Reset Condition of ID

- If the ID flag was not set, and a power-on reset has occurred (reload function after POR)
- Reset command and the ID flag inside the parameter field was set (new relative to Palomar)
- If the group_select command has resulted in a lost arbitration condition

13.5.6 Set Condition of ID_s During Deterministic Anticollision Procedure

- If the ID_s flag was set, and a power-on reset has occurred (reload function after POR)
- If an anticollision command was transmitted by the reader, and the ID flag was set before.

Note: During Aloha-based procedures, the ID_s flag will be also set if the tag was active (slot number equal to internal random number), and the slot number changes or the slot will be closed.

13.5.7 Reset Condition of ID_s

- If the ID_s flag was not set, and a power-on reset has occurred (reload function after POR)

Reset command and the ID_s flag inside the parameter field was set (new relative to Palomar)

13.6 Set and Reset Conditions of the Internal Flag Arbitration Lost

Each communication between tag and reader is influenced by the arbitration lost flag. As long as this flag is set, the tag does not backscatter any information to the reader. In fact, arbitration lost consists of two flags:

- The arb_lost_data flag, and
- The arb_lost_CRC flag

If the arb_lost_data flag is set to “1”, it can influence the pre_select, ID, or ID_s flags. If the arb_lost_CRC flag is set to “1”, the reader has indicated that the current anticollision or group-selection command has no influence on the status2 register.

13.6.1 Set Conditions of the Arb_lost_data Flag

During arbitration, if the tag has gotten acknowledgement from the reader that the reader wants to continue with another priority, this flag is set to “1”.

13.6.2 Set Conditions of the Arb_lost_CRC Flag

Synchronous deterministic arbitration is followed by a CRC field. If the tag has detected an error (wrong CRC transmitted by the reader, or the reader has sent a “1” to the tag), then this flag is set to “1”.

13.6.3 Reset Conditions of Both Flags

- During power-on reset or during the reset command
- During the return link header if the tag has received a Get_ID, Get_System, Wakeup_sb, slot, slot_sb, slot_s, slot_close or slot_skip command
- During the return header, if the tag has received a default command, and the parameter(0) flag was set to “0”
- During the return header, if the tag has received an anticollision or group_select command

13.6.4 Additional Reset Condition of the Arb_lost_data Flag

During Group_AFI a joker (00h) can be set. During this field the tag can lose the arbitration, but as long as the tag receives a “0” in this 8-bit field, the arb_lost_data flag will be reset.

13.7 Anticollision and Group-selection Commands

13.7.1 Anticollision_ID and Group_ID

The default Anticollision_ID and Group_ID commands are based on the Tag_ID. The Tag_ID type is stored at page 0 of the control memory.

The commands are

- 0Fh (Group_ID), and
- 01h (Anticollision_ID)

and they contain the 2-bit command CRC.

A parameter field follows the command field.

Table 13-1. Default Parameter Field of the Anticollision_ID or Group_ID Command

Index	Function
7	0
6	nCRC_adapt 0: adapt CRC 1: CRC will be transmitted by the reader
5:3	000
2:1	Return modulation type 00: NRZI soft locked 01: 3phase1 10: NIRZ notch locked 11: FM0
0	Selection control 0: to all tags in the field 1: to all selected tags in the field ((pre_select or ID) and not ID_s)

The structure of the whole frame is given by:

Table 13-2. Flow of the Anticollision_ID Procedure

Forward header	Anticollision_ID command	Parameter	EOT	Return header	Arbitration over ID	EOF	CRC	EOT

Notes: 1. EOT consists of 2 EOF symbols.
2. The arbitration field also points to lower pages because the address is decremented automatically.

The arbitration starts with bit 103 (MSB of the LSByte of block 3, page 0 of the control memory). Therefore, it starts with an 8-bit preamble (DSFID) which is used to describe the structure of the ID. This also enables a migration path from other ID structures.

The arbitration can be closed at each bit by transmitting an EOF symbol. If the arbitration round has reached bit 0 of the Tag_ID page, the arbitration goes further with bit 127 of page 7 of the user memory area, which is the upper page of the user memory area.

13.7.2 Further Possibilities of Group_ID Command

If the arbitration starts with bit 71 (MSB of the lowest Byte of block 2), bit 3 of the parameter field must be set to “1”. Then the space (bit 103 to 72) can be used for other kinds of data.

Table 13-3. Start Address of Arbitration as a Function of Parameter(3)

ID Page	Byte 3	Byte 2	Byte 1	Byte 0
Block 3				Bit 103 if parameter(3) = 0
Block 2				Bit 71 if parameter(3) = 1
Block 1				
Block 0				

The group_ID command can change the equation for comparison from = to ≤ or ≥. For a comparator other than equals, parameter(4) must be changed to “1”. Then parameter(5) defines the new equation: “1” for ≥, and “0” for ≤

Table 13-4. Rule Set for Comparison

Parameter(5:4)	Comparison
00	Reader stream = EEPROM value
10	Reader stream = EEPROM value
01	Reader stream ≥ EEPROM value
11	Reader stream ≤ EEPROM value

If the comparison is true, the pre_select flag will be set, if not the pre_select flag will be reset.

Note: If the select flag was set in the parameter field and the comparison condition was false, then the ID flag will also be reset.

13.7.3 Further Possibilities with Anticollision_ID Command

The start address of the arbitration can be selected by the parameter field.

- Parameter(3): If set to “0”, the arbitration starts in block 3 of the ID page; if set to “1”, it starts with block 2 of the ID page.
- Parameter(5:4) points to the byte of the selected block

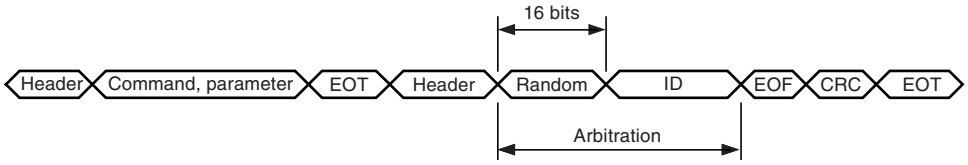
Table 13-5. Start Address of Arbitration as a Function of Parameter(5:3).

ID Page	Byte 3	Byte 2	Byte 1	Byte 0
Block 3	110	100	010	**000**
Block 2	111	101	011	001
Block 1				
Block 0				

Note: The value marked in bold is the default value.

If parameter(7) is set to “1”, the arbitration starts with a 16-bit random value. The memory contents follows. Therefore, the deterministic anticollision procedure can also handle ID structures which are not unique, opening a migration path from other data systems towards ATA5590.

Figure 13-3. Flow Considering the Random Value



13.7.4 Group_AFI

The Group_AFI command is based on the AFI byte stored in the Tag_ID page of the control memory. The Group_AFI command affects the pre_select flag.

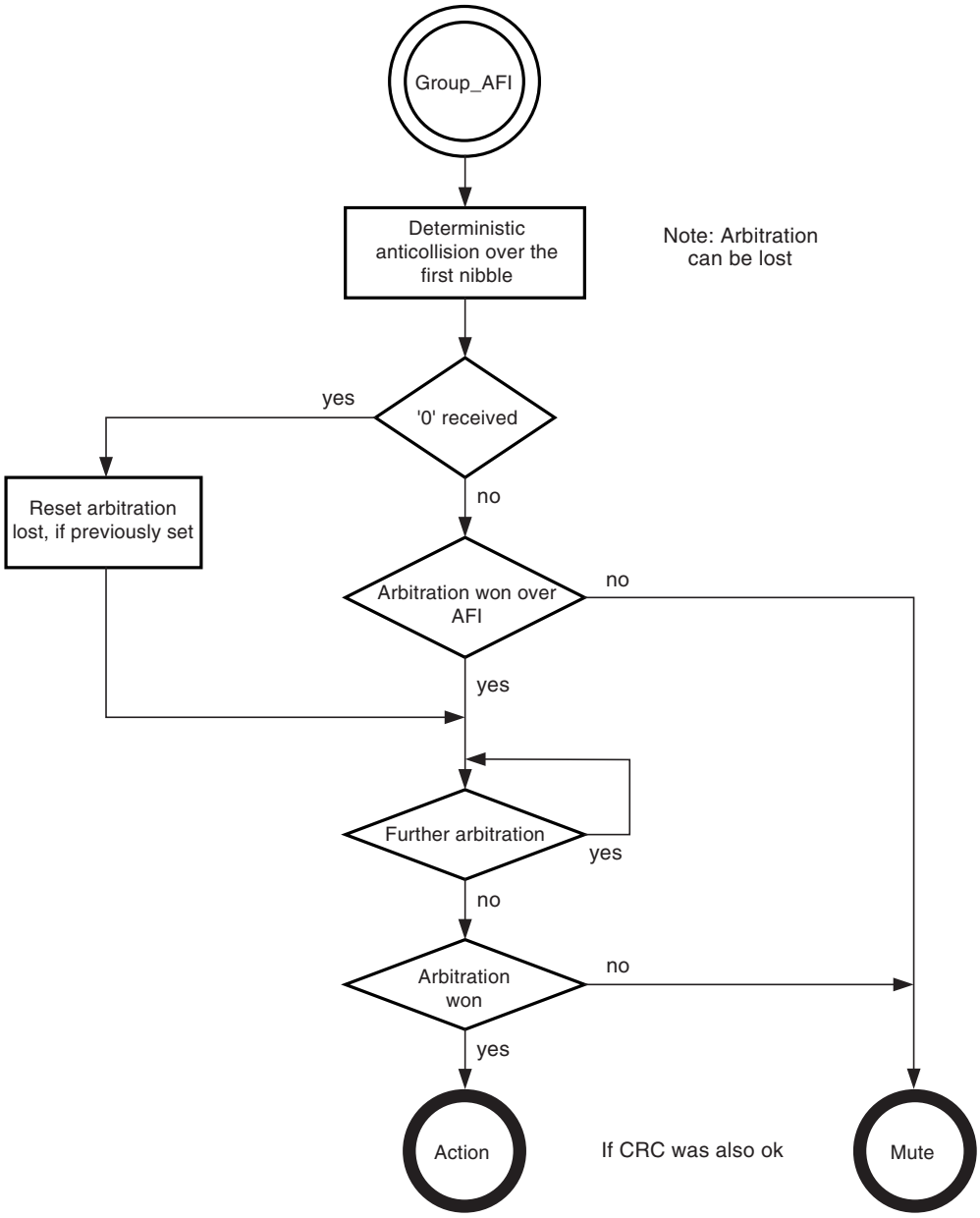
The flag will be set if:

- The contents of the AFI field is the same, or
- The reader has transmitted 00h.

If the reader transmits a 00h, the real value inside the EEPROM is ignored. As long as the reader transmits a series of logical 0’s, ATA5590 does not stop backscattering the real value.

Note: The Group_AFI command considers this mechanism only for the first 8 bits. Then the default arbitration mechanism works.

Figure 13-4. AFI Selection Tree



A “0” is sent by transmitting a symbol shorter than the reference symbol (second symbol of the return header) to the tag. If the arbitration lost flag is not set after checking the AFI contents and after accepting the CRC, the pre_select flag of the status1 register is set.

Table 13-6. Parameter Field of the Group_AFI Command

Index	Function
7	0 (default)
6	nCRC_adapt 0: adapt CRC 1: 16-bit CRC transmitted by the reader
5:3	010 (default)
2:1	Return modulation type 00: NRZI notch locked 01: 3phase1 10: NIRZ soft locked 11: FM0
0	Selection control 0: to all tags in the field 1: to all pre-selected tags in the field

The structure of the whole frame is as follows:

Table 13-7. Flow of the Group_AFI Procedure

Forward header	Group_AFI command	Parameter	EOT	Return header	Arbitration over AFI	EOF	CRC	EOT

Note: EOT consists of 2 EOF symbols

The arbitration starts at bit 125 of page 0 (MSB of AFI) of the control memory. The arbitration will be lost if the extracted data of the forward data stream is not the same as the data stored in the memory. After receiving 8 bits of AFI, the tag checks if it has received a 00h. If the tag has received a 00h, the result of the arbitration no longer matters and the backscatter mechanism of the return link will be active.

This pre_select flag can be reset by receiving a reset command or by cutting the power supply for more than 8 seconds (at 25°C).

Note: The Group_AFI command can be expanded. Therefore, it is possible to combine it directly with the 8 bits of the ID identifier (as an example). The auto decrement function of the addressing mechanism is enabled.

13.7.5 Further Possibilities with Group_AFI Command

The start address of the arbitration can be selected by the parameter field.

- Parameter(3): If set to “0”, arbitration starts with block 3 of the ID page; if set to “1”, arbitration starts with block 2 of the ID page.
- Parameter(5:4) points to the byte of the selected block

Table 13-8. Start Address of Arbitration as a Function of Parameter(5:3)

ID Page	Byte 3	Byte 2	Byte 1	Byte 0
Block 3	110	100	**010**	000
Block 2	111	101	011	001
Block 1				
Block 0				

Note: The value marked in bold is the default value.

13.7.6 Bit-pointer–addressing Deterministic-anticollision and Group-selection Commands

If the application requires the option of starting the arbitration outside the ID page, or to start with a different bit position, ATA5590 supports bit-pointer addressing methods.

Bit-pointer–based commands also support a care_ctrl bit (address(5)). If this bit is set to “1” and the reader transmits a “1”, the result of the arbitration is *don't care*.

13.7.7 Anticollision_pointer and Group_pointer

With these commands the reader can select tags, but the reader is free

- To address other memory locations as the ID page
- To start at a special bit value of the selected page

The commands codes are:

- 4Eh (Anticollision_pointer) and
- 49h (Group_pointer)

The 2-bit command CRC is included.

The result of the group routine will affect the pre_select flag. The result of the anticollision procedure will affect the ID and ID_s flags (anticollision_pointer), or the pre_select flag (Group_pointer).

Table 13-9. Parameter Field of the Anticollision_pointer and the Group_pointer Command

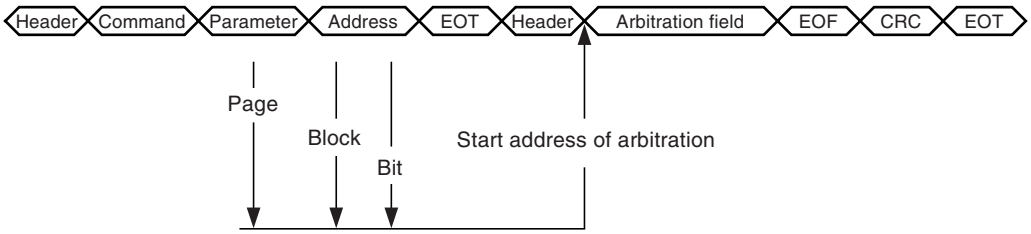
Index	Function
7	0: physical address 1: symbolic address
6	nCRC_adapt 0: adapt CRC 1: 16-bit CRC transmitted by the reader
5:3	Short symbolic or short physical address
2:1	Return modulation type 00: NRZI notch locked 01: 3phase1 10: NIRZ soft locked 11: FM0
0	Selection control 0: to all tags in the field 1: to all pre-selected tags in the field

Table 13-10. Address Information Stored in the Address Field

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Block(1:0)		0 (default)	Bit(4:0)				

Therefore, each bit in each block of the whole memory of ATA5590 can be addressed as the start address for arbitration.

Figure 13-5. Structure and Addressing Mechanism Supported by Group_pointer and Anticollision_pointer Commands



13.7.8 Group_p_leeq and Group_p_greq

These group-selection commands are pointer-based. The structure is the same as before (Group_pointer commands). The difference is that the compare algorithm during arbitration is expanded to less than or equal to (leeq), and greater than or equal to (greq).

Leeq: set pre_select flag (status1) if EEPROM ≤ forward stream
Greq: set pre_select flag (status1) if EEPROM ≥ forward stream

The 8-bit command code is:

- 5B, including the 2-bit CRC for Group_p_leeq
- 5C, including the 2-bit CRC for Group_p_greq

13.7.9 Anticollision_pointer_random

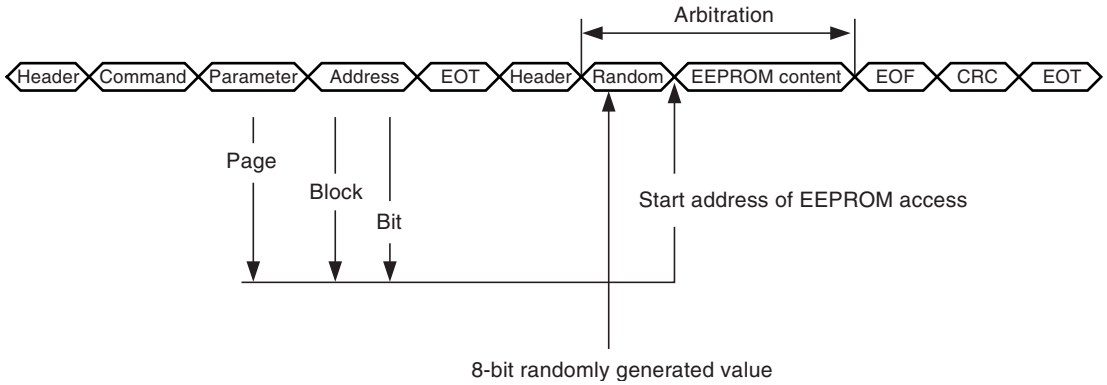
Addressing possibilities for the whole memory cannot guarantee unique data structures for arbitration.

Anticollision_pointer_random command supports non-unique data structures because the arbitration field contains an 8-bit random value.

The 8-bit command code is 55h, which includes the 2-bit CRC.

The structure of the parameter and address field is the same as for the anticollision_pointer command.

Figure 13-6. Structure and Addressing Mechanism Supported by Anticollision_pointer_random Command



Note: It is also possible to arbitrate only over the random value or a part of it.

13.7.10 Repeat_arb

Repeat_arb can be activated if the reader has previously transmitted a group-selection or a deterministic-arbitration command. Then the command which was received before is repeated. The command code of the repeat_arb command is not stored in the command register. Therefore, repeat_arb is a temporary command. The reader can send the repeat_arb command as long as the long group-select or deterministic-anticollision command is used.

If ATA5590 has not previously received a long-arbitration or group-select command, ATA5590 backscatters the error code command not known, which is marked as a sub-carrier during the first symbol after EOF1.

Table 13-11. Construction of the Repeat_arb Command

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	0	0	1	0	CRC(1:0)	

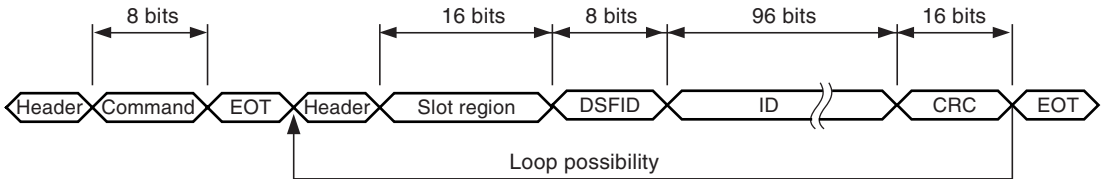
13.7.11 Wakeup_s and Wakeup_sb

The wake-up command generates an answer which is split in two parts:

- Slotted information: a tag modulates one of the 16 slots; the slot number is calculated by a random number generator
- ID information: the tag backscatters the 8-bit structure code (DSFID) of the ID, the ID, and the CRC (starting with bit 103 of the ID page)

The wakeup_s and wakeup_sb command are short commands. If the select condition is true, all addressed tags in the field backscatter information back to the reader indicating that they are in the field. The answering mechanism of the slot area is based on a random number.

Figure 13-7. Structure of the Wakeup_s and Wakeup_sb Procedure



The wakeup_s command results in an answer of all selected tags in the field (ID or pre_select is “1”, and ID_s is “0”).

Wakeup_sb results in an answer of all tags which are not selected (ID, ID_s, and pre_select are “0”).

After receiving a wake-up command, the tag which was addressed by the select condition answers. The return link stream is split in the following regions:

- A slot region which is based on 16 bits. The addressed tag modulates one of the 16 bit slots. The other slots are not modulated.
- A structure code area. The addressed tag backscatters the DSFID code (default) or the 8-bit information which is stored in the lower byte of block 3 of the ID page.
- ID information (the lower 96 bits of the ID page)
- A CRC region
- An EOT area

No status information byte will be sent during the stream.

A slot has the size of a bit. Each tag will calculate a slot number randomly, and modulate one bit slot.

The wake-up command can be used to get a first impression how many tags are in the field or to find out collisions and/or its pointers. As the wake-up command can be combined with a group_select command or an anticollision command, the reader can therefore also create an anticollision procedure.

14. Analog Timing

For wireless communication between the reader and the tag(s), the ATA5590 must be powered by the RF field. Therefore, the ramp up conditions are based on the field strength of the carrier signal and its timing.

To operate, ATA5590 observes the power level continuously. POR and stand_by levels control the functionality.

Table 14-1. Functionality Control

Signal	Comment
POR	The circuit will be reset if the voltage level after the rectifier is less than the POR threshold voltage.
Stand_by	The threshold voltage of the stand_by level is above the POR threshold voltage. If the power supply voltage is above the stand_by threshold voltage: - The oscillator is turned on (ramp-up phase) - Operation of the circuit is enabled If the power supply voltage is below the stand_by threshold voltage, the oscillator and the current operation is stopped. Therefore, current consumption decreases.

Notes: 1. If stand_by occurs during programming procedure, erase, or program, indicating flags will get a reset signal. The procedure is then finished, and the tag modulates the RF field.

2. If the supply voltage is below the POR threshold value and the RF field comes back, the status1 register will be refreshed.

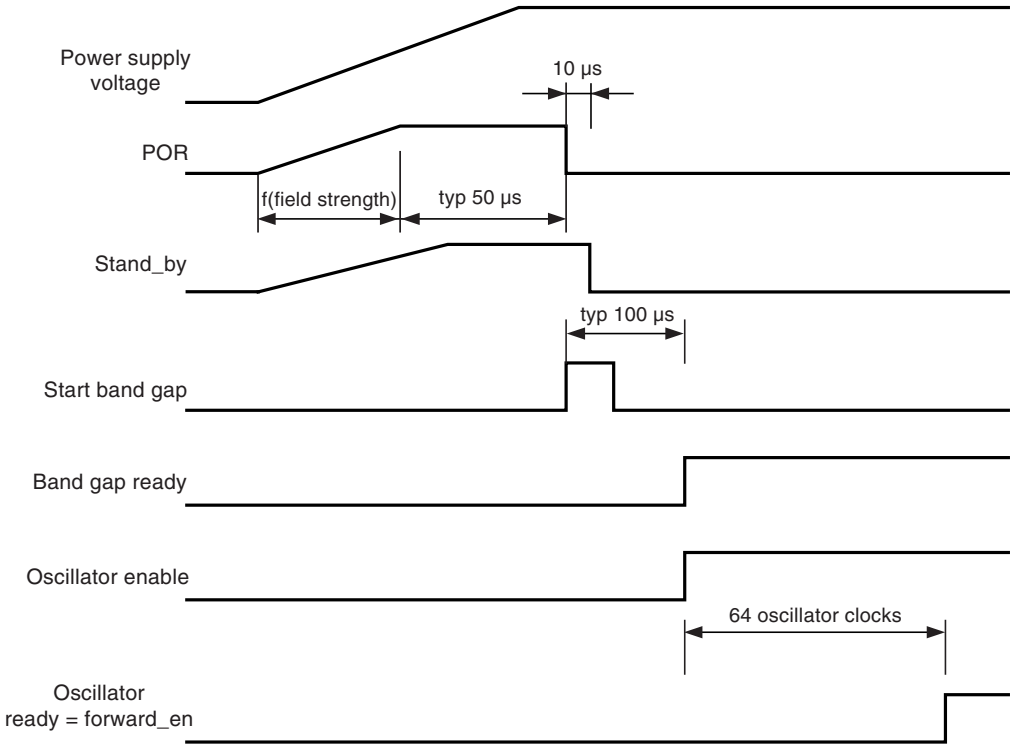
For communication, ATA5590 can extract modulation changes of the carrier which are under control of the reader. Modulation is based on a double sideband technique (PR-ASK) or a traditional ASK type. Both modulations result in an AM signal on the tag side, and therefore it can be detected very easily by an RSSI circuit.

14.1 Reset and Stand_by

14.1.1 Ramp Up

Figure 14-1 gives an overview of the analog timing during ramp up.

Figure 14-1. Analog Timing Relations at 25°C



After POR has reset the digital circuits, the band gap is started. The band gap needs time for stabilization. After this time (TBG_Start), the IC can decode the received signals from the reader correctly.

Table 14-2. Typical Timing Values for 25°C

Parameter	Value	Unit	Comment
T_{POR}	< 0.3	ms	50 µs + a variable time which depends on RF field strength 0.3 ms equates to a distance of 4 meters in an anechoic chamber
T_{BG_STAB}	0.1	ms	

After the oscillator function is enabled, it takes 64 oscillator clocks to enable normal operations. Based on a 400-kHz oscillator frequency, this takes 160 µs.

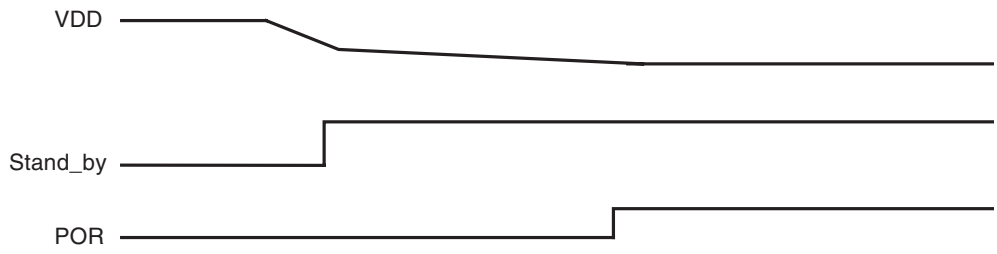
Table 14-3. Threshold Voltages as a Function of Temperature

Signal	–40°C	+25°C	+85°C
POR	1.25V	1.05V	0.9V
Stand_by	1.35V	1.15V	1.0V

14.1.2 Ramp Down

If RF field strength is decreasing, VDD goes down to the threshold voltage level of stand_by. Current consumption decreases because the oscillator is stopped. Therefore, the gradient of the VDD curve decreases also. If VDD passes the threshold voltage of POR, the circuit will be reset. The gradient of VDD decreases again because the band gap circuit is switched off.

Figure 14-2. Power Down Timing



14.2 Notch Detection

The notch detection is based on an RSSI concept. Therefore, the tag cannot detect the difference between PR-ASK, ASK, or AM. Nevertheless, the type of modulation has an influence on the power transport, the SNR, and the spectrum (necessary bandwidth).

Figure 14-3 shows the relations between modulation and notch detection.

Figure 14-3. Relationship Between Notch Detection and Modulation Using PR-ASK Modulation Scheme

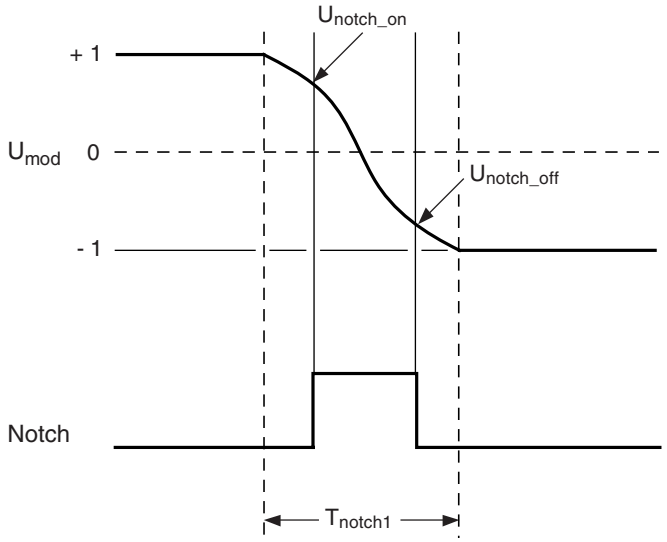


Table 14-4. Typical Values for Notch Detection Threshold Voltages and Timings at 25°C

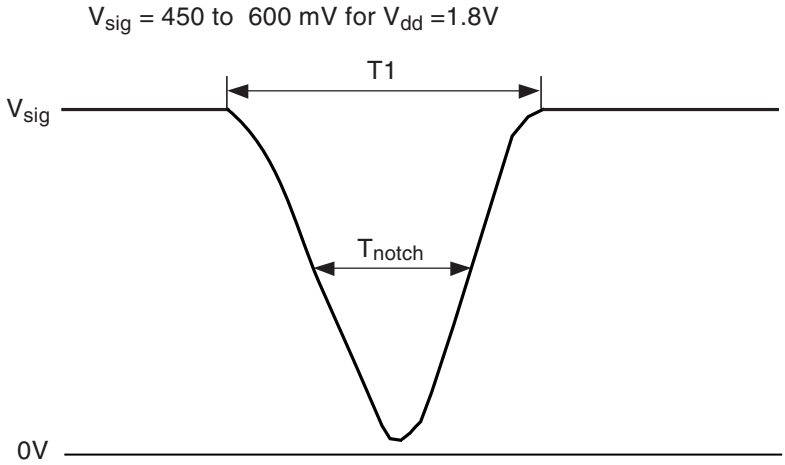
Parameter	Value	Unit	Comment
U_{notch_on}	0.5	V	Relative value (see Figure 14-3 on page 97)
U_{notch_off}	0.8	V	Relative value (see Figure 14-3 on page 97)
T_{notch1}	> 4	µs	PR-ASK modulation scheme, cosine shape restrictions are given by ETSI, 250-kHz bandwidth
T_{notch1}	> 8	µs	ASK modulation scheme (250-kHz bandwidth cosine shape)
Minimum T_{notch1}	1	µs	Released in the circuit, but depends also on the distance (power), and the shape of the transition

The minimum time for T_{notch} is given by ETSI. By using PR-ASK, the theoretical limit for a bandwidth of 250 kHz is 4 µs (sine transition between the two states of the modulation equals half of one period). When using the ASK or AM method, this minimum time is 8 µs.

This time must be changeable if other bandwidths are needed (200 kHz or 100 kHz). In the case of 100 kHz, the bandwidth is larger (1 MHz). Therefore, this time can be shorter (2 µs for ASK/AM, and 1 µs for PR-ASK).

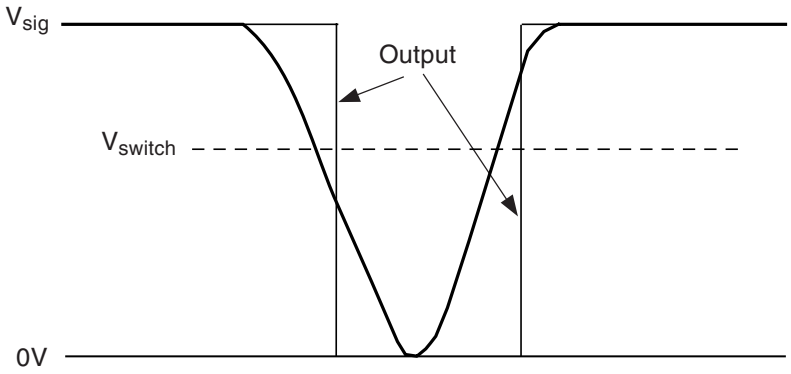
A typical notch that is received by the detection circuit of the tag is shown in Figure 14-4:

Figure 14-4. Notch Timing



Typical values are for T1 = 4 µs and for T_{notch} = 2 µs. The output of the detection circuit is shown in Figure 14-5 on page 99:

Figure 14-5. Notch Detection



V_{switch} is 0.66 × V_{sig}. There is also a small hysteresis implemented.

14.3 Notch Acceptance

A first notch can be accepted by ATA5590 64 oscillator clock cycles after the oscillator was enabled. The oscillator itself starts operation 100 µs after stand_by signal was set to “0”.

15. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Pin	Value	Unit
Maximum RF stress 1 ms at operating frequency	10	400	V/m
Maximum continuous RF stress at operating frequency	10	50	V/m
ESD antenna pad (HBM)	10	1.5	kV
ESD other pads (exclusive EEPROM test pads) (HBM)	1 to 9	> 1.5	kV
Operating temperature range (without programming)		–40 to +85	°C
Operating temperature range (programming)		–40 to +45	°C
Storage temperature range		–50 to +85	°C

16. Electrical Characteristics

Operating characteristics 1.8V V_{DD}, 25°C, 869 MHz

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
1	**Link Values**								
1.1	RF frequency range				800	900	2450	MHz	C
1.2	Notch detection	On: 0.5V, Off: 0.8V			0.3	2	20	µs	C
1.3	Symbol length min: “0” max: EOT	Inclusive. 4 µs notch time			12		92000	µs	C
2	**Environment**								
2.1	Diameter of RF pad				TBD	60	TBD	µm	D
2.2	Assembly method	Flip chip							
3	**IC Values**								
3.1	RF power between ant and ant_gnd	To allow read operation at 1.3V			15	18.6	25	µW	A
3.2	Supply current (read-mode)	After the rectifier (data rate 10 Kbit/s)			1.8	2	2.5	µA	C
3.3	Efficiency rectifier	At 868 MHz 1.3V and 1.3 µA			10	14	15	%	B
3.4	Input impedance mod state 1	1.3V, 1.3 µA				6.7 –j216		Ω	D
3.5	Input impedance mod state 2	1.3V, 1.3 µA				6.1 –j202		Ω	D
3.6	Input impedance program	1.6V, 4 µA load current				12.3 –j217		Ω	D
3.7	DC clamp voltage antenna pad	10 mA			700	750	800	mV	C
3.8	Start-up time	Forward enable			0.4	0.6	0.8	ms	C
3.9	POR threshold	Hysteresis = TBD			0.95	1.05	1.15	V	A
3.10	Stand_by threshold	Hysteresis = TBD			1.05	1.15	1.25	V	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

16. Electrical Characteristics (Continued)

Operating characteristics 1.8V V_{DD}, 25°C, 869 MHz

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
3.11	Storage time status1 register	0.5s at +60°C 17 minutes at –40°C			2			s	D
3.12	τ set status flag	1.8V				1		ms	D
3.13	τ reset status flag	1.8V				0.2		µs	D
3.14	Oscillator frequency	1.6V to 2.5V			350	400	600	kHz	A
3.15	Temperature drift	–40°C to +85°C			±5	±8	±15	%	C
3.16	Programming time (adapted timing)	1.6V after the rectifier				12		ms	C
3.17	Programming time (adapted timing)	2V after the rectifier				9		ms	C
3.18	Programming cycles	Erase/write				10^5		cycles	D
3.19	Data retention at 55°C					10		years	D
3.20	Data retention at 250°C					24		h	C

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

17. Ordering Information

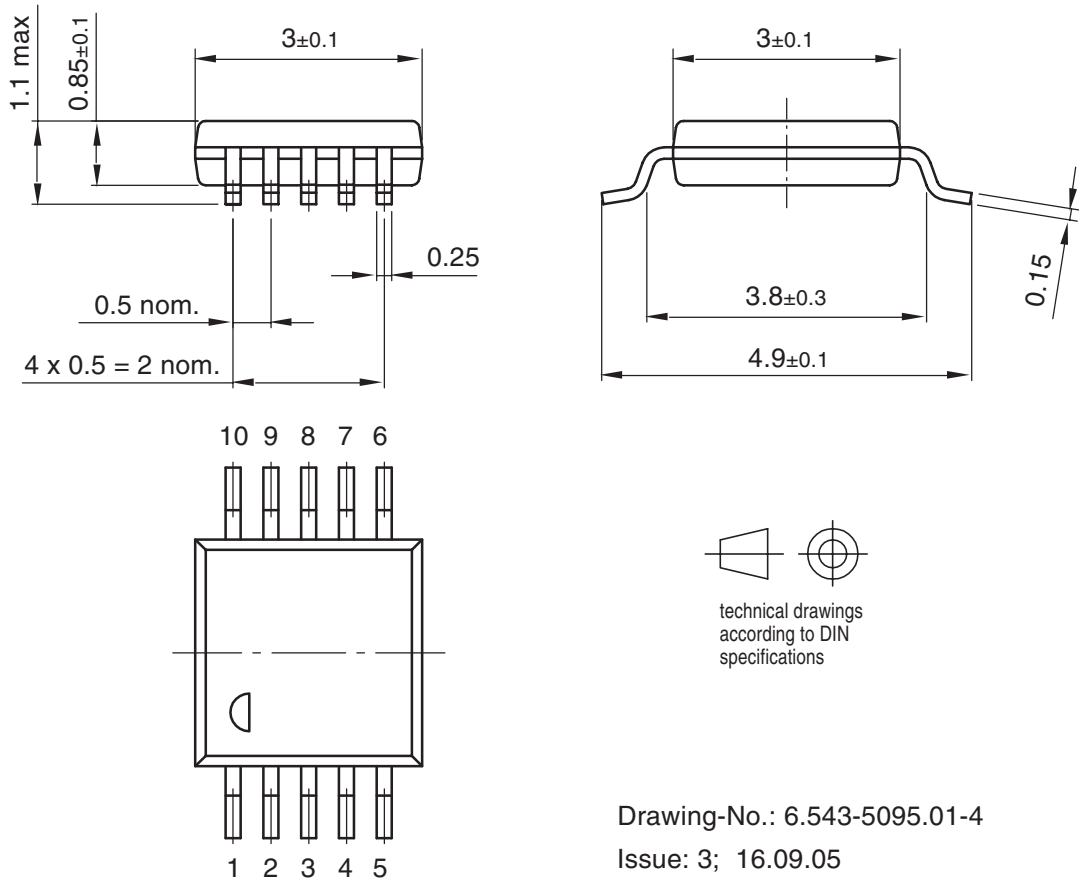
Extended Type Number	Package	Remarks
ATA559001-DBB	6” Wafer	25 µm NiAu bumps, 150 µm wafer thickness, sawn on foil, sample delivery, die in tray (DBT) (Figure 18-2 on page 103)
ATA559001-DDW	6” Wafer	300 µm thickness, not sawn (Figure 18-2 on page 103)
ATA559001-6DQY	TSSOP10	Taped and reeled, Pb-free (Figure 18-1)

18. Package Information

Figure 18-1. TSSOP10 Package

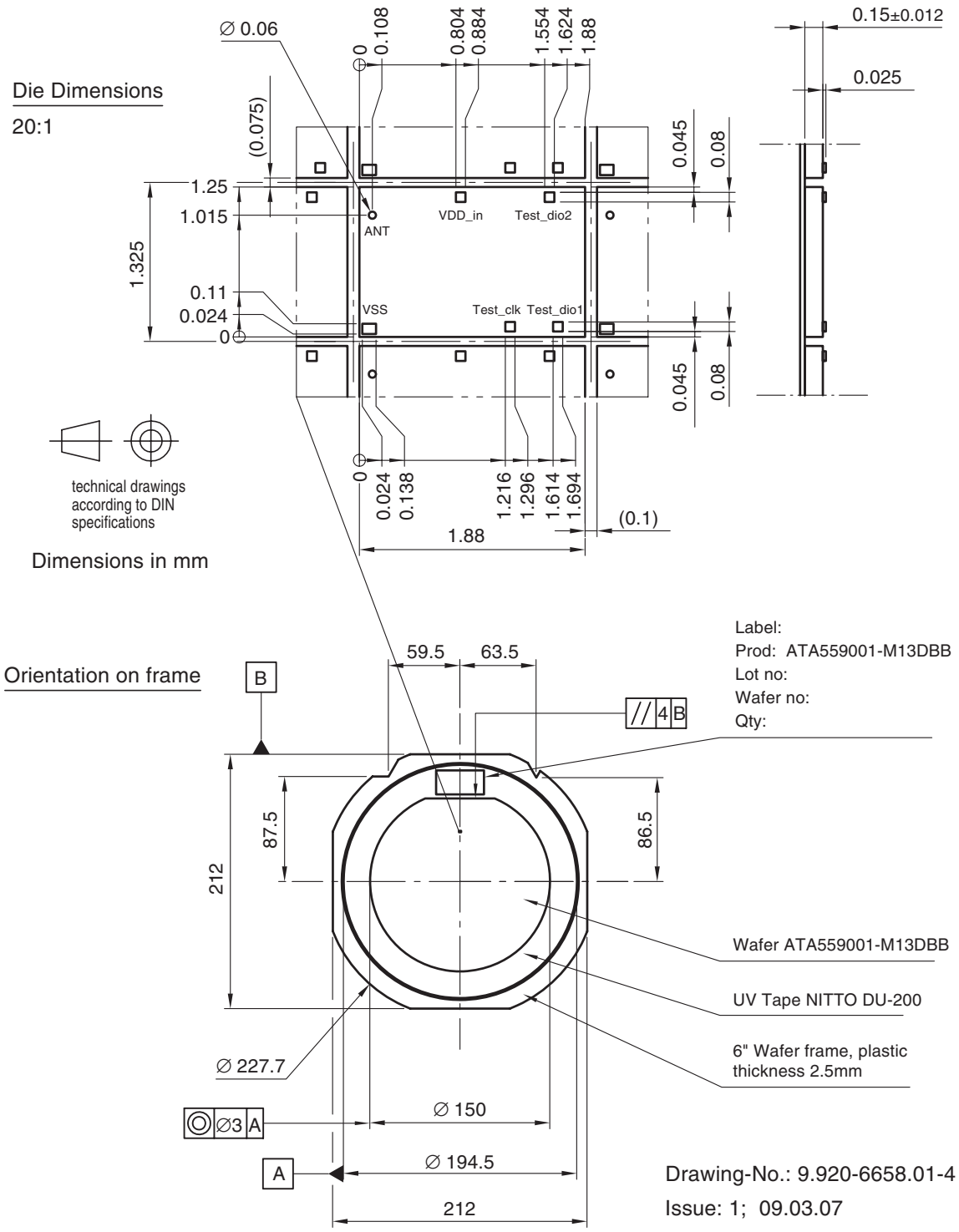
Package: TSSOP 10
(acc. to JEDEC Standard MO-187)

Dimensions in mm
Not indicated tolerances ± 0.05



Drawing-No.: 6.543-5095.01-4
Issue: 3; 16.09.05

Figure 18-2. 6” Wafer



19. Table of Contents

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