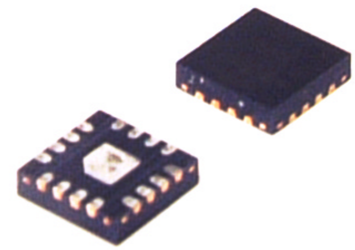
Complies with Directive 2002/95/EC (RoHS)

TXC100

300-450 MHz Transmitter



3x3 mm package

TXC100 Product Overview

TXC100 is a rugged single-chip ASK/FSK transmitter IC designed for operation in the 300-450 MHz frequency range. The highly integrated TXC100 includes a complete PLL frequency synthesizer plus an RF power amplifier that require very few external components. The TXC100 is very small in size and features high output power and low current consumption making it ideal for a wide range of short-range wireless applications in the industrial, automotive and consumer markets.

Key Features

- Operating Frequency Range: 300-450 MHz
- Modulation Types: ASK/FSK
- Operation supply voltage: 2.1 - 3.6V
- High Date rate:
  - OOK/ASK: 100 kbps
  - FSK: 20 kbps
- Low current consumption:
  - OOK/ASK mode: 7 mA typical
  - FSK mode: 10 mA typical
- Low Stand by current: < 1 nA
- Adjustable Output power: -10 to +10 dBm
- Adjustable FSK Shift
- Programmable Clock Output
- Very Low external component count
- Extended temperature range: -40 to +125 °C.
- Small Package: 3x3 mm 16-pin TQFN package
- Standard 13 inch reel, 2500 pieces

Typical Applications

- Active RFID tags
- Automated Meter reading
- Wireless sensor nodes
- Home Automation
- Security systems
- Tire pressure monitoring
- Remote keyless entry
- Automobile Immobilizers
- Sports & Performance monitoring
- Wireless Toys
- Medical equipment
- Command & Control systems

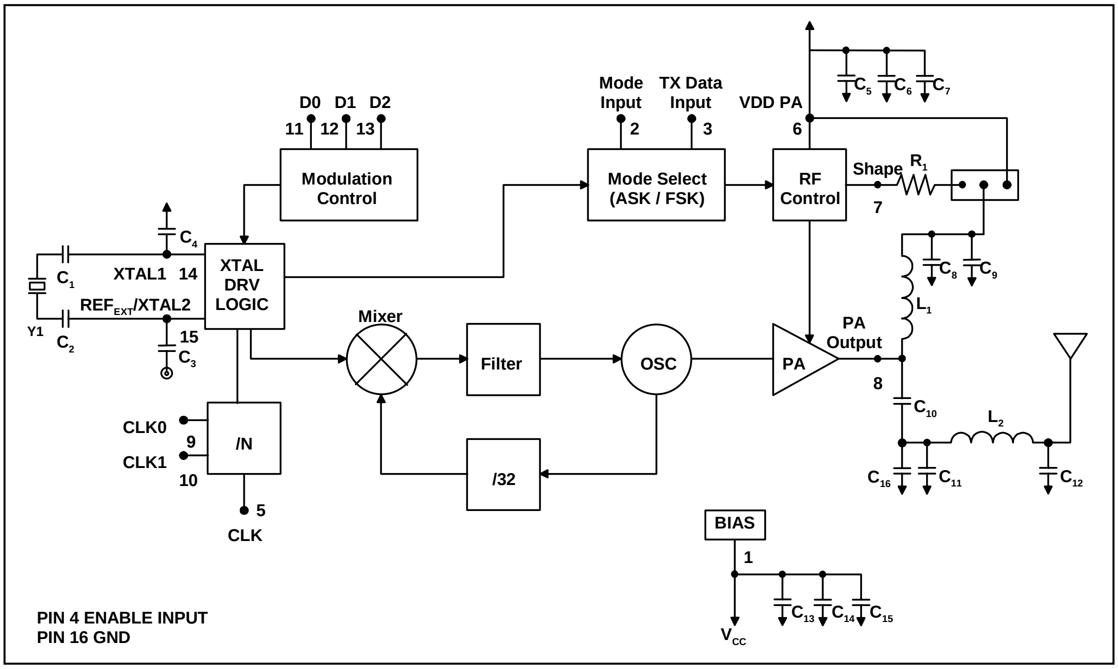
Electrical Characteristics

Characteristics	Sym	Min	Typical	Max	Units
Operating Frequency	fo	300		450	MHz
Modulation Types			OOK/ASK/ FSK		
ASK Data Rate				100	kbps
FSK Data Rate				20	kbps
Peak RF Output Power			+10		dBm
Standby Current				1	nA
Supply Voltage Range	V_{DD}	2.1		3.6	Vdc
Operating Temperature	Ta	-40		+125	°C

Reference Crystal Parameters

Characteristics	Sym	Min	Typical	Max	Units
Crystal Frequency	fc		fo/32		MHz
Load Capacitance	Cl			3	pF
Motional Capacitance	Cm	9		10	fF
Tolerance	Tol		±30		ppm

TXC100 Block Diagram and Typical Application Circuit

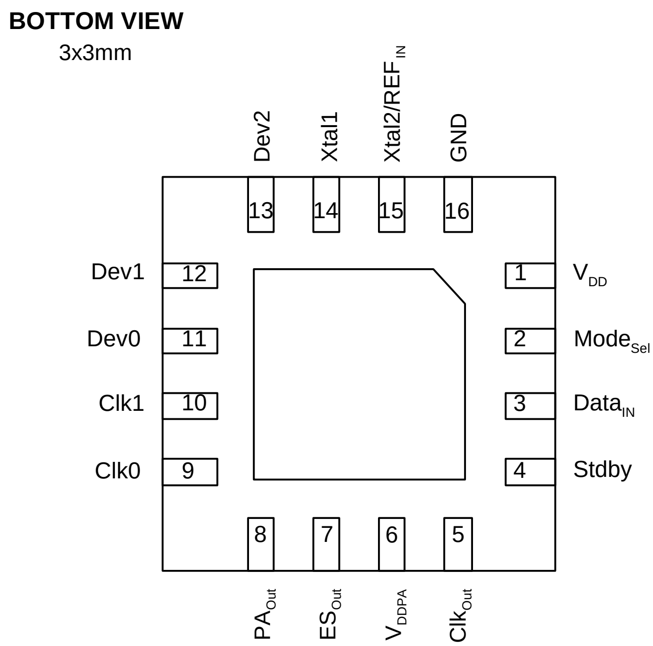


Component Values for Typical Application Circuit

Comp	315 MHz Band	433 MHz Band
C1	100 pF	100 pF
C2	100 pF	100 pF
C3[3]	DNP	DNP
C4[3]	DNP	DNP
C5	1.0 uF	1.0 uF
C6	0.01uF	0.01 uF
C7	220 pF	220 pF
C8	100 pF	100 pF
C9	680 pF	680 pF
C10[1]	15 pF	3.3 pF
C11[1]	22 pF	5.6 pF
C12[1]	15 pF	12 pF
C13	1.0 uF	1.0 uF
C14	0.01uF	0.01uF
C15	220 pF	220 pF
C16[1]	DNP	DNP
L1[1,2]	27nH	22 nH
L2[1,2]	22 nH	18 nH
Y1	9.84375 MHz*	13.5600 MHz**

[1]Matched to 50 ohms
[2]Use wirewound inductors *only*
[3]Use for External Reference Input
DNP - Do Not Populate
*Hong Kong Crystal P/N SSL9843750E03FAFR800
**Hong Kong Crystal P/N SSM1356000E03FAFR800

Pin Configuration



Pin Description

Pin	Name	Description
1	V_{DD}	V_{DD} is the supply voltage for the PLL and logic circuitry. Bypass this pin as close as possible with parallel 1.0 µF, 0.01 µF, 220 pF capacitors.
2	$Mode_{Sel}$	The Mode Select Pin allows the TXC100 to be set in either OOK/ASK or FSK mode: Logic Low: OOK/ASK mode Logic High: FSK mode In OOK/ASK mode, data input to the $Data_{IN}$ Pin (3) gates the internal power amplifier. A logic high turns the power amplifier on. A logic low turns off the power amplifier. In FSK mode, data input to the $Data_{IN}$ Pin shifts the carrier frequency by the amount programmed through the DEV[2..0] pins (11,12,13). A logic low performs no shift. The frequency of a logic low input in FSK mode is the same frequency as a logic high in OOK/ASK mode. The FSK deviation is achieved by pulling the crystal frequency. See *Crystal Reference* section (pin 15) for more details. The maximum FSK deviation for the 315 MHz band and 433 MHz band is approximately 55 kHz and 80 kHz, respectively.
3	$Data_{IN}$	The Data Input Pin turns the Power Amplifier on/off in OOK/ASK mode, or high/low frequency in FSK mode: Low (OOK/ASK mode): Power Amplifier off High (OOK/ASK mode): Power Amplifier on Low (FSK mode): Low frequency High (FSK mode): High frequency
4	Stdby	The Standby Input Pin selects active or low power shutdown/standby mode: If this pin unconnected or logic low, the TXC100 is placed in low current standby mode. If this pin is logic high, the TXC100 is in active mode and ready to transmit Note: Lowest current consumption is achieved when all configuration pins are logic low. When this pin sets the device in low power shutdown, the device draws nominally 0.2 nA. When the device is brought out of standby with a logic high input, it is ready for operation within 200 µs. This pin has an internal pull-down resistor so it can be pulled low or left unconnected.The 200 µs turn-on time is due to crystal start-up. An optimally matched crystal will minimize this turn-on time. See the *Crystal Reference* section (Pin 15) for details on crystal load matching.

5	Clk_{Out}	The clock output is a scaled and buffered version of the crystal frequency, which may be used to drive external logic or a microprocessor. The frequency is programmable through Pins 9 (Clk0) and 10(Clk1) as below: <table><tr><th>Clk0</th><th>Clk1</th><th>Clk_{Out}</th></tr><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>1</td><td>0</td><td>fc/4</td></tr><tr><td>0</td><td>1</td><td>fc/8</td></tr><tr><td>1</td><td>1</td><td>fc/16</td></tr></table> fc = Crystal Frequency
6	V_{DDPA}	This pin is a power supply voltage source for the transmitter power amplifier. Bypass this pin as close as possible with a 0.01 µF and 220 pF capacitor. ES_{Out} is the alternate power amplifier voltage source as discussed below.
7	ES_{Out}	This pin can be used to supply voltage to the power amplifier instead of V_{DDPA}, allowing the on/off rise and fall times of the power amplifier to be adjusted in ASK mode. Reducing the rise and fall times reduces the spectral bandwidth of the modulated output signal, and also reduces average transmitter power. Rise and fall times are adjusted by placing a resistor in the range of 1K to 5K in series with this output, as close as possible to the TXC100 IC to minimize circuit parasitics. The power amplifier side of the resistor should be bypassed with 680 pF and 220 pF capacitors in parallel, as close to the resistor as possible.
8	PA_{Out}	Power Amplifier - the power amplifier is an open-drain, Class C amplifier designed for a load impedance at PA_{OUT} (pin 8) of about 250 ohms. The power amplifier requires a DC path to the supply voltage through a series inductor, which can be part of the output matching network. A 50 ohm antenna matching network is shown in the *Typical Application Circuit* section. The matching network also suppresses carrier harmonics to aid in compliance testing.
10, 9	Clk[1..0]	See description for Pin 5
13, 12, 11	FreqDev[2..0]	The Frequency Deviation Pins set the amount of deviation between data logic states in FSK mode. Frequency deviation is programmable through pins 11, 12, 13 as shown in the table below: <table><tr><th>DEV Δ</th><th>DEV 2</th><th>DEV 1</th><th>DEV 0</th></tr><tr><td>.125 x Max</td><td>0</td><td>0</td><td>0</td></tr><tr><td>.250 x Max</td><td>0</td><td>0</td><td>1</td></tr><tr><td>.375 x Max</td><td>0</td><td>1</td><td>0</td></tr><tr><td>.500 x Max</td><td>0</td><td>1</td><td>1</td></tr><tr><td>.625 x Max</td><td>1</td><td>0</td><td>0</td></tr><tr><td>.750 x Max</td><td>1</td><td>0</td><td>1</td></tr><tr><td>.875 x Max</td><td>1</td><td>1</td><td>0</td></tr><tr><td>Max</td><td>1</td><td>1</td><td>1</td></tr></table> Deviation values are approximate and apply to a properly loaded crystal. Crystal characteristics and loading behavior can vary between suppliers.
14	Xtal1	External Crystal Input 1 presents a capacitance of 3 pF to GND in ASK and FSK ($Data_{IN}$ logic low) modes. Circuit parasitics add to this package capacitance, presenting a total load of about 4.5 pF.
15	$Xtal2/REF_{IN}$	External Crystal Input 2 presents a capacitance of 3 pF to GND in ASK and FSK($Data_{IN}$ logic low) mode. Circuit parasitics add to this package capacitance, presenting a total load of about 4.5 pF. The External Ref Input allows an external frequency source to be used to obtain the desired transmit frequency. In this case, the Xtal1 input must be bypassed with a 0.01µF capacitor, and a 0.01µF series capacitance should be added into External Reference input. Crystal Reference - the Xtal1 and Xtal2 inputs are designed to present a 3 pF load to GND to each reference crystal connection. Including PCB parasitic capacitances, this increases to about 4.5 pFat each connection. In ASK mode, the full 3 pF load is applied to the crystal allowing it to oscillate at the desired frequency. In FSK mode, a portion of the 3 pF load is removed in response to a logic high being applied to the $Data_{IN}$ (pin 2) as set by the frequency deviation pins DEV[0..2] (11,12,13). To achieve larger frequency deviations, use a crystal with large motional capacitance or reduce PCB parasitic capacitance to the extent possible.
16	GND	Connect to system ground. Note: The ground pad in the middle of the package is the power amplifier ground. It must be connected to system ground thru a low inductance path.

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		Min	Max	
Operating Temperature Range	T_O	-40	+125	°C
Junction Temperature Range	T_J	-40	+150	°C
Storage Temperature Ragne	T_S	-60	+150	°C
Supply Voltage - Vdd to GND	V_S	-0.3	+4	V
All pins to GND		-0.3	Vdd + 0.3	V
Note: Maximum ratings must not be exceeded under any circumstances and can cause permanent damage to the IC				

DC Electrical Characteristic

(Typical values taken at V_{DD} = +3.0 V, T_A = +25 °C, unless otherwise noted)

Characteristic	Sym	Notes	Limit Values			Unit	Test Conditions	
			min	typ	max			
Supply Voltage	V_{DD}		2.1		3.6	V		
Current Consumption								
Standby	I_{STDBY}			0.2	1	nA	T_A = +25 °C	
				120	300		T_A = +85 °C	
				700	1600		T_A = +125 °C	
Supply	I_{DD}	1,4		2.9	4.3		PA off, Data=0V (ASK)	315 MHz Band
				7	10.7		50% duty cycle (ASK)	
				10.5	17.1	mA	Data = V_{DD} (FSK and ASK)	
				3.3	4.8		PA off, Data=0V (ASK)	433 MHz Band
				7.3	11.4		50% duty cycle (ASK)	
				10	18.1		Data = V_{DD} (FSK and ASK)	
Digital Inputs								
Data Input Low	V_{IL}				0.25	V		
Data Input High	V_{IH}		V_{DD}-0.25			V		
Max Input Current	I_I			15.5	20	µA		
Digital Outputs								
Output Voltage Low	V_{OL}				0.25	V	Clkout, Load = 10 pF	
Output Voltage High	V_{OH}		V_{DD}-0.25			V	Clkout, Load = 10 pF	

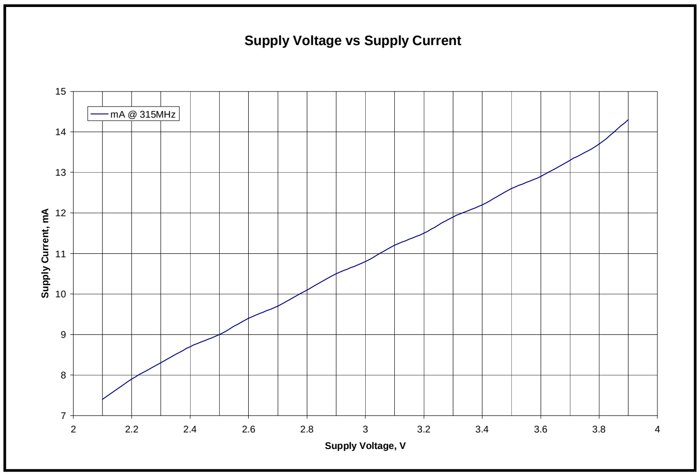
AC Electrical Characteristic

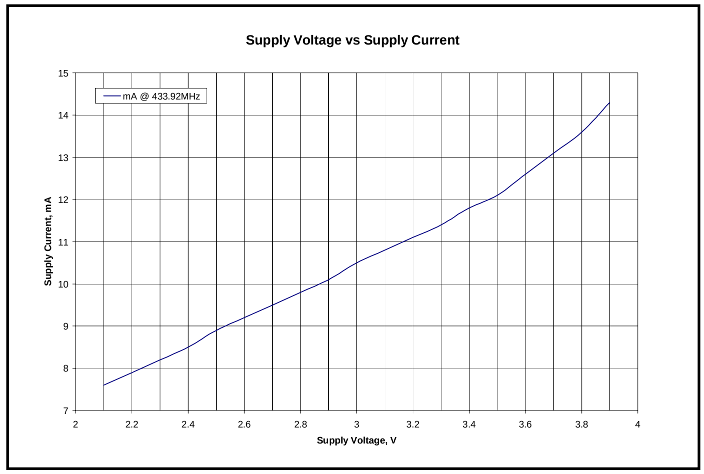
(Typical values taken at V_{DD} = +3.0 V, T_A = +25 °C, unless otherwise noted)

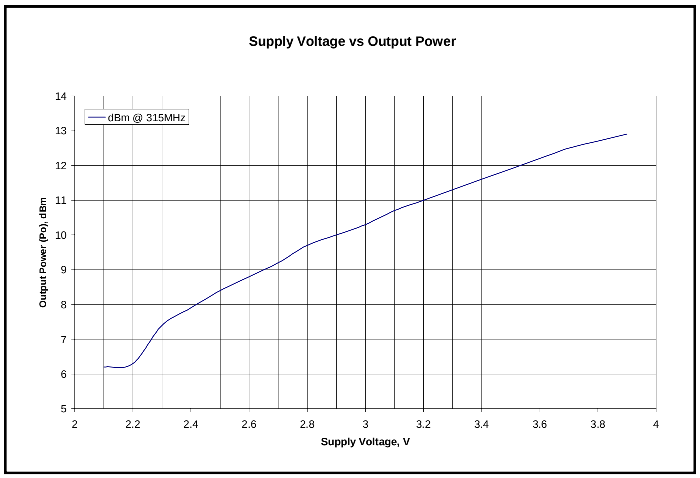
Parameter	Sym	Notes	Limit Values min	typ	max	Unit	Test Conditions	
PLL Performance								
VCO Gain	K_{VCO}			280		MHz/V		
Phase Noise				-75		dBc/Hz	315 MHz Band	Freq Offset = 100 kHz
				-74			433 MHz Band	
				-98			315 MHz Band	Freq Offset = 1 MHz
				-98			433 MHz Band	
Loop BW	BW			300		kHz		
Reference Spur				-40		dBc		
2nd Harmonic				-56		dBc	315 MHz Band	
				-52			433 MHz Band	
3rd Harmonic				-56		dBc	315 MHz Band	
				-50			433 MHz Band	
Crystal								
Frequency Range	f_{REF}			f_{RF}/32		MHz	fundamental mode, AT	
Tolerance		3		50		ppm		
Internal Load Capacitance		2		3		pF		
Clock Output Frequency	CLK_{OUT}			F_{XTAL}/N		MHz	Determined by CLK1 and CLK2	
System Characteristics								
Frequency Range			300		450	MHz		
Output Power		4		12.2	16.1	dBm	TA = -40 °C, V_{DD} = +3.6 V	into 50Ω matched load
			6.1	10	12.4		TA = +25 °C, VDD = +3.0 V	
			2.7	5.3			TA = +125 °C, VDD = +2.1 V	
Start-up time	t_{ON}	5		160		µs	STDBY to TX	
Rise Time	tr	5		300		ns		
Max Data Rate		5		20		kbps	FSK (50% Duty Cycle)	
				100			ASK (50% Duty Cycle)	
Frequency Deviation (FSK)				55		kHz	315 MHz Band	DEV[2..0]=111
				80			433 MHz Band	
Transmit Efficiency $\eta = P_{OUT}/(V_{DD}*I_{DD})$		4		35		%	315 MHz Band	CW
				31			433 MHz Band	
				27			315 MHz Band	50% duty cycle
				25			433 MHz Band	
Power ON/OFF Ratio				-77		dB	ASK Mode	
Frequency Stability vs. V_{DD}	Δdf_{VDD}			4		kHz		
Frequency Stability vs. Temp	Δdf_{TA}			TBD		kHz	-40 °C to +85 °C	

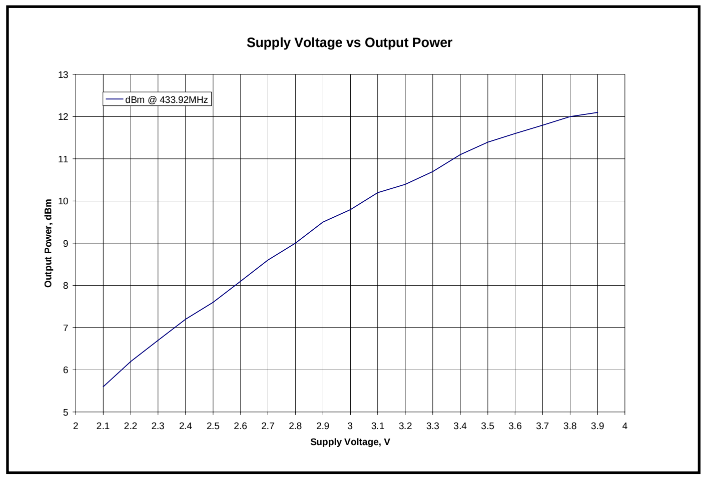
Notes:
1. 10 kHz, 50% duty cycle
2. Dependent on PCB parasitic trace capacitance and crystal parameters.
3. Dependent on crystal parameters.
4. Transmit Efficiency, RF Output Power, and Supply Current are heavily dependent on proper output matching and PCB layout.
5. No Envelope Shaping.

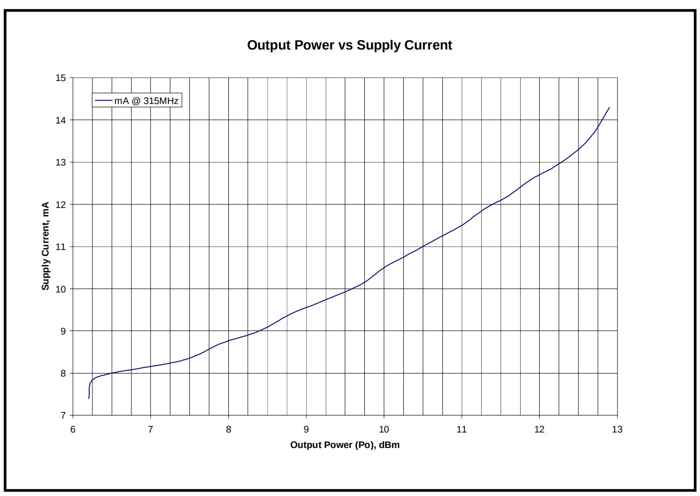
Typical Operating Characteristics

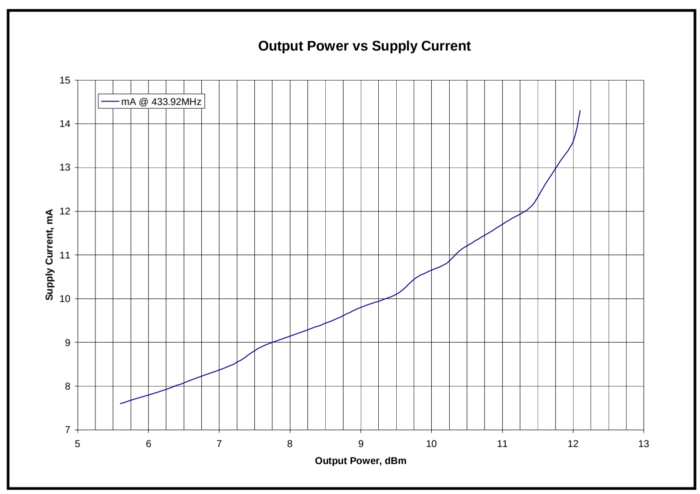


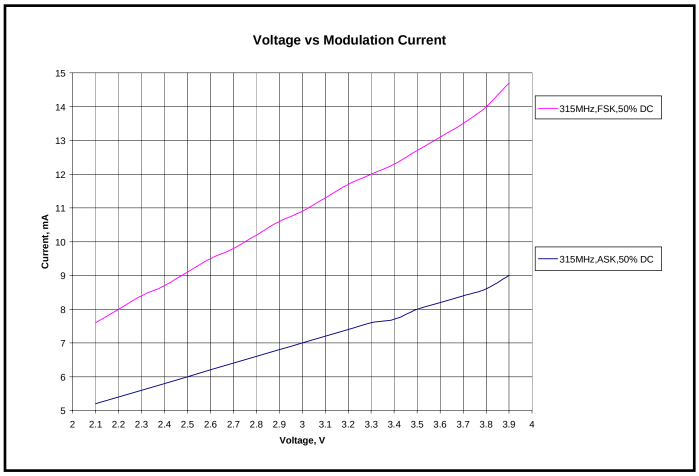


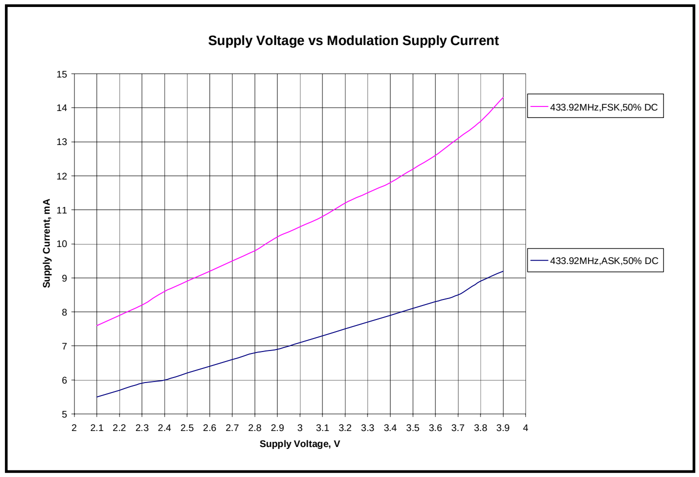


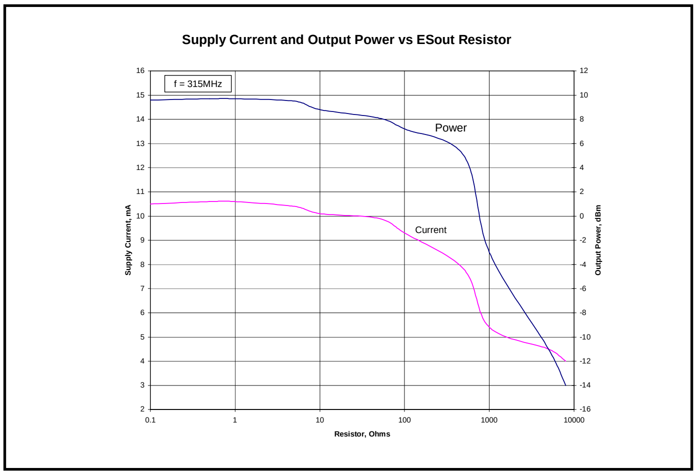


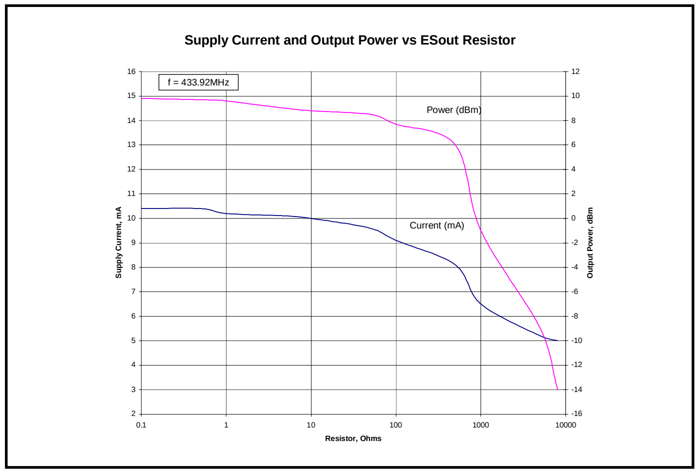





Voltage vs Modulation Current
315MHz,FSK,50% DC
315MHz,ASK,50% DC
Current, mA
Voltage, V


Supply Voltage vs Modulation Supply Current
433.92MHz,FSK,50% DC
433.92MHz,ASK,50% DC
Supply Current, mA
Supply Voltage, V


Supply Current and Output Power vs ESout Resistor
f = 315MHz
Power
Current
Supply Current, mA
Output Power, dBm
Resistor, Ohms


Supply Current and Output Power vs ESout Resistor
f = 433.92MHz
Power (dBm)
Current (mA)
Supply Current, mA
Output Power, dBm
Resistor, Ohms

Theory of Operation

Introduction

The TXC100 is a crystal-referenced transmitter designed to operate in the 315/433 MHz frequency spectrum. The carrier and crystal reference relation is given by:

$$f_C = f_{XTAL} * 32$$

It is capable of supporting ASK and FSK data transmissions at 100 and 20 kbps, respectively. The output power is adjustable from -10 dBm to +10 dBm thru a resistor at the ES_{OUT} (pin 7). The FSK frequency deviation is programmable with up to eight different deviation values. The IC also provides a scaled and buffered clock output of the reference crystal for use by an external processor. The clock output frequency scaling programmable.

Frequency Synthesizer

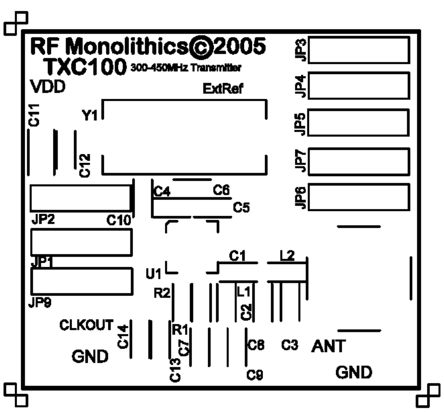
The frequency synthesizer is a phase locked loop (PLL) circuit with a loop bandwidth of 300 kHz. The PLL contains a phase detector, charge pump, VCO, integrated loop filter, ÷32 clock divider, and crystal oscillator drive circuit. The internal PLL is self contained and requires no external components for filtering or dividing. Only a reference crystal is needed.

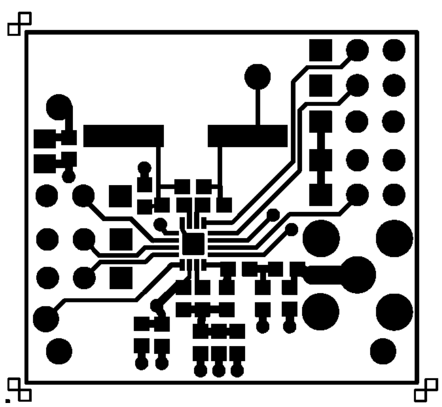
50Ω Output Matching

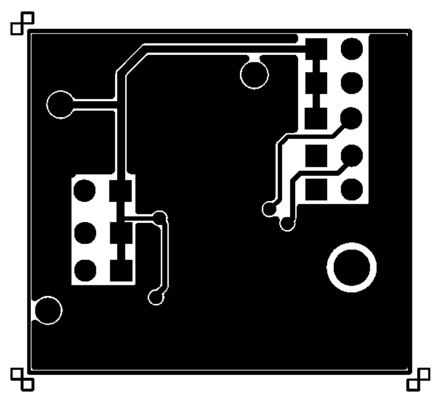
When properly matched, the TXC100 can output up to +12 dBm into a 50Ω load. The output is an open-drain configuration which requires a pull-up inductor for biasing. The pull-up inductance serves to provide biasing for the power amplifier and is a high frequency choke to reduce unwanted coupling back into the power supply. Maximum power transfer occurs when the output is closely matched to 250Ω. For best performance use wirewound inductors instead of chip inductors. Wirewound inductors provide lower insertion loss as opposed to chip inductors. See *Typical Application Circuit* (section IV) for topology and matching component values.

PCB Layout Considerations

PCB layout is critical to proper and consistent operation. Always use controlled impedance lines from the PA_{OUT} (pin 8). For a .062" thick FR4 board, a 50Ω impedance line is approximately 0.110" wide. Component spacing is critical as well. Keep all output matching components as close together as possible to minimize stray inductance and capacitance that can detune the matching network. Keep top side ground planes at least a board thickness away from the signal output leading to the antenna or RF connector.





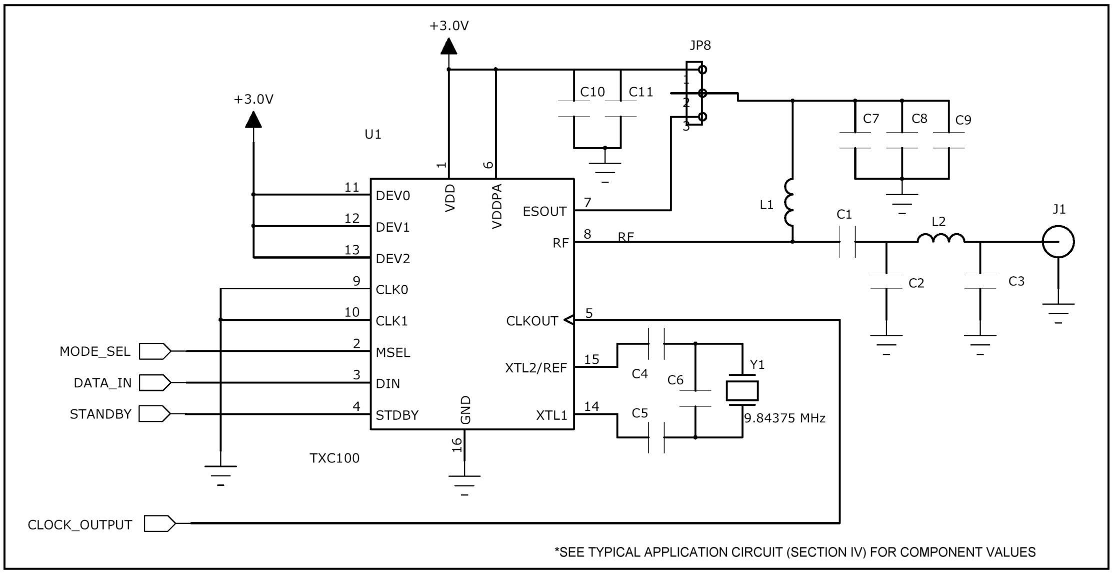


Antenna Layout Considerations

Most compact wireless designs require a small antenna. Loop antennas are often used as they can be designed into small spaces. The design of loop antennas is a fairly lengthy and detailed discussion which is beyond the scope of this datasheet. The object here is to provide a "rule of thumb" approach to achieve an appropriate starting point. Empirical data will provide the best path to take.

The circumference of the antenna should be less than λ/4 so that the antenna appears inductive. For this, a series matching capacitor is used to tune out the inductance of the antenna, since the antenna appears inductive. The capacitor may be located at the feed point of the antenna or at the "grounded" end. The capacitor may be a variable type or several fixed values may be attempted until an optimal match is reached. The use of a good network analyzer is essential for proper matching and maximum power transfer. For additional information on antenna design see the Application Notes section of our website: http://www.rfm.com/corp/apnotes.htm.

Typical Test Circuit



Package Dimensions - 3x3 mm 16-pin TQFN Package

(all values in mm)