19-5010; Rev 1; 3/10

EVALUATION KIT AVAILABLE

5GHz Receiver

MAX2852

General Description

The MAX2852 is a single-chip RF receiver IC designed for 5GHz wireless HDMI applications. The IC includes all circuitry required to implement the complete receiver function and crystal oscillator, providing a fully integrated transmit path, VCO, frequency synthesis, and baseband/control interface. It includes a fast-settling, sigma-delta RF fractional synthesizer with 76Hz frequency programming step size. The IC also integrates on-chip I/Q amplitude and phase-error calibration circuits.

The receiver includes both an in-channel RSSI and an RF RSSI.

The receiver chip is housed in a small, 68-pin thin QFN leadless plastic package with exposed pad.

Applications

5GHz Wireless HDMI™ (WHDI)

5GHz FDD Backhaul and WiMAX™

Features

- **5GHz Single IEEE 802.11a Receiver**
  - **4900MHz to 5900MHz Frequency Range**
  - **4.5dB Rx Noise Figure**
  - **70dB Rx Gain-Control Range with 2dB Step Size, Digitally Controlled**
  - **60dB Dynamic Range Receiver RSSI**
  - **RF Wideband Receiver RSSI**
  - **Programmable 20MHz/40MHz Rx I/Q Lowpass Channel Filters**
  - **Sigma-Delta Fractional-N PLL with 76Hz Resolution**
  - **Monolithic Low-Noise VCO with -35dBc Integrated Phase Noise**
  - **4-Wire SPI™ Digital Interface**
  - **I/Q Analog Baseband Interface**
  - **On-Chip Digital Temperature Sensor Readout**
  - **Complete Baseband Interface**
- **+2.7V to +3.6V Supply Voltage**
- **Small, 68-Pin Thin QFN Package (10mm x 10mm)**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX2852ITK+	-25°C to +85°C	68 Thin QFN-EP*

**EP = Exposed pad.*
+Denotes a lead(Pb)-free/RoHS-compliant package.

SPI is a trademark of Motorola, Inc.
HDMI is a trademark of HDMI Licensing, LLC.
WiMAX is a trademark of WiMAX Forum.

Typical Operating Circuit appears at end of data sheet.

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ABSOLUTE MAXIMUM RATINGS

$V_{CC\_}$ Pins to GND .....-0.3V to +3.9V
RF Inputs Maximum Current: RXRF+, RXRF- to GND .....-1mA to +1mA
RF Outputs: TXRF+, TXRF- to GND .....-0.3V to +3.9V
Analog Inputs: TXBBI+, TXBBI-, TXBBQ+, TXBBQ-, XTAL to GND.....-0.3V to +3.9V
Analog Outputs: RXBBI+, RXBBI-, RXBBQ+, RXBBQ-, RSSI, CLKOUT2, VCOBYP, CPOUT+, CPOUT- to GND .....-0.3V to +3.9V
Digital Inputs: ENABLE, $\overline{CS}$, SCLK, DIN to GND...-0.3V to +3.9V
Digital Outputs: DOUT, CLKOUT to GND.....-0.3V to +3.9V
Short-Circuit Duration
Analog Outputs 10s
Digital Outputs..... 10s
RF Input Power.....+10dBm
RF Output Differential Load VSWR 6:1
Continuous Power Dissipation (T_A = +85°C)
68-Pin Thin QFN (derate 29.4mW/°C above +70°C) 2352mW
Operating Temperature Range..... -25°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range..... -65°C to +160°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION! ESD SENSITIVE DEVICE

DC ELECTRICAL CHARACTERISTICS

(Operating conditions, unless otherwise specified: V_{CC} = 2.7V~3.6V, ENABLE set according to operating mode, $\overline{CS}$ = high, SCLK = DIN = low, transmitter in maximum gain, T_A = -25°C to +85°C. Power matching and termination for the differential RF output pins using the *Typical Operating Circuit*. 100mV_{RMS} differential I and Q signals applied to I/Q baseband inputs of transmitters in transmit calibration mode. Typical values measured at V_{CC} = 2.85V, LO frequency = 5.35GHz, T_A = +25°C. Channel bandwidth is set to 40MHz. PA control pins open circuit, $V_{CC\_PA\_BIAS}$ is disconnected.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage, V_{CC}		2.7		3.6	V
Supply Current	Shutdown mode, T_A = +25°C		10		µA
	Clock-out only mode		7.4	11	mA
	Standby mode		60	89	
	Receive mode		135	174	
	Transmit calibration mode, one transmitter is on		214	261	
	Receive calibration mode		268	327	
Rx I/Q Output Common-Mode Voltage		0.9	1.1	1.3	V
Tx Baseband Input Common-Mode Voltage Operating Range		0.5		1.1	V
Tx Baseband Input Bias Current	Source current		10	20	µA
LOGIC INPUTS: ENABLE, SCLK, DIN, $\overline{CS}$					
Digital Input-Voltage High, V_{IH}		V_{CC} - 0.4			V
Digital Input-Voltage Low, V_{IL}				0.4	V
Digital Input-Current High, I_{IH}		-1		+1	µA
Digital Input-Current Low, I_{IL}		-1		+1	µA

DC ELECTRICAL CHARACTERISTICS (continued)

(Operating conditions, unless otherwise specified: V_{CC} = 2.7V~3.6V, ENABLE set according to operating mode, $\overline{CS}$ = high, SCLK = DIN = low, transmitter in maximum gain, T_A = -25°C to +85°C. Power matching and termination for the differential RF output pins using the *Typical Operating Circuit*. 100mV_{RMS} differential I and Q signals applied to I/Q baseband inputs of transmitters in transmit calibration mode. Typical values measured at V_{CC} = 2.85V, LO frequency = 5.35GHz, T_A = +25°C. Channel bandwidth is set to 40MHz. PA control pins open circuit, $V_{CC\_PA\_BIAS}$ is disconnected.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC OUTPUTS: DOUT, CLKOUT					
Digital Output-Voltage High, V_{OH}	Sourcing 1mA	V_{CC} - 0.4			V
Digital Output-Voltage Low, V_{OL}	Sinking 1mA			0.4	V
Digital Output Voltage in Shutdown Mode	Sinking 1mA		V_{OL}		V

AC ELECTRICAL CHARACTERISTICS—Rx MODE

(Operating conditions, unless otherwise specified: V_{CC} = 2.7V~3.6V, RF frequency = 5.351GHz, T_A = -25°C to +85°C. LO frequency = 5.35GHz. Reference frequency = 40MHz, ENABLE = high, $\overline{CS}$ = high, SCLK = DIN = low, with power matching at RXRF+ and RXRF- differential ports using the *Typical Operating Circuit*. Receiver I/Q output at 100mV_{RMS} loaded with 10kΩ differential load resistance and 10pF load capacitance. The RSSI pin is loaded with 10kΩ load resistance to ground. Typical values measured at V_{CC} = 2.85V, channel bandwidths of 40MHz, T_A = +25°C.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
RECEIVER SECTION: RF INPUT TO I/Q BASEBAND LOADED OUTPUT (Includes 50Ω to 100Ω RF Balun and Matching)					
RF Input Frequency Range		4.9		5.9	GHz
Peak-to-Peak Gain Variation over RF Frequency Range at One Temperature	4.9GHz to 5.35GHz		0.3	2.6	dB
	5.35GHz to 5.9GHz		2.2	5.3	
RF Input Return Loss	All LNA settings		-6		dB
Total Voltage Gain	Maximum gain; Main address 1 D7:0 = 11111111	61	68		dB
	Minimum gain; Main address 1 D7:0 = 00000000		-2	+0.5	
RF Gain Steps Relative to Maximum Gain	Main address 1 D7:D5 = 110		-8		dB
	Main address 1 D7:D5 = 101		-16		
	Main address 1 D7:D5 = 001		-32		
	Main address 1 D7:D5 = 000		-40		
Baseband Gain Range	From maximum baseband gain (Main address 1 D3:D0 = 1111) to minimum baseband gain (Main address 1 D3:D0 = 0000)	27.5	30	32.5	dB
Baseband Gain Step			2		dB
RF Gain-Change Settling Time	Gain settling to within ±0.5dB of steady state; RXHP = 1		400		ns
Baseband Gain-Change Settling Time	Gain settling to within ±0.5dB of steady state; RXHP = 1		200		ns

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AC ELECTRICAL CHARACTERISTICS—Rx MODE (continued)

(Operating conditions, unless otherwise specified: V_{CC} = 2.7V~3.6V, RF frequency = 5.351GHz, T_A = -25°C to +85°C. LO frequency = 5.35GHz. Reference frequency = 40MHz, ENABLE = high, $\overline{CS}$ = high, SCLK = DIN = low, with power matching at RXRF+ and RXRF- differential ports using the *Typical Operating Circuit*. Receiver I/Q output at 100mV_{RMS} loaded with 10kΩ differential load resistance and 10pF load capacitance. The RSSI pin is loaded with 10kΩ load resistance to ground. Typical values measured at V_{CC} = 2.85V, channel bandwidths of 40MHz, T_A = +25°C.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DSB Noise Figure	Balun input referred, integrated from 10kHz to 9.5MHz at I/Q baseband output for 20MHz RF bandwidth	Maximum RF gain (Main address 1 D7:D5 = 111)		4.5		dB
		Maximum RF gain - 16dB (Main address 1 D7:D5 = 101)		15		
	Balun input referred, integrated from 10kHz to 19MHz at I/Q baseband output for 40MHz RF bandwidth	Maximum RF gain (Main address 1 D7:D5 = 111)		4.5		
		Maximum RF gain - 16dB (Main address 1 D7:D5 = 101)		15		
Out-of-Band Input IP3	20MHz RF channel; two-tone jammers at +25MHz and +48MHz frequency offset with -39dBm/tone	-65dBm wanted signal; RF gain = max (Main address 1 D7:D0 = 11101001)		-13		dBm
		-49dBm wanted signal; RF gain = max - 16dB (Main address 1 D7:D0 = 10101001)		-5		
		-45dBm wanted signal; RF gain = max - 32dB (Main address 1 D7:D0 = 00111111)		11		
	40MHz RF channel; two-tone jammers at +50MHz and +96MHz frequency offset with -39dBm/tone	-65dBm wanted signal; RF gain = max (Main address 1 D7:D0 = 11101001)		-13		
		-49dBm wanted signal; RF gain = max - 16dB (Main address 1 D7:D0 = 10101001)		-5		
		-45dBm wanted signal; RF gain = max - 32dB (Main address 1 D7:D0 = 00101001)		11		
1dB Gain Desensitization by Alternate Channel Blocker	Blocker at ±40MHz offset frequency for 20MHz RF channel			-24		dBm
	Blocker at ±80MHz offset frequency for 40MHz RF channel			-24		
Input 1dB Gain Compression	Max RF gain (Main address 1 D7:D5 = 111)			-32		dBm
	Max RF gain - 8dB (Main address 1 D7:D5 = 110)			-24		
	Max RF gain - 16dB (Main address 1 D7:D5 = 101)			-16		
	Max RF gain - 32dB (Main address 1 D7:D5 = 001)			0		
Output 1dB Gain Compression	Over passband frequency range; at any gain setting; 1dB compression point			0.63		V_{P-P}

AC ELECTRICAL CHARACTERISTICS—Rx MODE (continued)

(Operating conditions, unless otherwise specified: V_{CC} = 2.7V~3.6V, RF frequency = 5.351GHz, T_A = -25°C to +85°C. LO frequency = 5.35GHz. Reference frequency = 40MHz, ENABLE = high, $\overline{CS}$ = high, SCLK = DIN = low, with power matching at RXRF+ and RXRF- differential ports using the *Typical Operating Circuit*. Receiver I/Q output at 100mV_{RMS} loaded with 10kΩ differential load resistance and 10pF load capacitance. The RSSI pin is loaded with 10kΩ load resistance to ground. Typical values measured at V_{CC} = 2.85V, channel bandwidths of 40MHz, T_A = +25°C.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Baseband -3dB Lowpass Corner Frequency	Main address 0 D1 = 0		9.5		MHz
	Main address 0 D1 = 1		19		
Baseband Filter Stopband Rejection	Rejection at 30MHz offset frequency for 20MHz channel	57	70		dB
	Rejection at 60MHz offset frequency for 40MHz channel	57	70		
Baseband -3dB Highpass Corner Frequency	Main address 5 D1 = 1		600		kHz
	Main address 5 D1 = 0		10		
Steady-State I/Q Output DC Error with AC-Coupling	50µs after enabling receive mode and toggling RxHP from 1 to 0, averaged over many measurements if I/Q noise voltage exceeds 1mV_{RMS}, at any given gain setting, no input signal, 1-sigma value		2		mV
I/Q Gain Imbalance	1MHz baseband output, 1-sigma value		0.1		dB
I/Q Phase Imbalance	1MHz baseband output, 1-sigma value		0.2		degrees
Sideband Suppression	1MHz baseband output (Note 2)		40		dB
Receiver Spurious Signal Emissions	LO frequency		-75		dBm/MHz
	2 x LO frequency		-62		
	3 x LO frequency		-75		
	4 x LO frequency		-60		
RF RSSI Output Voltage	-20dBm input power		1.75		V
Baseband RSSI Slope		19.5	26.5	35.5	mV/dB
Baseband RSSI Maximum Output Voltage			2.3		V
Baseband RSSI Minimum Output Voltage			0.5		V
RF Loopback Conversion Gain	Tx VGA gain at maximum (Main address 9 D9:D4 = 111111); Rx VGA gain at maximum - 24dB (Main address 1 D3:D0 = 0101)	-6	+2	+10	dB

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AC ELECTRICAL CHARACTERISTICS—Tx CALIBRATION MODE

(Operating conditions, unless otherwise specified: V_{CC} = 2.7V~3.6V, RF frequency = 5.351GHz, T_A = -25°C to +85°C. LO frequency = 5.35GHz. Reference frequency = 40MHz, ENABLE = high, $\overline{CS}$ = high, SCLK = DIN = low, with power matching at TXRF+ and TXRF- differential ports using the *Typical Operating Circuit*. 100mV_{RMS} sine and cosine signal applied to I/Q baseband inputs of transmitter (differential DC-coupled). Typical values measured at V_{CC} = 2.85V, channel bandwidths of 40MHz, T_A = +25°C.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Tx I/Q Input Impedance (RIIC)	Minimum differential resistance		100		kΩ
	Maximum differential capacitance		1.2		pF
Tx Calibration Ftone Level	At Tx gain code (Main address 9 D9:D4) = 100010 and -15dBc carrier leakage (Local address 27 D2:D0 = 110 and Main address 1 D3:D0 = 0000)		-28		dBV_{RMS}
Tx Calibration Gain Range	Adjust Local address 27 D2:D0		35		dB

AC ELECTRICAL CHARACTERISTICS—FREQUENCY SYNTHESIS

(Operating conditions, unless otherwise specified: V_{CC} = 2.7V~3.6V, frequency = 5.35GHz, T_A = -25°C to +85°C. Reference frequency = 40MHz, ENABLE = high, $\overline{CS}$ = high, SCLK = DIN = low. Typical values measured at V_{CC} = 2.85V, T_A = +25°C, LO frequency = 5.35GHz, T_A = +25°C.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
FREQUENCY SYNTHESIZER					
RF Channel Center Frequency		4.9		5.9	GHz
Channel Center Frequency Programming Step			76.294		Hz
Closed-Loop Integrated Phase Noise	Loop BW = 200kHz, integrate phase noise from 1kHz to 10MHz		-35		dBc
Charge-Pump Output Current			0.8		mA
Spur Level	f_{OFFSET} = 0 to 19MHz		-42		dBc
	f_{OFFSET} = 40MHz		-66		
Reference Frequency			40		MHz
Reference Frequency Input Levels	AC-coupled to XTAL pin	800			mV_{P-P}
CLKOUT Signal Level	10pF load capacitance	V_{CC} - 0.8	V_{CC} - 0.1		V_{P-P}

AC ELECTRICAL CHARACTERISTICS—MISCELLANEOUS BLOCKS

(Operating conditions, unless otherwise specified: V_{CC} = 2.7V~3.6V, T_A = -25°C to +85°C. Reference frequency = 40MHz, ENABLE = high, $\overline{CS}$ = high, SCLK = DIN = low. Typical values measured at V_{CC} = 2.85V, T_A = +25°C.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
ON-CHIP TEMPERATURE SENSOR						
Digital Output Code	Read-out at DOUT pin through Main address 3 D4:D0	T_A = +25°C		17		
		T_A = +85°C		25		
		T_A = -20°C		9		

AC ELECTRICAL CHARACTERISTICS—TIMING

(Operating conditions, unless otherwise specified: V_{CC} = 2.7V~3.6V, frequency = 5.35GHz, T_A = -25°C to +85°C. Reference frequency = 40MHz, ENABLE = high, $\overline{CS}$ = high, SCLK = DIN = low. Typical values measured at V_{CC} = 2.85V, LO frequency = 5.35GHz, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SYSTEM TIMING						
Shutdown Time				2		µs
Maximum Channel Switching Time		Loop bandwidth = 200kHz, settling to within ±1kHz from steady state		2		ms
Maximum Channel Switching Time With Preselected VCO Sub-Band		Loop bandwidth = 200kHz, settling to within ±1kHz from steady state		56		µs
Rx Turn-On Time (from Standby Mode)		Measured from $\overline{CS}$ rising edge, Rx gain settles to within 0.5dB of steady state		2		µs
Rx Turn-Off Time (to Standby Mode)		From $\overline{CS}$ rising edge		0.1		µs
4-WIRE SERIAL-INTERFACE TIMING (See Figure 1)						
SCLK Rising Edge to $\overline{CS}$ Falling Edge Wait Time	t_{CSO}			6		ns
Falling Edge of $\overline{CS}$ to Rising Edge of First SCLK Time	t_{CSS}			6		ns
DIN to SCLK Setup Time	t_{DS}			6		ns
DIN to SCLK Hold Time	t_{DH}			6		ns

AC ELECTRICAL CHARACTERISTICS—TIMING (continued)

(Operating conditions, unless otherwise specified: V_{CC} = 2.7V~3.6V, frequency = 5.35GHz, T_A = -25°C to +85°C. Reference frequency = 40MHz, ENABLE = high, $\overline{CS}$ = high, SCLK = DIN = low. Typical values measured at V_{CC} = 2.85V, LO frequency = 5.35GHz, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Pulse-Width High	t_{CH}			6		ns
SCLK Pulse-Width Low	t_{CL}			6		ns
Last Rising Edge of SCLK to Rising Edge of $\overline{CS}$ or Clock to Load Enable Setup Time	t_{CSH}			6		ns
$\overline{CS}$ High Pulse Width	t_{CSW}			50		ns
Time Between Rising Edge of $\overline{CS}$ and the Next Rising Edge of SCLK	t_{CS1}			6		ns
SCLK Frequency	f_{CLK}				40	MHz
Rise Time	t_R			2.5		ns
Fall Time	t_F			2.5		ns
SCLK Falling Edge to Valid DOUT	t_D			12.5		ns

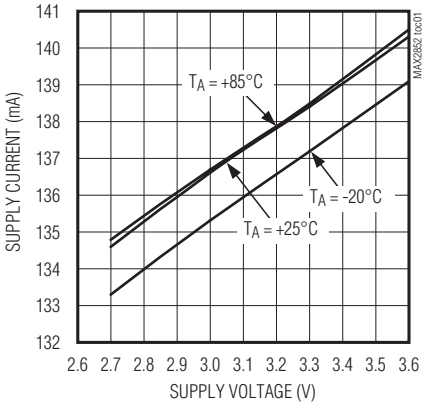
Note 1: The MAX2852 is production tested at T_A = +25°C; minimum/maximum limits at T_A = +25°C are guaranteed by test, unless specified otherwise. Minimum/maximum limits at T_A = -25°C and +85°C are guaranteed by design and characterization. There is no power-on register settings self-reset; recommended register settings must be loaded after V_{CC} is applied.

Note 2: For optimal Rx and Tx quadrature accuracy over temperature, the user can utilize the Rx calibration and Tx calibration circuit to assist quadrature calibration.

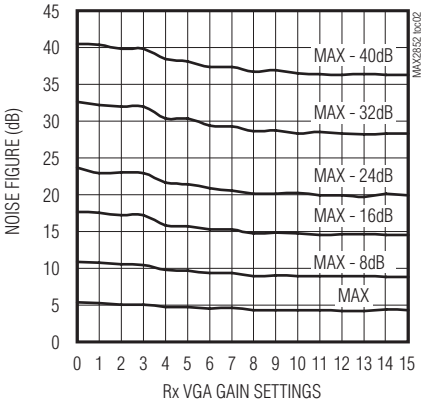
Typical Operating Characteristics

(V_{CC} = 2.8V, f_{LO} = 5.35GHz, f_{REF} = 40MHz, $\overline{CS}$ = high, SCLK = DIN = low, RF BW = 20MHz, Tx output at 50Ω unbalanced output of balun, T_A = +25°C, using the MAX2852 Evaluation Kit.)

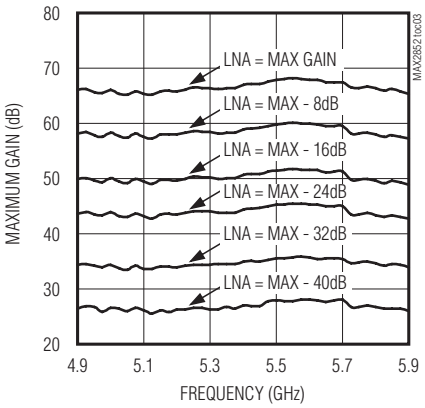
Rx MODE SUPPLY CURRENT



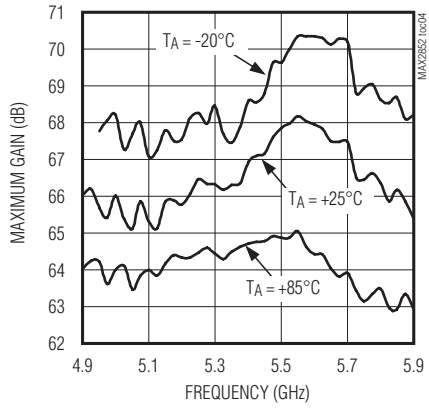
Rx NOISE FIGURE vs. VGA GAIN SETTINGS (BALUN INPUT REFERRED)



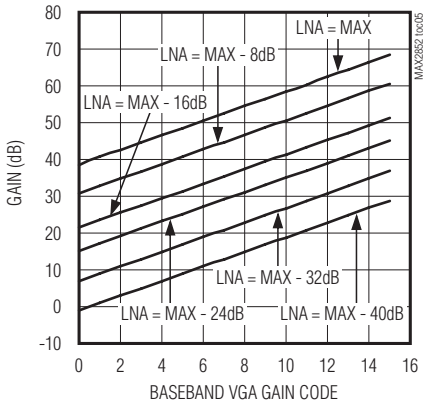
Rx MAXIMUM GAIN vs. FREQUENCY



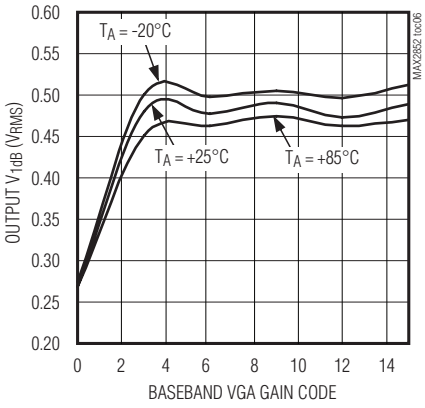
Rx MAXIMUM GAIN vs. TEMPERATURE AND FREQUENCY



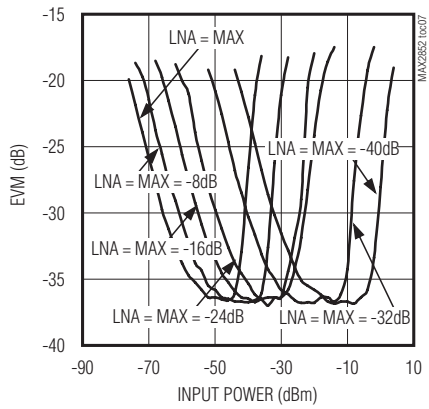
Rx GAIN vs. BASEBAND VGA GAIN



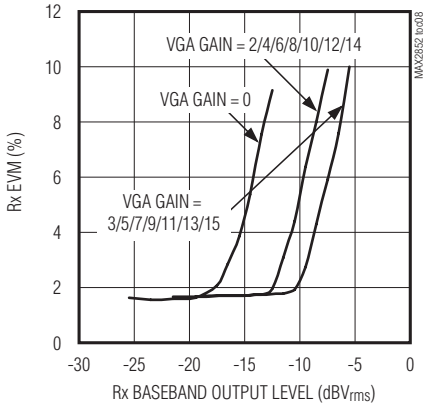
Rx OUTPUT V_{1dB} vs. GAIN SETTING



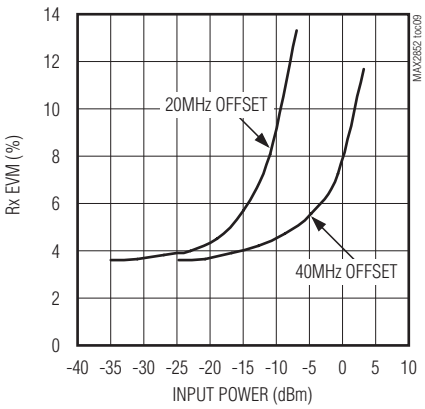
Rx EVM vs. INPUT POWER (CHANNEL BANDWIDTH = 20MHz)



Rx EVM vs. Rx BASEBAND OUTPUT LEVEL



Rx EVM vs. OFDM JAMMER POWER AT 20MHz AND 40MHz OFFSET FREQUENCY WITH WANTED SIGNAL AT -66dBm



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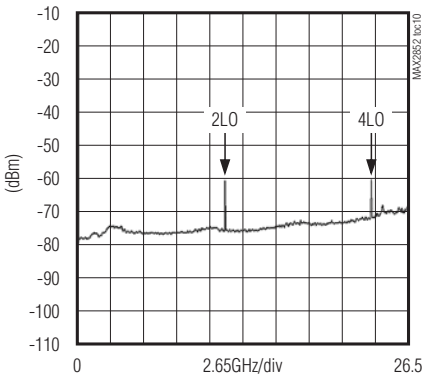
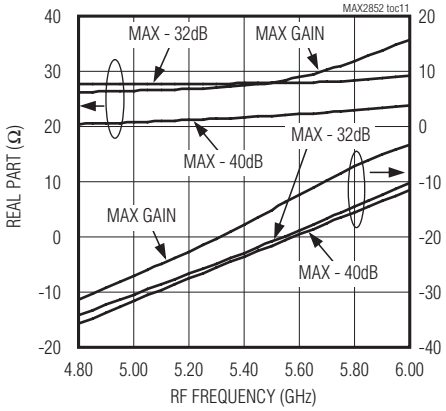
Typical Operating Characteristics (continued)

(V_{CC} = 2.8V, f_{LO} = 5.35GHz, f_{REF} = 40MHz, $\overline{CS}$ = high, SCLK = DIN = low, RF BW = 20MHz, Tx output at 50Ω unbalanced output of balun, T_A = +25°C, using the MAX2852 Evaluation Kit.)

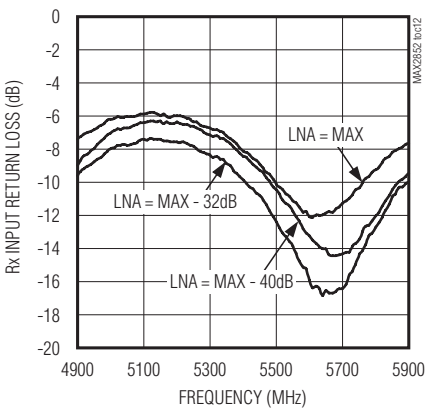
Rx EMISSION SPECTRUM AT LNA INPUT (LNA = MAX GAIN)



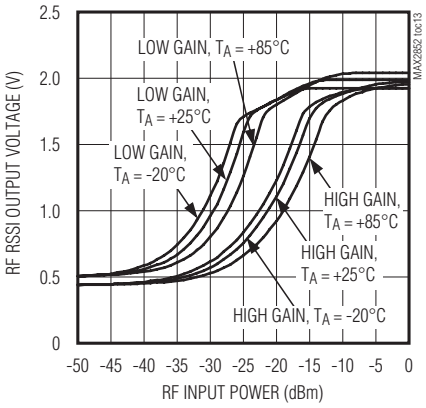
Rx INPUT IMPEDANCE



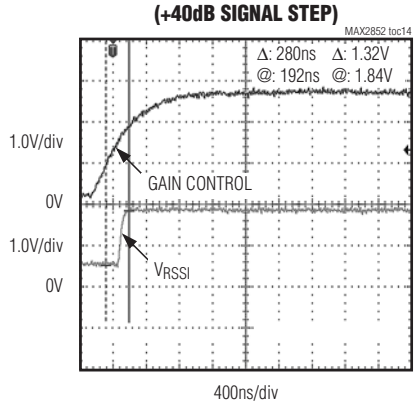
Rx INPUT RETURN LOSS



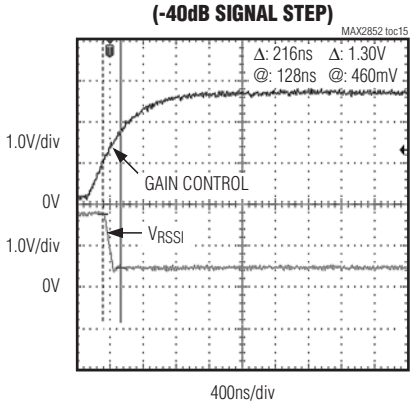
Rx RF RSSI OUTPUT



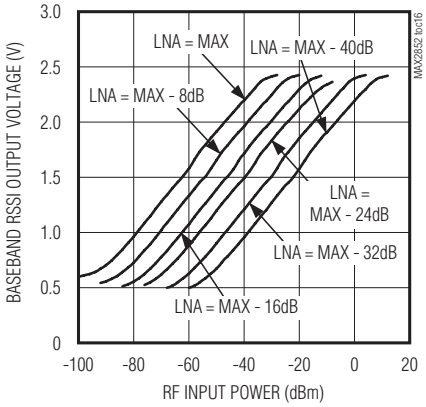
Rx RF RSSI ATTACK TIME (+40dB SIGNAL STEP)



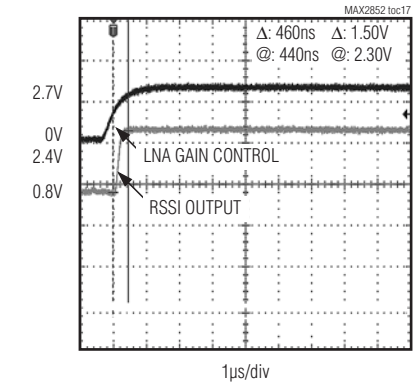
Rx RF RSSI DELAY TIME (-40dB SIGNAL STEP)



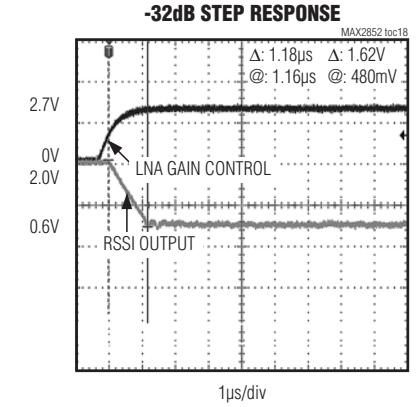
BASEBAND RSSI VOLTAGE vs. INPUT POWER



Rx BASEBAND RSSI +40dB STEP RESPONSE



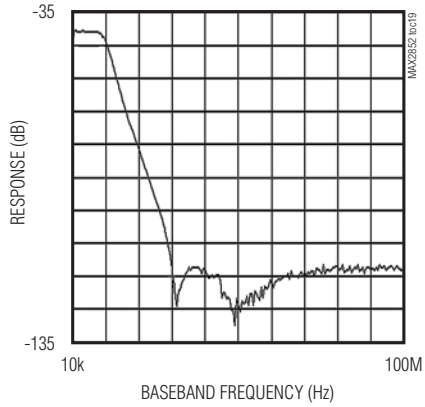
Rx BASEBAND RSSI -32dB STEP RESPONSE



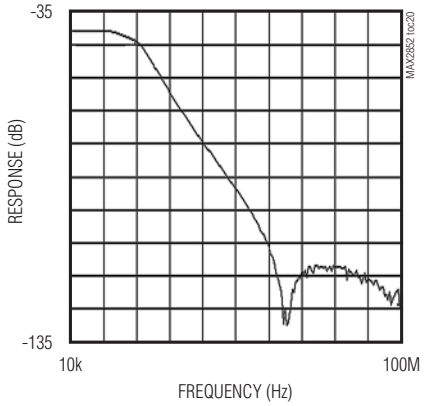
Typical Operating Characteristics (continued)

(V_{CC} = 2.8V, f_{LO} = 5.35GHz, f_{REF} = 40MHz, $\overline{CS}$ = high, SCLK = DIN = low, RF BW = 20MHz, Tx output at 50Ω unbalanced output of balun, T_A = +25°C, using the MAX2852 Evaluation Kit.)

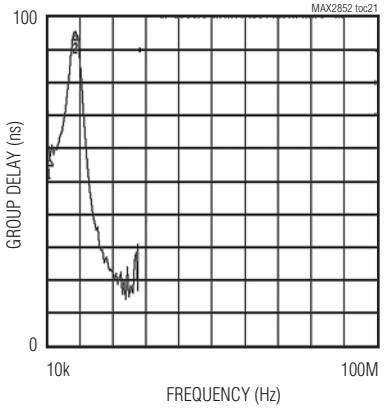
Rx LPF 20MHz CHANNEL BANDWIDTH RESPONSE



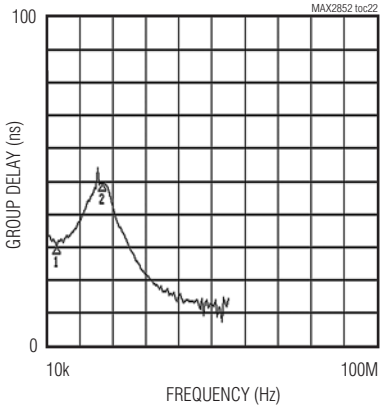
Rx LPF 40MHz CHANNEL BANDWIDTH RESPONSE



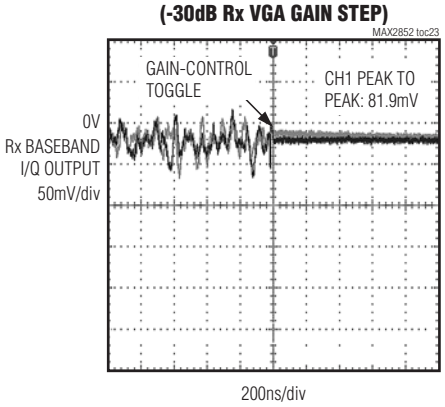
Rx LPF 20MHz CHANNEL BANDWIDTH GROUP DELAY



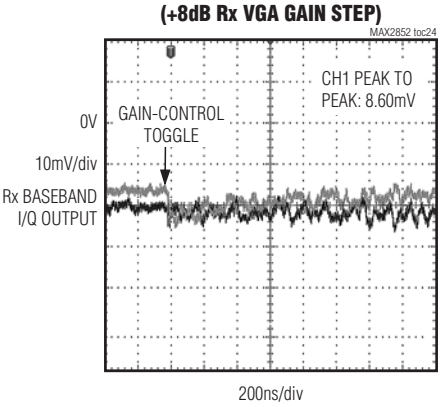
Rx LPF 40MHz CHANNEL BANDWIDTH GROUP DELAY



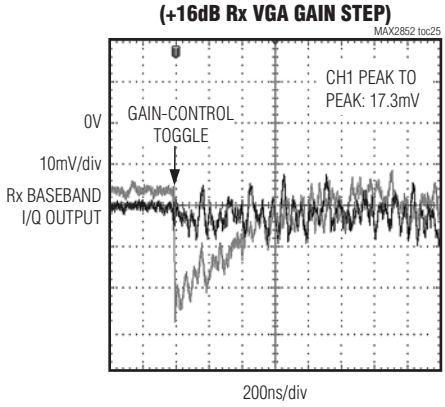
Rx DC OFFSET SETTLING RESPONSE (-30dB Rx VGA GAIN STEP)



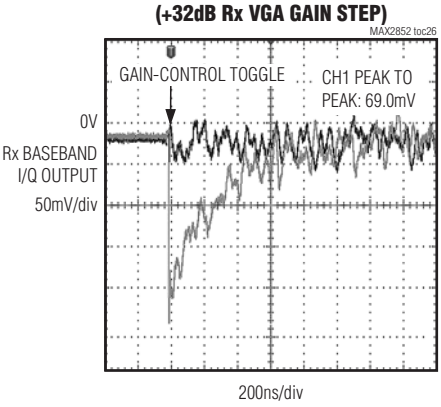
Rx DC OFFSET SETTLING RESPONSE (+8dB Rx VGA GAIN STEP)



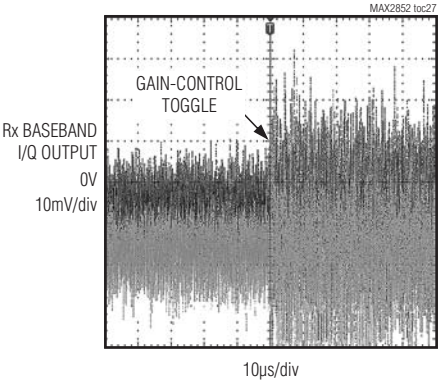
Rx DC OFFSET SETTLING RESPONSE (+16dB Rx VGA GAIN STEP)



Rx DC OFFSET SETTLING RESPONSE (+32dB Rx VGA GAIN STEP)



Rx BASEBAND DC OFFSET SETTLING RESPONSE WITH RxHP = 1 (MAX - 40dB TO MAX LNA GAIN STEP)

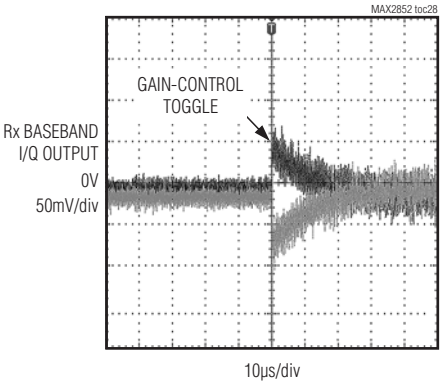


5GHz Receiver

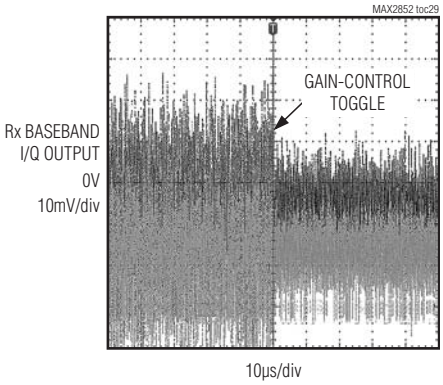
Typical Operating Characteristics (continued)

(V_{CC} = 2.8V, f_{LO} = 5.35GHz, f_{REF} = 40MHz, $\overline{CS}$ = high, SCLK = DIN = low, RF BW = 20MHz, Tx output at 50Ω unbalanced output of balun, T_A = +25°C, using the MAX2852 Evaluation Kit.)

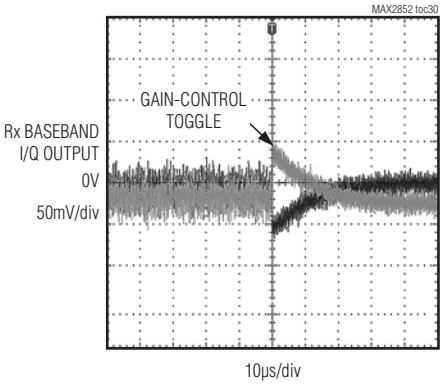
Rx BASEBAND DC OFFSET SETTLING RESPONSE WITH RxHP = 0 (MAX TO MAX - 40dB LNA GAIN STEP)



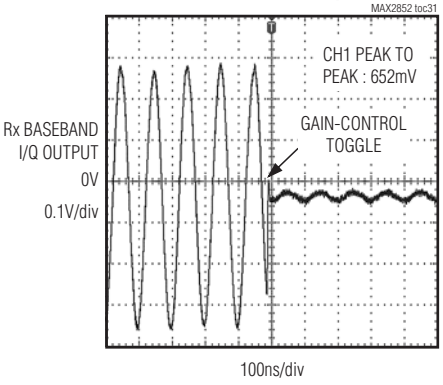
Rx BASEBAND DC OFFSET SETTLING RESPONSE WITH RxHP = 1 (MAX - 40dB TO MAX LNA GAIN STEP)



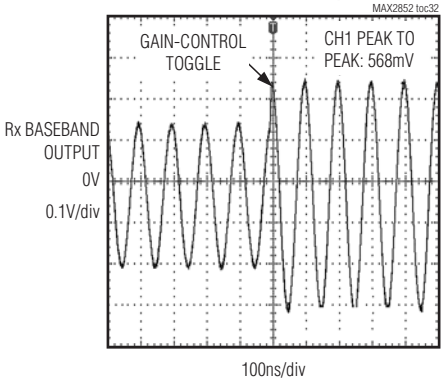
Rx BASEBAND DC OFFSET SETTLING RESPONSE WITH RxHP = 0 (MAX - 40dB TO MAX LNA GAIN STEP)



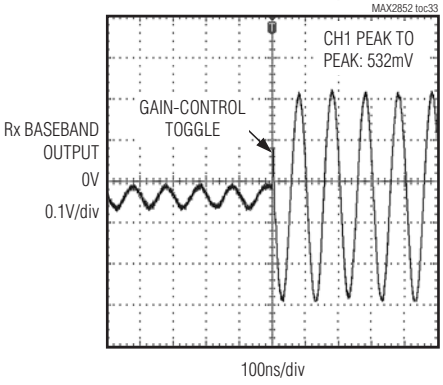
Rx BASEBAND VGA SETTLING RESPONSE (-30dB BASEBAND VGA GAIN STEP)



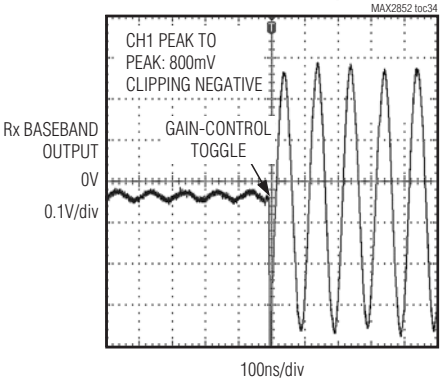
Rx BASEBAND VGA SETTLING RESPONSE (+4dB BASEBAND VGA GAIN STEP)



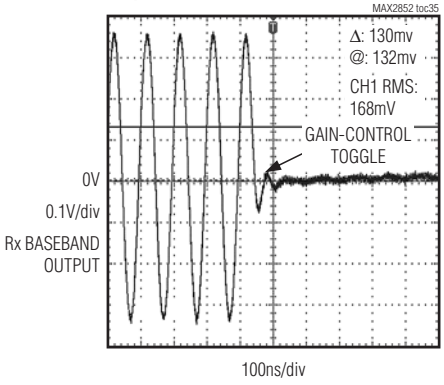
Rx BASEBAND VGA SETTLING RESPONSE (+16dB BASEBAND VGA GAIN STEP)



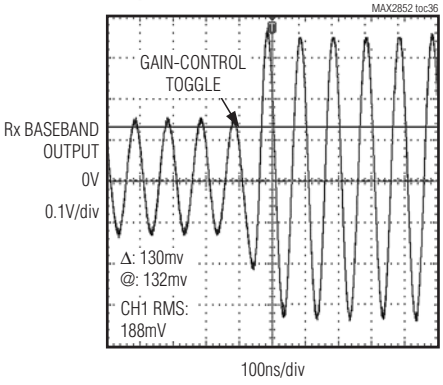
Rx BASEBAND VGA SETTLING RESPONSE (+30dB BASEBAND VGA GAIN STEP)



Rx LNA SETTLING RESPONSE (MAX TO MAX - 40dB GAIN STEP)



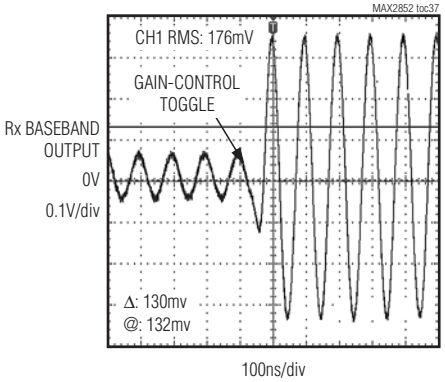
Rx LNA SETTLING RESPONSE (MAX - 8dB TO MAX GAIN STEP)



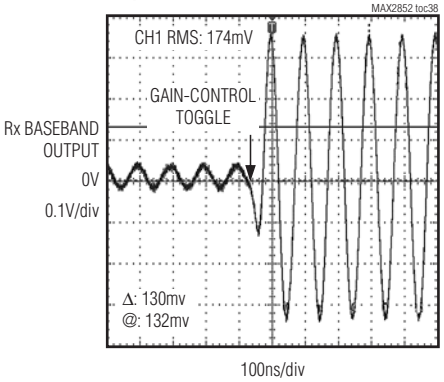
Typical Operating Characteristics (continued)

(V_{CC} = 2.8V, f_{LO} = 5.35GHz, f_{REF} = 40MHz, $\overline{CS}$ = high, SCLK = DIN = low, RF BW = 20MHz, Tx output at 50Ω unbalanced output of balun, T_A = +25°C, using the MAX2852 Evaluation Kit.)

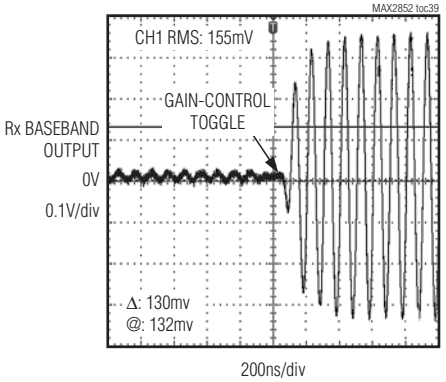
Rx LNA SETTLING RESPONSE (MAX - 16dB TO MAX GAIN STEP)



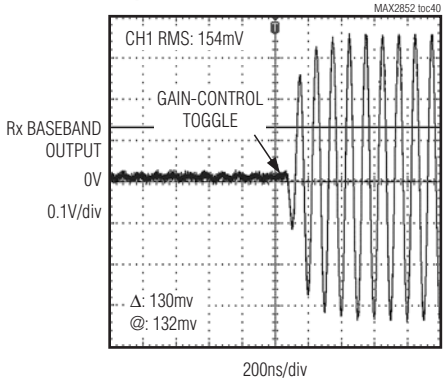
Rx LNA SETTLING RESPONSE (MAX - 24dB TO MAX GAIN STEP)



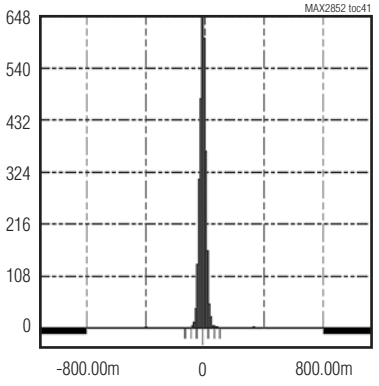
Rx LNA SETTLING RESPONSE (MAX - 32dB TO MAX GAIN STEP)



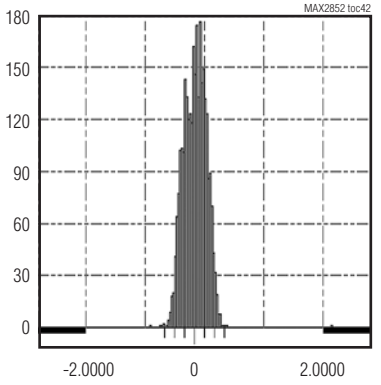
Rx LNA SETTLING RESPONSE (MAX - 40dB TO MAX GAIN STEP)



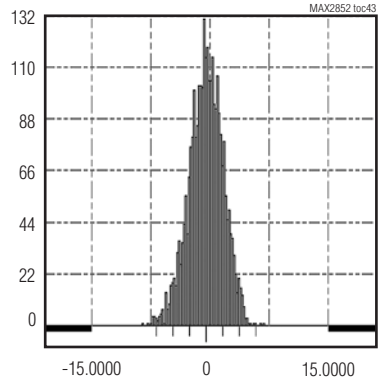
HISTOGRAM: Rx I/Q GAIN IMBALANCE



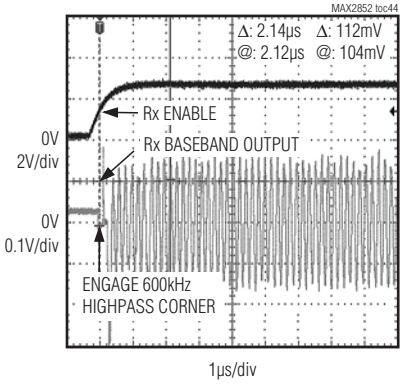
HISTOGRAM: Rx I/Q PHASE IMBALANCE



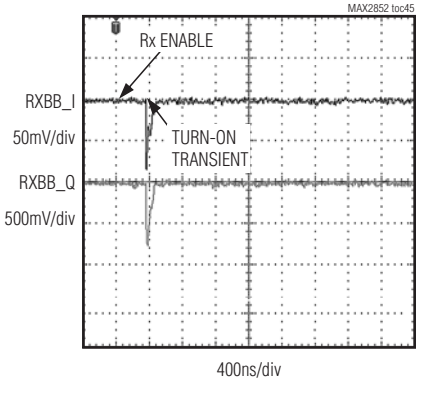
HISTOGRAM: Rx STATIC DC OFFSET



POWER-ON DC OFFSET CANCELLATION WITH INPUT SIGNAL



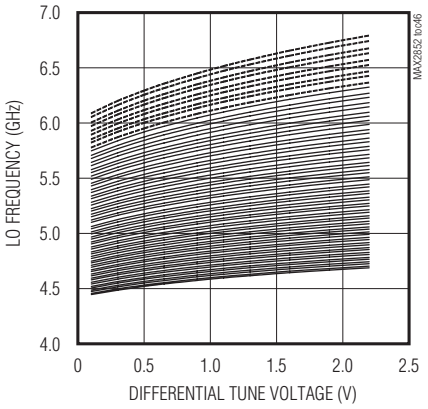
POWER-ON DC OFFSET CANCELLATION WITHOUT INPUT SIGNAL



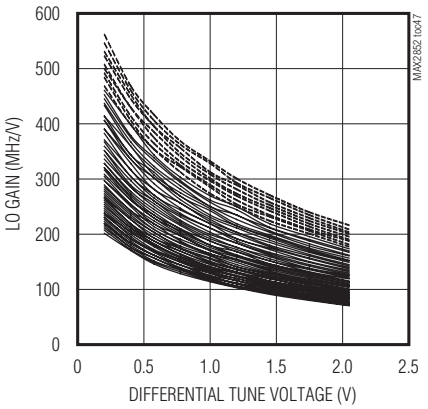
Typical Operating Characteristics (continued)

(V_{CC} = 2.8V, f_{LO} = 5.35GHz, f_{REF} = 40MHz, $\overline{CS}$ = high, SCLK = DIN = low, RF BW = 20MHz, Tx output at 50Ω unbalanced output of balun, T_A = +25°C, using the MAX2852 Evaluation Kit.)

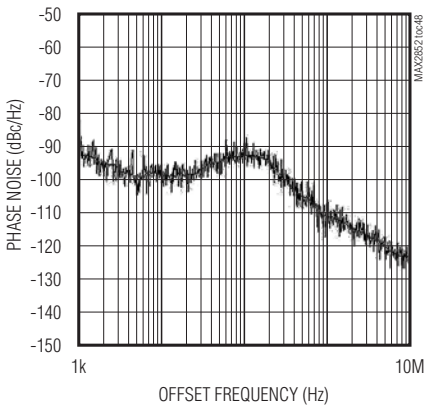
LO FREQUENCY vs. DIFFERENTIAL TUNE VOLTAGE AT T_A = +25°C



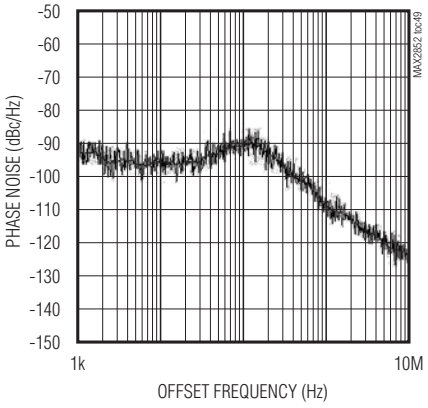
LO GAIN vs. DIFFERENTIAL TUNE VOLTAGE AT T_A = +25°C



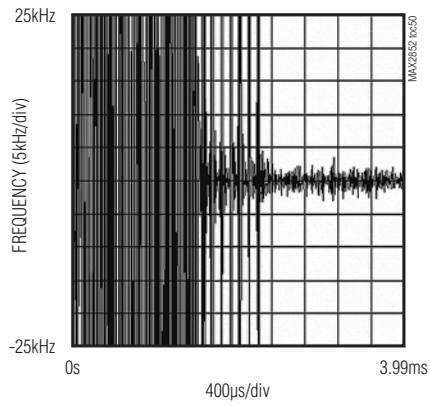
LO PHASE NOISE AT 5350MHz AND ROOM TEMPERATURE



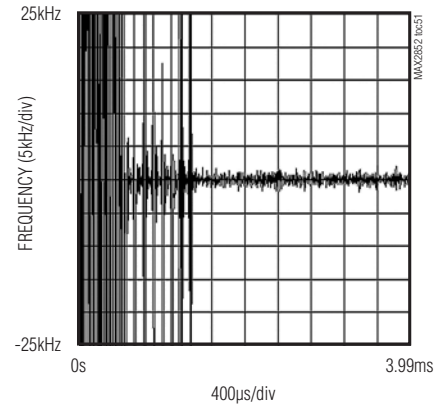
LO PHASE NOISE AT 5900MHz AND HOT TEMPERATURE



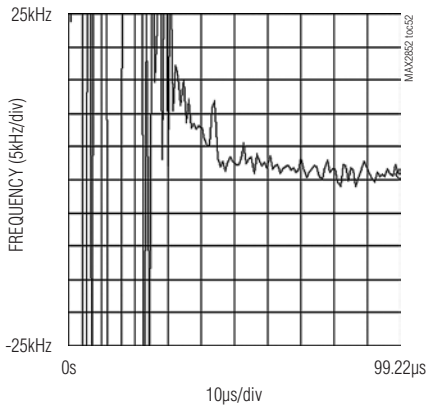
CHANNEL SWITCHING FREQUENCY SETTLING (4900MHz TO 5900MHz, AUTOMATIC VCO SUB-BAND SELECTION)



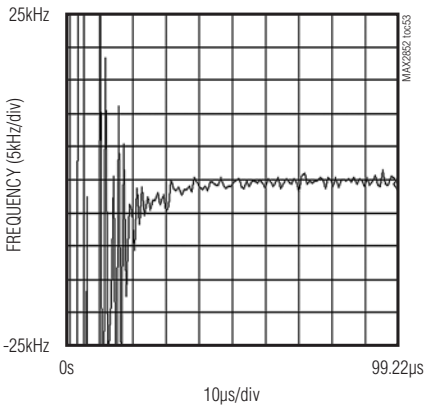
CHANNEL SWITCHING FREQUENCY SETTLING (5900MHz TO 4900MHz, AUTOMATIC VCO SUB-BAND SELECTION)



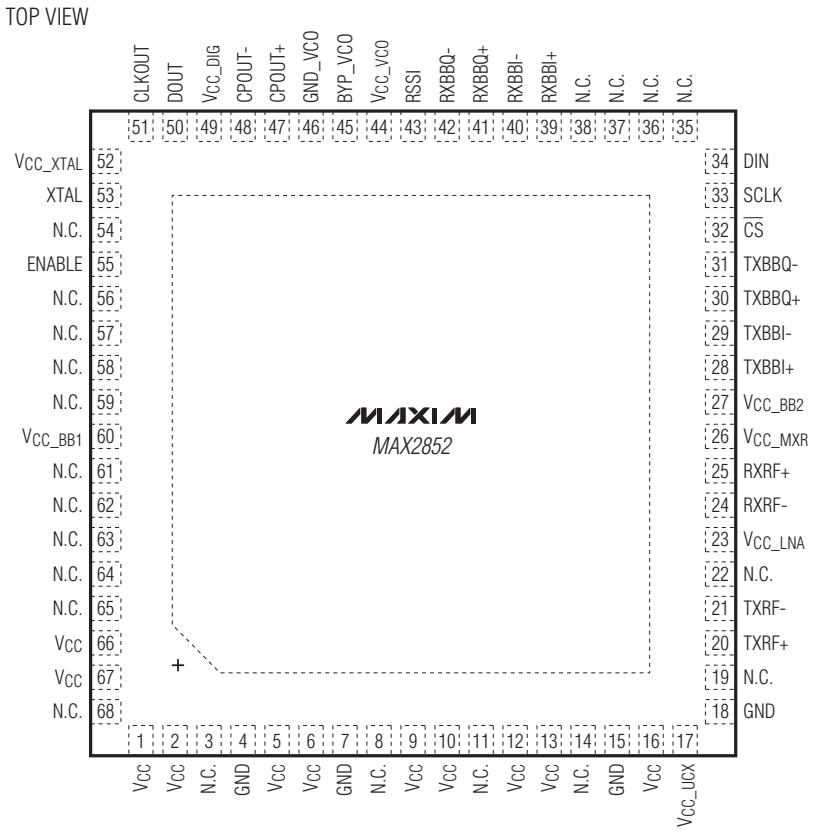
CHANNEL SWITCHING FREQUENCY SETTLING (4900MHz TO 5900MHz, MANUAL VCO SUB-BAND SELECTION)



CHANNEL SWITCHING FREQUENCY SETTLING (5900MHz TO 4900MHz, MANUAL VCO SUB-BAND SELECTION)



Pin Configuration



TQFN
10mm x 10mm

5GHz Receiver

Pin Description

PIN	NAME	FUNCTION
1, 2, 5, 6, 9, 10, 12, 13, 16, 66, 67	V_{CC}	Supply Voltage
3, 8, 11, 14, 19, 22, 35–38, 54, 56–59, 61–65, 68	N.C.	No Connection
4, 7, 15, 18	GND	Ground
17	V_{CC_UCX}	Transmitter Upconverter Supply Voltage. Bypass with a capacitor as close as possible to the pin.
20	TXRF-	Transmitter Differential Outputs. These pins are in open-collector configuration. They hould be biased at supply voltage with differential impedance terminated at 300Ω.
21	TXRF+	
23	V_{CC_LNA}	Receiver LNA Supply Voltage. Bypass with a capacitor as close as possible to the pin.
24	RXRF-	Receiver LNA Differential Inputs. Inputs are DC-coupled and biased internally at 1.2V.
25	RXRF+	
26	V_{CC_MXR}	Receiver Downconverter Supply Voltage. Bypass with a capacitor as close as possible to the pin.
27	V_{CC_BB2}	Receiver Baseband Supply Voltage 2. Bypass with a capacitor as close as possible to the pin.
28	TXBBI+	Transmitter Baseband I-Channel Differential Inputs
29	TXBBI-	
30	TXBBQ+	Transmitter Baseband Q-Channel Differential Inputs
31	TXBBQ-	
32	$\overline{CS}$	Chip-Select Logic Input of 4-Wire Serial Interface
33	SCLK	Serial-Clock Logic Input of 4-Wire Serial Interface
34	DIN	Data Logic Input of 4-Wire Serial Interface
39	RXBBI+	Receiver Baseband I-Channel Differential Outputs
40	RXBBI-	
41	RXBBQ+	Receiver Baseband Q-Channel Differential Outputs
42	RXBBQ-	
43	RSSI	Receiver Signal Strength Indicator Output
44	V_{CC_VCO}	VCO Supply Voltage. Bypass with a capacitor as close as possible to the pin.
45	BYP_VCO	On-Chip VCO Regulator Output Bypass. Bypass with an external 1µF capacitor to GND_VCO with minimum PCB trace. Do **not** connect other circuitry to this pin.
46	GND_VCO	VCO Ground
47	CPOUT+	Differential Charge-Pump Outputs. Connect the frequency synthesizer's loop filter between CPOUT+ and CPOUT- (see the *Typical Operating Circuit*).
48	CPOUT-	
49	V_{CC_DIG}	Digital Block Supply Voltage. Bypass with a capacitor as close as possible to the pin.
50	DOUT	Data Logic Output of 4-Wire Serial Interface
51	CLKOUT	Reference Clock Buffer Output
52	V_{CC_XTAL}	Crystal Oscillator Supply Voltage. Bypass with a capacitor as close as possible to the pin.

Pin Description (continued)

PIN	NAME	FUNCTION
53	XTAL	Crystal Oscillator Base Input. AC-couple crystal unit to this pin.
55	ENABLE	Enable Logic Input
60	V_{CC_BB1}	Receiver Baseband Supply Voltage 1. Bypass with a capacitor as close as possible to the pin.
—	EP	Exposed Paddle. Connect to the ground plane with multiple vias for proper operation and heat dissipation. Do not share with any other pin grounds and bypass capacitors' ground.

Table 1. Operating Modes

	MODE-CONTROL LOGIC INPUTS		CIRCUIT BLOCK STATES				
MODE	ENABLE PIN	SPI MAIN ADDRESS 0, D4:D2	Rx PATH	Tx PATH	LO PATH	CLKOUT*	Calibration Sections On
SHUTDOWN	0	XXX	Off	Off	Off	Off	None
CLKOUT	1	000	Off	Off	Off	On	None
STANDBY	1	001	Off	Off	On	On	None
Rx	1	010	On	Off	On	On	None
Tx CALIBRATION	1	100	Off	On	On	On	AM detector + Rx I/Q buffers
RF LOOPBACK	1	101	On (except LNA)	On	On	On	RF loopback
BASEBAND LOOPBACK	1	11X	On (except RXRF)	Off	On	On	Tx 4 baseband buffer

**CLKOUT signal is active independent of SPI, and is only dependent on the ENABLE pin.*

Detailed Description

Modes of Operation

The modes of operation for the MAX2852 are shutdown, clockout, standby, receive, transmit calibration, RF loopback, and baseband loopback. See Table 1 for a summary of the modes of operation. The logic input pin ENABLE (pin 55) and SPI Main address 0 D4:D2 control the various modes.

Shutdown Mode

The MAX2852 features a low-power shutdown mode. All circuit blocks are powered down, except the 4-wire serial bus and its internal programmable registers.

Clockout Mode

In clockout mode, only the crystal oscillator signal is active at the CLKOUT pin. The rest of the transceiver is powered down.

Standby Mode

In standby mode, PLL, VCO, and LO generation are on. Rx mode can be quickly enabled from this mode. Other blocks may be selectively enabled in this mode.

Receive (Rx) Mode

In receive mode, all Rx circuit blocks are powered on and active. Antenna signal is applied; RF is downconverted, filtered, and buffered at Rx baseband I and Q outputs.

Transmit Calibration

In transmit calibration mode, all Tx circuit blocks are powered on and active. The AM detector and receiver I/Q channel buffers are also on. Output signals are routed to Rx baseband I and Q outputs.

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The AM detector multiplies the Tx RF output signal with itself. The self-mixing product of the wanted sideband becomes DC voltage and is filtered on-chip. The mixing product between wanted sideband and the carrier leakage forms Ftone at Rx baseband output. The mixing product between the wanted sideband and the unwanted sideband forms 2Ftone at Rx baseband output.

RF Loopback

In RF loopback mode, part of the Rx and Tx circuit blocks (except the LNA) are powered on and active. The transmitter 4 I/Q input signal is upconverted to RF, and the output of the transmitter is fed to the receiver downconverter input. Output signals are delivered to receiver 4 baseband I/Q outputs. The I/Q lowpass filters in the transmitter signal path are bypassed.

Baseband Loopback

In baseband loopback mode, part of the Rx and Tx baseband circuit blocks are powered and active. The transmitter 4 IQ input signal is routed to receiver lowpass filter input. Output signals are delivered to receiver 4 baseband I/Q outputs.

Power-On Sequence

Set the ENABLE pin to V_{CC} for 2ms to start the crystal oscillator. Program all SPI addresses according to recommended values. Set SPI Main address 0 D4:D2 from 000 to 001 to engage standby mode. To lock the LO frequency, the user can set SPI in order of Main address 15, Main address 16, and then Main address 17 to trigger VCO sub-band autoacquisition; the acquisition will take 2ms. After the LO frequency is locked, set SPI Main address 0 D4:D2 = 010 and 011 for Rx and Tx operating modes, respectively. Before engaging Rx mode, set Main address 5 D1 = 1 to allow fast DC offset settling. After engaging Rx mode and Rx baseband DC offset settles, the user can set Main address 5 D1 = 0 to complete Rx DC offset cancellation.

Programmable Registers and 4-Wire SPI Interface

The MAX2852 includes 60 programmable 16-bit registers. The most significant bit (MSB) is the read/write selection bit (R/W in Figure 1). The next 5 bits are register address (A4:A0 in Figure 1). The 10 least significant bits (LSBs) are register data (D9:D0 in Figure 1). Register data is loaded through the 4-wire SPI/MICROWIRE™-compatible serial interface. MSB of data at the DIN pin is shifted in first and is framed by $\overline{CS}$. When $\overline{CS}$ is low, the clock is active, and input data is shifted at the rising edge of the clock at SCLK pin. At the $\overline{CS}$ rising edge, the 10-bit data bits are latched into the register selected by address bits. See Figure 1. To support more than a 32-register address using a 5-bit wide address word, the bit 0 of address 0 is used to select whether the 5-bit address word is applied to the main address or local address. The register values are preserved in shutdown mode as long as the power-supply voltage is maintained. There is no power-on SPI register self-reset functionality in the MAX2852, so the user must program all register values after power-up. During the read mode, register data selected by address bits is shifted out to the DOUT pin at the falling edges of the clock.

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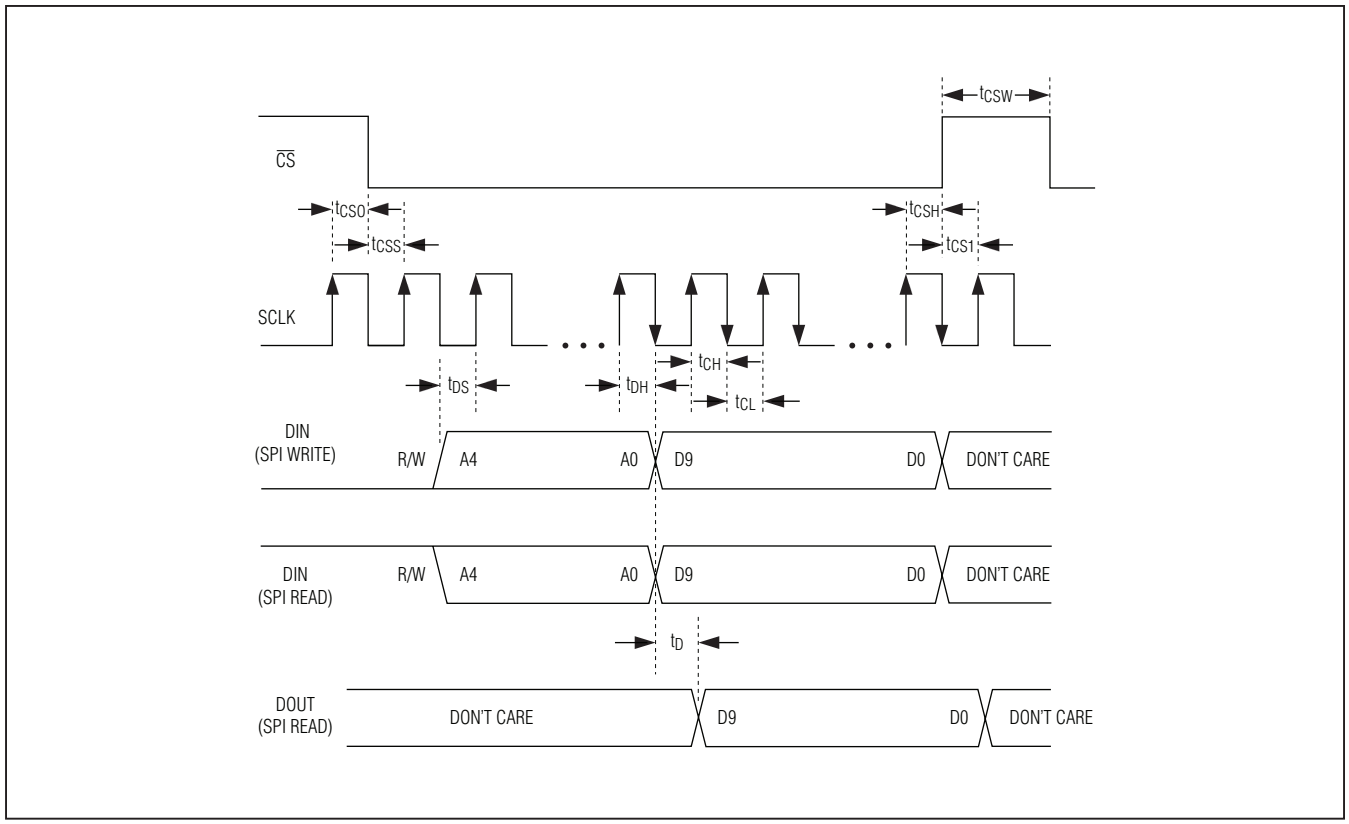

Figure 1. 4-Wire SPI Serial-Interface Timing Diagram

SPI Register Definition

(All values in the register summary table are typical numbers. The MAX2852 SPI does not have a power-on-default self-reset feature; the user must program all SPI addresses for normal operation. Prior to use of any untested settings, contact the factory.)

Table 2. Register Summary

REGISTER	READ/WRITE AND ADDRESS			DATA									
	Main0_ D0	A4:A0	WRITE (W)/ READ (R)	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Main0	0	00000	W/R	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	MODE<2:0>			RFBW	M/L_SEL
			Default	0	1	0	0	0	0	0	0	1	0
Main1	0	00001	W/R	RESERVED	RESERVED	LNA_GAIN<2:0>			RX_VGA<4:0>				
			Default	0	0	1	1	1	1	1	1	1	1
Main2	0	00010	W/R	RESERVED	RESERVED	RESERVED	LNA_BAND<1:0>		RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
			Default	0	1	1	0	1	0	0	0	0	0
Main3	0	00011	W	RESERVED	RESERVED	TS_EN	TS_TRIG	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
			R	RESERVED	RESERVED			RESERVED	TS_READ<4:0>				
			Default	0	0	0	0	0	0	0	0	0	0

Table 2. Register Summary (continued)

REGISTER	READ/WRITE AND ADDRESS			DATA									
	Main0_ D0	A4:A0	WRITE (W)/ READ (R)	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Main4	0	00100	Reserved	1	1	0	0	0	1	1	1	0	0
Main5	0	00101	W/R	RESERVED	RSSI_MUX_SEL<2:0>			RESERVED	RESERVED	RESERVED	RESERVED	RXHP	RESERVED
			Default	0	0	0	0	0	0	0	0	0	0
Main6	0	00110	Reserved	1	1	1	1	1	0	1	0	0	0
Main7	0	00111	Reserved	0	0	0	0	1	0	0	1	0	0
Main8	0	01000	W/R	0	0	0	0	0	0	0	0	0	0
Main9	0	01001	W/R	TX_GAIN<5:0>						RESERVED	RESERVED	RESERVED	RESERVED
			Default	0	0	0	0	0	0	1	1	1	1
Main10	0	01010	Reserved	0	0	0	0	0	0	0	0	0	0
Main11	0	01011	W/R	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
			Default	0	0	0	1	1	0	1	1	0	0
Main13	0	01101	Reserved	0	0	0	0	0	0	0	0	0	0
Main14	0	01110	W/R	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	DOUT_SEL	RESERVED
			Default	0	1	0	1	1	0	0	0	0	0
Main15	0	01111	W/R	VAS_ TRIG_EN	RESERVED		SYN_CONFIG_N<6:0>						
			Default	1	0	0	1	0	0	0	0	1	0
Main16	0	10000	W/R	SYN_CONFIG_F<19:10>									
			Default	1	1	1	0	0	0	0	0	0	0
Main17	0	10001	W/R	SYN_CONFIG_F<9:0>									
			Default	0	0	0	0	0	0	0	0	0	0
Main18	0	10010	W/R	RESERVED	RESERVED	XTAL_TUNE<7:0>							
			Default	0	0	1	0	0	0	0	0	0	0
Main19	0	10011	W/R	RESERVED	RESERVED	VAS_ RELOCK_ SEL	VAS_ MODE	VAS_SPI<5:0>					
			Read		VAS_ADC<2:0>			VCO_BAND<5:0>					
			Default	0	0	0	1	0	1	1	1	1	1
Main20	0	10100	Reserved	0	1	1	1	1	0	1	0	1	0
Main21	0	10101	Read	RESERVED	RESERVED	DIE_ID<2:0>			RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
			Default	0	0	1	0	1	1	1	1	1	1
Main22	0	10110	Reserved	0	1	1	0	1	1	1	0	0	0
Main23	0	10111	Reserved	0	0	0	1	1	0	0	1	0	1
Main24	0	11000	Reserved	1	0	0	1	0	0	1	1	1	1
Main25	0	11001	Reserved	1	1	1	0	1	0	1	0	0	0
Main26	0	11010	Reserved	0	0	0	0	0	1	0	1	0	1
Main27	0	11011	W/R	DIE_ID_ READ	RESERVED	RESERVED	RESERVED	VAS_VCO_ READ	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
			Default	0	1	1	0	0	0	0	0	0	0
Main28	0	11100	W/R	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
			Default	0	0	0	1	1	0	0	0	1	1

Table 2. Register Summary (continued)

REGISTER	READ/WRITE AND ADDRESS			DATA									
	Main0_ D0	A4:A0	WRITE (W)/ READ (R)	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Main29	0	11101	Reserved	0	0	0	0	0	0	0	0	0	0
Main30	0	11110	Reserved	0	0	0	0	0	0	0	0	0	0
Main31	0	11111	Reserved	0	0	0	0	0	0	0	0	0	0
Local1	1	00001	Reserved	0	0	0	0	0	0	0	0	0	0
Local2	1	00010	Reserved	0	0	0	0	0	0	0	0	0	0
Local3	1	00011	Reserved	0	0	0	0	0	0	0	0	0	0
Local4	1	00100	Reserved	1	1	1	0	0	0	0	0	0	0
Local5	1	00101	Reserved	0	0	0	0	0	0	0	0	0	0
Local6	1	00110	Reserved	0	0	0	0	0	0	0	0	0	0
Local7	1	00111	Reserved	0	0	0	0	0	0	0	0	0	0
Local8	1	01000	Reserved	0	1	1	0	1	0	1	0	1	0
Local9	1	01001	Reserved	0	1	0	0	0	1	0	1	0	0
Local10	1	01010	Reserved	1	1	0	1	0	1	0	1	0	0
Local11	1	01011	Reserved	0	0	0	1	1	1	0	0	1	1
Local12	1	01100	Reserved	0	0	0	0	0	0	0	0	0	0
Local13	1	01101	Reserved	0	0	0	0	0	0	0	0	0	0
Local14	1	01110	Reserved	0	0	0	0	0	0	0	0	0	0
Local15	1	01111	Reserved	0	0	0	0	0	0	0	0	0	0
Local16	1	10000	Reserved	0	0	0	0	0	0	0	0	0	0
Local17	1	10001	Reserved	0	0	0	0	0	0	0	0	0	0
Local18	1	10010	Reserved	0	0	0	0	0	0	0	0	0	0
Local19	1	10011	Reserved	0	0	0	0	0	0	0	0	0	0
Local20	1	10100	Reserved	0	0	0	0	0	0	0	0	0	0
Local21	1	10101	Reserved	0	0	0	0	0	0	0	0	0	0
Local22	1	10110	Reserved	0	0	0	0	0	0	0	0	0	0
Local23	1	10111	Reserved	0	0	0	0	0	0	0	0	0	0
Local24	1	11000	Reserved	0	0	1	1	0	0	0	1	0	0
Local25	1	11001	Reserved	0	1	0	0	1	0	1	0	1	1
Local26	1	11010	Reserved	0	1	0	1	1	0	0	1	0	1
Local27	1	11011	W/R	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	TX_AMD_ BB_GAIN	TX_AMD_RF_GAIN <1:0>	
			Default	0	0	0	0	0	0	0	0	0	0
Local28	1	11100	Reserved	0	0	0	0	0	0	0	1	0	0
Local31	1	11111	Reserved	0	0	0	0	0	0	0	0	0	0

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Table 3. Main Address 0: (A4:A0 = 00000)

BIT NAME	BIT LOCATION (D0 = LSB)	DESCRIPTION
RESERVED	D9:D5	Reserved bits; set to default
MODE<2:0>	D4:D2	**IC Operating Mode Select** 000 = Clockout (default) 001 = Standby 010 = Rx 011 = Do not use 100 = Tx calibration 101 = RF loopback 11x = Baseband loopback
RFBW	D1	**RF Bandwidth** 0 = 20MHz 1 = 40MHz (default)
M/L_SEL	D0	**Main or Local Address Select** 0 = Main registers (default) 1 = Local registers

Table 4. Main Address 1: (A4:A0 = 00001, Main Address 0 D0 = 0)

BIT NAME	BIT LOCATION (D0 = LSB)	DESCRIPTION
RESERVED	D9:D8	Reserved bits; set to default
LNA_GAIN<2:0>	D7:D5	**LNA Gain Control** Active when Rx channel is selected by corresponding RX_PATH_UNMASK<5:1> bits in Main address 6 D9:D5. 000 = Maximum - 40dB 001 = Maximum - 32dB 100 = Maximum - 24dB 101 = Maximum - 16dB 110 = Maximum - 8dB 111 = Maximum gain (default)
VGA_GAIN<4:0>	D4:D0	**Rx VGA Gain Control** Active when Rx channel is selected by corresponding RX_PATH_UNMASK<5:1> bits in Main address 6 D9:D5. 00000 = Minimum gain 00001 = Minimum + 2dB … 01110 = Minimum + 28dB 01111 = Minimum + 30dB … 1xxxx = Minimum + 30dB (default)

Table 5. Main Address 2: (A4:A0 = 00010, Main Address 0 D0 = 0)

BIT NAME	BIT LOCATION (D0 = LSB)	DESCRIPTION
RESERVED	D9:D7	Reserved bits; set to default
LNA_BAND<1:0>	D6:D5	**LNA Frequency Band Switch** 00 = 4.9GHz~5.2GHz 01 = 5.2GHz~5.5GHz (default) 10 = 5.5GHz~5.8GHz 11 = 5.8GHz~5.9GHz
RESERVED	D4:D0	Reserved bits; set to default

Table 6. Main Address 3: (A4:A0 = 00011, Main Address 0 D0 = 0)

BIT NAME	BIT LOCATION (D0 = LSB)	DESCRIPTION
RESERVED	D9:D8	Reserved bits; set to default
TS_EN	D7	**Temperature Sensor Enable** 0 = Disable (default) 1 = Enable except shutdown or clockout mode
TS_TRIG	D6	**Temperature Sensor Reading Trigger** 0 = Not trigger (default) 1 = Trigger temperature reading
RESERVED	D5	Reserved bits; set to default
TS_READ<4:0>	D4:D0	SPI readback only. Temperature sensor reading.

Table 7. Main Address 5: (A4:A0 = 00101, Main Address 0 D0 = 0)

BIT NAME	BIT LOCATION (D0 = LSB)	DESCRIPTION
RESERVED	D9	Reserved bits; set to default
RSSI_MUX_SEL<2:0>	D8:D6	**RSSI Output Select** 000 = Baseband RSSI (default) 001 = Do not use 010 = Do not use 011 = Do not use 100 = Rx RF detector 101 = Do not use 110 = Do not use 111 = Do not use
RESERVED	D5:D2	Reserved bits, set to default
RXHP	D1	**Rx VGA Highpass Corner Select after Rx Turn-On** RXHP starts at 1 during Rx gain adjustment, and set to 0 after gain is adjusted. 0 = 10kHz highpass corner after Rx gain is adjusted (default) 1 = 600kHz highpass corner during Rx gain adjustment
RESERVED	D0	Reserved bits; set to default

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Table 8. Main Address 9: (A4:A0 = 01001, Main Address 0 D0 = 0)

BIT NAME	BIT LOCATION (D0 = LSB)	DESCRIPTION
TX_GAIN<5:0>	D9:D4	**Tx VGA Gain Control** Tx channel is selected by Main address 9 D3:D0. 000000 = Minimum gain (default) … 111111 = Minimum gain + 31.5dB
RESERVED	D3:D0	Reserved bits; set to default

Table 9. Main Address 14: (A4:A0 = 01110, Main Address 0 D0 = 0)

BIT NAME	BIT LOCATION (D0 = LSB)	DESCRIPTION
RESERVED	D9:D2	Reserved bits; set to default
DOUT_SEL	D1	**DOUT Pin Output Select** 0 = PLL lock detect (default) 1 = SPI readback
RESERVED	D0	Reserved bits; set to default

Table 10. Main Address 15: (A4:A0 = 01111, Main Address 0 D0 = 0)

BIT NAME	BIT LOCATION (D0 = LSB)	DESCRIPTION
VAS_TRIG_EN	D9	**Enable VCO Sub-Band Acquisition Triggered by SYN_CONFIG_F<9:0> (Main Address 17) Programming** 0 = Disable for small frequency adjustment (i.e., ~100kHz) 1 = Enable for channel switching (default)
RESERVED	D8:D7	Reserved bits; set to default
SYN_CONFIG_N<6:0>	D6:D0	**Integer Divide Ratio** 1000010 = Default

Table 11. Main Address 16: (A4:A0 = 10000, Main Address 0 D0 = 0)

BIT NAME	BIT LOCATION (D0 = LSB)	DESCRIPTION
SYN_CONFIG_F<19:10>	D9:D0	**Fractional Divide Ratio LSBs** 0000000000 = Default

Table 12. Main Address 17: (A4:A0 = 10001, Main Address 0 D0 = 0)

BIT NAME	BIT LOCATION (D0 = LSB)	DESCRIPTION
SYN_CONFIG_F<19:10>	D9:D0	**Fractional Divide Ratio LSBs** 0000000000 = Default

Table 13. Main Address 18: (A4:A0 = 10010, Main Address 0 D0 = 0)

BIT NAME	BIT LOCATION (D0 = LSB)	DESCRIPTION
RESERVED	D9:D8	Reserved bits; set to default
XTAL_TUNE<7:0>	D7:D0	**Crystal Oscillator Frequency Tuning** 00000000 = Minimum frequency 10000000 = Default 11111111 = Maximum frequency

Table 14. Main Address 19: (A4:A0 = 10011, Main Address 0 D0 = 0)

BIT NAME	BIT LOCATION (D0 = LSB)	DESCRIPTION
RESERVED	D9:D8	Reserved bits; set to default
VAS_RELOCK_SEL	D7	**VAS Relock Select** 0 = Start at sub-band selected by VAS_SPI<5:0> (Main address 19 D5:D0) (default) 1 = Start at current sub-band
VAS_MODE	D6	**VCO Sub-Band Select** 0 = By VAS_SPI<5:0> (Main address 19 D5:D0) 1 = By on-chip VCO autoselect (VAS) (default)
VAS_SPI<5:0>	D5:D0	**VCO Autoselect Sub-Band Input** Select VCO sub-band when VAS_MODE (Main address 19 D6) = 0. Select initial VCO sub-band for autoacquisition when VAS_MODE = 1. 000000 = Minimum frequency sub-band … 011111 = Default … 111111 = Maximum frequency sub-band
VAS_ADC<2:0> (Readback Only)	D8:D6	**Read VCO Autoselect Tune Voltage ADC Output** Active when VCO_VAS_RB (Main address 27 D5) = 1. 000 = Lower than lock range and at risk of unlock 001 = Lower than acquisition range and maintain lock 010 or 101 = Within acquisition range and maintain lock 110 = Higher than acquisition range and maintain lock 111 = Higher than lock range and at risk of unlock
VCO_BAND<5:0> (Readback Only)	D5:D0	**Read the Current Acquired VCO Sub-Band by VCO Autoselect** Active when VCO_VAS_RB (Main address 27 D5) = 1.

Table 15. Main Address 21: (A4:A0 = 10101, Main Address 0 D0 = 0)

BIT NAME	BIT LOCATION (D0 = LSB)	DESCRIPTION
RESERVED	D9:D0	Reserved bits; set to default
DIE_ID<2:0> (Readback Only)	D7:D5	**Read Revision ID at Main Address 21 D7:D5** Active when DIE_ID_READ (Main address 27 D9) = 1. 000 = Pass1 001 = Pass2 …

Table 16. Main Address 27: (A4:A0 = 11011, Main Address 0 D0 = 0)

BIT NAME	BIT LOCATION (D0 = LSB)	DESCRIPTION
DIE_ID_READ	D9	**Die ID Readback Select** 0 = Main address 21 D9:D0 reads its own values (default) 1 = Main address 21 D7:D5 reads revision ID
RESERVED	D8:D6	Reserved bits, set to default
VAS_VCO_READ	D5	**VAS ADC and VCO Sub-Band Readback Select** 0 = Main address 19 D9:D0 reads its own values (default) 1 = Main address 19 D8:D6 reads VAS_ADC<2:0>; Main address 19 D5:D0 reads VCO_BAND<5:0>
RESERVED	D4:D0	Reserved bits; set to default

Table 17. Local Address 27: (A4:A0 = 11011, Main Address 0 D0 = 1)

BIT NAME	BIT LOCATION (D0 = LSB)	DESCRIPTION
RESERVED	D9:D3	Reserved bits, set to default
TX_AMD_BB_GAIN	D2	**Tx Calibration AM Detector Baseband Gain** 0 = Minimum gain (default) 1 = Minimum gain + 5dB
TX_AMD_RF_GAIN	D1:D0	**Tx Calibration AM Detector RF Gain** 00 = Minimum gain (default) 01 = Minimum gain + 14dB rise at output 1x = Minimum gain + 28dB rise at output

Chip Information

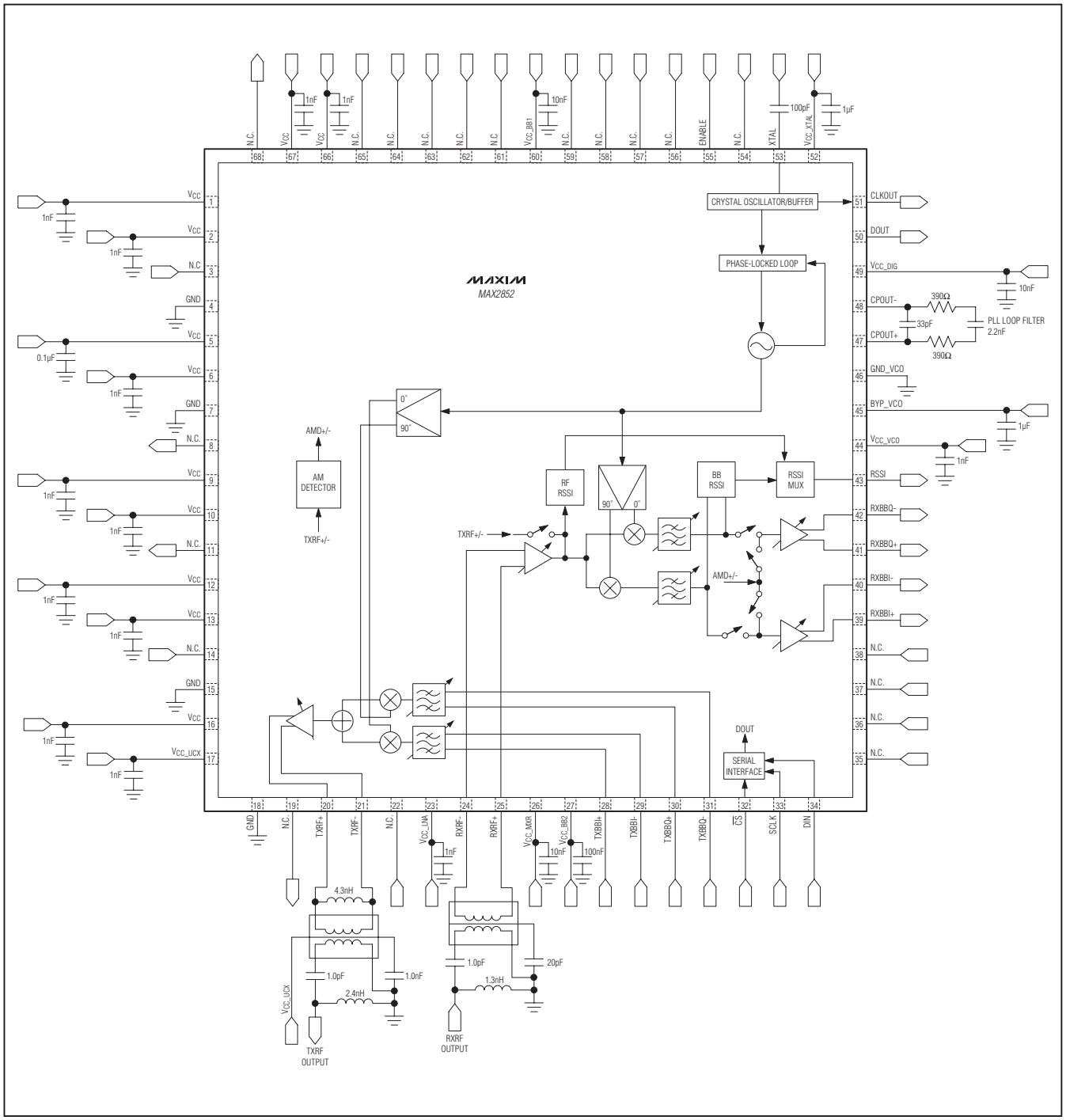
PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
68 TQFN-EP	T6800+2	21-0142

Typical Operating Circuit



Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/09	Initial release	—
1	3/10	Modified EC table to support single-pass room test flow	2, 3, 5, 8