DATASHEET

AX5042

Version 2.4

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Table of Contents

1. Overview

1.1. Features

- **Advanced multi-channel single chip UHF transceiver**
- **Configurable for usage in 400-470 (510) MHz MHz and 800-940 (1020) MHz ISM bands**
- **Wide variety of shaped modulations supported in RX and TX (ASK, PSK, OQPSK, MSK, FSK, GFSK)**
- **Data rates from 1 to 250 kbps (FSK, MSK, GFSK, GMSK, OQPSK) and 2 to 600kbps (ASK, PSK) with fully scaling narrow-band channel filtering**
-
- **4.8 kHz to 600 kHz programmable channel filter**
- **Ultra fast settling RF frequency synthesizer for low-power consumption**
- **802.15.4 compatible**
- **RS-232 (UART) compatible**
- **RF carrier frequency and FSK deviation programmable in 1 Hz steps**
- **Fully integrated frequency synthesizer with VCO auto-ranging and band-width boost modes for fast locking**
- **Few external components**
- **On-chip communication controller and flexible digital modem**
- **Channel hopping up to 2000 hops/s**
- **Sensitivity down to –123 dBm @ 1.2 kbps FSK**
- **Sensitivity down to –115 dBm @ 10 kbps FSK**
- **Up to +10 dBm (+13 dBm 433 MHz) programmable transmitter power amplifier for long range operation**
-
- **Crystal oscillator with programmable transconductance for low cost crystals (a TCXO is recommended for channel filter BW < 40 kHz)**
- **Automatic frequency control (AFC)**
- **SPI micro-controller interface**
- **Digital RSSI with 0.625 dB resolution**
- **Fully integrated current/voltage references**
- **Wire and frame mode**
- **QFN28 package**
- **Low power 17 - 23 mA at 2.5 V supply during receive and 13 - 37 mA during transmit**
- **24 bit RX/TX FIFO**
- **2.3 V to 2.8 V supply range**
- **Programmable Cyclic Redundancy Check (CRC-CCITT, CRC-16, CRC-32)**
- **Optional spectral shaping using a self synchronized shift register**
- **RoHS compliant**

1.2. Applications

400-470 MHz and 800-940 MHz data transmission and reception in the Short Range Device (SRD) band. The frequency range up to 510 MHz and 1020 MHz is with higher VDD limit accessible.

- Automatic meter reading
- FCC Part 90.210 6.25 kHz, 12.5 kHz and 25 kHz applications
- EN 300 220 V 2.1.1
- European paging applications
- Long range sensor read-out

Long range remote controls

2. Block Diagrams

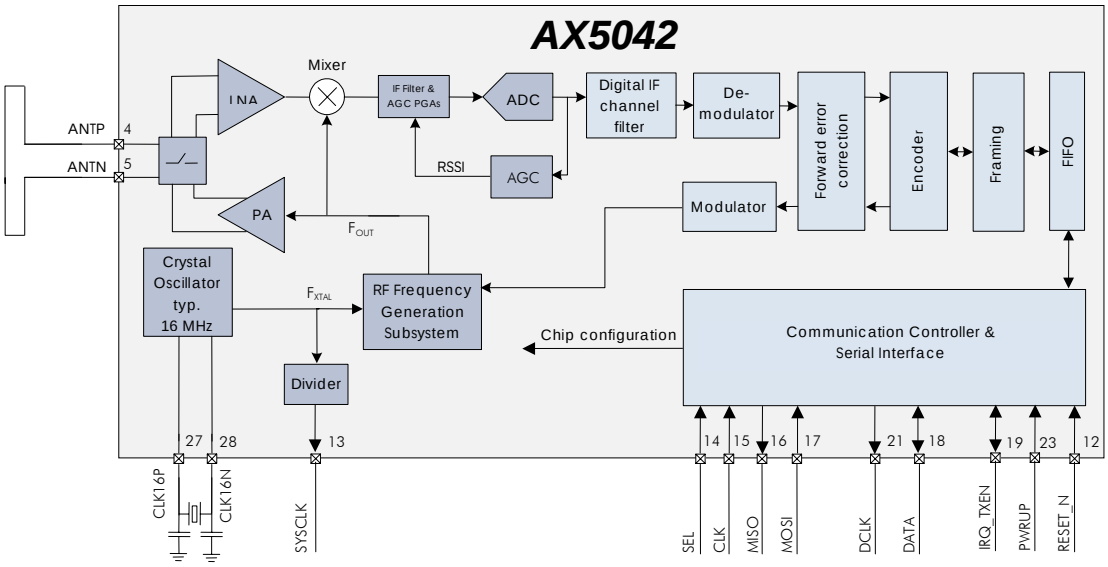


Figure 1 Functional block diagram of the AX5042

3. Pin Function Descriptions

Symbol	Pin(s)	Type	Description
NC	1	N	Not to be connected
VDD	2	P	Power supply
GND	3	G	Ground
ANTP	4	A	Antenna input/output
ANTN	5	A	Antenna input/output
GND	6	P	Ground
VDD	7	P	Power supply
NC	8	N	Not to be connected
LPFILT	9	A	Pin for optional external synthesizer loop filter; leave unconnected if not used It is recommended to use the internal loop filter
NC	10	N	Not to be connected
GND	11	P	Ground
RESET_N	12	I	Optional reset input. If not used this pin must be connected to VDD.
SYSCLK	13	I/O	Default functionality: Crystal oscillator (or divided) clock output Can be programmed to be used as a general purpose I/O pin
SEL	14	I	Serial peripheral interface select
CLK	15	I	Serial peripheral interface clock
MISO	16	O	Serial peripheral interface data output
MOSI	17	I	Serial peripheral interface data input
DATA	18	I/O	In wire mode: Data input/output Can be programmed to be used as a general purpose I/O pin
IRQ_TXEN	19	I/O	In frame mode: Interrupt request output In wire mode: Transmit enable input Can be programmed to be used as a general purpose I/O pin
VDD	20	P	Power supply
DCLK	21	I/O	In wire mode: Clock output Can be programmed to be used as a general purpose I/O pin
GND	22	P	Ground
PWRUP	23	I/O	Power-up/-down input; activates/deactivates analog blocks Can be programmed to be used as a general purpose I/O pin If the power-up/-down functionality is handled in software and no usage as general purpose I/O pin is planned then this pin should be tied to VDD
NC	24	N	Not to be connected
NC	25	N	Not to be connected
VDD	26	P	Power supply
CLK16P	27	A	Crystal oscillator input/output
CLK16N	28	A	Crystal oscillator input/output

A = analog signal
I = digital input signal
O = digital output signal
I/O = digital input/output signal
N = not to be connected
P = power or ground

All digital inputs are Schmitt trigger inputs, digital input and output levels are LVCMOS/LVTTL compatible and 3.3V/5V tolerant.

The centre pad of the QFN28 package should be connected to GND.

3.1. Pinout Drawing

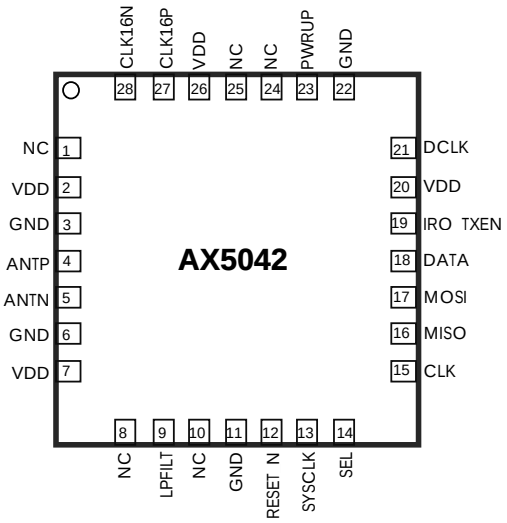


Figure 2: Pinout drawing (Top view)

4. Specifications

4.1. Absolute Maximum Ratings

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device.

This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SYMBOL	DESCRIPTION	CONDITION	MIN	MAX	UNIT
VDD	Supply voltage		-0.5	+2.8	V
IDD	Supply current			50	mA
P_{tot}	total power consumption			800	mW
P_i	Absolute maximum input power at receiver input			15	dBm
I_{I1}	DC current into any pin except ANTP, ANTN		-10	10	mA
I_{I2}	DC current into pins ANTP, ANTN		-100	100	mA
I_O	Output Current			40	mA
V_{ia}	Input voltage ANTP, ANTN pins		-0.5	VDD+2.0V	V
	Input voltage digital pins		-0.5	VDD+3V	V
V_{es}	Electrostatic handling	HBM	-2000	2000	V
T_{amb}	Operating ambient temperature		-40	85	°C
T_{stg}	Storage temperature		-65	150	°C
T_j	Junction Temperature			150	°C

4.2. DC Characteristics

Supplies

SYMBOL	DESCRIPTION	CONDITION	MIN.	TYP.	MAX.	UNIT
T_{AMB}	Operational ambient temperature		-40	27	85	°C
VDD	Power supply voltage		2.3	2.5	2.8	V
I_{PDOWN}	Power-down current			0.5		µA
I_{RX}	Current consumption RX	868 MHz; bit rate 10 kBit/s		21		mA
		868 MHz; bit rate 10 kBit/s low power mode, note 1		17		
		868 MHz; bit rate 600 kBit/s		23		
		868 MHz; bit rate 600 kBit/s low power mode, note 1		19		
		433 MHz; bit rate 10 kBit/s		21		
		433 MHz; bit rate 10 kBit/s low power mode, note 1		17		
		433 MHz; bit rate 600 kBit/s		23		
		433 MHz; bit rate 600 kBit/s low power mode, note 1		19		
I_{TX}	Current consumption TX	868 MHz, 10 dBm		36		mA
		868 MHz, 4 dBm		23		
		868 MHz, 0 dBm		19		
		868 MHz, -12 dBm		13		
		433 MHz, 12 dBm		37		
		433 MHz, 6 dBm		24		
		433 MHz, 2 dBm		20		
		433 MHz, -8 dBm		13		

Notes

1. Low power mode requires reprogramming of the device reference current (REF_I) as well as the synthesizer VCO current (VCO_I) and there are trade-offs with the lowest achievable power supply value as well as with sensitivity. Sensitivities and operating conditions in this data-sheet do not refer to low power mode.

Logic

SYMBOL	DESCRIPTION	CONDITION	MIN.	TYP.	MAX.	UNIT
DIGITAL INPUTS						
V_{T+}	Schmitt trigger low to high threshold point			1.9		V
V_{T-}	Schmitt trigger high to low threshold point			1.2		V
V_{IL}	Input voltage, low				0.8	V
V_{IH}	Input voltage, high		2.0			V
I_L	Input leakage current		-10		10	µA
DIGITAL OUTPUTS						
I_{OH}	Output Current, high	V_{OH}= 2.1V	4			mA
I_{OL}	Output Current, low	V_{OL}= 0.4V	4			mA
I_{OZ}	Tri-state output leakage current		-10		10	µA

4.3. AC Characteristics

Crystal Oscillator

SYMBOL	DESCRIPTION	CONDITION	MIN.	TYP.	MAX.	UNIT
f_{osc}	Crystal frequency	Note 1		16		MHz
gm_{osc}	Transconductance oscillator	XTALOSCGM =0000		1		mS
		XTALOSCGM =0001		2		
		XTALOSCGM =0010 default		3		
		XTALOSCGM =0011		4		
		XTALOSCGM =0100		5		
		XTALOSCGM =0101		6		
		XTALOSCGM =0110		6.5		
		XTALOSCGM =0111		7		
		XTALOSCGM =1000		7.5		
		XTALOSCGM =1001		8		
		XTALOSCGM =1010		8.5		
		XTALOSCGM =1011		9		
		XTALOSCGM =1100		9.5		
		XTALOSCGM =1101		10		
		XTALOSCGM =1110		10.5		
		XTALOSCGM =1111		11		
f_{ext}	External clock input	Note 2		16		MHz
RIN_{osc}	Input impedance		10			kΩ
CIN_{osc}	Input capacitance				4	pF

Notes

1. Tolerances and start-up times will depend on the crystal used. Depending on the RF frequency and channel spacing the IC must be calibrated to the exact crystal frequency using the readings of the register TRKFREQ
2. External clock should be input via an AC coupling at pin CLK16P with the oscillator powered up

RF Frequency Generation Subsystem (Synthesizer)

SYMBOL	DESCRIPTION	CONDITION	MIN.	TYP.	MAX.	UNIT
f_{REF}	Reference frequency			16		MHz
f_{range_hi}	Frequency range	BANDSEL=0	800		930	MHz
f_{range_low}		BANDSEL=1	400		470	MHz
f_{RESO}	Frequency resolution		1			Hz
BW_1	Synthesizer loop bandwidth Internal loop filter, pin LPFILT is unconnected	Loop filter configuration: FLT=01 Charge pump current: PLLCPI=111 default		100		kHz
BW_2		Loop filter configuration: FLT=01 Charge pump current: PLLCPI=001		50		
BW_3		Loop filter configuration: FLT=11 Charge pump current: PLLCPI=111		200		
BW_4		Loop filter configuration: FLT=10 Charge pump current: PLLCPI=111		500		
T_{set1}	Synthesizer settling time for 1MHz step as typically required for RX/TX switching Internal loop filter, pin LPFILT is unconnected	Loop filter configuration: FLT=01 Charge pump current: PLLCPI=111		15		µs
T_{set2}		Loop filter configuration: FLT=01 Charge pump current: PLLCPI=001		30		
T_{set3}		Loop filter configuration: FLT=11 Charge pump current: PLLCPI=111		7		
T_{set4}		Loop filter configuration: FLT=10 Charge pump current: PLLCPI=111		3		
T_{start1}	Synthesizer start-up time if crystal oscillator and reference are running Internal loop filter, pin LPFILT is unconnected	Loop filter configuration: FLT=01 Charge pump current: PLLCPI=111 default		25		µs
T_{start2}		Loop filter configuration: FLT=01 Charge pump current: PLLCPI=001		50		
T_{start3}		Loop filter configuration: FLT=11 Charge pump current: PLLCPI=111		12		
T_{start4}		Loop filter configuration: FLT=10 Charge pump current: PLLCPI=111		5		
$PN1_{868}$	Synthesizer phase noise Loop filter configuration: FLT=01 Charge pump current: PLLCPI=111 Internal loop filter, pin LPFILT is unconnected	868 MHz; 50 kHz from carrier		-77		dBc/Hz
		868 MHz; 100 kHz from carrier		-75		
		868 MHz; 300 kHz from carrier		-85		
		868 MHz; 2 MHz from carrier		-100		
$PN1_{433}$		433 MHz; 50 kHz from carrier		-85		
		433 MHz; 100 kHz from carrier		-80		
		433 MHz; 300 kHz from carrier		-90		
		433 MHz; 2 MHz from carrier		-105		
$PN2_{868}$	Synthesizer phase noise Loop filter configuration: FLT=01 Charge pump current: PLLCPI=001 Internal loop filter, pin LPFILT is unconnected	868 MHz; 50 kHz from carrier		-65		dBc/Hz
		868 MHz; 100 kHz from carrier		-90		
		868 MHz; 300 kHz from carrier		-105		
		868 MHz; 2 MHz from carrier		-110		
$PN2_{868}$		433 MHz; 50 kHz from carrier		-75		
		433 MHz; 100 kHz from carrier		-80		
		433 MHz; 300 kHz from carrier		-93		
		433 MHz; 2 MHz from carrier		-115		

Transmitter

SYMBOL	DESCRIPTION	CONDITION	MIN.	TYP.	MAX.	UNIT
SBR	Signal bit rate	ASK,	1		600	kbps
		PSK	10		600	
		FSK, MSK, OQPSK, GFSK, GMSK	1		200	
P_{TX868}	Transmitter power @ 868 MHz	TXRNG=0000			-50	dBm
		TXRNG=0001		-14		
		TXRNG=0010		-8		
		TXRNG=0011		-4		
		TXRNG=0100		-1		
		TXRNG=0101		0.5		
		TXRNG=0110		2		
		TXRNG=0111		3		
		TXRNG=1000		4		
		TXRNG=1001		5		
		TXRNG=1010		6		
		TXRNG=1011		7		
		TXRNG=1100		8		
		TXRNG=1101		8.5		
		TXRNG=1110		9		
		TXRNG=1111		10		
P_{TX433}	Transmitter power @ 433 MHz	TXRNG=1111		13.5		dBm
$P_{TX868\text{-}harm2}$	Emission @ 2nd harmonic	Note 1		-50		dBc
$P_{TX868\text{-}harm3}$	Emission @ 3rd harmonic			-55		

Notes

1. Additional low-pass filtering was applied to the antenna interface, see section 7: Application Information.

Receiver

	Input sensitivity TYP. on SMA connector of AX_mod_7-3 for BER=10^{-3}					
Datarate	**868 MHz**			**433 MHz**		
kbps	**ASK**	**FSK**	**PSK**	**ASK**	**FSK**	**PSK**
1.2	-118	-121	-	-119	-123	-
2	-115	-118	-	-117	-120	-
10	-111	-114	-117	-113	-116	-119
100	-101	-104	-107	-99	-106	-109
250	-97	-98	-103	-96	-100	-105
600	-93	%	-99	-99	%	-102

Notes
1. Measured on AX_mod_7-3 at SMA connector with BER measurement tool of AX-EVK software V1.3
2. For all FSK measurements was FREQGAIN = 0x06

SYMBOL	DESCRIPTION	CONDITION	MIN.	TYP.	MAX.	UNIT
SBR	Signal bit rate	ASK, PSK	1		600	kbps
		PSK	10		600	
		FSK, MSK, OQPSK, GFSK, GMSK	1		200	kbps
IL	Maximum input level				-20	dBm
CP_{1dB}	Input referred compression point	2 tones separated by 100 kHz		-35		dBm
IIP3	Input referred IP3			-25		
RSSIR	RSSI control range			85		dB
$RSSIS_1$	RSSI step size	Before digital channel filter; calculated from register AGCCOUNTER		0.625		dB
$RSSIS_2$	RSSI step size	Behind digital channel filter; calculated from registers AGCCOUNTER, TRKAMPL		0.1		dB
SEL_{868}	Adjacent channel suppression	FSK 4.8 kbps; notes 1 & 2		22		dB
	Alternate channel suppression			22		

SYMBOL	DESCRIPTION	CONDITION	MIN.	TYP.	MAX.	UNIT
	Adjacent channel suppression	FSK 12.5 kbps ; notes 1 & 3		20		dB
	Alternate channel suppression			22		
	Adjacent channel suppression	FSK 50 kbps; notes 1 & 4		18		dB
	Alternate channel suppression			19		
	Adjacent channel suppression	FSK 100 kbps ; notes 1 & 5		16		dB
	Alternate channel suppression			30		
	Adjacent channel suppression	PSK 200 kbps; notes 1 & 6		17		dB
	Alternate channel suppression			28		
BLK_{868}	Blocking at +/- 1MHz offset	FSK 4.8 kbps, notes 2 & 7		43		dB
	Blocking at - 2MHz offset			51		
	Blocking at +/- 10MHz offset			74		
	Blocking at +/- 100MHz offset			82		
$IMRR_{868}$	Image rejection			25		dB

Notes

1. Interferer/Channel @ BER = 10^{-3}, channel level is +10 dB above the typical sensitivity, the interfering signal is a random data signal (except PSK200); both channel and interferer are modulated without shaping
2. FSK 4.8 kbps: 868 MHz, 20kHz channel spacing, 2.4 kHz deviation, programming as recommended in Programming Manual
3. FSK 12.5 kbps: 868 MHz, 50kHz channel spacing, 6.25 kHz deviation, programming as recommended in Programming Manual
4. FSK 50 kbps: 868 MHz, 200 kHz channel spacing, 25 kHz deviation, programming as recommended in Programming Manual
5. FSK 100 kbps: 868 MHz, 400kHz channel spacing, 50 kHz deviation , programming as recommended in Programming Manual
6. PSK 200 kbps: 868 MHz, 400kHz channel spacing, programming as recommended in Programming Manual, interfering signal is a constant wave
7. Channel/Blocker @ BER = 10^{-3}, channel level is +10dB above the typical sensitivity, the blocker signal is a constant wave; channel signal is modulated without shaping, the image frequency lies 2 MHz above the wanted signal

SPI Timing

SYMBOL	DESCRIPTION	CONDITION	MIN.	TYP.	MAX.	UNIT
Tss	SEL falling edge to CLK rising edge		10			ns
Tsh	CLK falling edge to SEL rising edge		10			ns
Tssd	SEL falling edge to MISO driving		0		10	ns
Tssz	SEL rising edge to MISO high-Z		0		10	ns
Ts	MOSI setup time		10			ns
Th	MOSI hold time		10			ns
Tco	CLK falling edge to MISO output				10	ns
Tck	CLK period		50			ns
Tcl	CLK low duration		40			ns
Tch	CLK high duration		40			ns

For a figure showing the SPI timing parameters see section 5.16: Serial Peripheral Interface (SPI).

Wire Mode Interface Timing

SYMBOL	DESCRIPTION	CONDITION	MIN.	TYP.	MAX.	UNIT
Tdck	DCLK period	Depends on bit rate programming	1.6		10000	µs
Tdcl	DCLK low duration		25		75	%
Tdch	DCLK high duration		25		75	%
Tds	DATA setup time relative to active DCLK edge		10			ns
Tdh	DATA hold time relative to active DCLK edge		10			ns
Tdco	DATA output change relative to active DCLK edge				10	ns

For a figure showing the wire mode interface timing parameters see section 5.17: Wire Mode Interface.

5. Circuit Description

The **AX5042** is a true single chip low-power CMOS transceiver primarily for use in SRD bands. The on-chip transceiver consists of a fully integrated RF front-end with modulator and demodulator. Base band data processing is implemented in an advanced and flexible communication controller that enables user friendly communication via the SPI interface or in direct wire mode.

AX5042 can be operated from 2.3 V to 2.8 V power supply over a temperature range from -40°C to 85°C, it consumes 13 - 37 mA for transmitting depending on data mode and output power and 17 - 23 mA for receiving.

The **AX5042** features make it an ideal interface for integration into various battery powered SRD solutions such as ticketing or as transceiver for telemetric applications e.g. in sensors. As primary application, the transceiver is intended for UHF radio equipment in accordance with the European Telecommunication Standard Institute (ETSI) specification EN 300 220-1 and the US Federal Communications Commission (FCC) standard CFR47, part 15. The use of **AX5042** in accordance to FCC Par 15.247, allows for improved range in the 915 MHz band. Additionally **AX5042** is compatible with the low frequency standards of 802.15.4 (ZigBee).

The **AX5042** can be operated in two fundamentally different modes.

In **wire mode** the IC behaves as an extension of any wire. The internal communication controller is disabled and the modem data is directly available on a dedicated pin (DATA). The bit clock is also output on a dedicated pin (DCLK). In this mode the user can connect the data pin to any port of a micro-controller or to a UART, but has to control coding, checksums, pre and post ambles. The user can choose between synchronous and asynchronous wire mode, asynchronous wire mode performs RS232 start bit recognition and re-synchronization for transmit.

In **frame mode** data is sent and received via the SPI port in frames. Pre- and postambles as well as checksums can be generated automatically. Interrupts control the data flow between a micro-controller and the **AX5042**.

Both modes can be used both for transmit and receive. In both cases the **AX5042** behaves as a SPI slave interface. Configuration of the **AX5042** is always done via the SPI interface.

AX5042 supports any data rate from 1.2 kbps to 250 kbps for FSK, GFSK, GMSK , MSK and from 2 kbps to 600 kbps for ASK and PSK. To achieve optimum performance for specific data rates and modulation schemes several register settings to configure the **AX5042** are necessary, they are outlined in the following, for details see the **AX5042** Programming Manual.

Spreading and despreading is possible on all data rates and modulation schemes. The net transfer rate is reduced by a factor of 15 in this case. For 802.15.4 either 600 or 300 kbps modes have to be chosen.

The receiver supports multi-channel operation for all data rates and modulation schemes.

5.1. Crystal Oscillator

The on-chip crystal oscillator allows the use of an inexpensive quartz crystal as the RF generation subsystem's timing reference. Although a wider range of crystal frequencies can be handled by the crystal oscillator circuit, it is recommended to use 16 MHz as reference frequency since this choice allows all the typical SRD band RF frequencies to be generated.

The oscillator circuit is enabled by programming the ***PWRMODE*** register. After reset the oscillator is enabled.

To adjust the circuit's characteristics to the quartz crystal being used without using additional external components the transconductance of the crystal oscillator can be programmed.

The transconductance is programmed via register bits XTALOSCGM[3:0] in register ***XTALOSC***.

The recommended method to synchronize the receiver frequency to a carrier signal is to make use of the high resolution RF frequency generation subsystem together with the Automatic Frequency Control, both are described further down.

Alternatively a single ended reference (TXCO, CXO) may be used. The CMOS levels should be applied to pin CLK16P via an AC coupling with the crystal oscillator enabled.

5.2. SYSCLK Output

The SYSCLK pin outputs the reference clock signal divided by a programmable integer. Divisions from 1 to 2048 are possible. For divider ratios > 1 the duty cycle is 50%. Bits SYSCLK[3:0] in the ***PINCFG1*** register set the divider ratio. The output on pin SYSCLK can be disabled.

Outputting a frequency that is identical to the IF frequency (default 1 MHz) on the SYSCLK pin is not recommended during receive operation, since it requires extensive decoupling on the PCB to avoid interference.

5.3. PWRUP Input

The PWRUP pin disables all analog blocks when it is pulled low. If the pin is pulled high, then the power-up state of the analog blocks can be handled fully in software by programming register ***PWRMODE***. It is recommended to connect PWRUP to VDD.

5.4. RESET_N Input

The **AX5042** can be reset in two ways:

1. By SPI accesses: the bit RST in the ***PWRMODE*** register is toggled.
2. Via the RESET_N pin: A low pulse is applied at the RESET_N pin. With the rising edge of RESET_N the device goes into its operational state.

A reset must be applied after power-up. It is safe to perform this power-on reset using a SPI access, so using the RESET_N pin is strictly optional. If the RESET_N pin is not used it must be tied to VDD.

5.5. DATA Input/Output and DCLK Output

The DATA input/output pin is used for data transfer from and to **AX5042** in wire mode.

The transfer direction of data is set by programming the ***PWRMODE*** register or by the level applied to the pin IRQ_TXEN (1=TX, then DATA is an input pin; 0=RX, then DATA is an output pin).

The DCLK output pin supplies the corresponding data clock which depends on the data-rate settings programmed to **AX5042**. In synchronous wire mode a connected micro-controller must receive or supply data on the DATA pin synchronous to the clock available the DCLK pin. In asynchronous wire mode, the receive/transmit clock is still available on the DCLK pin, but its usage is optional.

If frame mode is used for data communication, the pins DCLK and DATA can optionally be used as general purpose I/O pins.

5.6. RF Frequency Generation Subsystem

The RF frequency generation subsystem consists of a fully integrated synthesizer, which multiplies the reference frequency from the crystal oscillator to get the desired RF frequency. The advanced architecture of the synthesizer enables frequency resolutions of 1 Hz, as well as fast settling times of 5 – 50 µs depending on the settings (see section 4.3: AC Characteristics). Fast settling times mean fast start-up and fast RX/TX switching, which enables low-power system design.

For receive operation the RF frequency is fed to the mixer, for transmit operation to the power-amplifier.

The frequency must be programmed to the desired carrier frequency. The RF frequency shift by the IF frequency that is required for RX operation, is automatically set when the receiver is activated and does not need to be programmed by the user. The default IF frequency is 1 MHz. It can be programmed to other values. Changing the IF frequency and thus the centre frequency of the digital channel filter can be used to adapt the blocking performance of the device to specific system requirements.

The synthesizer loop bandwidth can be programmed, this serves three purposes:

1. Start-up time optimisation, start-up is faster for higher synthesizer loop bandwidths
2. TX spectrum optimisation, phase-noise at 300 kHz to 1 MHz distance from the carrier improves with lower synthesizer loop bandwidths
3. Adaptation of the bandwidth to the data-rate. For transmission of FSK, GFSK and MSK it is required that the synthesizer bandwidth must be in the order of the data-rate.

VCO

An on-chip VCO converts the control voltage generated by the charge pump and loop filter into an output frequency. This frequency is used for transmit as well as for receive operation. The frequency can be programmed in 1 Hz steps in the ***FREQ*** registers. For operation in the 433 MHz band, the BANDSEL bit in the ***PLLLOOP*** register must be programmed.

VCO Auto-Ranging

The **AX5042** has an integrated auto-ranging function, which allows to set the correct VCO range for specific frequency generation subsystem settings automatically. Typically it has to be executed after power-up. The function is initiated by setting the RNG_START bit in the ***PLLRANGING*** register. The bit is readable and a 0 indicates the end of the ranging process. If the bit RNGERR is 0, then the auto-ranging has been executed successfully.

Loop Filter and Charge Pump

The **AX5042** internal loop filter configuration together with the charge pump current sets the synthesizer loop band width. The loop filter has three configurations that can be programmed via the register bits FLT[1:0] in register ***PLLLOOP***, the charge pump current can be programmed using register bits PLLCPI[2:0] also in register ***PLLLOOP***. Synthesizer bandwidths are typically 50 - 500 kHz depending on the ***PLLLOOP*** settings, for details see section 4.3: AC Characteristics.

Registers

Register	Bits	Purpose
PLLLOOP	FLT[1:0]	Synthesizer loop filter bandwidth, recommended usage is to increase the bandwidth for faster settling time, bandwidth increases of factor 2 and 5 are possible.
	PLLCPI[2:0]	Synthesizer charge pump current, recommended usage is to decrease the bandwidth (and improve the phase-noise) for low data-rate transmissions.
	BANDSEL	Switches between 868 MHz/915 MHz and 433 MHz bands
FREQ		Programming of the carrier frequency
IFFREQHI, IFFREQLO		Programming of the IF frequency
PLLRANGING		Initiate VCO auto-ranging and check results

5.7. RF Input and Output Stage (ANTP/ANTN)

The **AX5042** uses fully differential antenna pins. RX/TX switching is handled internally, an external RX/TX switch is not required.

LNA

The LNA amplifies the differential RF signal from the antenna and buffers it to drive the I/Q mixer. An external matching network is used to adapt the antenna impedance to the IC impedance. A DC feed to the supply voltage VDD must be provided at the antenna pins. For recommendations see section 7: Application Information.

I/Q mixer

The RF signal from the LNA is mixed down to an IF of typically 1 MHz. I- and Q-IF signals are buffered for the analog IF filter.

PA

In TX mode the PA drives the signal generated by the frequency generation subsystem out to the differential antenna terminals. The output power of the PA is programmed via bits TXRNG[3:0] in the register ***TXPWR***. Output power as well as harmonic content will depend on the external impedance seen by the PA, recommendations are given in the section 7: Application Information.

5.8. Analog IF Filter

The mixer is followed by a complex band-pass IF filter, which suppresses the down-mixed image while the wanted signal is amplified. The centre frequency of the filter is 1 MHz, with a passband width of 1 MHz. The RF frequency generation subsystem must be programmed in such a way that for all possible modulation schemes the IF frequency spectrum fits into the passband of the analog filter.

5.9. Digital IF Channel Filter and Demodulator

The digital IF channel filter and the demodulator extract the data bit-stream from the incoming IF signal. They must be programmed to match the modulation scheme as well as the bit rate. Inaccurate programming will lead to loss of sensitivity.

The channel filter offers bandwidths of 4.8 kHz up to 600 kHz. Data-rates down to 1.2 kbit/s can be demodulated, but sensitivities will not increase significantly vs. 4.8 kbit/s.

For detailed instructions how to program the digital channel filter and the demodulator see the **AX5042** Programming Manual, an overview of the registers involved is given in the following table. The register setups typically must be done once at power-up of the device.

Registers

Register	Remarks
CICDECHI, CICDECLO	This register programs the bandwidth of the digital channel filter.
DATARATEHI, DATARATELO	These registers specify the receiver bit rate, relative to the channel filter bandwidth.
TMGGAINHI, TMGGAINLO	These registers specify the aggressiveness of the receiver bit timing recovery. More aggressive settings allow the receiver to synchronize with shorter preambles, at the expense of more timing jitter and thus a higher bit error rate at a given signal-to-noise ratio.
MODULATION	This register selects the modulation to be used by the transmitter and the receiver, i.e. whether ASK, PSK , FSK, MSK, GFSK, GMSK or OQPSK should be used.
PHASEGAIN, FREQGAIN, FREQGAIN2, AMPLGAIN	These registers control the bandwidth of the phase, frequency offset and amplitude tracking loops. Recommended settings are provided in the Programming Manual.
AGCATTACK, AGCDECAY	These registers control the AGC (automatic gain control) loop slopes, and thus the speed of gain adjustments. The faster the bit rate, the faster the AGC loop should be. Recommended settings are provided in the Programming Manual.
TXRATE	These registers control the bit rate of the transmitter.
FSKDEV	These registers control the frequency deviation of the transmitter in FSK mode. The receiver does not explicitly need to know the frequency deviation, only the channel filter bandwidth has to be set wide enough for the complete modulation to pass.

5.10. Encoder

The encoder is located between the Framing Unit, the Demodulator and the Modulator. It can optionally transform the bit-stream in the following ways:

- It can invert the bit stream.
- It can perform differential encoding. This means that a zero is transmitted as no change in the level, and a one is transmitted as a change in the level. Differential encoding is useful for PSK, because PSK transmissions can be received either as transmitted or inverted, due to the uncertainty of the initial phase. Differential encoding / decoding removes this uncertainty.
- It can perform Manchester encoding. Manchester encoding ensures that the modulation has no DC content and enough transitions (changes from 0 to 1 and from 1 to 0) for the demodulator bit timing recovery to function correctly, but does so at a doubling of the data rate.
- It can perform Spectral Shaping. Spectral Shaping removes DC content of the bit stream, ensures transitions for the demodulator bit timing recovery, and makes sure that the transmitted spectrum does not have discrete lines even if the transmitted data is cyclic. It does so without adding additional bits, i.e. without changing the data rate. Spectral Shaping uses a self synchronizing feedback shift register.

The encoder is programmed using the register ***ENCODING***, details and recommendations on usage are given in the **AX5042** Programming Manual.

5.11. Framing and FIFO

Most radio systems today group data into packets. The framing unit is responsible for converting these packets into a bit-stream suitable for the modulator, and to extract packets from the continuous bit-stream arriving from the demodulator.

The Framing unit supports three different modes:

- HDLC
- Raw
- 802.15.4 compliant

The micro-controller communicates with the framing unit through a 3 level × 10 bit FIFO. The FIFO decouples micro-controller timing from the radio (modulator and demodulator) timing. The bottom 8 bit of the FIFO contain transmit or receive data. The top 2 bit are used to convey meta information in HDLC and 802.15.4 modes. They are unused in Raw mode. The meta information consists of packet begin / end information and the result of CRC checks.

The **AX5042** contains one FIFO. Its direction is switched depending on whether transmit or receive mode is selected.

The FIFO can be operated in polled or interrupt driven modes. In polled mode, the micro-controller must periodically read the FIFO status register or the FIFO count register to determine whether the FIFO needs servicing.

In interrupt mode EMPTY, NOT EMPTY, FULL, NOT FULL and programmable level interrupts are provided. The **AX5042** signals interrupts by asserting (driving high) its IRQ_TXEN line. The interrupt line is level triggered, active high. The IRQ line polarity can be inverted by programming register ***PINCFG2***. Interrupts are acknowledged by removing the cause for the interrupt, i.e. by emptying or filling the FIFO.

Basic FIFO status (EMPTY, FULL, Overrun, Underrun, and the top two bits of the top FIFO word) are also provided during each SPI access on MISO while the micro-controller shifts out the register address on MOSI. See the SPI interface section for details. This feature significantly reduces the number of SPI accesses necessary during transmit and receive.

HDLC Mode

Note: HDLC mode follows High-Level Data Link Control (HDLC, ISO 13239) protocol.

HDLC Mode is the main framing mode of the **AX5042**. In this mode, the **AX5042** performs automatic packet delimiting, and optional packet correctness check by inserting and checking a cyclic redundancy check (CRC) field.

The packet structure is given in the following table.

Flag	Address	Control	Information	FCS	(Optional flag)
8 bit	8 bit	8 or 16 bit	Variable length, 0 or more bit in multiples of 8	16 / 32 bit	8 bit

HDLC packets are delimited with flag sequences of content 0x7E.

In **AX5042** the meaning of address and control is user defined. The Frame Check Sequence (FCS) can be programmed to be CRC-CCITT, CRC-16 or CRC-32.

The receiver checks the CRC, the result can be retrieved from the FIFO, the CRC is appended to the received data.

For details on implementing a HDLC communication see the **AX5042** Programming Manual.

RAW Mode

In Raw mode, the **AX5042** does not perform any packet delimiting or byte synchronization. It simply serialises transmit bytes and de-serializes the received bit-stream and groups it into bytes.

This mode is ideal for implementing legacy protocols in software.

802.15.4 (ZigBee)

802.15.4 uses binary phase shift keying (PSK) with 300 kbit/s (868 MHz band) or 600 kbit/s (915 MHz band) on the radio. The usable bit rate is only a 15th of the radio bit rate, however. A spreading function in the transmitter expands the user bit rate by a factor of 15, to make the transmission more robust. The despreader function of the receiver undoes that.

In 802.15.4 mode, the **AX5042** framing unit performs the spreading and despreading function according to the 802.15.4 specification. In receive mode, the framing unit will also automatically search for the 802.15.4 preamble, meaning that no interrupts will have to be serviced by the micro-controller until a packet start is detected.

5.12. RX AGC and RSSI

AX5042 features two receiver signal strength indicators (RSSI):

1. RSSI before the digital IF channel filter.
   The gain of the receiver is adjusted in order to keep the analog IF filter output level inside the working range of the ADC and demodulator. The register ***AGCCOUNTER*** contains the current value of the AGC and can be used as an RSSI. The step size of this RSSI is 0.625 dB. The value can be used as soon as the RF frequency generation sub-system has been programmed.

2. RSSI behind the digital IF channel filter.
   The demodulator also provides amplitude information in the ***TRKAMPL*** register. By combining both the ***AGCCOUNTER*** and the ***TRKAMPL*** registers, a high resolution (better than 0.1 dB) RSSI value can be computed at the expense of a few arithmetic operations on the micro-controller. Formulas for this computation can be found in the **AX5042** Programming Manual.

5.13. Modulator

Depending on the transmitter settings the modulator generates various inputs for the PA:

Modulation	Bit = 0	Bit = 1	Main lobe bandwidth	Max. bit rate
ASK	PA off	PA on	BW=BITRATE	600kBit/s
FSK/MSK/GFSK	$\Delta f=-f_{deviation}$	$\Delta f=+f_{deviation}$	BW=(1+h) ·BITRATE	250kBit/s
PSK	$\Delta\Phi=0^0$	$\Delta\Phi=180^0$	BW=BITRATE	600kBit/s

h = modulation index. It is the ratio of the deviation compared to the bit rate; $f_{deviation}$ = 0.5·h·BITRATE, **AX5042** can demodulate signals with h < 4.

ASK = amplitude shift keying

FSK = frequency shift keying

MSK = minimum shift keying; MSK is a special case of FSK, where h = 0.5, and therefore $f_{deviation}$ = 0.25·BITRATE; the advantage of MSK over FSK is that it can be demodulated more robustly.

GFSK = gaussian frequency shift keying, same as FSK but shaped, BT=0.3

GMSK = GFSK with h=0.5

PSK = phase shift keying

OQPSK = offset quadrature shift keying. The **AX5042** supports OQPSK. However, unless compatibility to an existing system is required, MSK should be preferred.

All modulation schemes are binary.

5.14. Automatic Frequency Control (AFC)

The **AX5042** has a frequency tracking register ***TRKFREQ*** to synchronize the receiver frequency to a carrier signal. For AFC adjustment, the frequency offset can be computed with the following formula:

$$\Delta f = \frac{TRKFREQ}{2^{16}} \bullet BITRATE.$$

5.15. PWRMODE Register

The operation sequences of the chip can be controlled using the ***PWRMODE*** and ***APEOVER*** registers.

PWRMODE register	***APEOVER*** register	Name	Description	Typical Idd
0x00	0x80	POWERDOWN	All digital and analog functions, except the register file, are disabled. SPI registers are still accessible.	0.5 µA
0x60	0x00	STANDBY	The crystal oscillator is powered on; receiver and transmitter are off.	650 µA
0x00				
0x61	0x00	PWRUPPIN	The mode is determined by the state of the PWRUP and IRQ_TXEN pins. PWRUP = 0: Same function as POWERDOWN PWRUP = 1, IRQ_TXEN = 0: Same function as FULLRX PWRUP = 1, IRQ_TXEN = 1: Same function as FULLTX	0.5 µA 17 - 21 mA 13 - 37 mA
0x01				
0x68	0x00	SYNTHRX	The synthesizer is running on the receive frequency. Transmitter and receiver are still off. This mode is used to let the synthesizer settle on the correct frequency for receive.	12 mA
0x69	0x00	FULLRX	Synthesizer and receiver are running	17 - 21 mA
0x6C	0x00	SYNTHTX	The synthesizer is running on the transmit frequency. Transmitter and receiver are still off. This mode is used to let the synthesizer settle on the correct frequency for transmit.	11 mA
0x6D	0x00	FULLTX	Synthesizer and transmitter are running. Do not switch into this mode before the synthesizer has completely settled on the transmit frequency (in SYNTHTX mode), otherwise spurious spectral transmissions will occur.	13 - 37 mA

A typical ***PWRMODE*** and ***APEOVER*** sequence for a transmit session :

Step	***PWRMODE APEOVER***	Remarks
1	POWERDOWN	
2	STANDBY	The settling time is dominated by the crystal used, typical value 3ms.
3	SYNTHTX	The synthesizer settling time is 5 – 50 µs depending on settings, see section AC Characteristics
4	FULLTX	Data transmission
5	POWERDOWN	

A typical ***PWRMODE*** and ***APEOVER*** sequence for a receive session :

Step	***PWRMODE APEOVER***	Remarks
1	POWERDOWN	
2	STANDBY	The settling time is dominated by the crystal used, typical value 3ms
3	SYNTHRX	The synthesizer settling time is 5 – 50 µs depending on settings, see section AC Characteristics
4	FULLRX	Data reception
5	POWERDOWN	

5.16. Serial Peripheral Interface (SPI)

The **AX5042** can be programmed via a four wire serial interface according SPI using the pins CLK, MOSI, MISO and SEL. Registers for setting up the **AX5042** are programmed via the serial peripheral interface in all device modes.

When the interface signal SEL is pulled low, a 16 bit configuration data stream is expected on the input signal pin MOSI, which is interpreted as D0...D7, A0...A6, R_N/W.

Data read from the interface appears on MISO.

Figure 3 shows a write/read access to the interface. The data stream is built of an address byte including read/write information and a data byte. Depending on the R_N/W bit and address bits A[6..0] the data D[7..0] can be written via MOSI or read at the pin MISO.

R_N/W = 0 means read mode, R_N/W = 1 means write mode.

The read sequence starts with 7 bits of status information S[6..0] followed by 8 data bits.

The status bits contain the following information:

S6	**S5**	**S4**	**S3**	**S2**	**S1**	**S0**
PLL LOCK	FIFO OVER	FIFO UNDER	FIFO FULL	FIFO EMPTY	FIFOSTAT(1)	FIFOSTAT(0)

SPI Timing

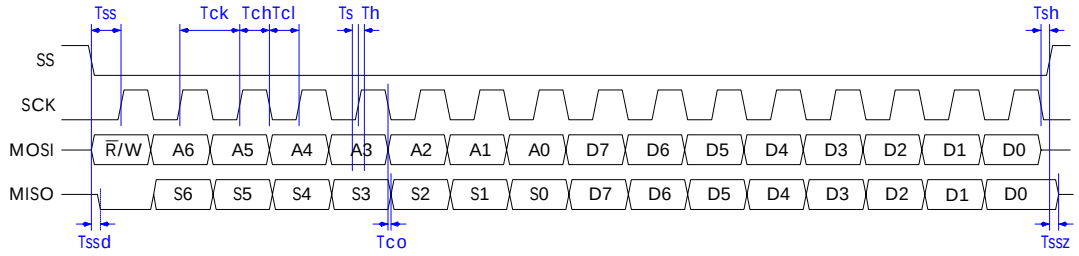


Figure 3 Serial peripheral interface timing

5.17. Wire Mode Interface

In wire mode the transmitted or received data are transferred from and to the **AX5042** using the pins DATA and DCLK. DATA is an input when transmitting and an output when receiving.

The direction can be chosen by programming the ***PWRMODE*** register (recommended), or by using the IRQ_TXEN pin.

Wire mode offers two variants: synchronous or asynchronous.

In synchronous wire mode the, the **AX5042** always drives DCLK. Transmit data must be applied to DATA synchronously to DCLK, and receive data must be sampled synchronously to DCLK. Timing is given in Figure 4. Setting the bit DCLKI in register ***PINCFG2*** inverts the DCLK signal.

In asynchronous wire mode, a low voltage RS232 type UART can be connected to DATA. DCLK is optional in this mode. The UART must be programmed to send two stop bits, but must be able to accept only one stop bit. Both the UART data rate and the **AX5042** transmit and receive bit rate must match. The **AX5042** synchronizes the RS232 signal to its internal transmission clock, by inserting or deleting a stop bit.

Registers for setting up the **AX5042** are programmed via the serial peripheral interface (SPI).

Wire Mode Timing

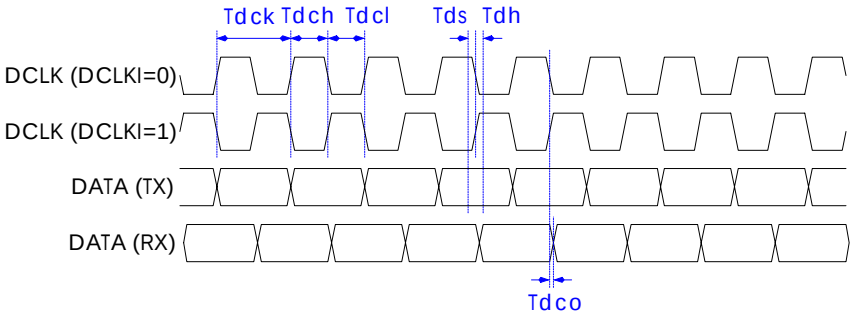


Figure 4 Wire mode interface timing

6. Register Bank Description

This section describes the bits of the register bank in detail. The registers are grouped by functional block to facilitate programming.

No checks are made whether the programmed combination of bits makes sense! Bit 0 is always the LSB.

Note Whole registers or register bits marked as reserved should be kept at their default values.

Note All addresses not documented here must not be accessed, neither in reading nor in writing.

6.1. Control Register Map

Addr	Name	Dir	Reset	Bit								Description
				7	6	5	4	3	2	1	0	
Revision & Interface Probing												
0	***REVISION***	R	00000010	SILICONREV(7:0)								Silicon Revision
1	***SCRATCH***	RW	11000101	SCRATCH(7:0)								Scratch Register
Operating Mode												
2	***PWRMODE***	RW	011-0000	RST	REFEN	XOEN	-	PWRMODE(3:0)				Power Mode
3	***XTALOSC***	RW	----0010	-	-	-	-	XTALOSCGM(3:0)				GM of Crystal Oscillator
FIFO												
4	***FIFOCTRL***	RW	------11	FIFOSTAT(1:0)		FIFO OVER	FIFO UNDER	FIFO FULL	FIFO EMPTY	FIFOCMD(1:0)		FIFO Control
5	***FIFODATA***	RW	--------	FIFODATA(7:0)								FIFO Data
Interrupt Control												
6	***IRQMASK***	RW	----0000	-	-	-	-	IRQMASK(3:0)				IRQ Mask
7	***IRQREQUEST***	R	--------	-	-	-	-	IRQREQUEST(3:0)				IRQ Request
Interface & Pin Control												
8	***IFMODE***	RW	----0011	-	-	-	-	IFMODE(3:0)				Interface Mode
0C	***PINCFG1***	RW	11111000	DATAZ	DCLKZ	IRQ_TXENZ	PWRUPZ	SYSCLK(3:0)				Pin Configuration 1
0D	***PINCFG2***	RW	00000000	DATAE	DCLKE	PWRUP_IRQ_TXENE		DATAI	DCLKI	IRQPTTI	PWRUPI	Pin Configuration 2
0E	***PINCFG3***	R	--------	-	-	-	SYSCLKR	DATAR	DCLKR	IRQPTTR	PWRUPR	Pin Configuration 3
0F	***IRQINVERSION***	RW	----0000	-	-	-	-	IRQINVERSION(3:0)				IRQ Inversion
Modulation & Framing												
10	***MODULATION***	RW	----0010	-	-	-	-	MODULATION(3:0)				Modulation
11	***ENCODING***	RW	----0010	-	-	-	-	ENC MANCH	ENC SCRAM	ENC DIFF	ENC INV	Encoder/Decoder Settings
12	***FRAMING***	RW	-0000000	-	HSUPP	CRCMODE(1:0)		FRMMODE(2:0)			FABORT	Framing settings
14	***CRCINIT3***	RW	11111111	CRCINIT(31:24)								CRC Initialisation Data
15	***CRCINIT2***	RW	11111111	CRCINIT(23:16)								CRC Initialisation Data
16	***CRCINIT1***	RW	11111111	CRCINIT(15:8)								CRC Initialisation Data
17	***CRCINIT0***	RW	11111111	CRCINIT(7:0)								CRC Initialisation Data

Synthesizer												
20	***FREQ3***	RW	00111001	FREQ(31:24)								Synthesizer Frequency
21	***FREQ2***	RW	00110100	FREQ(23:16)								Synthesizer Frequency
22	***FREQ1***	RW	11001100	FREQ(15:8)								Synthesizer Frequency
23	***FREQ0***	RW	11001101	FREQ(7:0)								Synthesizer Frequency
25	***FSKDEV2***	RW	00000010	FSKDEV(23:16)								FSK Frequency Deviation
26	***FSKDEV1***	RW	01100110	FSKDEV(15:8)								FSK Frequency Deviation
27	***FSKDEV0***	RW	01100110	FSKDEV(7:0)								FSK Frequency Deviation
28	***IFFREQHI***	RW	00100000	IFFREQ(15:8)								2nd LO / IF Frequency
29	***IFFREQLO***	RW	00000000	IFFREQ(7:0)								2nd LO / IF Frequency
2C	***PLLLOOP***	RW	-0011101	-	Reserved	BANDSEL	PLLCPI(2:0)			FLT(1:0)		Synthesizer Loop Filter Settings
2D	***PLLRANGING***	RW	---01000	STICKY LOCK	PLL LOCK	RNGERR	RNG START	VCOR(3:0)				Synthesizer VCO Auto-Ranging
Transmitter												
30	***TXPWR***	RW	----1000	–	–	–	–	TXRNG(3:0)				Transmit Power
31	***TXRATEHI***	RW	00001001	TXRATE(23:16)								Transmitter Bit Rate
32	***TXRATEMID***	RW	10011001	TXRATE(15:8)								Transmitter Bit Rate
33	***TXRATELO***	RW	10011010	TXRATE(7:0)								Transmitter Bit Rate
34	***MODMISC***	RW	------11	–	–	–	–	–	–	reserved	PTTCLK GATE	Misc RF Flags
Receiver												
39	***AGCTARGET***	RW	---01010	–	–	–	AGCTARGET(4:0)					AGC Target **Must be set to 0x0E**
3A	***AGCATTACK***	RW	00010110	reserved			AGCATTACK(4:0)					AGC Attack
3B	***AGCDECAY***	RW	0-010011	reserved	–	reserved	AGCDECAY(4:0)					AGC Decay
3C	***AGCCOUNTER***	R	--------	AGCCOUNTER(7:0)								AGC Current Value
3D	***CICSHIFT***	R	--000100	–	–	reserved	CICSHIFT(4:0)					CIC Shifter
3E	***CICDECHI***	RW	------00	–	–	–	–	–	–	CICDEC(9:8)		CIC Decimation Factor
3F	***CICDECLO***	RW	00000100	CICDEC(7:0)								CIC Decimation Factor
40	***DATARATEHI***	RW	00011010	DATARATE(15:8)								Data rate
41	***DATARATELO***	RW	10101011	DATARATE(7:0)								Data rate

42	***TMGGAINHI***	RW	00000000	TIMINGGAIN(15:8)								Timing Gain
43	***TMGGAINLO***	RW	11010101	TIMINGGAIN(7:0)								Timing Gain
44	***PHASEGAIN***	RW	00--0011	reserved			–	–	PHASEGAIN(3:0)			Phase Gain
45	***FREQGAIN***	RW	----1010	–	–	–	–	FREQGAIN(3:0)				Frequency Gain
46	***FREQGAIN2***	RW	----1010	–	–	–	–	FREQGAIN2(3:0)				Frequency Gain 2
47	***AMPLGAIN***	RW	---00110	–	–	–	reserved	AMPLGAIN(3:0)				Amplitude Gain
48	***TRKAMPLHI***	R	--------	TRKAMPL(15:8)								Amplitude Tracking
49	***TRKAMPLLO***	R	--------	TRKAMPL(7:0)								Amplitude Tracking
4A	***TRKPHASEHI***	R	--------	–	–	–	–	TRKPHASE(11:8)				Phase Tracking
4B	***TRKPHASELO***	R	--------	TRKPHASE(7:0)								Phase Tracking
4C	***TRKFREQHI***	R	--------	TRKFREQ(15:8)								Frequency Tracking
4D	***TRKFREQLO***	R	--------	TRKFREQ(7:0)								Frequency Tracking
Misc												
70	***APEOVER***	R	00000000	APEOVER	OSCAPE	REFAPE	reserved					APE Overrride
72	***PLLVCOI***	RW	--000100	-	-	reserved			VCO_I(2:0)			Synthesizer VCO current Leave at default
74	***PLLRNG***	RW	00---000	reserved			-	-	-	reserved	PLLARNG	Auto-ranging internal settings **PLLARNG must be set to 1**
7C	***REF***	RW	--100011	-	-	reserved			REF_I(2:0)			Reference adjust Leave at default
7D	***RXMISC***	RW	--110110	-	-	reserved				RXIMIX(1:0)		Misc RF settings **RXIMIX(1:0) must be set to 01**

7. Application Information

7.1. Typical Application Diagram

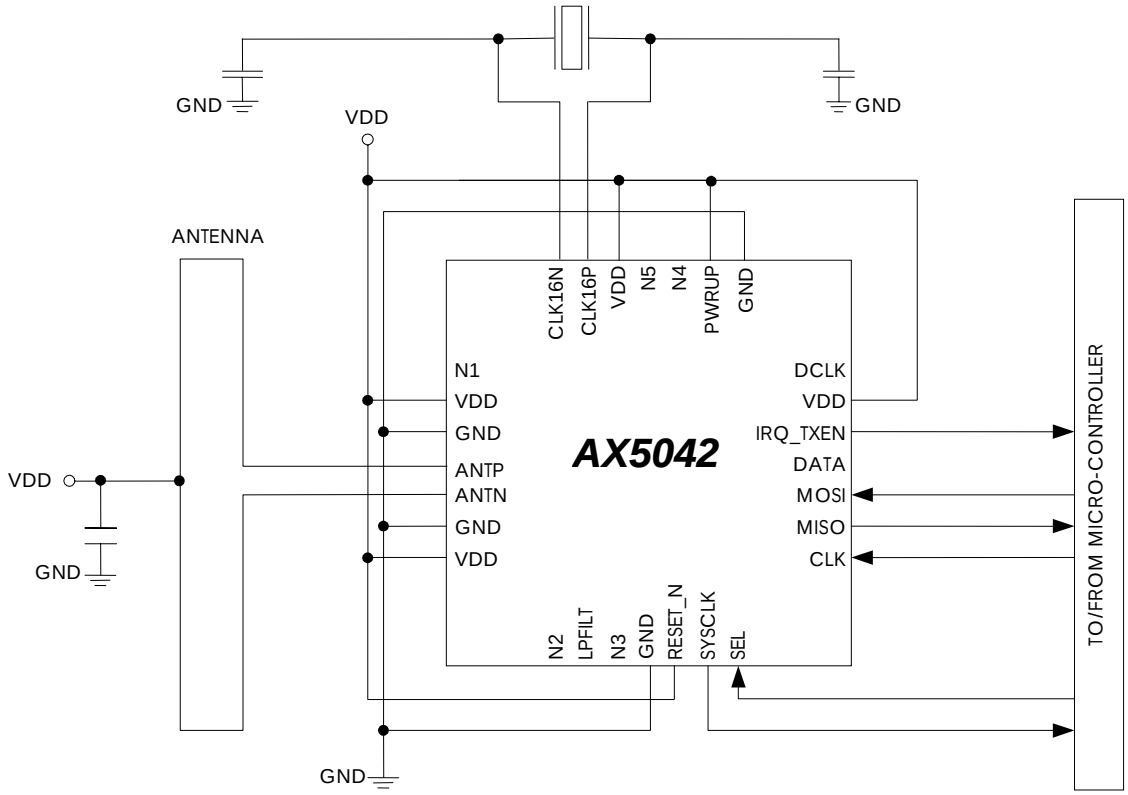


Figure 5 Typical application diagram

Decoupling capacitors are not drawn. It is recommended to add 100nF decoupling capacitor for every VDD pin. In order to reduce noise on the antenna inputs it is recommended to add 27pF on the VDD pins close to the antenna interface.

7.2. Antenna Interface Circuitry

Single-Ended Antenna Interface

The ANTP and ANTN pins provide RF input to the LNA when **AX5042** is in receive mode, and RF output from the PA when **AX5042** is in transmit mode. A small antenna can be connected with an optional matching network. The network must provide DC power to the PA and LNA. A biasing to VDD is necessary.

Beside biasing and impedance matching, the proposed networks also provide low pass filtering to limit spurious emission.

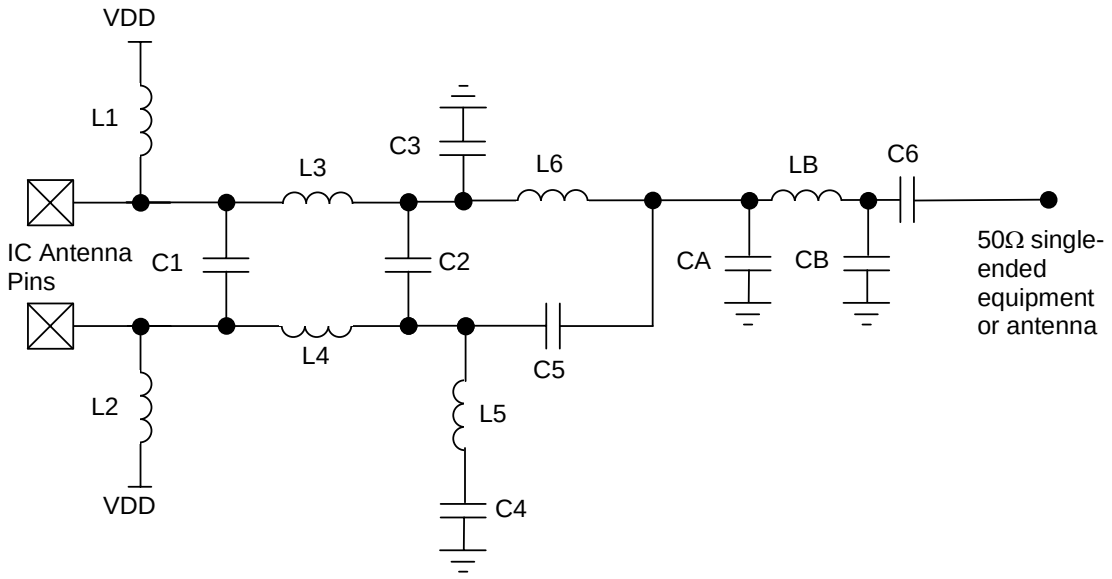


Figure 6 Structure of the antenna interface to 50Ω single-ended equipment or antenna

Frequency Band	L1=L2 [nH]	C1 [pF]	L3=L4 [nH]	C2 [pF]	C3=C5 [pF]	L5=L6 [nH]	LB [nH]	CA=CB [pF]	C4=C6 [pF]
868 / 915 MHz	18	2.2	12	2.2	1.8	18	6.2	8.2	220
433 MHz	33	3	33	3.3	3.3	39	12	18	220

Dipole Antenna Interface

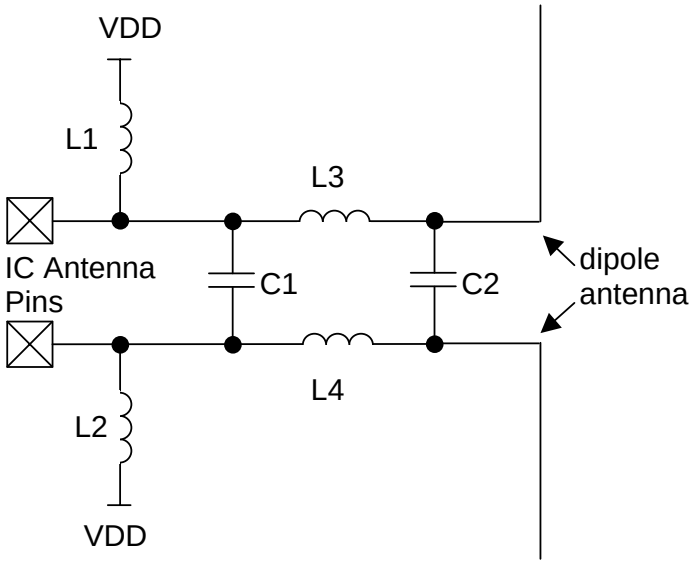
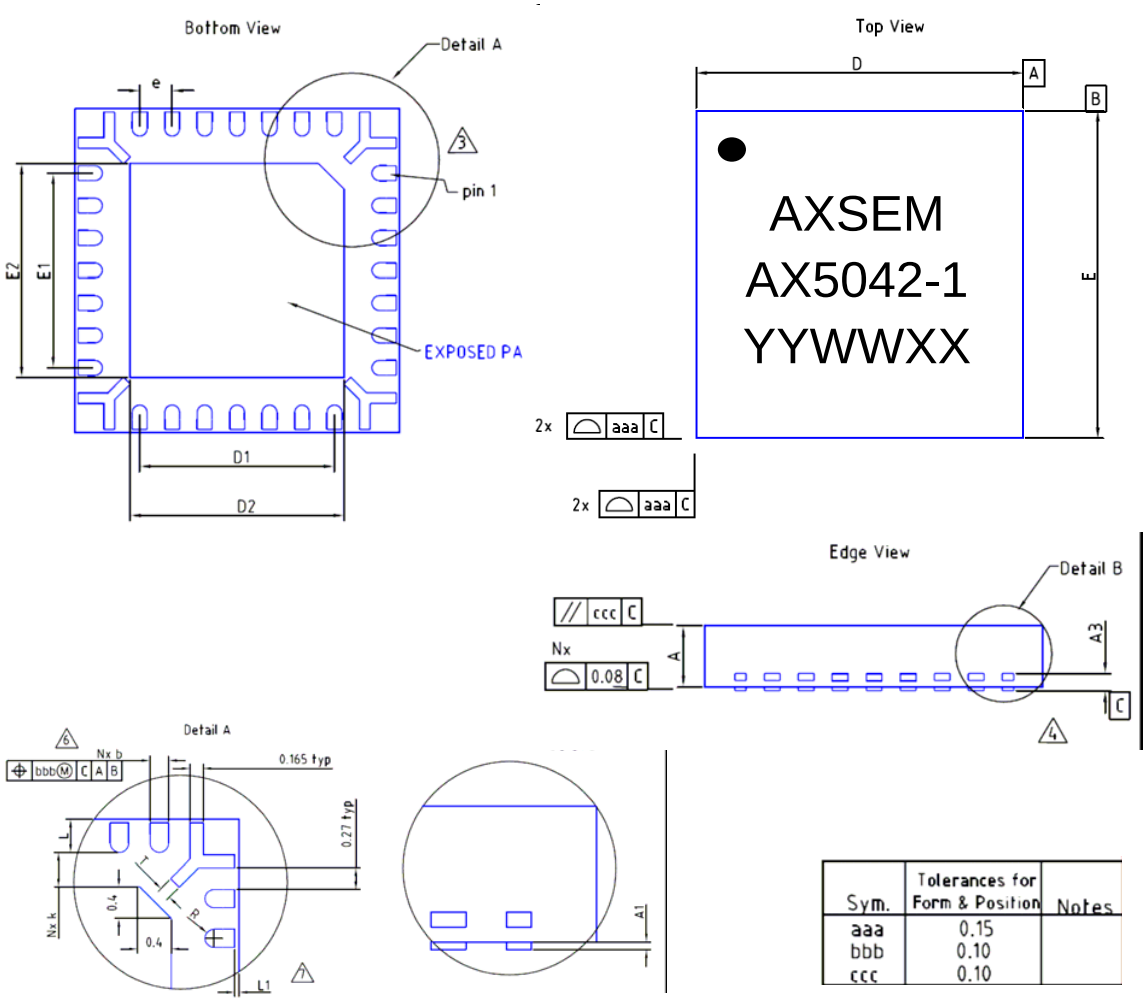


Figure 7 Structure of the antenna interface to a dipole antenna

Frequency Band	L1=L2 [nH]	C1 [pF]	L3=L4 [nH]	C2 [pF]
868 / 915 MHz	18	3.9	6.8	3.3
433 MHz	33	8	15	6.8

8. QFN28 Package Information

8.1. Package Outline QFN28



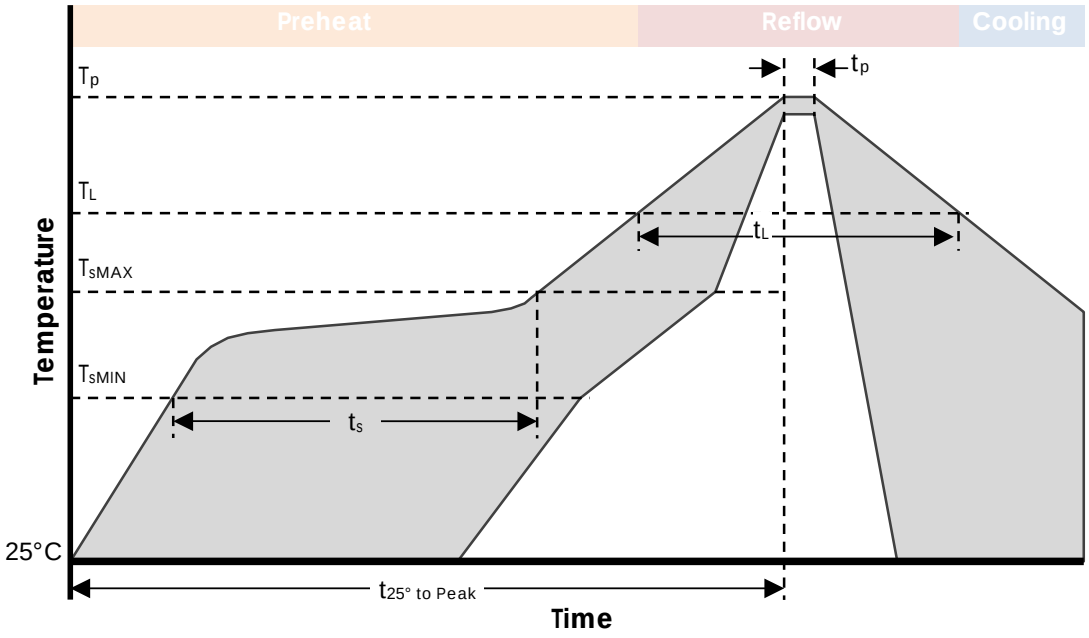
Sym.	Tolerances for Form & Position	Notes
aaa	0.15	
bbb	0.10	
ccc	0.10	

Notes

1. JEDEC ref MO-220
2. All dimensions are in millimeters
3. Pin 1 is identified by chamfer on corner of exposed die pad.
4. Datum C and the seating plane are defined by the flat surface of the metallised terminal
5. Dimension 'e' represent the terminal pitch
6. Dimension b applies to metallised terminal and is measured 0.25 to 0.30mm from terminal tip.
7. Dimension L1 represents terminal pull back from package edge. There terminal pull back esists, only upper half of lead is visible on package edge du to half etching of leadframe.
8. Package surface shall be matte finish, Ra 1.6-2.2
9. Package warp shall be 0.050 maximum
10. Leadframe material is copper A194
11. Coplanarity applies to the exposed pad as well as the terminal
12. YYWWXX is the packaging lot code
13. RoHS compliant

Common Dimensions			
Sym.	Minimum	Nominal	Maximum
A	0.85	0.90	1.0
A1	0	0.02	0.05
A3		0.20 ref	
D	4.90	5.0	5.10
D1		3.00	
D2	3.20	3.30	3.40
E	4.90	5.0	5.10
E1		3.0	
E2	3.20	3.30	3.40
L	0.35	0.40	0.45
L1			0.1
b	0.18	0.23	0.30
N		28	
e		0.50	
k	0.20		
R	b min / 2		
T		0.15	

8.2. QFN28 Soldering Profile



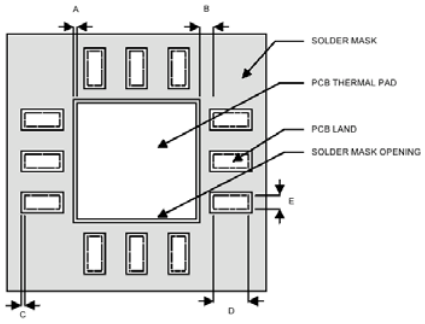
Profile Feature		Pb-Free Process
Average Ramp-Up Rate		3 °C/sec max.
Preheat Preheat		
Temperature Min	T_{sMIN}	150°C
Temperature Max	T_{sMAX}	200°C
Time (T_{sMIN} to T_{sMAX})	t_s	60 – 180 sec
Time 25°C to Peak Temperature	$T_{25\,°\,to\,Peak}$	8min max.
Reflow Phase		
Liquidus Temperature	T_L	217°C
Time over Liquidus Temperature	t_L	60 – 150 sec
Peak Temperature	t_p	260°C
Time within 5°C of actual Peak Temperature	T_p	20 – 40 sec
Cooling Phase		
Ramp-down rate		6°C/sec max.

Notes:

All temperatures refer to the top side of the package, measured on the package body surface.

8.3. QFN28 Recommended Pad Layout

1. PCB land and solder masking recommendations are shown in Figure 8.



A = Clearance from PCB thermal pad to solder mask opening, 0.0635 mm minimum
B = Clearance from edge of PCB thermal pad to PCB land, 0.2 mm minimum
C = Clearance from PCB land edge to solder mask opening to be as tight as possible to ensure that some solder mask remains between PCB pads
D = PCB land length = QFN solder pad length + 0.1mm
E = PCB land width = QFN solder pad width + 0.1 mm

Figure 8: PCB land and solder mask recommendations

2. Thermal vias should be used on the PCB thermal pad (middle ground pad) to improve thermal conductivity from the device to a copper ground plane area on the reverse side of the printed circuit board. The number of vias depends on the package thermal requirements, as determined by thermal simulation or actual testing.

3. Increasing the number of vias through the printed circuit board will improve the thermal conductivity to the reverse side ground plane and external heat sink. In general, adding more metal through the PC board under the IC will improve operational heat transfer, but will require careful attention to uniform heating of the board during assembly.

8.4. Assembly Process

Stencil Design & Solder Paste Application

1. Stainless steel stencils are recommended for solder paste application.

2. A stencil thickness of 0.125 – 0.150 mm (5 – 6 mils) is recommended for screening.

3. For the PCB thermal pad, solder paste should be printed on the PCB by designing a stencil with an array of smaller openings that sum to 50% of the QFN exposed pad area. Solder paste should be applied through an array of squares (or circles) as shown in Figure 9.

4. The aperture opening for the signal pads should be between 50-80% of the QFN pad area as shown in Figure 10.

5. Optionally, for better solder paste release, the aperture walls should be trapezoidal and the corners rounded.

6. The fine pitch of the IC leads requires accurate alignment of the stencil and the printed circuit board. The stencil and printed circuit assembly should be aligned to within + 1 mil prior to application of the solder paste.

7. No-clean flux is recommended since flux from underneath the thermal pad will be difficult to clean if water-soluble flux is used.

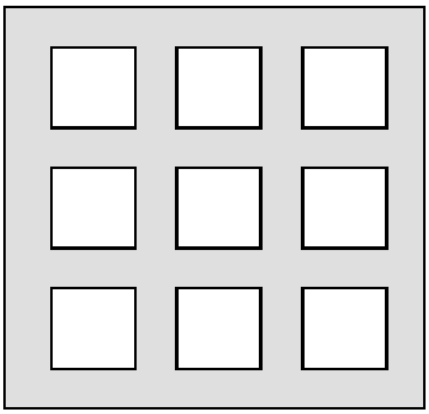


Figure 9: Solder paste application on exposed pad

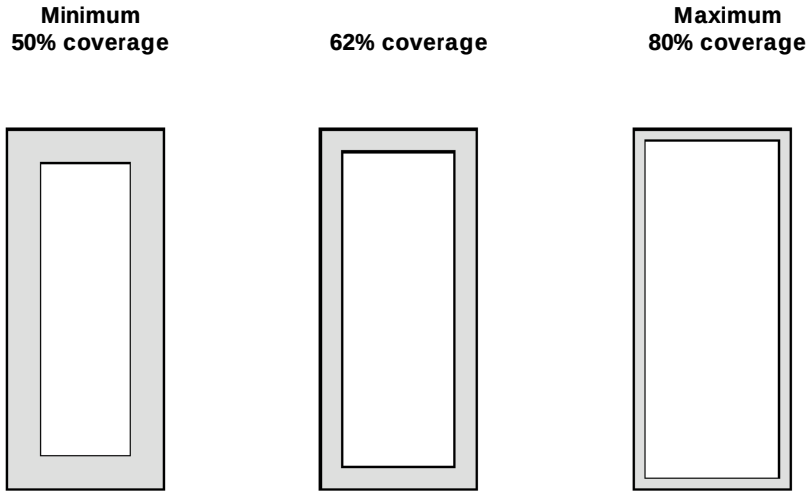


Figure 10: Solder paste application on pins

9. Life Support Applications

This product is not designed for use in life support appliances, devices, or in systems where malfunction of this product can reasonably be expected to result in personal injury. AXSEM customers using or selling this product for use in such applications do so at their own risk and agree to fully indemnify AXSEM for any damages resulting from such improper use or sale.

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