

TAT7430B

CATV 75 Ω pHEMT High Gain RF Amplifier

Applications

- Single-ended and Push-pull Optical Receivers
- Low-noise Drop Amplifiers
- Distribution Amplifiers
- Multi-Dwelling Units
- Single-ended Gain Block

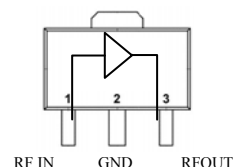


SOT-89 package

Product Features

- High typical gain of 22 dB in application circuit
- On-chip active bias for consistent bias current and repeatable performance
- 50 – 1200 MHz bandwidth
- Low noise: typical NF < 2.2 dB to 1000MHz
- Flexible 5 V to 8 V biasing
- $I_{DD}(8V) = 190$ mA typical in application circuit
- +41 dBm typical OIP3
- +65 dBm typical OIP2
- +22 dBm typical P1dB
- Low distortion: CSO -61 dBc, CTB -81 dBc (10 dBmV/ch at input, 80 ch NTSC flat)
- pHEMT device technology
- SOT-89 package

Functional Block Diagram



General Description

The TAT7430B is a low cost RF amplifier designed for applications from DC to 1200 MHz. The balance of low noise and distortion provides an ideal solution for a wide range of broadband amplifiers used in cable television applications.

It is particularly well suited for new home networks requiring higher gain for a large number of splits. In addition, the TAT7430B's combination of high gain, low noise, and good return loss make it an excellent choice for optical receiver applications and low noise front ends.

An internal bias circuit mitigates the effect of temperature and process variation. The bias current can be adjusted with an external resistor. It is able to work in low noise applications from a 5 V supply.

The TAT7430B is fabricated using 6-inch GaAs pHEMT technology to optimize performance and cost. It provides excellent gain and return loss consistency inherent to the pHEMT process.

Pin Configuration

Pin #	Symbol
1	RF IN
2	GND
3	RF OUT
4	GND PADDLE

Ordering Information

Part No.	Description
TAT7430B	75 Ω High linearity pHEMT amplifier (lead-free/RoHS compliant SOT-89 Pkg)
TAT7430B-EB	Amplifier evaluation board

Standard T/R size = 1000 pieces on a 7" reel.

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Specifications

Absolute Maximum Ratings¹

Parameter	Rating
Storage Temperature	-65 to +150 °C
Device Voltage	+10 V

1. Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
V _{cc}	5		8	V
I _{cc}		190		mA
T _J (for >10 ⁶ hours MTF)			150	°C

Electrical Specifications

Test conditions unless otherwise noted: 25°C case temp, +8V Vsupply, DC to 1200 MHz

Parameter	Conditions	Min	Typical	Max	Units
Operational Frequency Range		50		1002	MHz
Gain			22		dB
Gain Flatness			+/- 0.5		dB
Noise Figure at 1 GHz			2.0		dB
Input Return Loss			-22		dB
Output Return Loss			-18		dB
P1dB			+22		dBm
Output IP3	See Note 1.		+41		dBm
Output IP2	See Note 1.		+65		dBm
CSO	See Note 2.		-61		dBc
CTB	See Note 2.		-81		dBc
I _{dd}			190		mA
Thermal Resistance (jnc. to case) θ_{jc}				32	°C/W

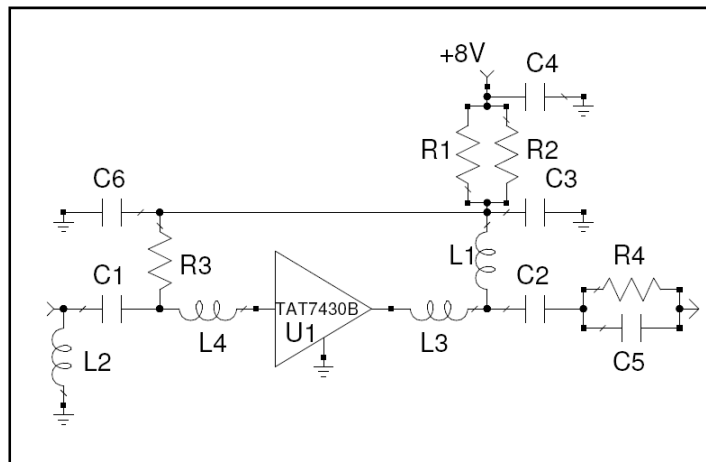
Notes:

1. At -21 dBm/line at input.
2. 10 dBmV/ch at input, 80 ch flat NTSC
3. Electrical specifications are measured at specified test conditions.
4. Specifications are not guaranteed over all recommended operating conditions.

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Reference Design DC-1200 MHz



Notes:

1. See PC Board Layout, page 5 for more information

Bill of Material

Ref Des	Value	Description	Manufacturer	Part Number
U1		Amplifier, SOT-89	TriQuint	TAT7430B
R1, R2	20 Ω	Thick Film Res., 1206, 1%, 1/4 W	various	
R3	15 k Ω	Thick Film Res., 0402, 5%, 1/10 W	various	
R4	5.1 Ω	Thick Film Res., 0402, 5%, 1/10 W	various	
C1	150 pF	Ceramic Cap, 0603, COG, 16V, 5%	various	
C2	220 pF	Ceramic Cap, 0402, COG, 16V, 5%	various	
C3, C4, C6	0.01 μ F	Ceramic Cap, 0603, X7R, 50V, 10%	various	
C5	47 pF	Ceramic Cap, 0402, COG, 16V, 5%	various	
L1, L2	500 nH	Ferrite Ind., Vertical Wire-Wound, 1206, 10%	various	
L3	5.6 nH	Ceramic Wire-Wound Ind, 0402, 5%	various	
L4	7.5 nH	Ceramic Wire-Wound Ind, 0402, 5%	various	

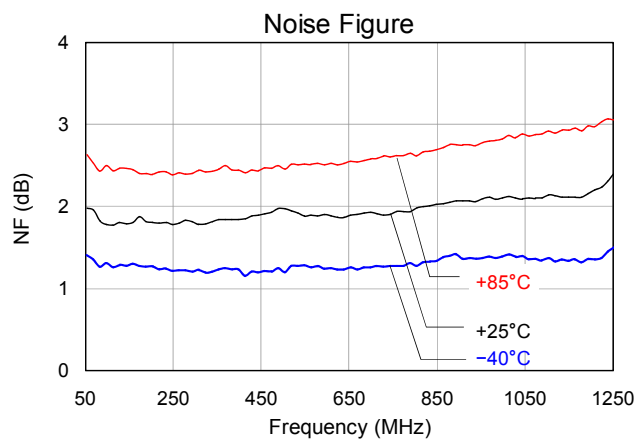
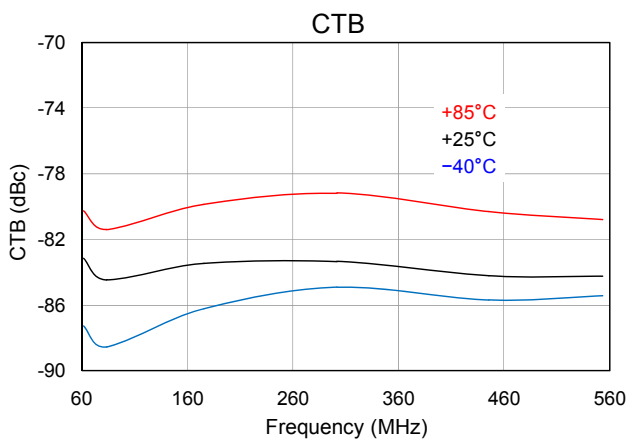
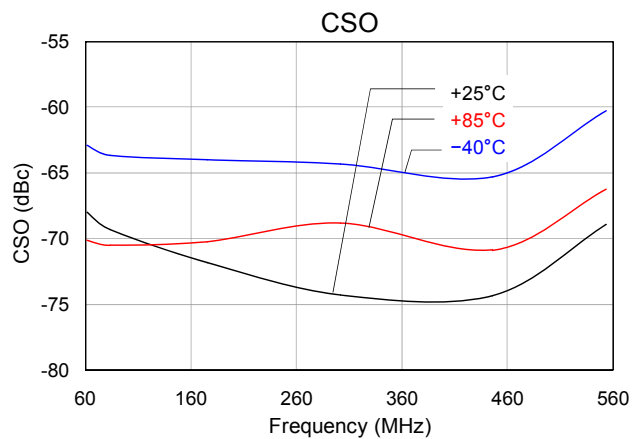
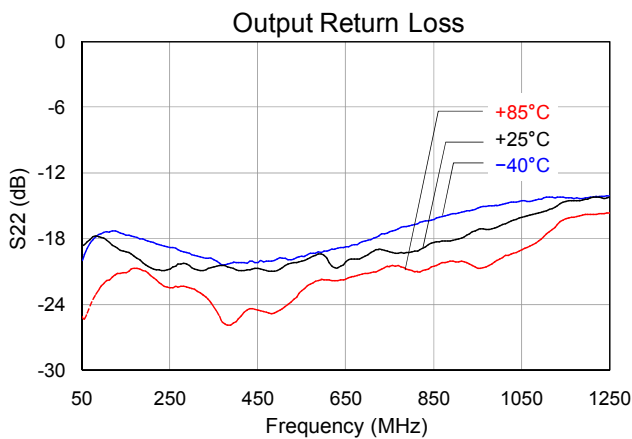
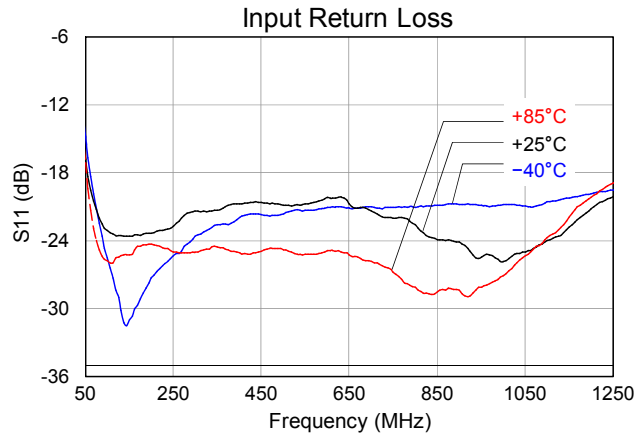
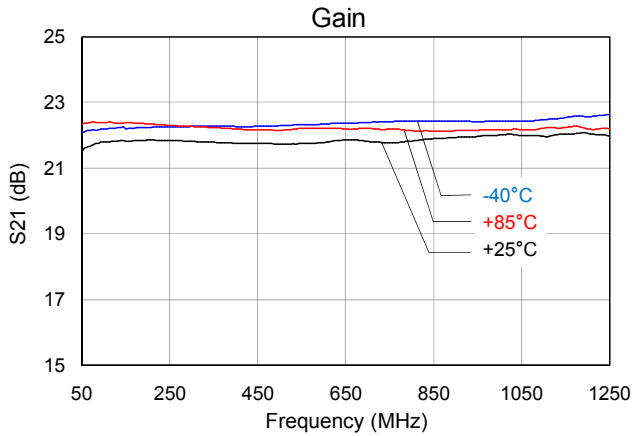
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Application Board Typical Performance

Case temperature noted on graphs. $V_{supply} = 8V$, $I_{cc} = 190\text{ mA}$.



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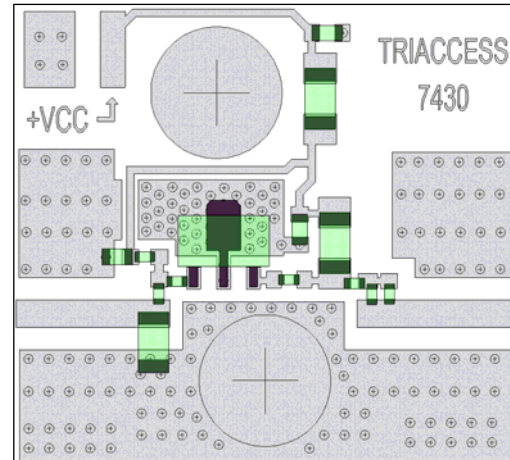
Applications Information

PC Board Layout

Core is .062" FR-4, $\epsilon_r = 4.7$ at 1 MHz. Metal layers are 1-oz copper.

The pad pattern shown has been developed and tested for optimized assembly at TriQuint Semiconductor. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.

For further technical information, Refer to <http://www.triquint.com/TAT7430B>



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Mechanical Information

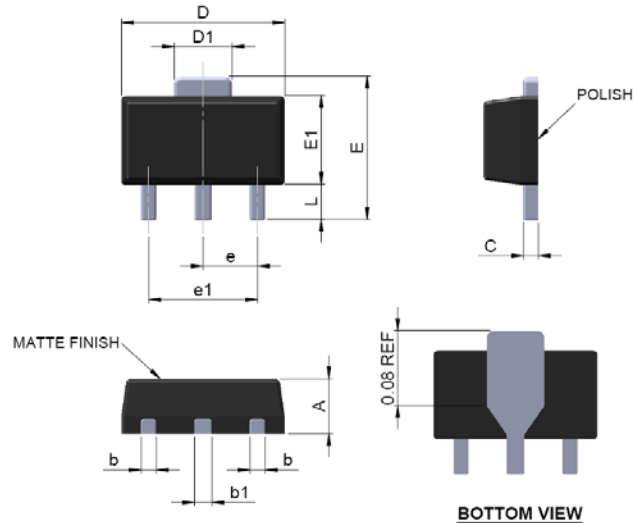
Package Information and Dimensions

This package is lead-free/RoHS-compliant. The plating material on the leads is 100 % Matte Tin. It is compatible with both lead-free (maximum 260 °C reflow temperature) and lead (maximum 245 °C reflow temperature) soldering processes.

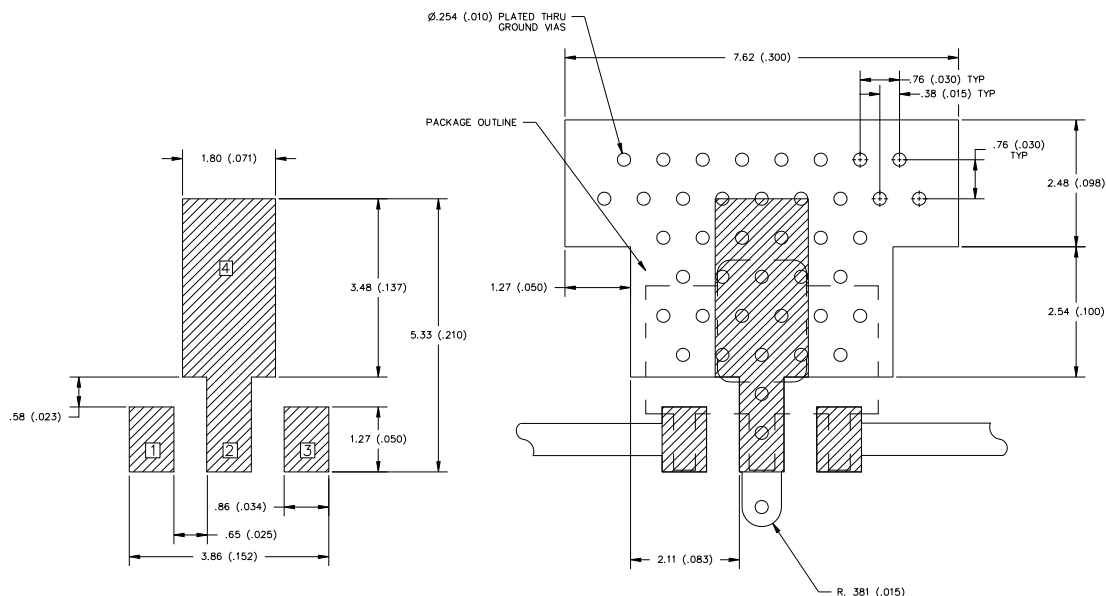
The TAT7430B will be marked with a “TAT7430B” designator and an alphanumeric lot code.

SYMBOL	MIN	NOM	MAX
A - Thickness	1.40	1.50	1.60
C - Lead thickness	0.35		0.43
D - Body width	4.40		4.60
E1 - Body length	2.30		2.60
E - Total length	3.64		4.25
e - Lead spacing	1.40	1.50	1.60
e1 - Dual lead spacing	2.90	3.00	3.10
b - Outer lead width	0.35		0.48
b1 - Center lead width	0.40		0.56
L - Lead length	0.74		1.20
d1 - Tab lead width	1.40		1.80
Above body	0.35		0.64

DIMENSIONS ARE IN MM



Mounting Configuration



Notes:

1. Ground / thermal vias are critical for the proper performance of this device. Vias should use a .35 mm (#80/.0135”) diameter drill and have a final, plated thru diameter of .25 mm (.010”).
2. Add as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.
3. RF trace width depends upon the PC board material and construction.
4. All dimensions are in millimeters (inches). Angles are in degrees.

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Product Compliance Information

ESD Information



Caution! ESD-Sensitive Device

ESD Rating: Class 1B
Value: Passes ≥ 600 V min.
Test: Human Body Model (HBM)
Standard: JEDEC Standard JESD22-A114

ESD Rating: Class IV
Value: Passes ≥ 2000 V min.
Test: Charged Device Model (CDM)
Standard: JEDEC Standard JESD22-C101

MSL Rating

Level 3 at +260 °C convection reflow
JEDEC standard IPC/JEDEC J-STD-020.

Solderability

Compatible with the latest version of J-STD-020, Lead free solder, 260 °C.

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

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