19-0806; Rev 1; 11/08

EVALUATION KIT AVAILABLE

2.3GHz to 2.7GHz Wireless Broadband RF Transceiver

MAX2837

General Description

The MAX2837 direct-conversion zero-IF RF transceiver is designed specifically for 2.3GHz to 2.7GHz wireless broadband systems. The MAX2837 completely integrates all circuitry required to implement the RF transceiver function, providing RF-to-baseband receive path; and baseband-to-RF transmit path, VCO, frequency synthesizer, crystal oscillator, and baseband/control interface. The device includes a fast-settling sigma-delta RF synthesizer with smaller than 20Hz frequency steps and a crystal oscillator, which allows the use of a low-cost crystal in place of a TCXO. The transceiver IC also integrates circuits for on-chip DC offset cancellation, I/Q error, and carrier-leakage detection circuits. Only an RF bandpass filter (BPF), crystal, RF switch, PA, and a small number of passive components are needed to form a complete wireless broadband RF radio solution.

The MAX2837 completely eliminates the need for an external SAW filter by implementing on-chip monolithic filters for both the receiver and transmitter. The baseband filters along with the Rx and Tx signal paths are optimized to meet stringent noise figure and linearity specifications. The device supports up to 2048 FFT OFDM and implements programmable channel filters for 1.75MHz to 28MHz RF channel bandwidths. The transceiver requires only 2µs Tx-Rx switching time, which includes frequency transient settling. The IC is available in a small, 48-pin thin QFN package measuring only 6mm x 6mm x 0.8mm.

Applications

802.16-2004 Fixed WiMAX

Korea Wibro and 802.16e Mobile WiMAX

Dual Mode™ WiMAX/802.11b/g Wi-Fi

Proprietary Wireless Broadband Systems

4G/LTE Systems

Dual Mode is a trademark of Maxim Integrated Products, Inc.

SPI is a trademark of Motorola, Inc.

Features

- **2.3GHz to 2.7GHz Wideband Operation**
- **Complete RF Transceiver, PA Driver, and Crystal Oscillator**
  - **0dBm Linear OFDM Transmit Power**
  - **-70dBr Tx Spectral Emission Mask**
  - **2.3dB Rx Noise Figure**
  - **Tx/Rx I/Q Error and LO Leakage Detection**
  - **Monolithic Low-Noise VCO with -39dBc Integrated Phase Noise**
  - **Programmable Tx I/Q Lowpass Anti-Aliasing Filter**
  - **Sigma-Delta Fractional-N PLL with 20Hz Step Size**
  - **45dB Tx Gain-Control Range**
  - **94dB Receive Gain-Control Range**
  - **60dB Analog RSSI Instantaneous Dynamic Range**
  - **4-Wire SPI™ Digital Interface**
  - **I/Q Analog Baseband Interface**
  - **Digitally Tuned Crystal Oscillator**
  - **On-Chip Digital Temperature Sensor Read-Out**
- **+2.7V to +3.6V Transceiver Supply**
- **Low-Power Shutdown Current**
- **Small 48-Pin Thin QFN Package (6mm x 6mm x 0.8mm)**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX2837ETM+TD	-40°C to +85°C	48 TQFN-EP*

**EP = Exposed paddle.*

+Denotes a lead-free package.

Pin Configuration appears at end of data sheet.

ABSOLUTE MAXIMUM RATINGS

V_{CCLNA}, V_{CCTXMX}, $V_{CCTXPAD}$, V_{CCDIG}, V_{CCCP}, V_{CCXTAL}, V_{CCVCO}, $V_{CCRXVGA}$, V_{CCRXFL} and V_{CCRXMX} to GND....-0.3V to +3.9V
B1–B7, TXRF_, $\overline{CS}$, SCLK, DIN, DOUT, TXBBI_, TXBBQ_, RXHP, RXBBI_, RXBBQ_, RSSI, ENABLE, BYPASS, CPOUT_, CLOCKOUT, XTAL1, XTAL2, RXRF_,RXENABLE, TXENABLE to GND....-0.3V to (Operating V_{CC} + 0.3V)
RXBBI_, RXBBQ_, RSSI, BYPASS, CPOUT_, DOUT, CLOCKOUT, PABIAS Short-Circuit Duration....10s
RF Input Power....+10dBm

Continuous Power Dissipation (T_A = +70°C)
48-Pin Thin QFN (derates 37mW/°C above +70°C).......2.96W
Operating Temperature Range ....-40°C to +85°C
Junction Temperature....+150°C
Storage Temperature Range ....-65°C to +160°C
Lead Temperature (soldering, 10s) ....+260°C

CAUTION! ESD SENSITIVE DEVICE

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(MAX2837 evaluation kit: $V_{CC\_}$ = 2.7V to 3.6V, Rx set to the maximum gain; $\overline{CS}$ = high, RXHP = SCLK = DIN = low, RSSI and clock output buffer are off, no signal at RF inputs, all RF inputs and outputs terminated into 50Ω, receiver baseband outputs are open; $90mV_{RMS}$ differential I and Q signals applied to I, Q baseband inputs of transmitter in transmit mode, f_{REF} = 40MHz, registers set to recommended settings and corresponding test mode, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 2.8V, f_{LO} = 2.5GHz, and T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	$V_{CC\_}$	2.7		3.6	V
Supply Current	Shutdown mode, T_A = +25°C		10		µA
	Standby mode		35	45	mA
	Rx mode		91	110	
	Tx mode, T_A = +25°C		145	170	
	Rx calibration mode		135	160	
	Tx calibration mode		110	135	
Rx I/Q Output Common-Mode Voltage	D9:D8 = 00 in A4:A0 = 00100	0.85	1.0	1.20	V
	D9:D8 = 01 in A4:A0 = 00100		1.1		
	D9:D8 = 10 in A4:A0 = 00100		1.2		
	D9:D8 = 11 in A4:A0 = 00100		1.35		
Tx Baseband Input Common-Mode Voltage Operating Range	DC-coupled	0.5		1.2	V
Tx Baseband Input Bias Current	Source current		10	20	µA
LOGIC INPUTS: ENABLE, TXENABLE, RXENABLE, SCLK, DIN, $\overline{CS}$, B7:B1, RXHP					
Digital Input-Voltage High, V_{IH}		V_{CC} - 0.4			V
Digital Input-Voltage Low, V_{IL}				0.4	V
Digital Input-Current High, I_{IH}		-1		+1	µA
Digital Input-Current Low, I_{IL}		-1		+1	µA

DC ELECTRICAL CHARACTERISTICS (continued)

(MAX2837 evaluation kit: $V_{CC\_}$ = 2.7V to 3.6V, Rx set to the maximum gain; $\overline{CS}$ = high, RXHP = SCLK = DIN = low, RSSI and clock output buffer are off, no signal at RF inputs, all RF inputs and outputs terminated into 50Ω, receiver baseband outputs are open; $90mV_{RMS}$ differential I and Q signals applied to I, Q baseband inputs of transmitter in transmit mode, f_{REF} = 40MHz, registers set to recommended settings and corresponding test mode, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 2.8V, f_{LO} = 2.5GHz, and T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC OUTPUTS: DOUT					
Digital Output-Voltage High, V_{OH}	Sourcing 100µA	V_{CC} - 0.4			V
Digital Output-Voltage Low, V_{OL}	Sinking 100µA			0.4	V

AC ELECTRICAL CHARACTERISTICS—Rx MODE

(MAX2837 evaluation kit: $V_{CC\_}$ = 2.8V, f_{RF} = 2.502GHz, f_{LO} = 2.5GHz; receiver baseband I/Q outputs at $90mV_{RMS}$ (-21dBV), f_{REF} = 40MHz, ENABLE = RXENABLE = $\overline{CS}$ = high, TXENABLE = SCLK = DIN = low, with power matching for the differential RF pins using the typical applications and registers set to default settings and corresponding test mode, T_A = +25°C, unless otherwise noted. Lowpass filter is set to 10MHz RF channel BW. Unmodulated single-tone RF input signal is used, unless otherwise indicated.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
RECEIVER SECTION: LNA RF INPUT TO BASEBAND I/Q OUTPUTS						
RF Input Frequency Range			2.3		2.7	GHz
Peak-to-Peak Gain Variation over RF Input Frequency Range	Tested at band edges and band center			0.8		dB
RF Input Return Loss	All LNA gain settings			13		dB
Total Voltage Gain	T_A = -40°C to +85°C	Maximum gain, B7:B1 = 0000000	90	99		dB
		Minimum gain, B7:B1 = 1111111		5	13	
RF Gain Steps	From max RF gain to max RF gain - 8dB			8		dB
	From max RF gain to max RF gain - 16dB			16		
	From max RF gain to max RF gain - 32dB			32		
Gain Change Settling Time	Any RF or baseband gain change; gain settling to within ±1dB of steady state; RXHP = 1			0.2		µs
	Any RF or baseband gain change; gain settling to within ±0.1dB of steady state; RXHP = 1			2		
Baseband Gain Range	From maximum baseband gain (B5:B1 = 00000) to minimum baseband gain (B5:B1 = 11111), T_A = -40°C to +85°C		58	62	66	dB
Baseband Gain Minimum Step Size				2		dB
DSB Noise Figure	Voltage gain ≥ 65dB with max RF gain (B7:B6 = 00)			2.3		dB
	Voltage gain = 50dB with max RF gain - 8dB (B7:B6 = 01)			5.5		
	Voltage gain = 45dB with max RF gain - 16dB (B7:B6 = 10)			17		
	Voltage gain = 15dB with max RF gain - 32dB (B7:B6 = 11)			27		

AC ELECTRICAL CHARACTERISTICS—Rx MODE (continued)

MAX2837 evaluation kit: $V_{CC\_}$ = 2.8V, f_{RF} = 2.502GHz, f_{LO} = 2.5GHz; receiver baseband I/Q outputs at 90mV_{RMS} (-21dBV), f_{REF} = 40MHz, ENABLE = RXENABLE = $\overline{CS}$ = high, TXENABLE = SCLK = DIN = low, with power matching for the differential RF pins using the typical applications and registers set to default settings and corresponding test mode, T_A = +25°C, unless otherwise noted. Lowpass filter is set to 10MHz RF channel BW. Unmodulated single-tone RF input signal is used, unless otherwise indicated.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
In-Band Input P-1dB	Max RF gain (B7:B6 = 00)			-37		dBm
	Max RF gain - 8dB (B7:B6 = 01)			-29		
	Max RF gain - 16dB (B7:B6 = 10)			-21		
	Max RF gain - 32dB (B7:B6 = 11)			-4		
Maximum Output Signal Level	Over passband frequency range; at any gain setting; 1dB compression point			2.5		V_{P-P}
Out-of-Band Input IP3 (Note 2)	Max RF gain (B7:B6 = 00), AGC set for -65dBm wanted signal			-11		dBm
	Max RF gain - 8dB (B7:B6 = 01), AGC set for -55dBm wanted signal			-8		
	Max RF gain - 16dB (B7:B6 = 10), AGC set for -40dBm wanted signal			-6		
	Max RF gain - 32dB (B7:B6 = 11), AGC set for -30dBm wanted signal			+16		
I/Q Phase Error	50kHz baseband output; 1σ variation			0.15		Degrees
I/Q Gain Imbalance	50kHz baseband output; 1σ variation			0.1		dB
Rx I/Q Output Load Impedance (R II C)	Minimum differential resistance			10		kΩ
	Maximum differential capacitance			5		pF
I/Q Output DC Droop	After switching RXHP to 0; average over 1µs after any gain change, or 2µs after receive enabled with 100Hz interval AC-coupling, 1σ variation			±1		mV/ms
I/Q Static DC Offset	No RF input signal; measure at 3µs after receive enable; RXHP = 1 for 0 to 2µs and set to 0 after 2µs, 1σ variation			±1		mV
Loopback Gain (for Receiver I/Q Calibration)	Transmitter I/Q input to receiver I/Q output; transmitter B6:B1 = 000011, receiver B5:B1 = 10100 programmed through SPI		-4.5	0	+4.5	dB
RECEIVER BASEBAND FILTERS						
Baseband Filter Rejection	At 15MHz			57		dB
	At 20MHz			75		
	At > 40MHz			90		
Baseband Highpass Filter Corner Frequency	RXHP = 1 (used before AGC completion)			650		kHz
	RXHP = 0 (used after AGC completion) address A4:A0 = 01110	D5:D4 = 00		0.1		
		D5:D4 = 01		1		
		D5:D4 = 10		30		
		D5:D4 = 11		100		

AC ELECTRICAL CHARACTERISTICS—Rx MODE (continued)

MAX2837 evaluation kit: $V_{CC\_}$ = 2.8V, f_{RF} = 2.502GHz, f_{LO} = 2.5GHz; receiver baseband I/Q outputs at 90mV$_{RMS}$ (-21dBV), f_{REF} = 40MHz, ENABLE = RXENABLE = $\overline{CS}$ = high, TXENABLE = SCLK = DIN = low, with power matching for the differential RF pins using the typical applications and registers set to default settings and corresponding test mode, T_A = +25°C, unless otherwise noted. Lowpass filter is set to 10MHz RF channel BW. Unmodulated single-tone RF input signal is used, unless otherwise indicated.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
RF Channel BW Supported by Baseband Filter	A4:A0 = 00010 serial bits D7:D4 = 0000			1.75		MHz
	A4:A0 = 00010 serial bits D7:D4 = 0001			2.25		
	A4:A0 = 00010 serial bits D7:D4 = 0010			3.5		
	A4:A0 = 00010 serial bits D7:D4 = 0011			5.0		
	A4:A0 = 00010 serial bits D7:D4 = 0100			5.5		
	A4:A0 = 00010 serial bits D7:D4 = 0101			6.0		
	A4:A0 = 00010 serial bits D7:D4 = 0110			7.0		
	A4:A0 = 00010 serial bits D7:D4 = 0111			8.0		
	A4:A0 = 00010 serial bits D7:D4 = 1000			9.0		
	A4:A0 = 00010 serial bits D7:D4 = 1001			10.0		
	A4:A0 = 00010 serial bits D7:D4 = 1010			12.0		
	A4:A0 = 00010 serial bits D7:D4 = 1011			14.0		
	A4:A0 = 00010 serial bits D7:D4 = 1100			15.0		
	A4:A0 = 00010 serial bits D7:D4 = 1101			20.0		
	A4:A0 = 00010 serial bits D7:D4 = 1110			24.0		
	A4:A0 = 00010 serial bits D7:D4 = 1111			28.0		
Baseband Gain Ripple	0 to 2.3MHz for BW = 5MHz			1.3		dB_{P-P}
	0 to 4.6MHz for BW = 10MHz			1.3		
Baseband Group Delay Ripple	0 to 2.3MHz for BW = 5MHz			90		ns_{P-P}
	0 to 4.6MHz for BW = 10MHz			50		
Baseband Filter Rejection for 5MHz RF Channel BW	At 3.3MHz			7		dB
	At > 21MHz			85		
Baseband Filter Rejection for 10MHz RF Channel BW	At 6.7MHz			7		dB
	At > 41.6MHz			85		
RSSI						
RSSI Minimum Output Voltage	$R_{LOAD} \geq 10k\Omega$			0.4		V
RSSI Maximum Output Voltage	$R_{LOAD} \geq 10k\Omega$			2.2		V
RSSI Slope				30		mV/dB
RSSI Output Settling Time	To within 3dB of steady state	+32dB signal step		200		ns
		-32dB signal step		800		

AC ELECTRICAL CHARACTERISTICS—Tx MODE

(MAX2837 evaluation kit: $V_{CC\_}$ = 2.8V, T_A = +25°C, f_{RF} = 2.502GHz, f_{LO} = 2.5GHz; f_{REF} = 40MHz, ENABLE = TXENABLE = $\overline{CS}$ = high, and RXENABLE = SCLK = DIN = low, with power matching for the differential RF pins using the *Typical Operating Circuit*. Lowpass filter is set to 10MHz RF channel BW, 90mV$_{RMS}$ sine and cosine signal (or 90mV$_{RMS}$ 64QAM 1024-FFT OFDMA FUSC I/Q signals wherever OFDM is mentioned) applied to baseband I/Q inputs of transmitter (differential DC-coupled).) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
TRANSMIT SECTION: Tx BASEBAND I/Q INPUTS TO RF OUTPUTS					
RF Output Frequency Range		2.3		2.7	GHz
Peak-to-Peak Gain Variation over RF Band	Output optimally matched over 200MHz RF BW		2.5		dB
Total Voltage Gain	Max gain; at unbalanced 50Ω balun output		12		dB
Maximum Output Power over Frequency for Any Given 200MHz Band	OFDM signal conforming to spectral emission mask and -36dB EVM after I/Q imbalance calibration by modem (Note 3)		0		dBm
RF Output Return Loss	Given 200MHz band in the 2.3GHz to 2.7GHz range, for which the matching has been optimized		8		dB
RF Gain Control Range			45		dB
Unwanted Sideband Suppression	Without calibration by modem, and excludes modem I/Q imbalance; P_{OUT} = 0dBm		45		dBc
RF Gain-Control Binary Weights	B1		1		dB
	B2		2		
	B3		4		
	B4		8		
	B5		16		
	B6		16		
Carrier Leakage	Relative to 0dBm output power; without calibration by modem		-35		dBc
Tx I/Q Input Impedance (R ll C)	Minimum differential resistance		100		kΩ
	Maximum differential capacitance		0.5		pF
Baseband Frequency Response for 5MHz RF Channel BW	0 to 2.3MHz		0.2		dB
	At > 25MHz		80		
Baseband Frequency Response for 10MHz RF Channel BW	0 to 4.6MHz		0.2		dB
	At > 17MHz		80		
Baseband Group Delay Ripple	0 to 2.3MHz (BW = 5MHz)		20		ns
	0 to 4.6MHz (BW = 10MHz)		12		

AC ELECTRICAL CHARACTERISTICS—FREQUENCY SYNTHESIS

(MAX2837 evaluation kit: $V_{CC\_}$ = 2.8V, f_{LO} = 2.5GHz, f_{REF} = 40MHz, ENABLE = $\overline{CS}$ = high, SCLK = DIN = low, PLL loop bandwidth = 120kHz, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
FREQUENCY SYNTHESIZER					
RF Channel Center Frequency		2.3		2.7	GHz
Channel Center Frequency Programming Minimum Step Size			20		Hz
Charge-Pump Comparison Frequency		11	40		MHz
Reference Frequency Range		11	40	80	MHz
Reference Frequency Input Levels	AC-coupled to XTAL2 pin	800			mV_{P-P}
Reference Frequency Input Impedance (R II C)	Resistance (XTAL2 pin)		10		kΩ
	Capacitance (XTAL2 pin)		1		pF
Programmable Reference Divider Values		1	2	4	
Closed-Loop Integrated Phase Noise	Loop BW = 120kHz; integrate phase noise from 200Hz to 5MHz, charge-pump comparison frequency = 40MHz		-39		dBc
Charge-Pump Output Current	On each differential side		1.6		mA
Close-In Spur Level	f_{OFFSET} = 0 to 1.8MHz		-40		dBc
	f_{OFFSET} = 1.8MHz to 7MHz		-70		
	f_{OFFSET} > 7MHz		-80		
Reference Spur Level			-85		dBc
Turnaround LO Frequency Error	Relative to steady state; measured 35µs after Tx-Rx or Rx-Tx switching instant, and 4µs after any receiver gain changes		±50		Hz
Temperature Range over Which VCO Maintains Lock	Relative to the ambient temperature T_A, as long as the VCO lock temperature range is within operating temperature range		T_A ±40		°C
Reference Output Clock Divider Values		1		2	
Output Clock Drive Level	20MHz output, 1x drive setting		1.5		V_{P-P}
Output Clock Minimum Load Impedance (R II C)	Resistance		10		kΩ
	Capacitance		2		pF

AC ELECTRICAL CHARACTERISTICS—MISCELLANEOUS BLOCKS

(MAX2837 evaluation kit: $V_{CC\_}$ = 2.8V, f_{REF} = 40MHz, ENABLE = $\overline{CS}$ = high, SCLK = DIN = low, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
PA BIAS DAC: CURRENT MODE						
Numbers of Bits				6		Bits
Minimum Output Sink Current	D5:D0 = 000000 in A4:A0 = 11100			0		µA
Maximum Output Sink Current	D5:D0 = 111111 in A4:A0 = 11100			310		µA
Compliance Voltage Range			0.8		2.0	V
Turn-On Time	Excludes programmable delay of 0 to 7µs in steps of 0.5µs			200		ns
DNL				1		LSB
PA BIAS DAC: VOLTAGE MODE						
Output High Level	10mA source current			V_{CC} - 0.2		V
Output Low Level	10mA sink current			0.1		V
Turn-On Time	Excludes programmable delay of 0 to 7µs in steps of 0.5µs			200		ns
CRYSTAL OSCILLATOR						
On-Chip Tuning Capacitance Range	Maximum capacitance, A4:A0 = 11000, D6:D0 =1111111			15.5		pF
	Minimum capacitance, A4:A0 = 11000, D6:D0 =0000000			0.5		
On-Chip Tuning Capacitance Step Size				0.12		pF
ON-CHIP TEMPERATURE SENSOR						
Digital Output Code	Read-out at DOUT pin through SPI A4:A0 = 00111, D4:D0	T_A = +25°C		01111		
		T_A = +85°C		11101		
		T_A = -40°C		00001		

AC ELECTRICAL CHARACTERISTICS—TIMING

(MAX2837 evaluation kit: $V_{CC\_}$ = 2.8V, f_{LO} = 2.5GHz, f_{REF} = 40MHz, ENABLE = $\overline{CS}$ = high, SCLK = DIN = low, PLL loop bandwidth = 120kHz, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SYSTEM TIMING							
Turnaround Time		Measured from Tx or Rx enable rising edge; signal settling to within 0.5dB of steady state	Rx to Tx		2		µs
			Tx to Rx, RXHP = 1		2		
Tx Turn-On Time (from Standby Mode)		Measured from Tx enable rising edge; signal settling to within 0.5dB of steady state			2		µs

AC ELECTRICAL CHARACTERISTICS—TIMING (continued)

(MAX2837 evaluation kit: $V_{CC\_}$ = 2.8V, f_{LO} = 2.5GHz, f_{REF} = 40MHz, ENABLE = $\overline{CS}$ = high, SCLK = DIN = low, PLL loop bandwidth = 120kHz, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Tx Turn-Off Time (to Standby Mode)		From Tx enable falling edge		0.1		µs
Rx Turn-On Time (from Standby Mode)		Measured from Rx enable rising edge; signal settling to within 0.5dB of steady state		2		µs
Rx Turn-Off Time (to Standby Mode)		From Rx enable falling edge		0.1		µs
4-WIRE SERIAL-INTERFACE TIMING (See Figure 1)						
SCLK Rising Edge to $\overline{CS}$ Falling Edge Wait Time	t_{CSO}			6		ns
Falling Edge of $\overline{CS}$ to Rising Edge of First SCLK Time	t_{CSS}			6		ns
DIN to SCLK Setup Time	t_{DS}			6		ns
DIN to SCLK Hold Time	t_{DH}			6		ns
SCLK Pulse-Width High	t_{CH}			6		ns
SCLK Pulse-Width Low	t_{CL}			6		ns
Last Rising Edge of SCLK to Rising Edge of $\overline{CS}$ or Clock to Load Enable Setup Time	t_{CSH}			6		ns
$\overline{CS}$ High Pulse Width	t_{CSW}			20		ns
Time Between Rising Edge of $\overline{CS}$ and the Next Rising Edge of SCLK	t_{CS1}			6		ns
Clock Frequency	f_{CLK}				45	MHz
Rise Time	t_R			f_{CLK} / 10		ns
Fall Time	t_F			f_{CLK} / 10		ns
SCLK Falling Edge to Valid DOUT	t_D			12.5		ns

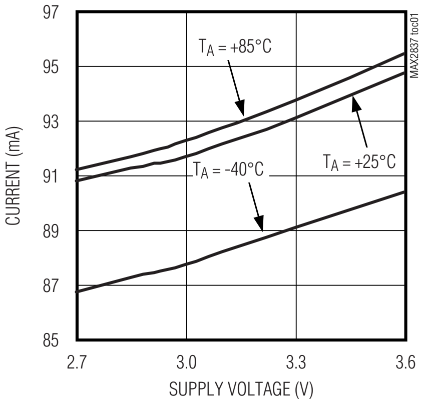
Note 1: Min and max limits guaranteed by test above T_A = +25°C and guaranteed by design and characterization at T_A = -40°C. The power-on register settings are not production tested. Recommended register setting must be loaded after V_{CC} is supplied.
Note 2: Two tones at +25MHz and +39MHz offset with -35dBm/tone. Measure IM3 at 1MHz.
Note 3: Gain adjusted over max gain and max gain - 3dB. Optimally matched over given 200MHz band.

2.3GHz to 2.7GHz Wireless Broadband RF Transceiver

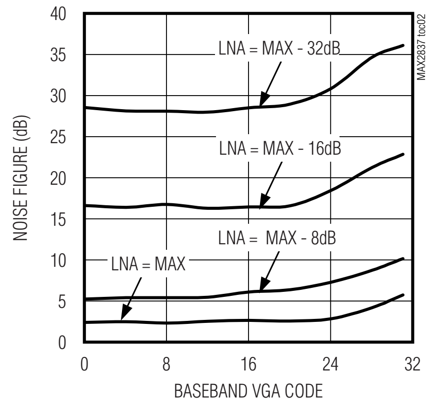
Typical Operating Characteristics

(MAX2837 evaluation kit: $V_{CC\_}$ = 2.8V, f_{LO} = 2.5GHz, 10MHz channel 16E UL/DL WiMax signal, f_{REF} = 40MHz, ENABLE = $\overline{CS}$ = high, RXHP = SCLK = DIN = low, T_A = +25°C, unless otherwise noted.)

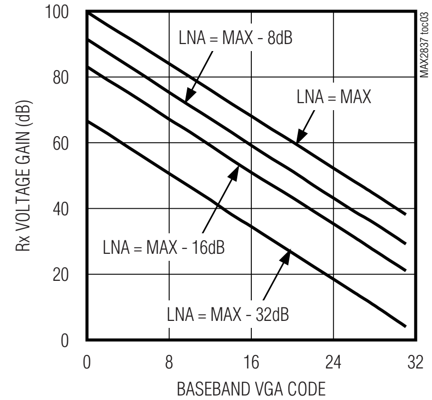
Rx CURRENT vs. SUPPLY VOLTAGE



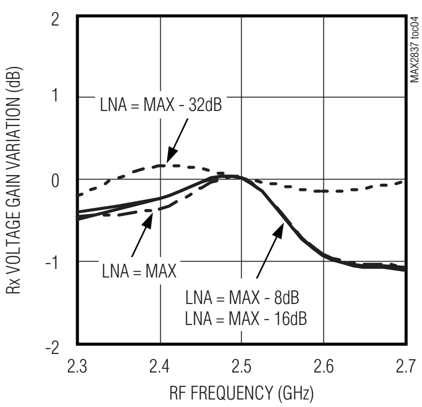
NOISE FIGURE vs. BASEBAND VGA GAIN SETTING



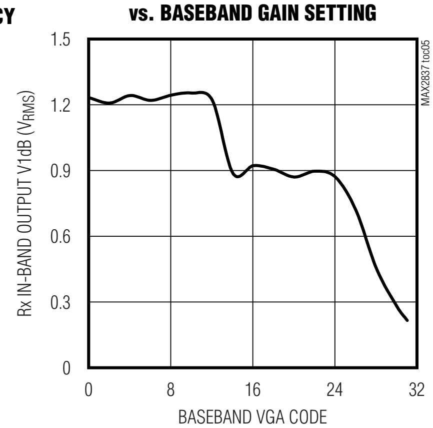
Rx VOLTAGE GAIN vs. BASEBAND GAIN SETTING



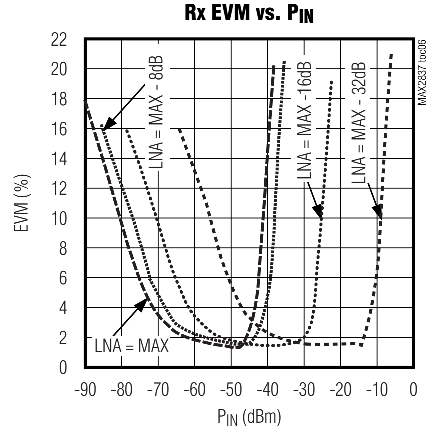
Rx VOLTAGE GAIN VARIATION vs. RF FREQUENCY



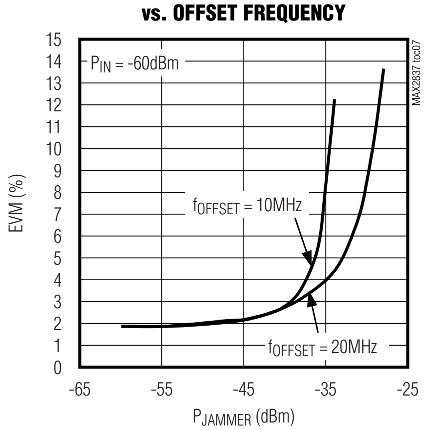
Rx IN-BAND OUTPUT V1dB vs. BASEBAND GAIN SETTING



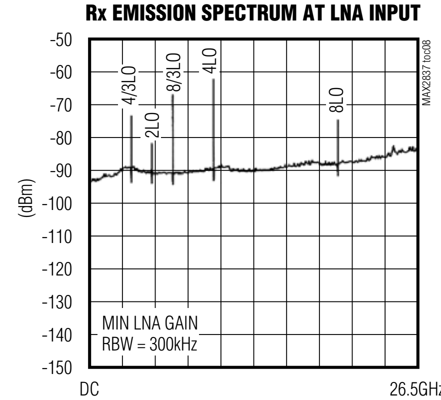
Rx EVM vs. P_{IN}



WiMAX EVM WITH OFDM JAMMER vs. OFFSET FREQUENCY



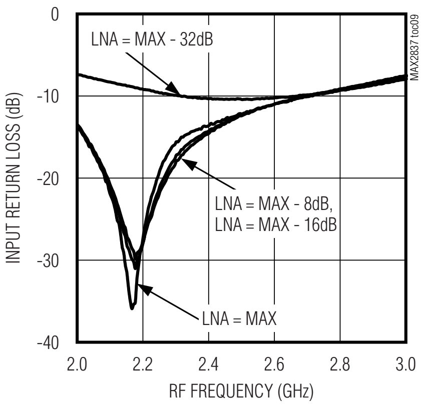
Rx EMISSION SPECTRUM AT LNA INPUT



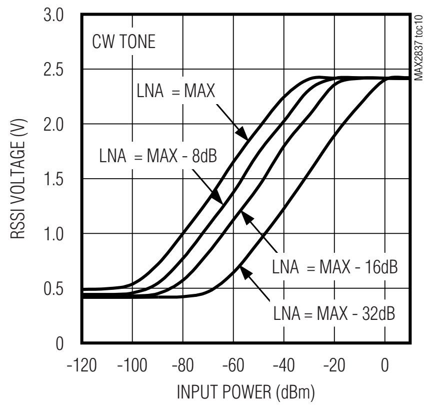
Typical Operating Characteristics (continued)

(MAX2837 evaluation kit: $V_{CC\_}$ = 2.8V, f_{LO} = 2.5GHz, 10MHz channel 16E UL/DL WiMax signal, f_{REF} = 40MHz, ENABLE = $\overline{CS}$ = high, RXHP = SCLK = DIN = low, T_A = +25°C, unless otherwise noted.)

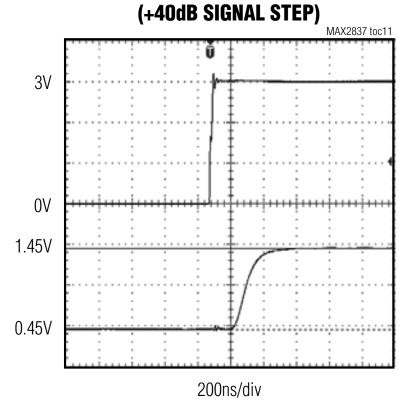
INPUT RETURN LOSS vs. RF FREQUENCY



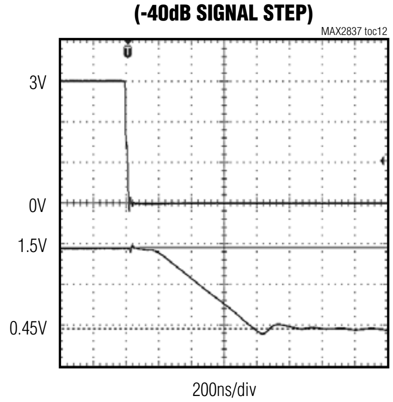
RSSI VOLTAGE vs. INPUT POWER



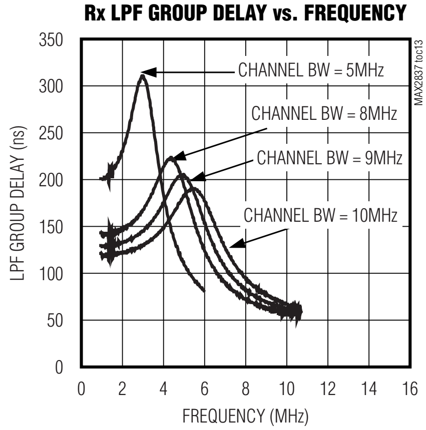
Rx RSSI STEP RESPONSE (+40dB SIGNAL STEP)



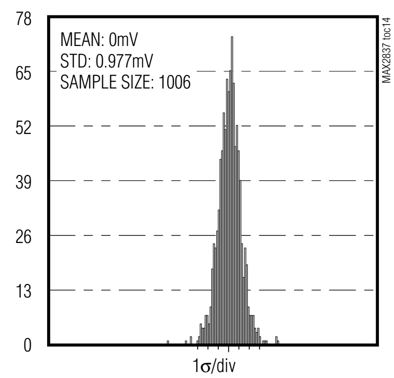
Rx RSSI STEP RESPONSE (-40dB SIGNAL STEP)



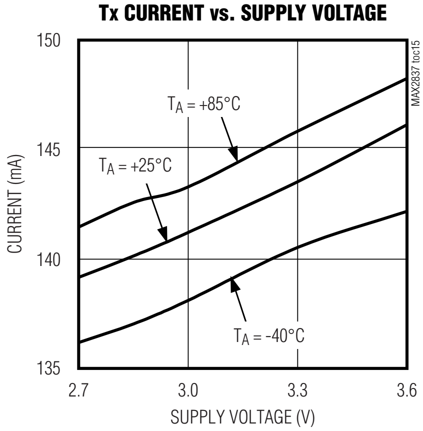
Rx LPF GROUP DELAY vs. FREQUENCY



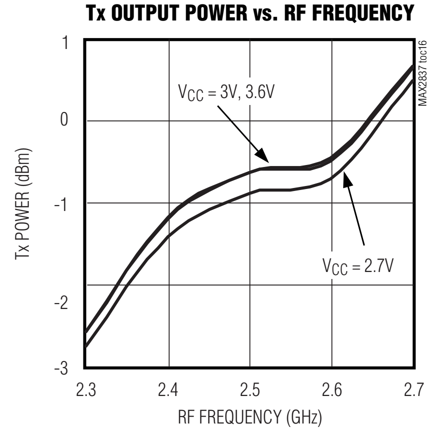
HISTOGRAM: Rx STATIC DC OFFSET



Tx CURRENT vs. SUPPLY VOLTAGE



Tx OUTPUT POWER vs. RF FREQUENCY

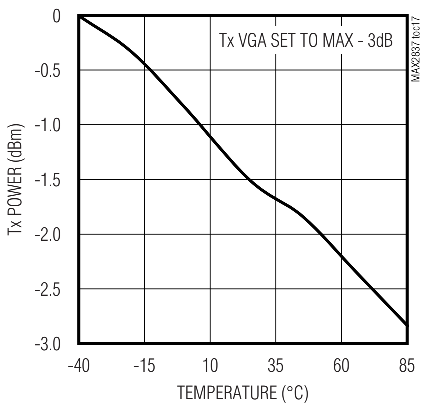


2.3GHz to 2.7GHz Wireless Broadband RF Transceiver

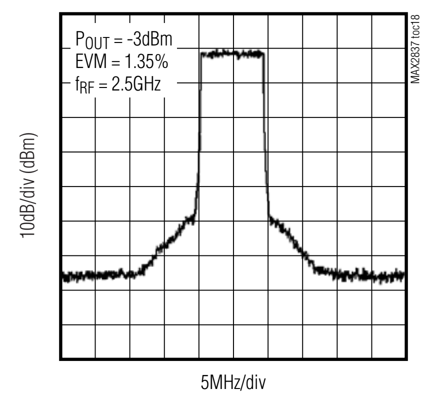
Typical Operating Characteristics (continued)

(MAX2837 evaluation kit: $V_{CC\_}$ = 2.8V, f_{LO} = 2.5GHz, 10MHz channel 16E UL/DL WiMax signal, f_{REF} = 40MHz, ENABLE = $\overline{CS}$ = high, RXHP = SCLK = DIN = low, T_A = +25°C, unless otherwise noted.)

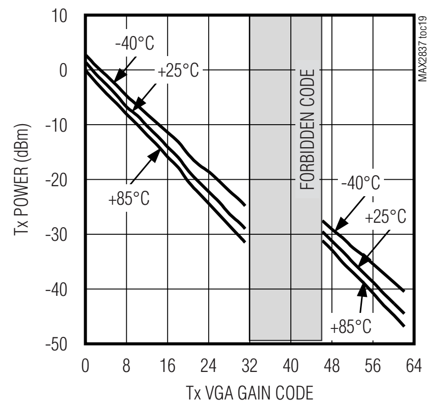
Tx OUTPUT POWER vs. TEMPERATURE



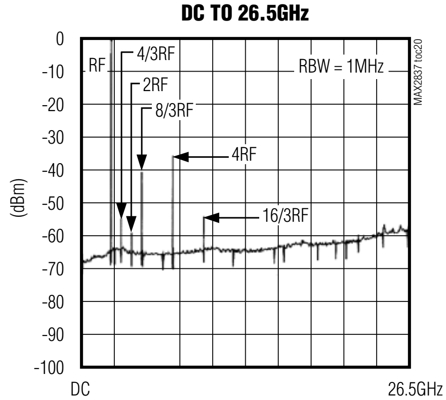
Tx OUTPUT SPECTRUM



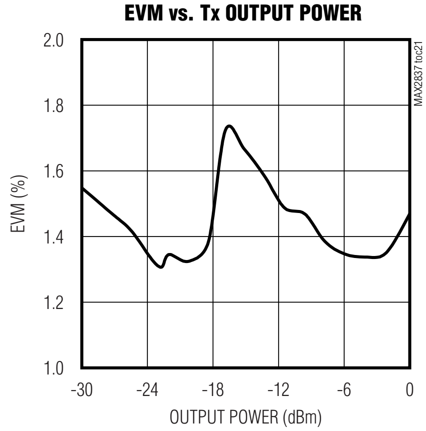
Tx POUT vs. GAIN SETTING



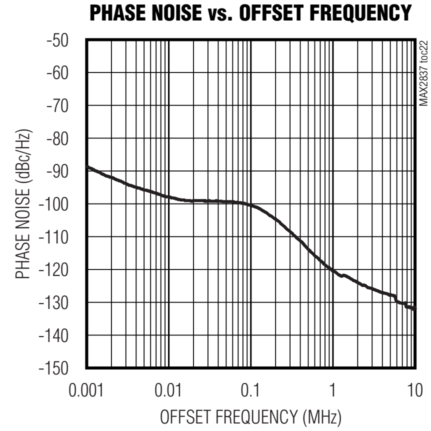
Tx TRANSMIT SPECTRUM FROM DC TO 26.5GHz



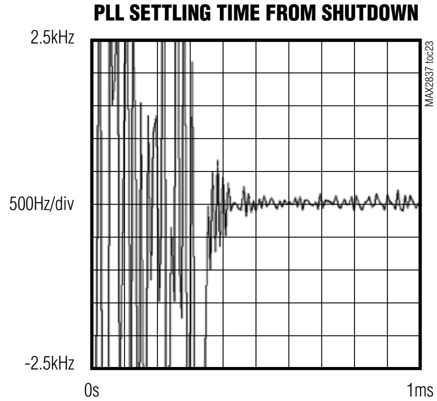
EVM vs. Tx OUTPUT POWER



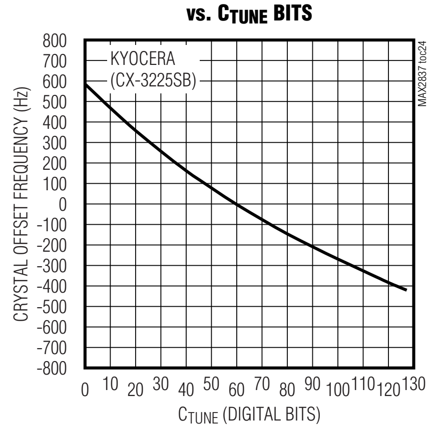
PHASE NOISE vs. OFFSET FREQUENCY



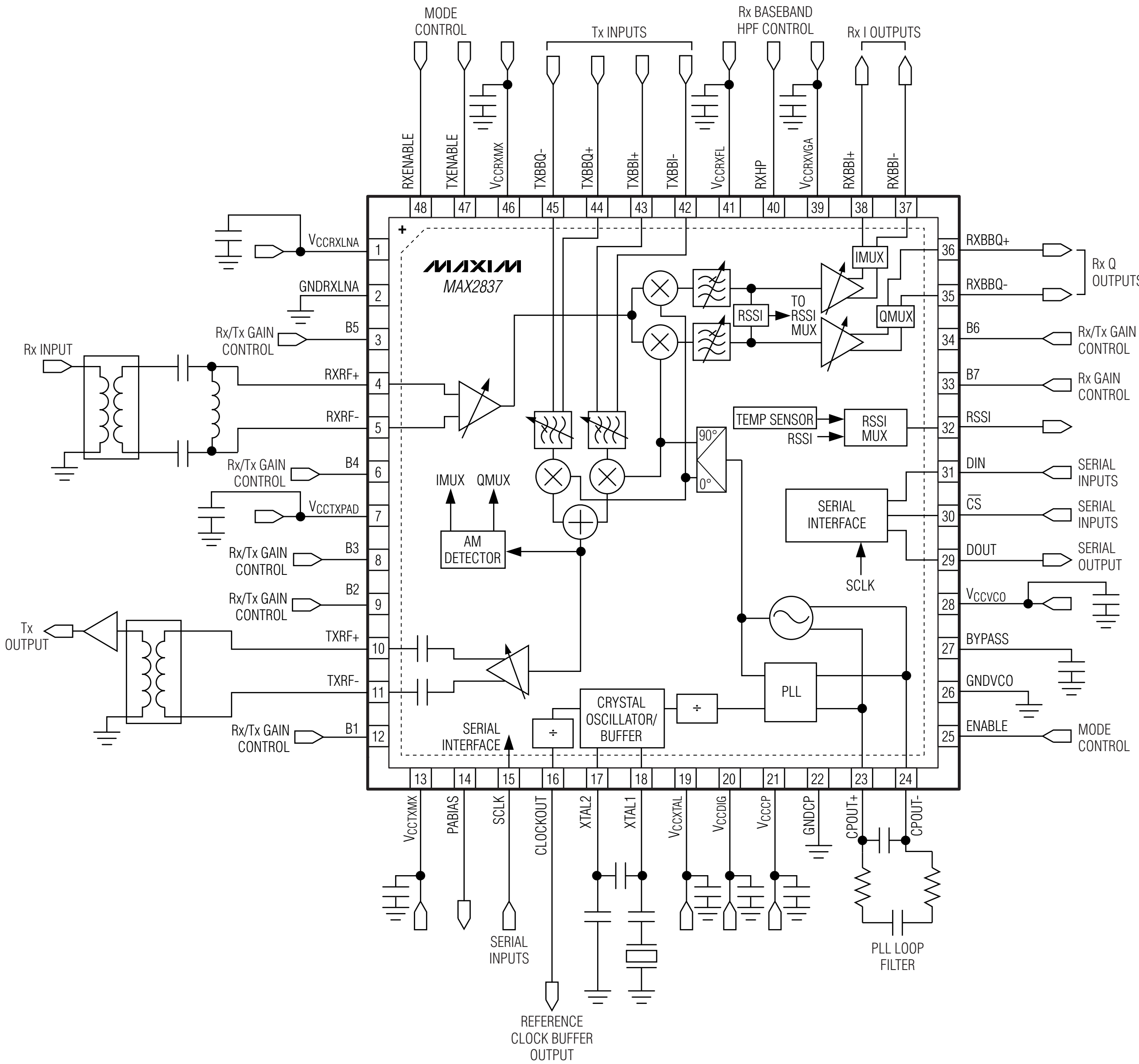
PLL SETTLING TIME FROM SHUTDOWN



CRYSTAL OFFSET FREQUENCY vs. C_{TUNE} BITS



Block Diagram/Typical Operating Circuit



2.3GHz to 2.7GHz Wireless Broadband RF Transceiver

Pin Description

PIN	NAME	FUNCTION
1	$V_{CCRXLNA}$	LNA Supply Voltage. Bypass with a capacitor as close as possible to the pin.
2	GNDRXLNA	LNA Ground
3	B5	Receiver and Transmitter Gain-Control Logic Input Bit 5
4	RXRF+	LNA Differential Inputs. Inputs are internally DC-coupled. An external shunt inductor and series capacitors match the inputs to 100Ω differential.
5	RXRF-	
6	B4	Receiver and Transmitter Gain-Control Logic Input Bit 4
7	$V_{CCTXPAD}$	Supply Voltage for Power-Amplifier Driver. Bypass with a capacitor as close as possible to the pin.
8	B3	Receiver and Transmitter Gain-Control Logic Input Bit 3
9	B2	Receiver and Transmitter Gain-Control Logic Input Bit 2
10	TXRF+	Power-Amplifier Driver Differential Output. PA driver output is internally matched to a 100Ω differential. The pins have internal DC-blocking capacitors.
11	TXRF-	
12	B1	Receiver and Transmitter Gain-Control Logic Input Bit 1
13	V_{CCTXMX}	Transmitter Upconverter Supply Voltage. Bypass with a capacitor as close as possible to the pin.
14	PABIAS	Transmit PA Bias DAC Output
15	SCLK	Serial-Clock Logic Input of 4-Wire Serial Interface (See Figure 1)
16	CLOCKOUT	Reference Clock Buffer Output
17	XTAL2	Crystal or Reference Clock Input. AC-couple a crystal or a reference clock to this analog input.
18	XTAL1	Connection for Crystal-Oscillator Off-Chip Capacitors. When using an external reference clock input, leave XTAL1 unconnected.
19	V_{CCXTAL}	Crystal-Oscillator Supply Voltage. Bypass with a capacitor as close as possible to the pin.
20	V_{CCDIG}	Digital Circuit Supply Voltage. Bypass with a capacitor as close as possible to the pin.
21	V_{CCCP}	PLL Charge-Pump Supply Voltage. Bypass with a capacitor as close as possible to the pin.
22	GNDCP	Charge-Pump Circuit Ground
23	CPOUT+	Differential Charge-Pump Output. Connect the frequency synthesizer's loop filter between CPOUT+ and CPOUT-. (See the *Typical Operating Circuit*.)
24	CPOUT-	
25	ENABLE	Operation Mode Logic Input. See Table 1 for operating modes.
26	GNDVCO	VCO Ground
27	BYPASS	On-Chip VCO Regulator Output Bypass. Bypass with a 1µF capacitor to GND. Do not connect other circuitry to this point.
28	V_{CCVCO}	VCO Supply Voltage. Bypass with a capacitor as close as possible to the pin.
29	DOUT	Data Logic Output of 4-Wire Serial Interface (See Figure 1)
30	$\overline{CS}$	Chip-Select Logic Input of 4-Wire Serial Interface (See Figure 1)
31	DIN	Data Logic Input of 4-Wire Serial Interface (See Figure 1)
32	RSSI	RSSI or Temperature Sensor Multiplexed Analog Output
33	B7	Receiver Gain-Control Logic Input Bit 7
34	B6	Receiver and Transmitter Gain-Control Logic Input Bit 6
35	RXBBQ-	Receiver Baseband Q-Channel Differential Outputs. In Tx calibration mode, these pins are the LO leakage and sideband detector outputs.
36	RXBBQ+	
37	RXBBI-	Receiver Baseband I-Channel Differential Outputs. In Tx calibration mode, these pins are the LO leakage and sideband detector outputs.
38	RXBBI+	
39	$V_{CCRXVGA}$	Receiver VGA Supply Voltage
40	RXHP	Receiver Baseband AC-Coupling Highpass Corner Frequency Control Logic Input
41	V_{CCRXFL}	Receiver Baseband Filter Supply Voltage

Pin Description (continued)

PIN	NAME	FUNCTION
42	TXBBI-	Transmitter Baseband I-Channel Differential Inputs
43	TXBBI+	
44	TXBBQ+	Transmitter Baseband Q-Channel Differential Inputs
45	TXBBQ-	
46	V_{CCRXMX}	Receiver Downconverters Supply Voltage. Bypass with a capacitor as close as possible to the pin.
47	TXENABLE	Tx Mode Control Logic Input. See Table 1 for operating modes.
48	RXENABLE	Rx Mode Control Logic Input. See Table 1 for operating modes.
EP	EP	Exposed Paddle. Connect to the ground plane with multiple vias for proper operation and heat dissipation. Do not share with any other pin grounds and bypass capacitors' ground.

Table 1. Operating Mode Table

MODE	LOGIC PINS			REGISTER SETTING		CIRCUIT BLOCK STATES				
	ENABLE	RXENABLE	TXENABLE	D1:D0 A4:A0 = 10000		Rx PATH	Tx PATH	PLL, VCO, LO GEN	CALIBRATION SECTIONS ON	CLOCK OUT
Clock-Out	1	0	0	0	0	Off	Off	Off	None	On
Shutdown	0	0	0	0	X	Off	Off	Off	None	Off
Standby	1	0	0	0	1	Off*	Off*	On	None	On
Rx	1	1	0	0	1	On	Off	On	None	On
Tx	1	0	1	0	1	Off	On	On	None	On
Rx Calibration	1	1	0	1	1	On (Except LNA)	Off (Except Upconverters)	On	Tx Baseband Buffer	On
Tx Calibration	1	0	1	1	1	Off	On (Except PA Driver)	On	AM Detector, Rx I/Q Buffers	On

*Blocks of the transceiver can be selectively enabled through SPI.

Detailed Description

Modes of Operation

The modes of operation for the MAX2837 are clock-out, shutdown, transmit, receive, transmitter calibration, and receiver calibration. See Table 1 for a summary of the modes of operation. The logic input pins—ENABLE (pin 25), TXENABLE (pin 47), and RXENABLE (pin 48)—control the various modes. When the parts are active, various blocks can be shut down individually through SPI.

Shutdown Mode

The MAX2837 features a low-power shutdown mode. Current drain is the minimum possible with the supply voltages applied. In shutdown mode, all circuit blocks are powered down, except the 4-wire serial bus and its internal programmable registers. If the supply voltage is applied, the registers are loaded and retained.

Standby Mode

The standby mode is used to enable the frequency synthesizer block while the rest of the device is powered down. In this mode, PLL, VCO, and LO generator are on, so that Tx or Rx modes can be quickly enabled from this mode. These and other blocks can be selectively enabled in this mode.

Receive (Rx) Mode

In receive mode, all Rx circuit blocks are powered on and active. Antenna signal is applied; RF is downconverted, filtered, and buffered at Rx BB I and Q outputs. The slow-charging Tx circuits are in a precharged "idle-off" state for fast Rx-to-Tx turnaround time.

Transmit (Tx) Mode

In transmit mode, all Tx circuit blocks are powered on. The external PA is powered on after a programmable

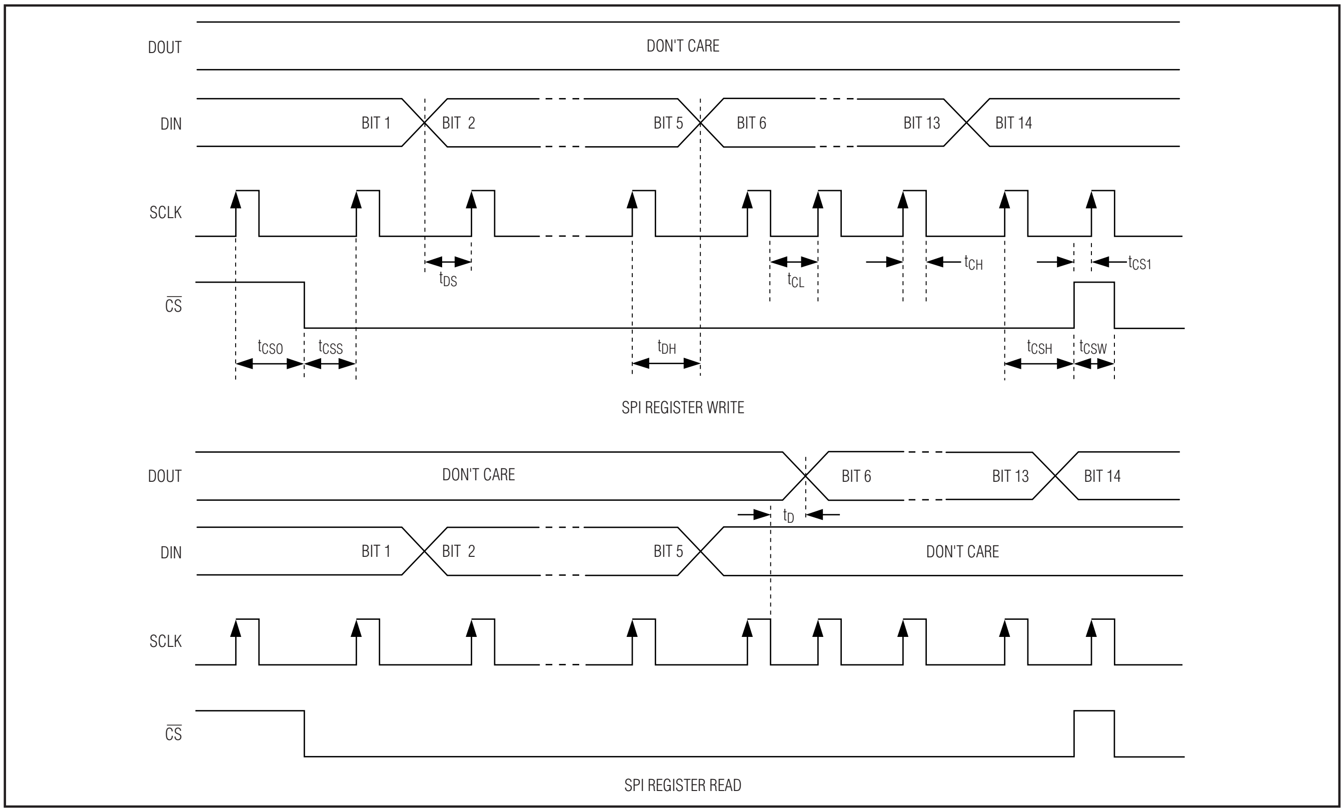


Figure 1. 4-Wire SPI Serial-Interface Timing Diagram

delay using the on-chip PA bias DAC. The slow-charging Rx circuits are in a precharged "idle-off" state for fast Tx-to-Rx turnaround time.

Clock-Out Only

In clock-out mode, the entire transceiver is off except the divided reference clock output on the CLKOUT pin and the clock divider, which remains on.

Programmable Registers and 4-Wire SPI Interface

The MAX2837 includes 32 programmable 16-bit registers. The most significant bit (MSB) is the read/write selection bit. The next 5 bits are register address. The 10 least significant bits (LSBs) are register data. Register data is loaded through the 4-wire SPI/MICROWIRE™-compatible serial interface. Data at DIN is shifted in MSB first and is framed by $\overline{CS}$. When $\overline{CS}$ is low, the clock is active, and input data is shifted at the rising edge of the clock. During the read mode, register data selected by address bits is shifted out to DOUT at the falling edges of the clock. At the $\overline{CS}$ rising edge, the 10-bit data bits are latched into the register selected by address bits. See Figure 1. The register values are preserved in shutdown mode as long as the power-supply voltage is maintained. However, every time the power-supply voltage is turned on, the registers are reset to the default values. Note that default register states are not guaranteed, and the user should always reprogram all registers after power-up.

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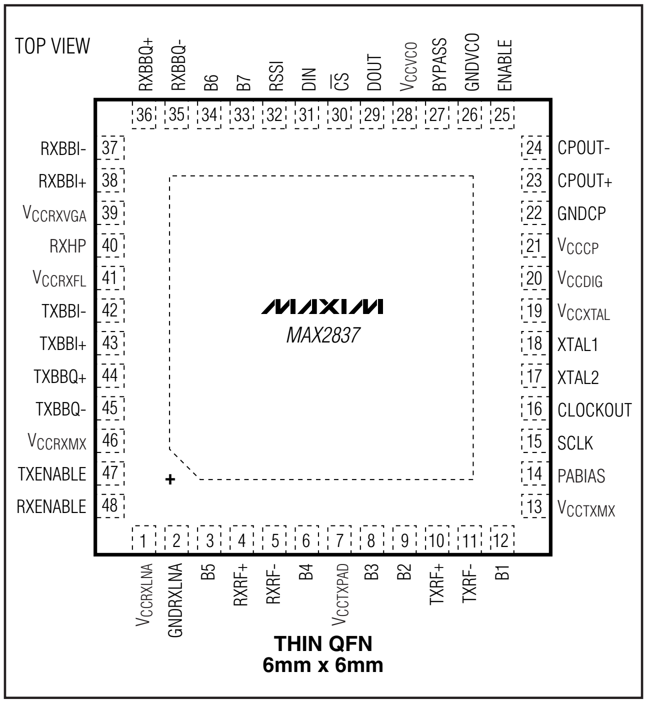
Pin Configuration



Chip Information

PROCESS: SiGe BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
48 TQFN-EP	T4866-2	21-0141

MAX2837

2.3GHz to 2.7GHz Wireless Broadband RF Transceiver

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	5/07	Initial release	—
1	11/08	Corrected SPI description in *Programmable Registers and 4-Wire SPI-Interface* section	16