

LM117QML

3-Terminal Adjustable Regulator

General Description

The LM117 series of adjustable 3-terminal positive voltage regulators is capable of supplying either 0.5A or 1.5A over a 1.2V to 37V output range. They are exceptionally easy to use and require only two external resistors to set the output voltage. Further, both line and load regulation are better than standard fixed regulators.

In addition to higher performance than fixed regulators, the LM117 series offers full overload protection available only in IC's. Included on the chip are current limit, thermal overload protection and safe area protection. All overload protection circuitry remains fully functional even if the adjustment terminal is disconnected.

Normally, no capacitors are needed unless the device is situated more than 6 inches from the input filter capacitors in which case an input bypass is needed. An optional output capacitor can be added to improve transient response. The adjustment terminal can be bypassed to achieve very high ripple rejection ratios which are difficult to achieve with standard 3-terminal regulators.

Besides replacing fixed regulators, the LM117 is useful in a wide variety of other applications. Since the regulator is "floating" and sees only the input-to-output differential voltage,

supplies of several hundred volts can be regulated as long as the maximum input to output differential is not exceeded, i.e., avoid short-circuiting the output.

Also, it makes an especially simple adjustable switching regulator, a programmable output regulator, or by connecting a fixed resistor between the adjustment pin and output, the LM117 can be used as a precision current regulator. Supplies with electronic shutdown can be achieved by clamping the adjustment terminal to ground which programs the output to 1.2V where most loads draw little current.

For the negative complement, see LM137 series data sheet.

Features

- Available with Radiation Guarantee
 - High Dose Rate

100 krad(Si)

— ELDRS Free

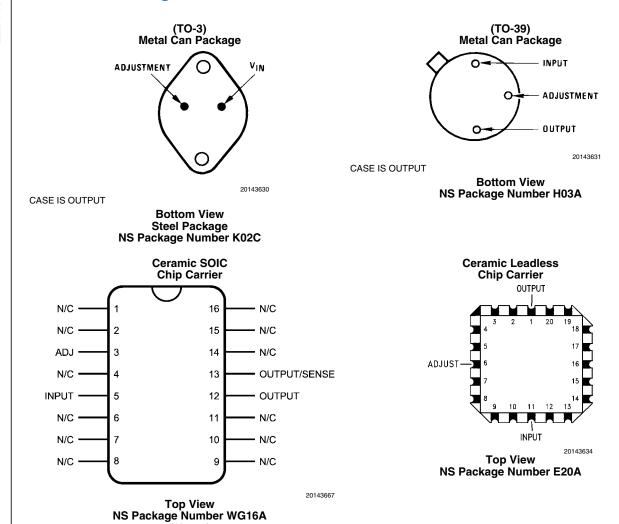
- 100 krad(Si)
- Guaranteed max. 0.3% load regulation (LM117)
- Guaranteed 0.5A or 1.5A output current
- Adjustable output down to 1.2V
- Current limit constant with temperature
- 80 dB ripple rejection
- Output is short-circuit protected

Ordering Information

NS Part Number	SMD Part Number	NS Package Number	Package Description
LM117E/883		E20A	20LD LCC
LM117H/883		H03A	3LD T0-39 Metal Can
LM117HRQMLV (Note 12)	5962R9951703VXA 100 krad(Si)	H03A	3LD T0-39 Metal Can
LM117HRLQMLV (<i>Note 13</i>) ELDRS Free	5962R9951705VXA 100 krad(Si)	H03A	3LD T0-39 Metal Can
LM117K/883		K02C	2LD T0-3 Metal Can
LM117KRQMLV (<i>Note 12</i>)	5962R9951704VYA 100 krad(Si)	K02C	2LD T0-3 Metal Can
LM117WGRQMLV (Note 12)	5962R9951703VZA 100 krad(Si)	WG16A	16LD Ceramic SOIC
LM117WGRLQMLV (<i>Note 13</i>) ELDRS Free	5962R9951705VZA 100 krad(Si)	WG16A	16LD Ceramic SOIC
LM117H MDE (<i>Note 13</i>) ELDRS Free	5962R9951705V9A 100 krad(Si)	(Note 1)	Bare Die
LM117H MDR (<i>Note 12</i>)	5962R9951703V9A 100 krad(Si)	(Note 1)	Bare Die
LM117H MD8		(Note 1)	Bare Die
LM117KG MD8		(Note 1)	Bare Die

Note 1: FOR ADDITIONAL DIE INFORMATION, PLEASE VISIT THE HI REL WEB SITE AT: www.national.com/analog/space/level_die

Connection Diagrams

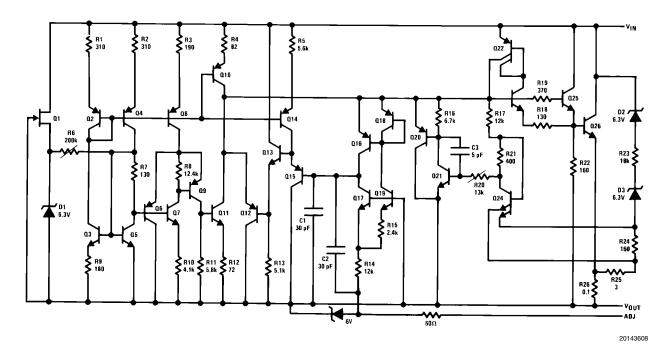


LM117 Series Packages

(Note 5)

Part		Design
Number	Package	Load
Suffix		Current
K	TO-3	1.5A
Н	T0–39	0.5A
WG	Ceramic SOIC	0.5A
E	LCC	0.5A

Schematic Diagram



Absolute Maximum Ratings (Note 2)

Power Dissipation (Note 3) Internally Limited Input-Output Voltage Differential +40V, -0.3V Storage Temperature $-65^{\circ}\text{C} \le \text{T}_{\text{A}} \le +150^{\circ}\text{C}$ Maximum Junction Temperature (T_{Jmax} +150°C Lead Temperature Metal Package 300°C Thermal Resistance θ_{JA} T0-3 Still Air 39°C/W T0-3 500LF/Min Air flow 14°C/W T0-39 Still Air 186°C/W T0-39 500LF/Min Air flow 64°C/W Ceramic SOIC Still Air 115°C/W Ceramic SOIC 500LF/Min Air flow 66°C/W LCC Still Air 88°C/W LCC 500LF/Min Air flow 62°C/W θ_{JC} T0-3 1.9°C/W T0-39 Metal Can 21°C/W Ceramic SOIC (Note 6) 3.4°C/W LCC 12°C/W Package Weight T0-39 Metal Can 960mg SOIC 365mg ESD Tolerance (Note 4) 3KV

Recommended Operating Conditions

Operating Temperature Range $-55^{\circ}\text{C} \le \text{T}_{\text{A}} \le +125^{\circ}\text{C}$ Input Voltage Range 4.25V to 41.25V

Quality Conformance Inspection

MIL-STD-883, Method 5005 - Group A

Subgroup	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55
12	Settling time at	+25
13	Settling time at	+125
14	Settling time at	-55

LM117H & WG Electrical Characteristics

DC Parameters

The following conditions apply, unless otherwise specified. $V_{Diff} = (V_I - V_O), I_L = 8mA$

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub- groups
		$V_{Diff} = 3V$			100	μA	1
I_{Adj}	Adjustment Pin Current	$V_{Diff} = 3.3V$			100	μΑ	2, 3
		$V_{Diff} = 40V$			100	μΑ	1, 2, 3
		$V_{Diff} = 3V, V_O = 1.7V$			5.0	mA	1
I_Q	Minimum Load Current	$V_{Diff} = 3.3V, V_{O} = 1.7V$			5.0	mA	2, 3
		$V_{Diff} = 40V, V_{O} = 1.7V$			5.0	mA	1, 2, 3
		$V_{Diff} = 3V$		1.2	1.3	٧	1
V_{Ref}	Reference Voltage	$V_{Diff} = 3.3V$		1.2	1.3	٧	2, 3
		$V_{Diff} = 40V$		1.2	1.3	٧	1, 2, 3
W	Line Book Line	$3V \le V_{Diff} \le 40V,$ $V_{O} = 1.2V$		-8.9	8.9	mV	1
V _{RLine}	Line Regulation	$3.3V \le V_{Diff} \le 40V,$ $V_{O} = 1.2V$		-22.2	22.2	mV	2, 3
	Load Regulation	V _{Diff} = 3V, I _L = 10mA to 500mA		-15	15	mV	1
V		V _{Diff} = 3.3V, I _L = 10mA to 500mA		-15	15	mV	2, 3
V _{RLoad}		V _{Diff} = 40V, I _L = 10mA to 150mA		-15	15	mV	1
		V_{Diff} = 40V, I_L = 10mA to 100mA		-15	15	mV	2, 3
		$V_{Diff} = 3V$, $I_L = 10$ mA to 500mA		-5.0	5.0	μΑ	1
Al /lood	Adjusted and Comment Change	$V_{Diff} = 3.3V$, $I_L = 10$ mA to 500mA		-5.0	5.0	μΑ	2, 3
Δi _{Adj} / Load	Adjustment Current Change	$V_{Diff} = 40V$, $I_L = 10mA$ to 150mA		-5.0	5.0	μΑ	1
		$V_{Diff} = 40V$, $I_L = 10mA$ to $100mA$		-5.0	5.0	μΑ	2, 3
A1 /1:	A discrete and Occurrent Observan	$3V \le V_{Diff} \le 40V$		-5.0	5.0	μΑ	1
ΔI_{Adj} / Line	Adjustment Current Change	$3.3V \le V_{Diff} \le 40V$		-5.0	5.0	μA	2, 3
I _{os}	Short Circuit Current	V _{Diff} = 10V		0.45	1.6	Α	1
θ_{R}	Thermal Regulation	$T_A = 25$ °C, $t = 20$ mS, $V_{Diff} = 40$ V, $I_L = 150$ mA		-6.0	6.0	mV	1
	O	V _{Diff} ≤ 15V	(Note 7)	0.5		Α	1, 2, 3
I _{CL}	Current Limit	$V_{\text{Diff}} = 40V$	(Note 7)	0.15		Α	1

AC Parameters

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub- groups
RR		$V_{l} = +6.25V, V_{O} = V_{Ref},$ $f = 120Hz, e_{l} = 1V_{RMS},$ $I_{L} = 125mA$	(Note 8)	66		dB	4, 5, 6
			•				

LM117K Electrical Characteristics

DC Parameters

The following conditions apply, unless otherwise specified. $V_{Diff} = (V_I - V_O), I_L = 10 \text{mA}$

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub- groups
		V _{Diff} = 3V			100	μA	1
I_{Adj}	Adjustment Pin Current	$V_{Diff} = 3.3V$			100	μΑ	2, 3
		$V_{Diff} = 40V$			100	μΑ	1, 2, 3
		$V_{Diff} = 3V, V_O = 1.7V$			5.0	mA	1
I_Q	Minimum Load Current	$V_{Diff} = 3.3V, V_{O} = 1.7V$			5.0	mA	2, 3
		$V_{Diff} = 40V, V_{O} = 1.7V$			5.0	mA	1, 2, 3
		$V_{Diff} = 3V$		1.2	1.3	V	1
V_{Ref}	Reference Voltage	$V_{Diff} = 3.3V$		1.2	1.3	٧	2, 3
		$V_{Diff} = 40V$		1.2	1.3	٧	1, 2, 3
V	Line Deculation	$3V \le V_{Diff} \le 40V$, $V_O = 1.2V$		-8.9	8.9	mV	1
V _{RLine}	Line Regulation	$3.3V \le V_{Diff} \le 40V,$ $V_{O} = 1.2V$		-22.2	22.2	mV	2, 3
	Load Regulation	$V_{\text{Diff}} = 3V$, $I_{\text{L}} = 10\text{mA}$ to 1.5A		-15	15	mV	1
V		V_{Diff} = 3.3V, I_L = 10mA to 1.5A		-15	15	mV	2, 3
V_{RLoad}		$V_{Diff} = 40V$, $I_{L} = 10mA$ to 300mA		-15	15	mV	1
		$V_{Diff} = 40V$, $I_{L} = 10mA$ to 195mA		-15	15	mV	2, 3
		$V_{Diff} = 3V$, $I_{L} = 10mA$ to 1.5A		-5.0	5.0	μΑ	1
Al /Lood	Adjustment Current Change	$V_{Diff} = 3.3V$, $I_L = 10mA$ to 1.5A		-5.0	5.0	μΑ	2, 3
Δι _{Adj} / Load	Adjustment Current Change	$V_{Diff} = 40V$, $I_L = 10mA$ to 300mA		-5.0	5.0	μΑ	1
		$V_{Diff} = 40V$, $I_L = 10mA$ to 195mA		-5.0	5.0	μΑ	2, 3
A		$3V \le V_{Diff} \le 40V$		-5.0	5.0	μΑ	1
ΔI_{Adj} / Line	Adjustment Current Change	3.3V ≤ V _{Diff} ≤ 40V		-5.0	5.0	μA	2, 3
I _{os}	Short Circuit Current	$V_{\text{Diff}} = 10V$		1.6	3.4	Α	1
θ_{R}	Thermal Regulation	$T_A = 25^{\circ}C$, $t = 20mS$, $V_{Diff} = 40V$, $I_L = 300mA$		-10.5	10.5	mV	1
	0	V _{Diff} ≤ 15V	(Note 7)	1.5		Α	1, 2, 3
I _{CL}	Current Limit	$V_{\text{Diff}} = 40V$	(Note 7)	0.3		Α	1

AC Parameters

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub- groups
RR	Ripple Rejection	$V_{\rm I} = +6.25 \text{V}, V_{\rm O} = V_{\rm Ref},$ $f = 120 \text{Hz}, e_{\rm I} = 1 V_{\rm RMS},$ $I_{\rm L} = 0.5 \text{A}$	(Note 8)	66		dB	4, 5, 6

LM117E Electrical Characteristics

DC Parameters

The following conditions apply, unless otherwise specified. $V_{Diff} = (V_I - V_O), I_L = 8mA, P_D \le 1.5W$

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub- groups
		V _{Diff} = 3V			100	μΑ	1
I_{Adj}	Adjustment Pin Current	$V_{Diff} = 3.3V$			100	μΑ	2, 3
		$V_{\text{Diff}} = 40V$			100	μΑ	1, 2, 3
		$V_{Diff} = 3V, V_{O} = 1.7V$			5.0	mA	1
I_Q	Minimum Load Current	$V_{Diff} = 3.3V, V_{O} = 1.7V$			5.0	mA	2, 3
		$V_{Diff} = 40V, V_{O} = 1.7V$			5.0	mA	1, 2, 3
		V _{Diff} = 3V		1.2	1.3	V	1
V_{Ref}	Reference Voltage	$V_{\text{Diff}} = 3.3V$		1.2	1.3	V	2, 3
		V _{Diff} = 40V		1.2	1.3	V	1, 2, 3
V	Line Regulation	$3V \le V_{Diff} \le 40V,$ $V_{O} = 1.2V$		-8.9	8.9	mV	1
V _{RLine}	Line negulation	$3.3V \le V_{Diff} \le 40V$, $V_O = 1.2V$		-22.2	22.2	mV	2, 3
		V _{Diff} = 3V, I _L = 10mA to 100mA		-15	15	mV	1
	Load Regulation	V_{Diff} = 3.3V, I_L = 10mA to 100mA		-15	15	mV	2, 3
V _{RLoad}		V _{Diff} = 40V,		-15	15	mV	1,2
* RLoad		I _L = 10mA to 100mA		-25	25	mV	3
		V_{Diff} = 3V, I_L = 10mA to 500mA		-15	15	mV	1
		V_{Diff} = 3.3V, I_{L} = 10mA to 500mA		-15	15	mV	2, 3
		$V_{Diff} = 3V$, $I_L = 10mA$ to 500mA		-5.0	5.0	μΑ	1
ΔI_{Adj} / Load	Adjustment Current Change	$V_{Diff} = 3.3V$, $I_L = 10$ mA to 500mA		-5.0	5.0	μΑ	2, 3
		$V_{Diff} = 40V$, $I_L = 10mA$ to 100mA		-5.0	5.0	μΑ	1, 2, 3
A1 /11	A l'adam de Cara de Characa	$3V \le V_{Diff} \le 40V$		-5.0	5.0	μΑ	1
ΔI _{Adj} / Line	Adjustment Current Change	3.3V ≤ V _{Diff} ≤ 40V		-5.0	5.0	μA	2, 3
I _{os}	Short Circuit Current	V _{Diff} = 10V		0.45	1.6	Α	1
θ_{R}	Thermal Regulation	$T_A = 25^{\circ}C$, $t = 20mS$, $V_{Diff} = 40V$, $I_L = 75mA$		-6.0	6.0	mV	1
	Course at Limit	V _{Diff} ≤ 15V	(Note 7)	0.5		Α	1, 2, 3
I _{CL}	Current Limit	V _{Diff} = 40V	(Note 7)	0.15		Α	1

AC Parameters

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub- groups
RR	Ripple Rejection	$V_{I} = +6.25V, V_{O} = V_{Ref},$ $f = 120Hz, e_{I} = 1V_{RMS},$ $I_{L} = 100mA, C_{Adj} = 10\mu f$	(Note 8)	66		dB	4, 5, 6
		E Auj I					

LM117H & WG RH Electrical Characteristics

DC Parameters (Note 12, Note 13)

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub- groups
		V _I = 4.25V, I _L = -5mA		1.2	1.3	V	1, 2, 3
V	Output Voltage	V _I = 4.25V, I _L = -500mA		1.2	1.3	V	1, 2, 3
V _O		V _I = 41.25V, I _L = -5mA		1.2	1.3	V	1, 2, 3
		V _I = 41.25V, I _L = -50mA		1.2	1.3	V	1, 2, 3
V	Line Deculation	$4.25V \le V_1 \le 41.25V$,		-9.0	9.0	mV	1
V _{RLine}	Line Regulation	$I_L = -5mA$		-23	23	mV	2,3
V	Lood Dogwletics	$V_{I} = 6.25V,$ -500mA \le I_{L} \le -5mA		-12	12	mV	1, 2, 3
V_{RLoad}	Load Regulation	$V_{I} = 41.25V,$ -50mA \le I _L \le -5mA		-12	12	mV	1, 2, 3
V _{RTh}	Thermal Regulation	V _I = 14.6V, I _L = -500mA		-12	12	mV	1
1	Adiust Din Current	V _I = 4.25V, I _L = -5mA		-100	-15	μA	1, 2, 3
l _{Adj}	Adjust Pin Current	V _I = 41.25V, I _L = -5mA		-100	-15	μA	1, 2, 3
ΔI _{Adj} / Line	Adjust Pin Current Change	$4.25V \le V_1 \le 41.25V$, $I_L = -5mA$		-5.0	5.0	μΑ	1, 2, 3
ΔI _{Adj} / Load	Adjust Pin Current Change	$V_{I} = 6.25V,$ -500mA \leq I_{L} \leq -5mA		-5.0	5.0	μΑ	1, 2, 3
		$V_1 = 4.25V$, Forced $V_0 = 1.4V$		-3.0	-0.5	mA	1, 2, 3
I_Q	Minimum Load Current	$V_{I} = 14.25V,$ Forced $V_{O} = 1.4V$		-3.0	-0.5	mA	1, 2, 3
		$V_I = 41.25V$, Forced $V_O = 1.4V$		-5.0	-1.0	mA	1, 2, 3
I _{os}	Output Short Circuit Current	$V_1 = 4.25V$		-1.8	-0.5	Α	1, 2, 3
'os	Output Short Circuit Current	V _I = 40V		-0.5	-0.05	Α	1, 2, 3
V _O (Recov)	Output Voltage Recovery	$V_{I} = 4.25V, R_{L} = 2.5\Omega,$ $C_{L} = 20\mu F$		1.2	1.3	V	1, 2, 3
		$V_{I} = 40V, R_{L} = 250\Omega$		1.2	1.3	V	1, 2, 3
V _O	Output Voltage	$V_{I} = 6.25V, I_{L} = -5mA$	(Note 9)	1.2	1.3	V	2
V _{Start}	Voltage Start-Up	$V_{I} = 4.25V, R_{L} = 2.5\Omega,$ $C_{L} = 20\mu F, I_{L} = -500mA$		1.2	1.3	V	1, 2, 3

AC Parameters (Note 12, Note 13)

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub -
							groups
V _{NO}	Output Noise Voltage	$V_1 = 6.25V, I_L = -50mA$			120	μV_{RMS}	7
$\Delta V_{O} / \Delta V_{I}$	Line Transient Response	$V_{I} = 6.25V, \Delta V_{I} = 3V,$ $I_{L} = -10mA$			6.0	mV/V	7
ΔV _O / ΔΙ _L	Load Transient Response	$V_{l} = 6.25V, \Delta I_{L} = -200mA,$ $I_{L} = -50mA$			0.6	mV/mA	7
$\Delta V_{I} / \Delta V_{O}$	Ripple Rejection	$V_{I} = 6.25V, I_{L} = -125mA,$ $E_{I} = 1V_{RMS}$ at $f = 2400Hz$		65		dB	4

DC Drift Parameters

The following conditions apply, unless otherwise specified.

Deltas performed on QMLV devices at Group B, Subgroup 5, only.

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-
							groups
		$V_{I} = 4.25V, I_{L} = -5mA$		-0.01	0.01	V	1
V	Output Voltage	$V_{I} = 4.25V, I_{L} = -500mA$		-0.01	0.01	V	1
V _O	Output Voltage	$V_{I} = 41.25V, I_{L} = -5mA$		-0.01	0.01	V	1
		$V_{I} = 41.25V, I_{L} = -50mA$		-0.01	0.01	V	1
V _{RLine}	Line Regulation	$4.25V \le V_1 \le 41.25V$, $I_L = -5mA$		-4.0	4.0	mV	1
I _{Adj}	Adjust Pin Current	$V_{I} = 4.25V, I_{L} = -5mA$		-10	10	μΑ	1
		$V_{I} = 41.25V, I_{L} = -5mA$		-10	10	μΑ	1
V _O (Recov)	Output Voltage Recovery	$V_I = 4.25V, R_L = 2.5\Omega,$ $C_L = 20\mu f$		-0.01	0.01	V	1
		$V_{I} = 40V, R_{L} = 250\Omega$		-0.01	0.01	V	1

AC/DC Post Radiation Limits @ +25°C (Note 12, Note 13)

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-
							groups
		$V_{I} = 4.25V, I_{L} = -5mA$		1.2	1.350	V	1
V	Output Valtage	$V_{I} = 4.25V, I_{L} = -500mA$		1.2	1.350	V	1
V _O	Output Voltage	$V_{I} = 41.25V, I_{L} = -5mA$		1.2	1.350	V	1
		$V_{I} = 41.25V, I_{L} = -50mA$		1.2	1.350	V	1
V _{RLine}	Line Regulation	$4.25V \le V_1 \le 41.25V$,		-25	25	mV	1
* RLine	Line riegulation	$I_L = -5mA$					
$\Delta V_1 / \Delta V_0$	Ripple Rejection	$V_{I} = 6.25V, I_{L} = -125mA$		60	60	dB	4
ΔV ₁ /ΔV ₀	Thippie Hejection	$E_I = 1V_{RMS}$ at $f = 2400Hz$		60			
V _O (Recov)		$V_{l} = 4.25V, R_{L} = 2.5\Omega,$		1.20	1.350	V	4
	Output Voltage Recovery	$C_L = 20\mu f$		1.20	1.330	٧	<u> </u>
		$V_{I} = 40V, R_{L} = 250\Omega$		1.20	1.350	V	1

LM117K RH Electrical Characteristics

DC Parameters (Note 12)

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub- groups
		V _I = 4.25V, I _L = -5mA		1.2	1.3	V	1, 2, 3
M	Output Valtage	V _I = 4.25V, I _L = -1.5A		1.2	1.2 1.3 1.2 1.3 1.2 1.3 1.2 1.3 -9.0 9.0 -23 23 -3.5 3.5 -12 12 -3.5 3.5 -12 12 -12 12 -100 -15	٧	1, 2, 3
V _o	Output Voltage	V _I = 41.25V, I _L = -5mA		1.2		٧	1, 2, 3
		V _I = 41.25V, I _L = -200mA		1.2	1.3	V	1, 2, 3
V	Line Regulation	$4.25V \le V_1 \le 41.25V$,		-9.0	9.0	mV	1
V _{RLine}	Line negulation	$I_L = -5mA$		-23	23	mV	2,3
		$V_1 = 6.25V,$		-3.5	3.5	mV	1
V	Load Regulation	-1.5A ≤ I _L ≤ -5mA		-12	12	mV	2, 3
V_{RLoad}	Load Regulation	V _I = 41.25V,		-3.5	3.5	mV	1
		-200mA ≤ I _L ≤ -5 mA		-12	12	mV	2, 3
V_{RTh}	Thermal Regulation	$V_{I} = 14.6V, I_{L} = -1.5A$		-12	12	mV	1
1	Adjust Din Current	$V_{I} = 4.25V, I_{L} = -5mA$		-100	-15	μA	1, 2, 3
l _{Adj}	Adjust Pin Current	V _I = 41.25V, I _L = -5mA		-100	-15	μA	1, 2, 3
ΔI _{Adj} / Line	Adjust Pin Current Change	$4.25V \le V_1 \le 41.25V$, $I_L = -5mA$		-5.0	5.0	μΑ	1, 2, 3
ΔI _{Adj} / Load	Adjust Pin Current Change	$V_{I} = 6.25V,$ -1.5A \le I_{L} \le -5mA		-5.0	5.0	μΑ	1, 2, 3
		$V_I = 4.25V$, Forced $V_O = 1.4V$		-3.0	-0.2	mA	1, 2, 3
Ι _Q	Minimum Load Current	V _I = 14.25V, Forced V _O = 1.4V		-3.0	-0.2	mA	1, 2, 3
		$V_I = 41.25V$, Forced $V_O = 1.4V$		-5.0	-0.2	mA	1, 2, 3
1	Output Short Circuit Current	$V_1 = 4.25V$		-3.5	-1.5	Α	1, 2, 3
l _{os}	Output Short Circuit Current	V _I = 40V		-1.0	-0.18	Α	1, 2, 3
V _O (Recov)	Output Voltage Recovery	$V_I = 4.25V, R_L = 0.833\Omega,$ $C_L = 20\mu F$		1.2	1.3	V	1, 2, 3
		$V_{l} = 40V, R_{L} = 250\Omega$		1.2	1.3	V	1, 2, 3
$\overline{V_0}$	Output Voltage	$V_{l} = 6.25V, I_{L} = -5mA$	(Note 9)	1.2	1.3	٧	2
V _{Start}	Voltage Start-Up	$V_I = 4.25V, R_L = 0.833\Omega,$ $C_L = 20\mu F, I_L = -1.5A$		1.2	1.3	V	1, 2, 3

AC Parameters (Note 12)

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-
							groups
V _{NO}	Output Noise Voltage	$V_{I} = 6.25V, I_{L} = -100mA$			120	μV_{RMS}	7
$\Delta V_{O} / \Delta V_{I}$	Line Transient Response	$V_1 = 6.25V, \Delta V_1 = 3V,$ $I_L = -10mA$	(Note 10)		18	mV	7
$\Delta V_{O} / \Delta I_{L}$	Load Transient Response	$V_1 = 6.25V, \Delta I_L = -400mA,$ $I_L = -100mA$	(Note 11)		120	mV	7
$\Delta V_I / \Delta V_O$	Ripple Rejection	$V_I = 6.25V, I_L = -500mA,$ $E_I = 1V_{RMS}$ at $f = 2400Hz$		65		dB	4

DC Drift Parameters

The following conditions apply, unless otherwise specified.

Deltas performed on QMLV devices at Group B, Subgroup 5, only.

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-
							groups
		$V_{I} = 4.25V, I_{L} = -5mA$		-0.01 0.01 -0.01 0.01 -0.01 0.01 -0.01 0.01 -4.0 4.0 -10 10 -10 10	V	1	
V	Output Voltage	$V_1 = 4.25V, I_L = -1.5A$		-0.01	0.01	V	1
V _O	Output Voltage	$V_{I} = 41.25V, I_{L} = -5mA$		-0.01 0.01 -0.01 0.01 -0.01 0.01 -0.01 0.01 -0.01 4.0 -10 10	V	1	
		$V_1 = 41.25V, I_L = -200mA$		-0.01	0.01	V	1
V _{RLine}	Line Regulation	$4.25V \le V_1 \le 41.25V$, $I_L = -5mA$		-4.0	4.0	mV	1
1	Adjust Dip Current	$V_{I} = 4.25V, I_{L} = -5mA$		-10	10	μΑ	1
l _{Adj}	Adjust Pin Current	$V_{I} = 41.25V, I_{L} = -5mA$		-10	10	μΑ	1
V _O (Recov)	Output Voltage Recovery	$V_I = 4.25V, R_L = 0.833\Omega,$ $C_L = 20\mu S$		-0.01	0.01	V	1
		$V_{I} = 40V, R_{L} = 250\Omega$		-0.01	0.01	V	1

AC/DC Post Radiation Limits @ +25°C (Note 12)

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-
							groups
		$V_{I} = 4.25V, I_{L} = -5mA$		1.2	1.350 1.350 1.350 1.350 2.1.350 2.5 2.5 7.0 7.0	V	1
V	Output Valtage	$V_{l} = 4.25V, I_{L} = -1.5A$		1.2	1.350	V	1
V _O	Output Voltage	$V_{I} = 41.25V, I_{L} = -5mA$		1.2	1.350	V	1
		$V_{l} = 41.25V, I_{L} = -200mA$		1.2	1.350	V	1
V _{RLine}	Line Regulation	$4.25V \le V_1 \le 41.25V$, $I_L = -5mA$		-25	25	mV	1
.,	Load Bandation	$V_I = 6.25V$, -1.5A $\leq I_L \leq -5mA$			mV	1	
V_{RLoad}	Load Regulation	$V_I = 41.25V$, -200mA $\leq I_L \leq -5mA$		-7.0	7.0	mV	1
ΔV _I / ΔV _O	Ripple Rejection	$V_{I} = 6.25V, I_{L} = -500mA$ $E_{I} = 1V_{RMS}$ at f = 2400Hz		60		dB	4
V _O (Recov)	Output Voltage Recovery	$V_{I} = 4.25V, R_{L} = 0.833\Omega,$ $C_{L} = 20\mu S$		1.20	1.350 1.350 1.350 1.350 25 7.0 7.0	V	1
		$V_I = 40V$, $R_L = 250\Omega$		1.20	1.350	V	1

Note 2: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by $T_{J_{max}}$ (maximum junction temperature), θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{D_{max}} = (T_{J_{max}} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. "Although power dissipation is internally limited, these specifications are applicable for power dissipations of 2W for the TO39, LCC, and ceramic SOIC packages, and 20W for the TO3 package."

Note 4: Human body model, 100 pF discharged through a 1.5 k Ω resistor.

Note 5: For the Ceramic SOIC device to function properly, the "Output" and "Output/Sense" pins must be connected on the users printed circuit board.

Note 6: The package material for these devices allows much improved heat transfer over our standard ceramic packages. In order to take full advantage of this improved heat transfer, heat sinking must be provided between the package base (directly beneath the die), and either metal traces on, or thermal vias through, the printed circuit board. Without this additional heat sinking, device power dissipation must be calculated using θ_{JA} , rather than θ_{JC} , thermal resistance. It must not be assumed that the device leads will provide substantial heat transfer out the package, since the thermal resistance of the leadframe material is very poor, relative to the material of the package base. The stated θ_{JC} thermal resistance is for the package material only, and does not account for the additional thermal resistance between the package base and the printed circuit board. The user must determine the value of the additional thermal resistance and must combine this with the stated value for the package, to calculate the total allowed power dissipation for the device.

Note 7: Guaranteed parameter, not tested.

Note 8: Tested @ 25°C; guaranteed, but not tested @ 125°C & -55°C

Note 9: Tested @ $T_A = 125$ °C, correlated to $T_A = 150$ °C

Note 10: SMD limit of 6mV/V is equivalent to 18mV

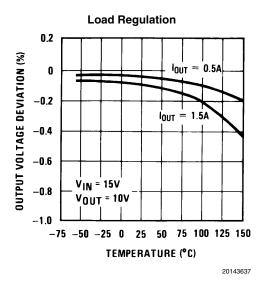
Note 11: SMD limit of 0.3mV/V is equivalent to 120mV

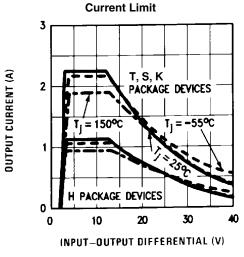
Note 12: Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics except as listed in the "Post Radiation Limits" table. These parts may be dose rate sensitive in a space environment and demonstrate enhanced low dose rate effect. Radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in Mil-Std-883, Method 1019.5, Condition A.

Note 13: Low dose rate testing has been performed on a wafer-by-wafer basis, per test method 1019 condition D of MIL-STD-883, with no enhanced low dose rate sensitivity (ELDRS) effect.

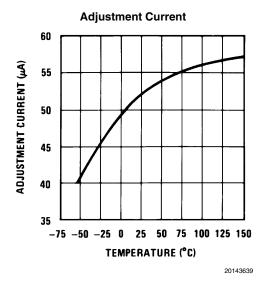
12

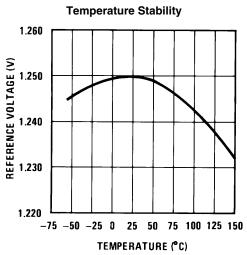
Typical Performance Characteristics Output Capacitor = 0µF unless otherwise noted

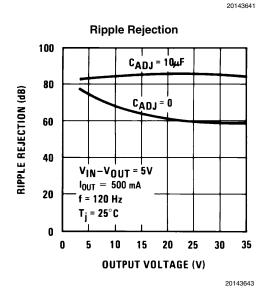


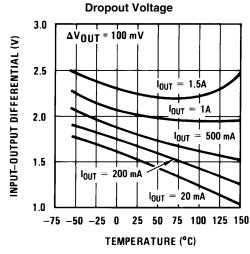


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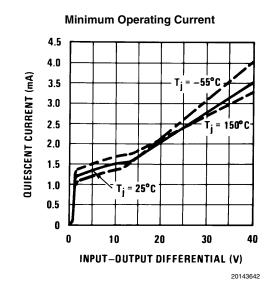


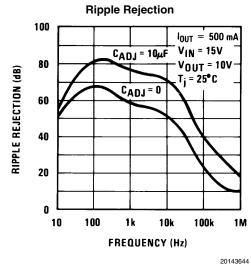


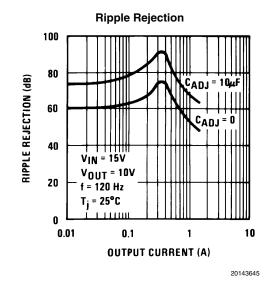


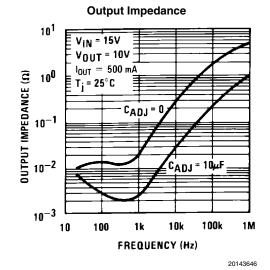


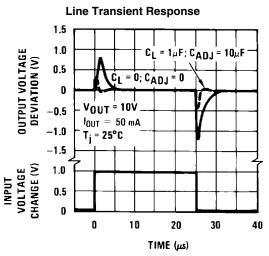
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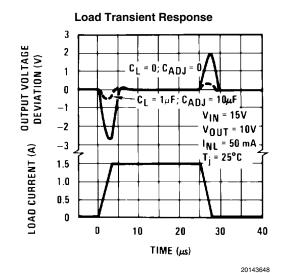








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Application Hints

In operation, the LM117 develops a nominal 1.25V reference voltage, $\rm V_{REF}$, between the output and adjustment terminal. The reference voltage is impressed across program resistor R1 and, since the voltage is constant, a constant current $\rm I_1$ then flows through the output set resistor R2, giving an output voltage of

$$V_{OUT} = V_{REF} \left(1 + \frac{R2}{R1} \right) + I_{ADJ}R2$$

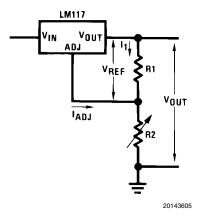


FIGURE 1.

Since the 100 μ A current from the adjustment terminal represents an error term, the LM117 was designed to minimize I_{ADJ} and make it very constant with line and load changes. To do this, all quiescent operating current is returned to the output establishing a minimum load current requirement. If there is insufficient load on the output, the output will rise.

EXTERNAL CAPACITORS

An input bypass capacitor is recommended. A $0.1\mu F$ disc or $1\mu F$ solid tantalum on the input is suitable input bypassing for almost all applications. The device is more sensitive to the absence of input bypassing when adjustment or output capacitors are used but the above values will eliminate the possibility of problems.

The adjustment terminal can be bypassed to ground on the LM117 to improve ripple rejection. This bypass capacitor prevents ripple from being amplified as the output voltage is increased. With a 10µF bypass capacitor 80dB ripple rejection is obtainable at any output level. Increases over 10µF do not appreciably improve the ripple rejection at frequencies above 120Hz. If the bypass capacitor is used, it is sometimes necessary to include protection diodes to prevent the capacitor from discharging through internal low current paths and damaging the device.

In general, the best type of capacitors to use is solid tantalum. Solid tantalum capacitors have low impedance even at high frequencies. Depending upon capacitor construction, it takes about $25\mu F$ in aluminum electrolytic to equal $1\mu F$ solid tantalum at high frequencies. Ceramic capacitors are also good at high frequencies; but some types have a large decrease in capacitance at frequencies around 0.5MHz. For this reason, $0.01\mu F$ disc may seem to work better than a $0.1\mu F$ disc as a bypass.

Although the LM117 is stable with no output capacitors, like any feedback circuit, certain values of external capacitance can cause excessive ringing. This occurs with values be-

tween 500 pF and 5000 pF. A 1 μ F solid tantalum (or 25 μ F aluminum electrolytic) on the output swamps this effect and insures stability. Any increase of the load capacitance larger than 10 μ F will merely improve the loop stability and output impedance.

LOAD REGULATION

The LM117 is capable of providing extremely good load regulation but a few precautions are needed to obtain maximum performance. The current set resistor connected between the adjustment terminal and the output terminal (usually 240 Ω) should be tied directly to the output (case) of the regulator rather than near the load. This eliminates line drops from appearing effectively in series with the reference and degrading regulation. For example, a 15V regulator with 0.05 Ω resistance between the regulator and load will have a load regulation due to line resistance of $0.05\Omega \times I_L$. If the set resistor is connected near the load the effective line resistance will be 0.05Ω (1 + R2/R1) or in this case, 11.5 times worse.

Figure 2 shows the effect of resistance between the regulator and 240Ω set resistor.

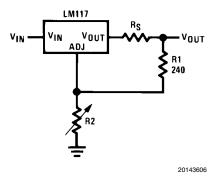


FIGURE 2. Regulator with Line Resistance in Output Lead

With the TO-3 package, it is easy to minimize the resistance from the case to the set resistor, by using two separate leads to the case. However, with the TO-39 package, care should be taken to minimize the wire length of the output lead. The ground of R2 can be returned near the ground of the load to provide remote ground sensing and improve load regulation.

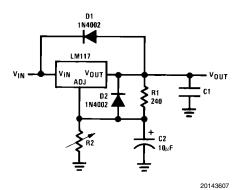
PROTECTION DIODES

When external capacitors are used with *any* IC regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator. Most $10\mu F$ capacitors have low enough internal series resistance to deliver 20A spikes when shorted. Although the surge is short, there is enough energy to damage parts of the IC.

When an output capacitor is connected to a regulator and the input is shorted, the output capacitor will discharge into the output of the regulator. The discharge current depends on the value of the capacitor, the output voltage of the regulator, and the rate of decrease of $V_{\text{IN}}.$ In the LM117, this discharge path is through a large junction that is able to sustain 15A surge with no problem. This is not true of other types of positive regulators. For output capacitors of $25\mu\text{F}$ or less, there is no need to use diodes.

The bypass capacitor on the adjustment terminal can discharge through a low current junction. Discharge occurs when *either* the input or output is shorted. Internal to the LM117 is a 50Ω resistor which limits the peak discharge current. No protection is needed for output voltages of 25V or less and

 $10\mu F$ capacitance. Figure 3 shows an LM117 with protection diodes included for use with outputs greater than 25V and high values of output capacitance.



 $V_{OUT} = 1.25V \left(1 + \frac{R2}{R1}\right) + I_{ADJ}R2$

D1 protects against C1 D2 protects against C2

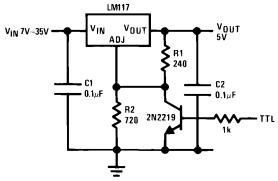
FIGURE 3. Regulator with Protection Diodes

When a value for $\theta_{(H-A)}$ is found using the equation shown, a heatsink must be selected that has a value that is less than or equal to this number.

 $\theta_{(H-A)}$ is specified numerically by the heatsink manufacturer in the catalog, or shown in a curve that plots temperature rise vs power dissipation for the heatsink.

Typical Applications

5V Logic Regulator with Electronic Shutdown*

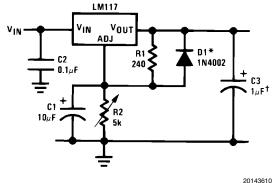


*Min. output ≅ 1.2V

Slow Turn-On 15V Regulator LM117 V_{1N} V_{0UT} ADJ R1 240 1N4002 R2 2.7k 2N2905 + C1 25μF

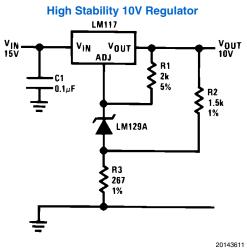
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Adjustable Regulator with Improved Ripple Rejection

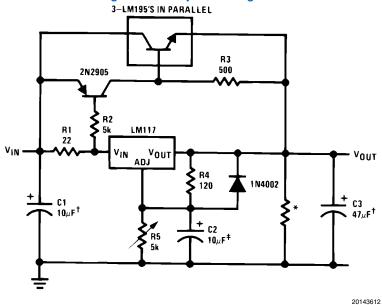


†Solid tantalum

*Discharges C1 if output is shorted to ground



High Current Adjustable Regulator



‡Optional—improves ripple rejection

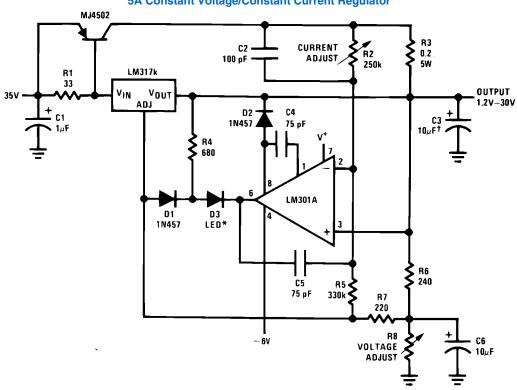
†Solid tantalum

*Minimum load current = 30 mA

0 to 30V Regulator **Power Follower** 10V-40V LM117 Vout - Vout 0.1μF 150 C1 LM195 • 0.1µF 10k OUTPUT ±0.6A LM113 VIN VOUT 1.2V LM117 ADJ **₹** R3 680 -107 20143614

Full output current not available at high input-output voltages

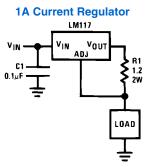
5A Constant Voltage/Constant Current Regulator



20143615

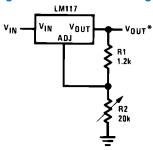
†Solid tantalum

*Lights in constant current mode



20143616

1.2V-20V Regulator with Minimum Program Current

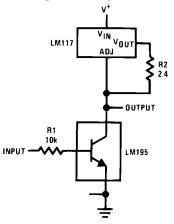


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20143618

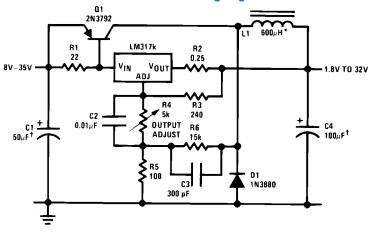
*Minimum load current ≅ 4 mA

High Gain Amplifier



19

Low Cost 3A Switching Regulator

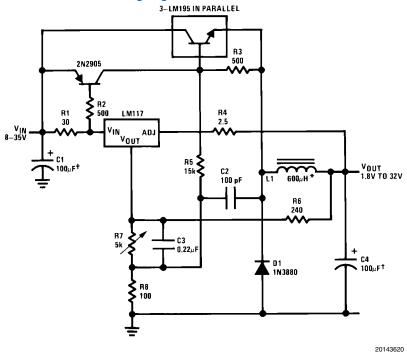


†Solid tantalum

*Core—Arnold A-254168-2 60 turns

4A Switching Regulator with Overload Protection

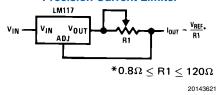
20143619



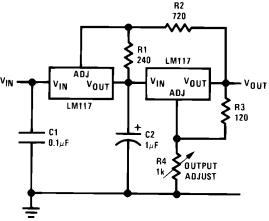
†Solid tantalum

*Core—Arnold A-254168-2 60 turns

Precision Current Limiter

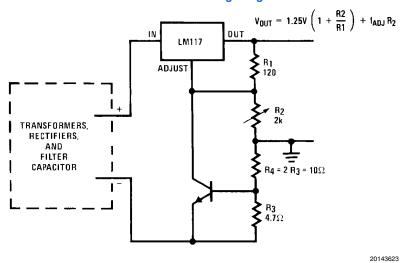


Tracking Preregulator



20143622

Current Limited Voltage Regulator

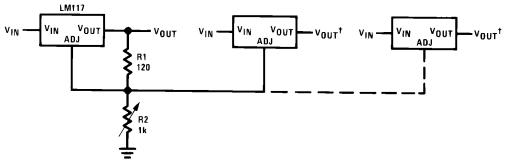


– Short circuit current is approximately $\frac{600~\text{mV}}{\text{R3}},$ or 120 mA

(Compared to LM117's higher current limit)

—At 50 mA output only $^{3}\!\!\!/\!\!\!4$ volt of drop occurs in $\rm R_3$ and $\rm R_4$

Adjusting Multiple On-Card Regulators with Single Control*



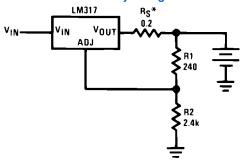
20143624

*All outputs within ±100 mV †Minimum load—10 mA

AC Voltage Regulator LM317 VIN VOUT 480 480 120 VIN VOUT LM317

20143625

12V Battery Charger

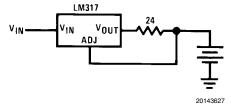


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*R_S—sets output impedance of charger:
$$Z_{OUT} = R_S \left(1 + \frac{R2}{R1} \right)$$

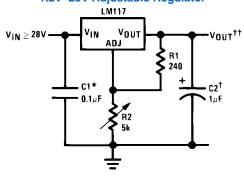
Use of R_S allows low charging rates with fully charged battery.

50mA Constant Current Battery Charger



Adjustable 4A Regulator LM317 LM317 LM317 VIN ADJ 100 2N2905 LM308 150 1.5k 5k

1.2V-25V Adjustable Regulator



20143601

20143628

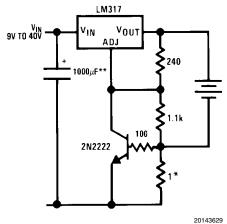
Full output current not available at high input-output voltages

*Needed if device is more than 6 inches from filter capacitors.

†Optional—improves transient response. Output capacitors in the range of $1\mu F$ to $1000\mu F$ of aluminum or tantalum electrolytic are commonly used to provide improved output impedance and rejection of transients.

$$\dagger\dagger V_{OUT} = 1.25V \left(1 + \frac{R2}{R1}\right) + I_{ADJ}(R_2)$$

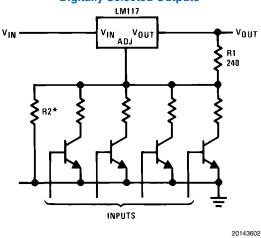
Current Limited 6V Charger



*Sets peak current (0.6A for 1Ω)

**The $1000\mu F$ is recommended to filter out input transients

Digitally Selected Outputs

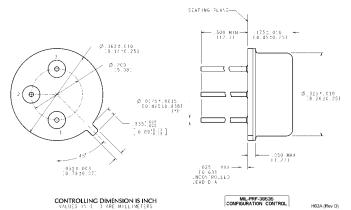


*Sets maximum V_{OUT}

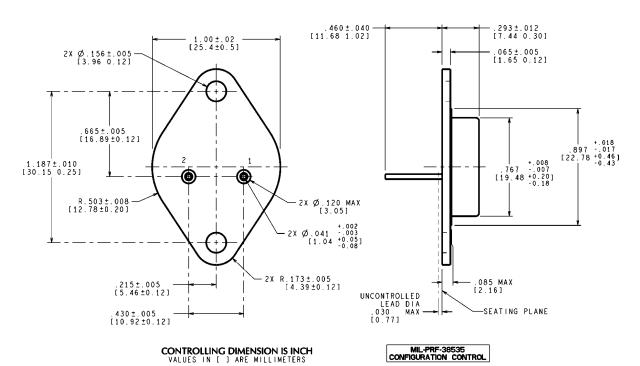
Revision History

Date Released	Revision	Section	Changes
03/17/06	Α	New Release to corporate format	5 MDS data sheets were consolidated into one
			corporate data sheet format. Clarified ΔI _{Adj} / Line
			versus ΔI _{Adj} / Load by separating the parameters in
			all of the tables. MNLM117-K Rev 1C1,
			MNLM117-X Rev 0A0, MNLM117-E Rev 0B1,
			MRLM117–X-RH Rev 2A0, MRLM117–K-RH Rev
			3A0 will be archived.
06/29/06	В	Features, Ordering Information Table, Rad	Deleted NSID LM117WGRQML, no longer
		Hard Electrical Section for H and WG	available. Added Available with Radiation
		packages and Notes	Guarantee, Low Dose NSID's to table
			5962R9951705VXA LM117HRLQMLV,
			5962R9951705VZA LM117WGRLQMLV, and
			reference to Note 11 and 12. Note 12 to Rad Hard
			Electrical Heading for H and WG packages. Note
			12 to Notes. Archive Revision A.
11/30/2010	С	Features, Ordering Table, Absolute	Added radiation info., Update with current device
		Ratings, LM117H, WG and K RH Drift	information and format, T0-39 Pkg weight, Vo
		Electrical Table	(Recov). Revision B will be Archived.

Physical Dimensions inches (millimeters) unless otherwise noted



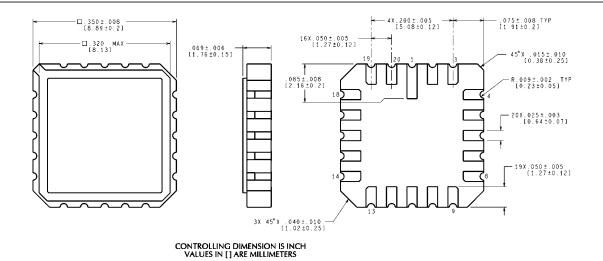
(TO-39) Metal Can Package NS Package Number H03A



TO-3 Metal Can Package (K) NS Package Number K02C

25 www.national.com

K02C (Rev E)



Ceramic Leadless Chip Carrier NS Package Number E20A

(R.015 TYP)

.040±.003 [1.02±0.07] TYP .006±.002 TYP

WG16A (Rev E)

E20A (Rev F)

SUPPLIER'S OPTION

LEAD 1 ID

16X .010±.002
[0.25±0.050]

14X .050±.002
[1.27±0.051]

Ceramic SOIC NS Package Number WG16A

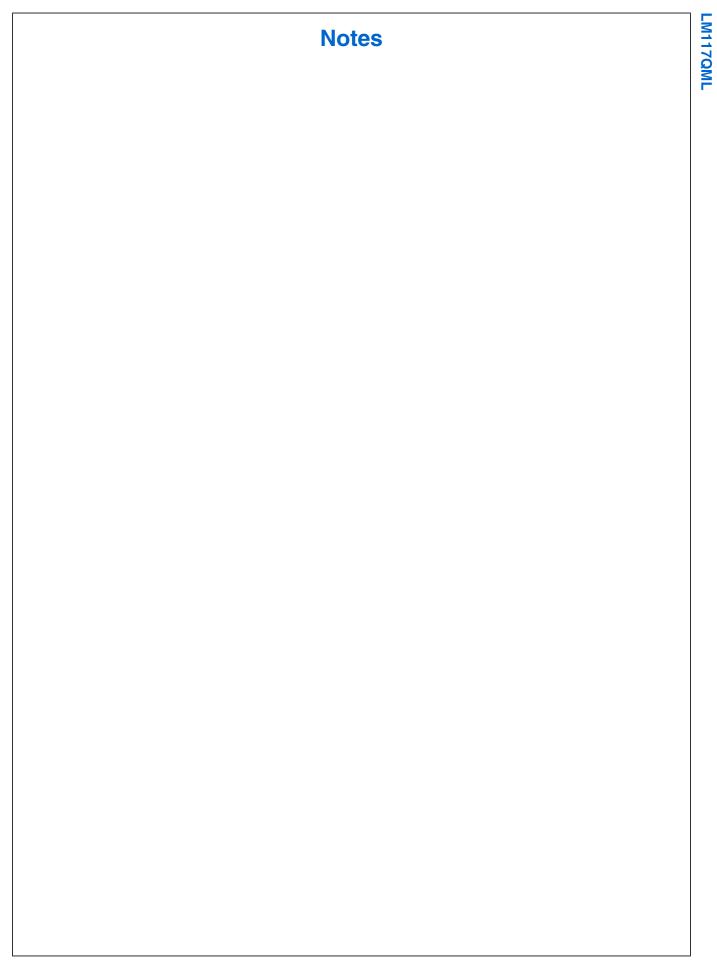
SEATING PLANE

MIL-PRF-38535 CONFIGURATION CONTROL .004 [0.1] .008±.004 [0.2±0.1]

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