S71GL016A Based MCPs

Stacked Multi-Chip Product (MCP)
Flash Memory and RAM
16 Megabit (1M x 16-bit) CMOS 3.0 Volt-only Page Mode Flash Memory
4 Megabit (256K x 16-bit) pSRAM

Data Sheet *(Advance Information)*

Notice to Readers: This document states the current technical specifications regarding the Spansion product(s) described herein. Each product described herein may be designated as Advance Information, Preliminary, or Full Production. See *Notice On Data Sheet Designations* for definitions.

Publication Number S71GL016A_00 **Revision** A **Amendment** 1 **Issue Date** June 20, 2006

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When a product has been in production for a period of time such that no changes or only nominal changes are expected, the Preliminary designation is removed from the data sheet. Nominal changes may include those affecting the number of ordering part numbers available, such as the addition or deletion of a speed option, temperature range, package type, or V_{IO} range. Changes may also include those needed to clarify a description or to correct a typographical error or incorrect specification. Spansion LLC applies the following conditions to documents in this category:

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Data Sheet *(Advance Information)*

Features

- **Power supply voltage of 2.7 V to 3.1 V**
- **High performance**
  - 100 ns (100 ns Flash, 70 ns pSRAM/SRAM)
- **Packages**
  - 7 x 9 x 1.2 mm 56 ball FBGA
- **Operating Temperature**
  - –25°C to +85°C

General Description

The S71GL series is a product line of stacked Multi-Chip Product (MCP) packages and consists of:

- One S29GL016A Flash memory die
- pSRAM

The products covered by this document are listed in the table below:

		Flash Memory Density
		16Mb
pSRAM Density	4Mb	S71GL016A40

For detailed specifications, please refer to the individual data sheets.

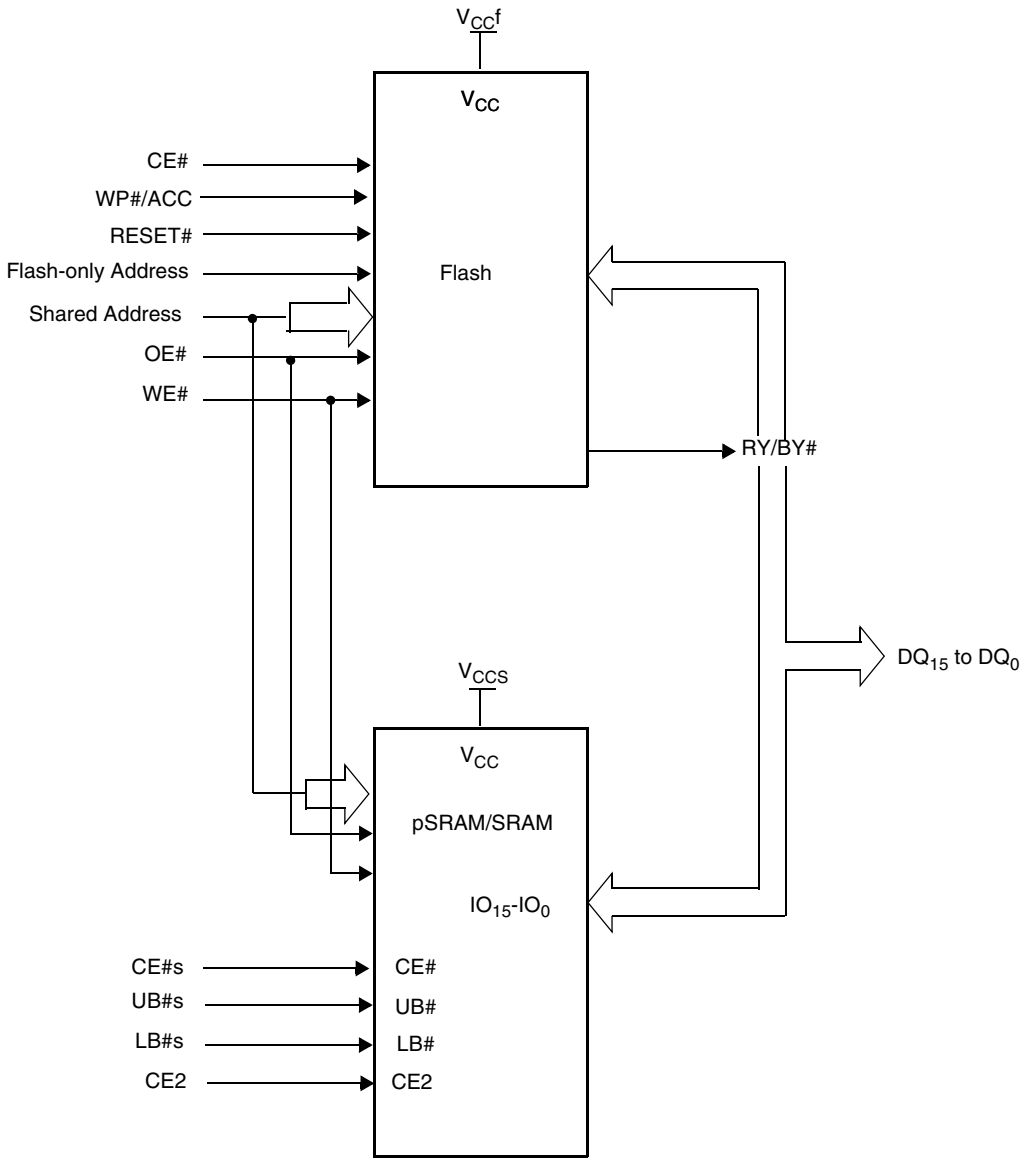
Document	Publication Identification Number (PID)
S29GL-A	S29GL-A_00
pSRAM Type 4	psram_18

Publication Number S71GL016A_00 **Revision** A **Amendment** 1 **Issue Date** June 20, 2006

1. Product Selector Guide

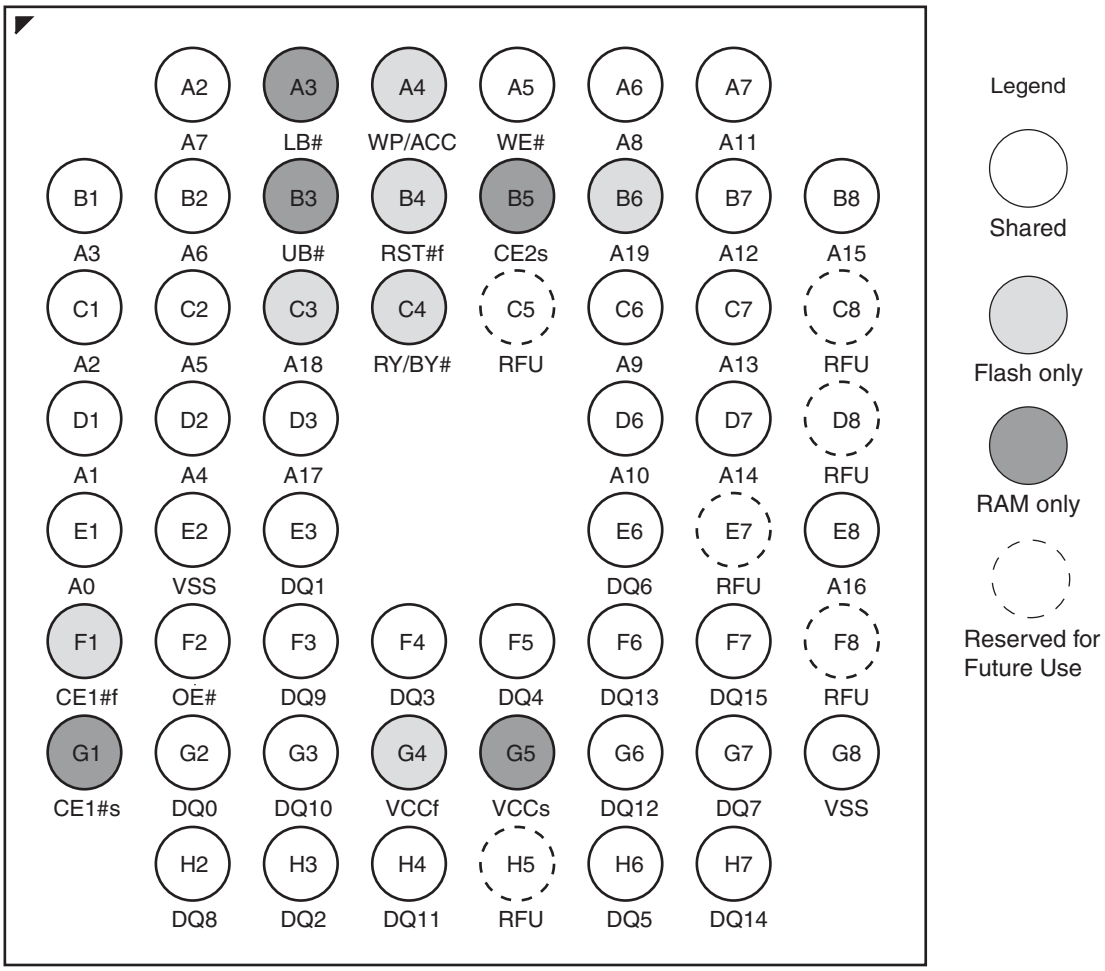
Device-Model#	Flash Access time (ns)	pSRAM density	pSRAM Access time (ns)	pSRAM type	Package
S71GL016A40-1J	100	4 M pSRAM	70	Type 4	TLC056
S71GL016A40-3J					

2. MCP Block Diagram



3. Connection Diagram

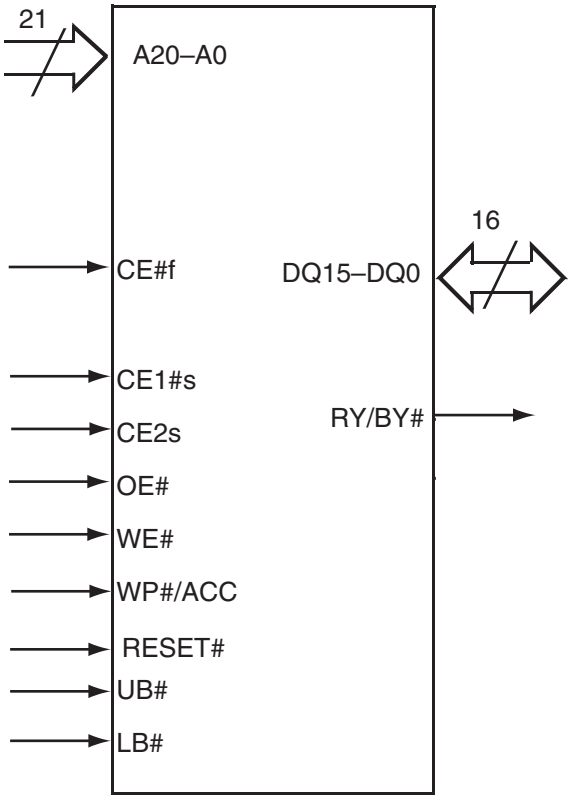
Figure 3.1 56-ball Fine-Pitch Ball Grid Array (Top View, Balls Facing Down)



4. Pin Description

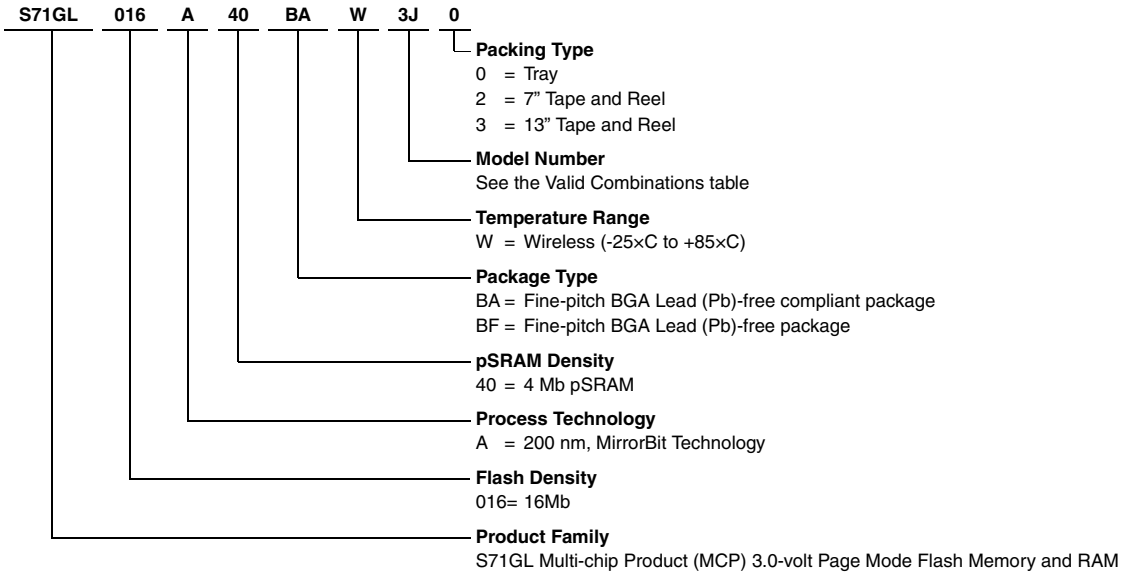
A19–A0	=	20 Address Inputs (Common and Flash only)
DQ15–DQ0	=	16 Data Inputs/Outputs (Common)
CE#f	=	Chip Enable (Flash)
CE#s	=	Chip Enable 1 (pSRAM)
OE#	=	Output Enable (Common)
WE#	=	Write Enable (Common)
RY/BY#	=	Ready/Busy Output (Flash 1)
UB#	=	Upper Byte Control (pSRAM/SRAM)
LB#	=	Lower Byte Control (pSRAM/SRAM)
RESET#	=	Hardware Reset Pin, Active Low (Flash)
WP#/ACC	=	Hardware Write Protect/Acceleration Pin (Flash)
VCCf	=	Flash 3.0 volt-only single power supply (see Product Selector Guide for speed options and voltage supply tolerances)
VCCs	=	pSRAM/SRAM Power Supply
V_{SS}	=	Device Ground (Common)
NC	=	Pin Not Connected Internally

5. Logic Symbol



6. Ordering Information

The order number is formed by a valid combinations of the following:



6.1 Valid Combinations

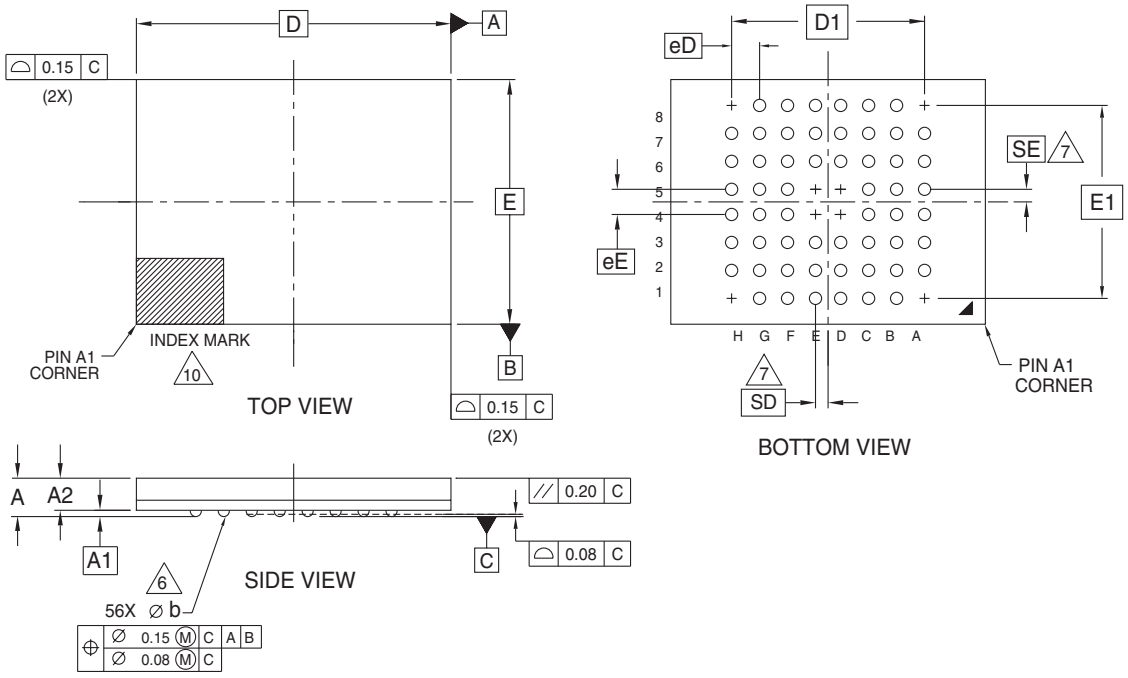
Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Base Ordering Part Number	Package & Temperature	Package Modifier/ Model Number	Packing Type	Speed Options (ns)/ Boot Sector Option	pSRAM Type/ Access Time (ns)	Package Marking
S71GL016A40	BAW	3J	0, 2, 3 (See Note)	100 / Bottom Boot Sector	pSRAM4/ 70	TLC056
S71GL016A40		1J		100 / Top Boot Sector		
S71GL016A40	BFW	3J		100 / Bottom Boot Sector		
S71GL016A40		1J		100 / Top Boot Sector		

Note:
Type 0 is standard. Specify other options as required.

7. Physical Dimensions

Figure 7.1 TLC056—56-ball Fine-Pitch Ball Grid Array (FBGA) 9 x 7 mm



PACKAGE	TLC 056			
JEDEC	N/A			
D x E	9.00 mm x 7.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.20	PROFILE
A1	0.20	---	---	BALL HEIGHT
A2	0.81	---	0.97	BODY THICKNESS
D	9.00 BSC.			BODY SIZE
E	7.00 BSC.			BODY SIZE
D1	5.60 BSC.			MATRIX FOOTPRINT
E1	5.60 BSC.			MATRIX FOOTPRINT
MD	8			MATRIX SIZE D DIRECTION
ME	8			MATRIX SIZE E DIRECTION
n	56			BALL COUNT
ϕb	0.35	0.40	0.45	BALL DIAMETER
eE	0.80 BSC.			BALL PITCH
eD	0.80 BSC			BALL PITCH
SD / SE	0.40 BSC.			SOLDER BALL PLACEMENT
	A1,A8,D4,D5,E4,E5,H1,H8			DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

   n IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. N/A
10. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

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8. Revision History

Section	Description
Revision A (May 17, 2005)	
	Initial Release
Revision A1 (June 20, 2006)	
Global	Data sheet updated to new template
General Description	Added a table referencing the individual specification documents for the Flash and pSRAM data sheets

Colophon

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