MINDSPEED
BUILD IT FIRST®

M28480 Multi-Channel Synchronous Communications Controller – MUSYCC™

Product Brief

Product Overview

Multi-Channel HDLC controller with enhanced SS7 support

The M28480 is the next generation advanced multi-channel synchronous communications controller (MUSYCC) that formats and de-formats 512 bi-directional high-level datalink control (HDLC) channels. MUSYCC-512 operates at Layer 2 of the open systems interconnection (OSI) protocol reference model. MUSYCC-512 provides a comprehensive, high-density solution for processing HDLC and SS7 channels for media gateway and base station controller applications.

Features	Benefits
512 HDLC channels with SS7 or 84 channels with high speed SS7 support	Integrated high density solution for signalling applications
155.52 Mbps full-duplex throughput	Ideal for high data rate applications
Complete MTP1, enhanced MTP2 HW protocol with software driver	Off-loads host processor, increases performance and lowers overall system cost
PM counters (SUERM,AERM and EIM)	Software programmable up-down counters
8 serial interfaces	Supports various line rates ranging from (T1/E1,T3/E3 or OC-3)
33/66MHz, 32bit PCI 2.1 bus interface	Legacy support for current generation designs
Compliant to ITU-T Q.703 (including Annex A) and Q.781	Ensures interoperability with the deployed systems

HDLC Features

The HDLC engine supports general purpose HDLC processing, frame relay, and LAPD/LAPB. The on-chip DMA controller streamlines autonomous buffer management for each channel thus reducing the host processor intervention. The 8 serial interfaces support mixed data rates including T1/E1/T3/E3, HSSI, and 8.192/16.364/32.728Mbps TDM modes. Each logical channel can be assigned to a physical stream ranging from 8 Kbps (sub-channeling mode) to 52 Mbps.

SS7 Support

MUSYCC-512 is the first device of its kind to include a complete MTP-1 layer support in hardware. Hardware implementation of the MTP2 layer on the M28480 is capable of LSSU/FISU message transmission and generation, filtering of received messages, programmable filter message lengths, and extended sequence number format support for high speed SS7. In addition, various PM counters are provided including SUERM, AERM, and EIM. The inclusion of these hardware features reduces reliance on a host processor for these functions while increasing overall system performance and reducing cost.

System Interfaces

On the system side MUSYCC offers a 32-bit, 33/66 MHz PCI 2.1 interface for the packet traffic, accessing the full set of performance-monitoring counters and initial configuration and channel controls such as dynamic activation and deactivation of channels.

Software and MTP-2 Stack Support

Industry leading software drivers are provided with the M28480 device. The software is fully documented and uses structured APIs to abstract the hardware. In addition, the device and accompanying software has been tested with a commercial MTP-2/SS7 stack to ensure a complete system solution.

Applications

The MUSYCC-512 is ideal for signaling applications requiring high density HDLC support. Typical applications for this device include media gateways, signaling gateways, signaling transfer points, and base station controllers. With support for 84 high speed SS7 links, the MUSYCC-512 addresses future growth requirements for these applications. Mindspeed also provides complete line card solutions for these applications with VoIP DSPs, Network Processors, and T3/E3 and SONET products.

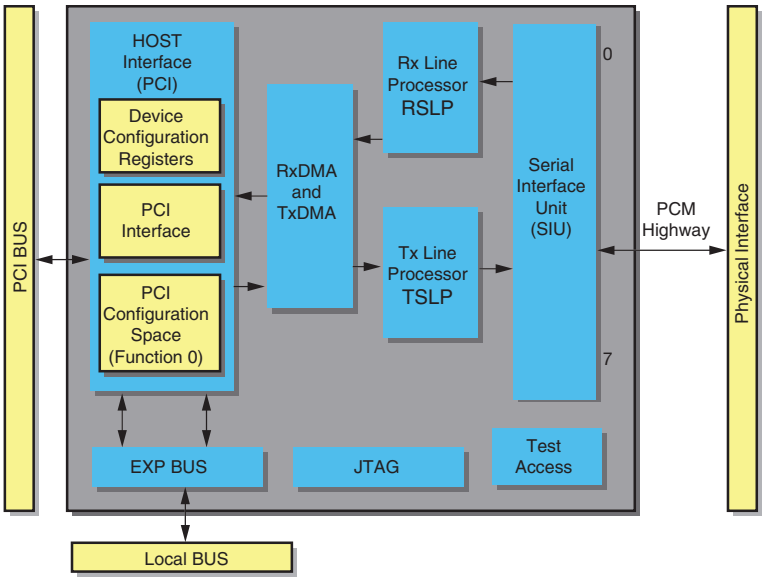

Figure 1: M28480 Functional Block Diagram

M28480 MUSYCC Product Highlights

- 512-channel HDLC controller
- OSI Layer 2 protocol support
- General purpose HDLC (ISO 3309)
  - SS7 protocol
  - X.25 (LAPB)
  - Frame relay (LAPF/ANSI T1.618)
  - ISDN D-channel (LAPD/ Q.921)
  - ISLP support
- HW MTP1 and convergence layer MTP2 protocols
  - SS7 FISU/LSSU filters, auto transmission and error monitors included
  - High speed SS7 (Q.703 Annex A)
  - JT-Q.703
  - Chinese 2M GB STD
  -
- 8 independent serial interfaces, which support:
  - Mixed data rates (combination of T1/E1/, T3/E3, etc.) as long as they do not exceed each port's respective bandwidth limitation and the overall device bandwidth of 155.52 Mbps per direction
- 8 T1/E1 data streams
- 3 HSSI interfaces (52 Mbps)
- 8x 16.384 Mbps (or any lower rate) serial interfaces
- Configurable logical channels
  - Standard DS0 (56, 64 Kbps)
  - Sub-channeling (N x 8 Kbps)
  - Hyper-channel (N x 64 Kbps)
  - Unchannelized mode
- Per-channel protocol mode selection
  - Non-FCS mode
  - 16-bit FCS mode
  - 32-bit FCS mode
  - Transparent mode (unformatted data)
- Hardware flow control (CTS)
- Selectable Endian configuration on data
- Per-channel DMA buffer management
  - Table-like data structures
  - Variable size transmit/ receive FIFO
- Per-channel message length check
  - Select no length checking
  - Select from one of three 14-bit max length registers
- Direct PCI bus interface
  - 32-bit, 33/66 MHz operation
  - Bus master and slave operation
  - PCI Version 2.1
- HSSI interfaces (52 Mbps)
- Local expansion bus interface (EBUS)
  - 32-bit multiplexed address/data bus
- Support of 64-bit ECC host memory
- Low power, 1.2V/3.3V CMOS operation
- 23mm, 484 pin PBGA package

www.mindspeed.com/salesoffices
General Information: (949) 579-3000
Headquarters – Newport Beach
4000 MacArthur Blvd., East Tower
Newport Beach, CA 92660-3007
M28480-BRF-001-C.pdf

Ordering Info:

M28480-11 : PCI Interface
M28480G-11 : PCI Interface ROHS