ADQ112 is a high speed digitizer. The ADQ112 has outstanding dynamic performance from a combination of high bandwidth and high dynamic range, which enables demanding measurements such as RF/IF sampling. Excellent spectral purity in combination with low noise makes ADQ112 ideal for noise measurements.

Features

- 1.1 GSPS sampling rate
- 780 MHz analog bandwidth
- 12 bits resolution
- Internal and external clock
- External trigger
- Multi record >1 MHz PRF
- 170 MSamples data memory
- Data interface USB 2.0 / cPCIe / PXIe
- FPGAs available for customized applications
- Support for C/C++ and MATLAB

Applications

- RADAR
- LIDAR
- Wireless communication
- Optical transmission
- High-speed data recording
- Test and measurement

Software support

- MATLAB
- C/C++

Ordering information

ORDERING INFORMATION	
ADQ112 standard	ADQ112
OPTIONS	
Low frequency AC AFE	–LFAFE
Buffered DC coupled AFE	–DCAFE
cPCIe / PXIe	–PXIE
Decimation	–DEC
FPGA upgrade	–SX50T
RELATED PRODUCTS	
ADQ Development Kit	ADQ112 Dev Kit

Example: ADQ112–DCAFE–PXIE

Introduction

The ADQ112 digitizer features single channel, 12 bits resolution, 1.1 GSPS capture rate with 780 MHz analog input bandwidth, and 170 MSamples memory buffer.

The ADQ112 is optimized for spectral purity over a large bandwidth, which makes it ideal for broad-band applications such as IF/RF sampling and high-speed data recording. The ADQ112 offers an easy-to-use API that allows easy integration into any application. The card connects to the host via a high-speed USB 2.0 cable. cPCIe / PXIe x8 interface is available as an option. The ADQ112 is equipped with two advanced Xilinx V5 series FPGAs that are available for customized real time applications.

ADQ Development Kit

SP Devices' ADQ Development Kit is an optional software tool that rapidly enhances the customization process of your next DSP application for the ADQ-series onboard FPGAs. More details about this product can be found in the product brief for the ADQ Development Kit.

1 Technical data[1]

KEY PARAMETERS	
Number of channels	1
Digitizer Resolution	12 bits
Sampling rate	140 - 1100 MSps
Data memory	170 MSamples
Trigger	Software / External / Edge
Number of GPIOs	6
Front panel connectors	SMA / Micro-D Plug 9 way
Clock	Internal / External / Ext ref

ANALOG INPUT		
ENOB @ 70 MHz	10.2	bits
SFDR @ 70 MHz	76	dB
SNDR @ 70 MHz	63	dB
Impedance AC	50	Ω
Bandwidth (–3 dB)	10 – 780M	Hz
Input voltage range	2.2	V_{PP}

INTERNAL CLOCK		
Accuracy	400	fs RMS
Internal sampling rate	2200/n, n=2...15	MHz
Clock references source	10 MHz external Internal TCXO	

EXTERNAL CLOCK		
Frequency (min – max)[1]	70 - 550	MHz
Signal level (min – max)	0.25 – 2	V_{PP}
Impedance AC	50	Ω
Duty cycle	50% ± 5%	

1. The sampling frequency is 2X clock frequency due to interleaving.

MEMORY	
Data memory	170 MSamples
Pre-trigger buffer	Up to batch size
Trigger hold off	2^{34} samples
Multi record batch size	1 – memory size
Multi record max PRF	1.8 MHz

EXTERNAL REFERENCE		
Frequency	10	MHz
Signal level (min – max)	0.8 – 3.3	V_{PP}
Impedance AC	50	Ω

EXTERNAL TRIGGER INPUT		
Input impedance DC	50	Ω
Input range (min – max)	–2.5 – +3.3	V
Threshold rising edge	0.5	V
Time resolution	454	ps

TRIGGER USED AS GPIO		
Output impedance	20	Ω
Output (low – high)	0.1 – 2	V

GPIO		
Output imp. GPIO-pin	30	Ω
Out. imp. dedicated output	100	Ω
Output (low – high)	0.1 – 3.2	V
Input impedance	10	$k\Omega$
Input (low – high)	1 – 2.3	V

HI-SPEED USB 2.0 INTERFACE		
Sustained data rate	25	MByte/s
Connector	Mini–B	

POWER SUPPLY		
Supply voltage	12	V
Power consumption	20	W

ENVIRONMENTAL / MECHANICAL		
Operating temperature	0 – 45	^oC
Storage temperature	–20 – 70	^oC
Relative humidity, non-condensing	5% – 95%	
Board size	100 x 163	mm^2
Case size	103 x 166 x 31	mm^3

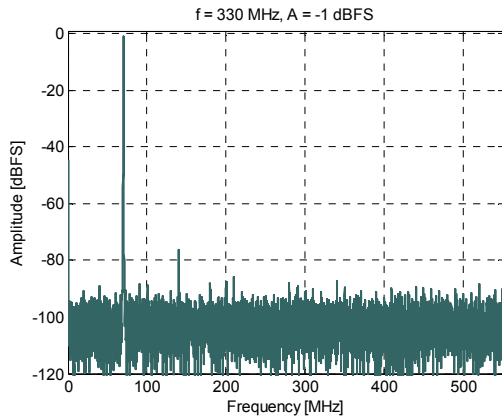| OPERATING SYSTEM	
Windows XP	SP 2 and higher
Windows Vista	All versions

APPLICATION SOFTWARE	
ADCaptureLab	Data capture and analysis
MATLAB	Data capture interface
C/C++	Data capture interface

CERTIFICATION AND COMPLIANCE
CE, FCC Part 15 B

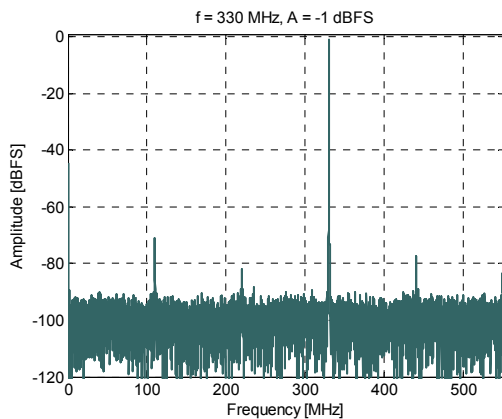1. All values are typical unless otherwise noted.

2 Dynamic performance

2.1 Noise and distortion

f = 330 MHz, A = -1 dBFS

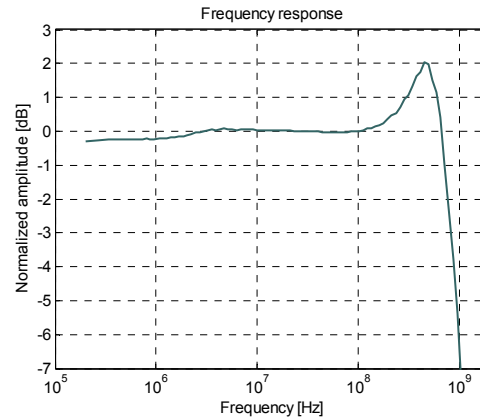| SFDR | 75 | dB |
| SNR | 62 | dB |
| ENOB | 10 | bits |

Figure 1: FFT of 70 MHz input signal.

f = 330 MHz, A = -1 dBFS

SFDR	69	dB
SNR	60	dB
ENOB	9.7	bits

Figure 2: FFT of 330 MHz input signal.

2.2 Frequency response

Frequency response

Full scale	2.2 V_{PP}
Bandwidth (–3 dB)	780 MHz
1 dB flatness	300 MHz

Figure 3: Frequency response.

3 Absolute Maximum ratings

Exposure to conditions exceeding these rating may reduce life time or permanently damage the device.

ABSOLUTE MAXIMUM RATINGS		
	Min	Max
Supply voltage (to GND)	–0.4 V	14 V
Analog input (AC)		4.4 V_{PP}
Trigger input (to GND)	–3 V	3.7 V
Clock input (AC)		3.3 V_{PP}
Ambient temperature (operation)	0 °C	45 °C

The ADQ112 has a built in fan to cool the device. If the air flow is blocked or the fan malfunctions, the temperature surveillance unit will protect the ADQ112 from overheating by shutting down parts of the device.

The SMA connectors have an expected life time of 500 operations. For frequent connecting and disconnecting of cables, connector savers are recommended.
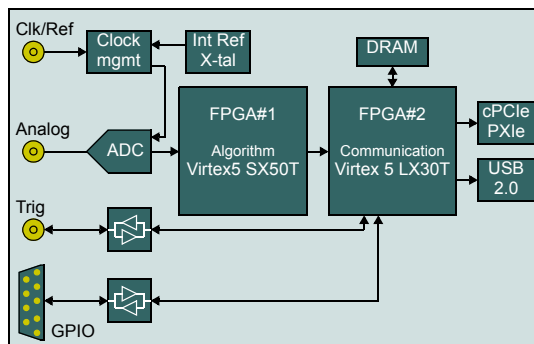
4 Architecture

4.1 Overview

Figure 4: Block diagram

4.2 Analog Front End, AFE

The analog input is single ended AC coupled 50 ohm. The single ended signal is converted to a differential signal in a balun.

4.3 ADC

The ADC configuration is two 12 bit 550MSps ADCs which are time interleaved to reach 1.1 GSps effective sampling rate. The time inter-

leaving is enabled by SP Devices' time interleaving algorithm ADX216.

4.4 Clock

The clock generator consists of a crystal oscillator as a clock reference and a PLL with built in VCO. The PLL has also built in dividers for generating necessary clock frequencies on the board. The sampling frequency is set by configuring these frequency dividers.

There is also an external SMA connector for either an external clock reference or an external clock source.

4.5 FPGAs

The data outputs of the ADCs are connected to a first Xilinx XC5VSX50T-3 FPGA which runs the time interleaving algorithm ADX216. The data is then transferred to a second FPGA, Xilinx XC5VLX30T-1, which handles the communication with the host and the batch data RAM. This FPGA is open for user applications through the ADQ Development Kit. 29 DSP elements and 30 % of the logic is available for user applications.

4.6 Memory

There is 170 MSamples data batch memory. The data batch length for each recording is set to any value within this range. For more information about memory handling, see **Section 4.8**.

4.7 Interface

The ADQ112 is connected to the host computer through a Hi-Speed USB interface which is used for control and uploading of data.

The USB connection can be configured in a streaming mode. The sustained data rate is then 25 MBytes/s[1]. This is typically used together with a data reduction algorithm, implemented through the ADQ Development Kit.

See **Section 6.1** for Compact PCI Express (cPCIe) / PXI Express (PXIe) interface.

4.8 Trigger

4.8.1 Overview

The ADQ112 has several trigger options

- Software trigger
- Level trigger

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1. This is highly dependent of other tasks performed by the operating system on the host computer.

- External trigger

When armed, the system is waiting for the selected trigger event. At the trigger event, a data batch of selected length is recorded in the batch memory. A pre-trigger buffer is available. The length of the pre-trigger buffer is fully controllable[1]. The pre-trigger buffer is a part of the total batch length.

The trigger hold-off is up to 2^{34} samples and is set in steps of 4 samples.

4.8.2 Software trigger

Data capture is triggered by a software command. This is suitable for measurements on continuous waves.

4.8.3 Level trigger

Data capture is triggered by an event on the input data. This is useful for capturing pulses. The level trigger combined with the pre-trigger or trigger hold-off setting can capture any pulse shape.

4.8.4 External trigger

Data capture is triggered by positive edge on the trigger input connector. This is intended for synchronizing the signal source with the ADQ112. It can also be used for synchronizing several ADQ112.

4.8.5 Multi record

The ADQ112 can be set up in a multi record mode. At each trigger, a record of data is recorded in the memory. The length of each record and number of records is user defined. Multi record works together with pre-trigger buffer and trigger hold off.

Figure 5 shows an example, where an external trigger is used for triggering each record. The analog channel samples a low frequency sine wave. The records has been reconstructed in time domain to illustrate the slow sine wave.

The pulse repeat frequency (PRF) can be set up to 1.8 MHz depending on the record length.
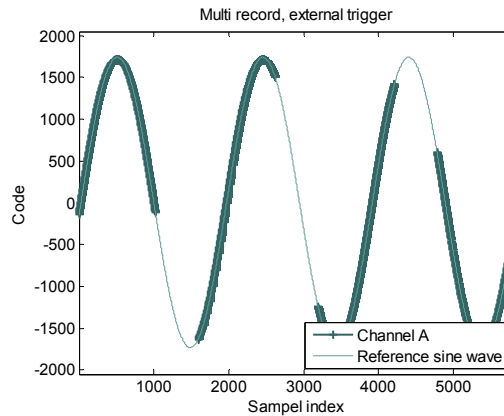
PRF	690	kHz
Record length	1024	samples

Figure 5: Multi Record

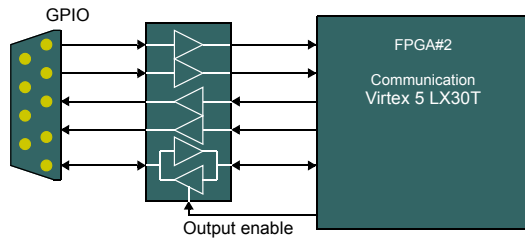| PULSE REPEAT FREQUENCY MULTI TRIG MODE	
Record length	Maximum PRF kHz
16	1800
64	1700
256	1200
1024	690
4096	235
16384	65
65536	16.6

4.9 GPIO

The ADQ112 is equipped with one bi-directional GPIO, two dedicated inputs and 2 dedicated outputs. The GPIOs are controlled from software, but can also be accessed from the ADQ Development Kit.

The connector is Micro D plug 9 way. A suitable socket with lead is for example MOLEX 83421-9044.

The trigger port can also be used as a bi-directional GPIO. The trigger can be configured as a trigger output, see **Figure 7**.

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1. There is a fixed amount of delay between the trigger and data depending on the length of the wires and the internal signal paths. This delay will change for a custom application using the ADQ Development Kit

Figure 6: GPIO block diagram.
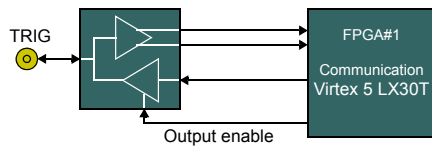
Figure 7: Trigger as GPIO: block diagram.

#	Function
1	In
2	In
3	Out
4	Out
5	GPIO
6	GND
7	GND
8	GND
9	GND

5 Software tools

5.1 ADCaptureLab

The ADQ112 is supplied with the ADCaptureLab software that provides quick and easy control of the digitizer. The tool also offers both time domain and frequency domain analysis, see **Figure 8**. Data can be saved in different file formats for off-line analysis. Comparison of results is easily done by importing data from file and analyze it in ADCaptureLab.
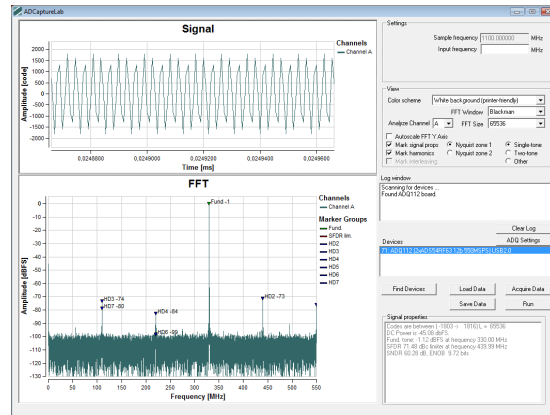

Figure 8: ADCaptureLab

5.2 Software development kit (SDK)

The ADQ112 data acquisition system is easily integrated into your own application by using the included Software development kit. The SDK includes programming examples and reference projects for C/C++ and MATLAB.

6 Options

6.1 cPCIe / PXIe interface

The ADQ112 is available with cPCIe / PXIe interface.

cPCIe / PXIe INTERFACE		
Bus width	8	lanes
Bus peak capacity	16	Gbit/s
Sustained data rate, 4 lanes	400	MByte/s
PXIe card size	1 slot 3U 4TE	

Figure 9: cPCIe / PXIe interface

Order code: –PXIE

6.2 Low frequency AC AFE[1]

The AFE is available with a low frequency configuration. The AC coupling is tuned to get a lower cut off frequency (–3dB) at typically 0.4 Hz. This configuration maintains low noise performance of the standard AFE.

Order code: –LFAFE

6.3 Active DC coupled AFE[2]

The ADQ112 is available with an active buffered DC coupled AFE. The gain compared to the AC AFE options is 18 dB which means that full scale analog input is 0.25 V_{PP}.

Order code: –DCAFE

6.4 Decimation IP

A Decimation IP is available for integration in FPGA#2. Decimation IP requires FPGA upgrade to SX50T. The Decimation IP can decimate up to 2^{34} times. The Decimation IP together with the low frequency option is ideal for low frequency noise measurements.

The Decimation IP implements a close to ideal low pass filter, which suppresses the wide band quantization noise in digitizer. The theory of decimation gives that each factor of 4 in decimation yields one extra bit in resolution. The effect is an increased dynamic range.

The Decimation IP makes the ADQ112 very flexible and a large set of measurements specifications can be met with the same device.

DECIMATION IP CONFIGURATIONS (EXAMPLES)		
Decimation order	Sampling rate	Resolution
$2^0 = 1$	1100 MSps	12 bits
$2^4 = 16$	68 MSps	14 bits
$2^{12} = 4096$	269 kSps	18 bits

Order code: –DEC

6.5 FPGA upgrade

The ADQ Development Kit opens a user area in FPGA#2 for custom designs. The standard configuration for FPGA#2 is a Xilinx Virtex 5 LX30T-1 FPGA, which is enough for many applications. However, for demanding real time signal processing applications, an FPGA upgrade to Xilinx Virtex 5 SX50T-3 is available. This gives the user access to more than 285 DSP elements. 60% of the logic in this FPGA is also available.

Order code: –SX50T

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1. It is not possible to switch between different AFEs.

2. It is not possible to switch between different AFEs.