

**MDLM119-X REV 2A2**

 Original Creation Date: 07/02/01  
 Last Update Date: 07/11/01  
 Last Major Revision Date:

**HIGH SPEED DUAL COMPARATOR**
**General Description**

The LM119 precision high speed dual comparator is fabricated on a single monolithic chip. It is designed to operate over a wide range of supply voltages down to a single 5V logic supply and ground. Furthermore, it has a higher gain and lower input current than other devices. The uncommitted collector of the output stage makes the LM119 compatible with RTL, DTL and TTL as well as capable of driving lamps and relays at currents up to 25mA.

**Industry Part Number**

LM119

**Prime Die**

LM119

**Controlling Document**

SEE FEATURES SECTION

**NS Part Numbers**

 LM119E-SMD  
 LM119H-QMLV  
 LM119H-SMD  
 LM119J-QMLV  
 LM119J-SMD  
 LM119W-QMLV  
 LM119W-SMD  
 LM119WG-QMLV  
 LM119WG-SMD

**Processing**

MIL-STD-883, Method 5004

**Quality Conformance Inspection**

MIL-STD-883, Method 5005

Subgrp	Description	Temp ( °C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

## Features

- Two independent comparators.
- Operates from a single 5V supply.
- Typically 80nS response time at  $\pm 15V$ .
- Minimum fan-out of 2 each side.
- Maximum input current of 1 $\mu$ A over temperature.
- Inputs and outputs can be isolated from system ground.
- High common mode slew rate.
- CONTROLLING DOCUMENTS

LM119E-SMD	86014012A
LM119H-QMLV	5962-9679801VIA
LM119H-SMD	8601401IA
LM119J-QMLV	5962-9679801VCA
LM119J-SMD	8601401CA
LM119W-QMLV	5962-9679801VHA
LM119W-SMD	8601401HA
LM119WG-QMLV	5962-9679801VXA
LM119WG-SMD	8601401X

Although designed primarily for applications requiring operation from digital logic supplies, the LM119 is fully specified for power supplies up to  $\pm 15V$ . It features faster response than the LM111 at the expense of higher power dissipation. However, the high speed, wide operating voltage range and low package count make the LM119 much more versatile than older devices.

**(Absolute Maximum Ratings)**

(Note 1)

Total Supply Voltage	36V
Output to Negative Supply Voltage	36V
Ground to Negative Supply Voltage	25V
Ground to Positive Supply Voltage	18V
Differential Input Voltage	±5V
Input Voltage (Note 3)	±15V
Power Dissipation (Note 2)	500mW
Output Short Circuit Duration	10 seconds
Maximum Junction Temperature	150 C
Storage Temperature Range	-65 C to 150 C
Lead Temperature (Soldering, 10 seconds)	260 C
Thermal Resistance	
ThetaJA	
E Package (Still Air)	89 C/W
E Package (500LF/Min Air flow)	63 C/W
H Package (Still Air)	162 C/W
H Package (500LF/Min Air flow)	88 C/W
J Package (Still Air)	94 C/W
J Package (500LF/Min Air flow)	52 C/W
W Package (Still Air)	215 C/W
W Package (500LF/Min Air flow)	132 C/W
WG Package (Still Air)	215 C/W
WG Package (500LF/Min Air flow)	132 C/W
ThetaJC	
E Package	5 C/W
H Package	31 C/W
J Package	11 C/W
W Package	13 C/W
WG Package	13 C/W
Package Weight	
E Package	TBD
H Package	TBD
J Package	TBD
W Package	TBD
WG Package	225mg
ESD Tolerance (Note 4)	800V

- Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
- Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by  $T_{jmax}$  (maximum junction temperature),  $\Theta_{JA}$  (package junction to ambient thermal resistance), and  $T_A$  (ambient temperature). The maximum allowable power dissipation at any temperature is  $P_{dmax} = (T_{jmax} - T_A)/\Theta_{JA}$  or the number given in the Absolute Maximum Ratings, whichever is lower.
- Note 3: For supply voltages less than  $\pm 15V$  the absolute maximum input voltage is equal to the supply voltage.
- Note 4: Human body model, 1.5K Ohm in series with 100pF.

## Recommended Operating Conditions

Operating Temperature Range

$$-55\text{ C} \leq T_a \leq 125\text{ C}$$

## Electrical Characteristics

### DC PARAMETERS:

(The following conditions apply to all the following parameters, unless otherwise specified.)

DC:  $V_{cm} = 0V$

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Icc+	Positive Supply Current	$\pm V_{cc} = \pm 15V$			11		mA	1
					11.5		mA	2, 3
Icc-	Negative Supply Current	$\pm V_{cc} = \pm 15V$			-4.2		mA	1
					-4.5		mA	2
					-6		mA	3
Ileak	Output Leakage Current	$+V_{cc} = 15V, -V_{cc} = -1V, V_{gnd} = 0V, V_{out} = 35V$	1			1.8	$\mu A$	1
						10	$\mu A$	2, 3
Iib	Input Bias Current	$\pm V_{cc} = \pm 15V$			0.475		$\mu A$	1
					0.95		$\mu A$	2, 3
		$V_{cc} = 5V$			0.475		$\mu A$	1
					.95		$\mu A$	2, 3
Vio	Input Offset Voltage	$V_{cc} = 5V, V_{cm} = 1V, R_s \leq 5K$	2		-3.8	3.8	mV	1
					-6.8	6.8	mV	2, 3
		$V_{cc} = 5V, V_{cm} = 3V, R_s \leq 5K$	2		-3.8	3.8	mV	1
					-6.8	6.8	mV	2, 3
		$\pm V_{cc} = \pm 15V, V_{cm} = 12V, R_s \leq 5K$			-3.8	3.8	mV	1
					-6.8	6.8	mV	2, 3
		$\pm V_{cc} = \pm 15V, V_{cm} = -12V, R_s \leq 5K$			-3.8	3.8	mV	1
					-6.8	6.8	mV	2, 3
Iio	Input Offset Current	$V_{cc} = 5V, V_{cm} = 1V$	2		-75	75	nA	1
					-100	100	nA	2, 3
		$V_{cc} = 5V, V_{cm} = 3V$	2		-75	75	nA	1
					-100	100	nA	2, 3
		$\pm V_{cc} = \pm 15V, V_{cm} = 12V$			-75	75	nA	1
					-100	100	nA	2, 3
		$\pm V_{cc} = \pm 15V, V_{cm} = -12V$			-75	75	nA	1
					-100	100	nA	2, 3
Vi	Input Voltage Range	$V_{cc} = 5V$	2, 3		1	3	V	1, 2, 3
		$V_{cc} = \pm 15V$	3		-12	12	V	1, 2, 3

## Electrical Characteristics

### DC PARAMETERS: (Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)  
DC:  $V_{cm} = 0V$

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vsat	Output Saturation Voltage	$V_{cc} = \pm 15V, I_{out} = 25mA, V_{in} \leq -5mV$	1			1.5	V	1, 2, 3
		$+V_{cc} = 3.5V, -V_{cc} = -1V, V_{in} \leq -6mV, I_{sink} \leq 3.2mA$				0.4	V	1, 2
						0.6	V	3
Av	Voltage Gain	$\pm V_{cc} = \pm 15V, \Delta V_{out} = 12V$	4		10.5		K	4
			4		10		K	5, 6
		$V_{cc} = 5V, \Delta V_{out} = 4.5V$	2, 4		8		K	4
			2, 4		5		K	5
			2, 4		5.8		K	6
CMRR	Common Mode Rejection Ratio	$\pm V_{cc} = \pm 15V, V_{cm} = \pm 12V$			80		dB	4

### DC PARAMETERS: DRIFT VALUES

(The following conditions apply to all the following parameters, unless otherwise specified.)  
DC:  $V_{cm} = 0V$ . Delta calculations performed on JAN S and QMLV devices at group B, subgroup 5 ONLY.

Icc+	Positive Supply Current	$\pm V_{cc} = \pm 15V$			-1	1	mA	1
Icc-	Negative Supply Current	$\pm V_{cc} = \pm 15V$			-0.5	0.5	mA	1
Vio	Input Offset Voltage	$V_{cc} = 5V, V_{cm} = 1V, R_s \leq 5K$			-0.4	0.4	mV	1

Note 1:  $V_{in} \geq 8mV$  at extremes for  $I_{leak}$  and  $V_{in} \leq -8mV$  at extremes for Vsat ( $V_{in}$  to exceed Vos).

Note 2: 5 Volt differential across +Vcc and -Vcc.

Note 3: Parameter guaranteed by Vio and Iio tests.

Note 4:  $K = V/mV$ .

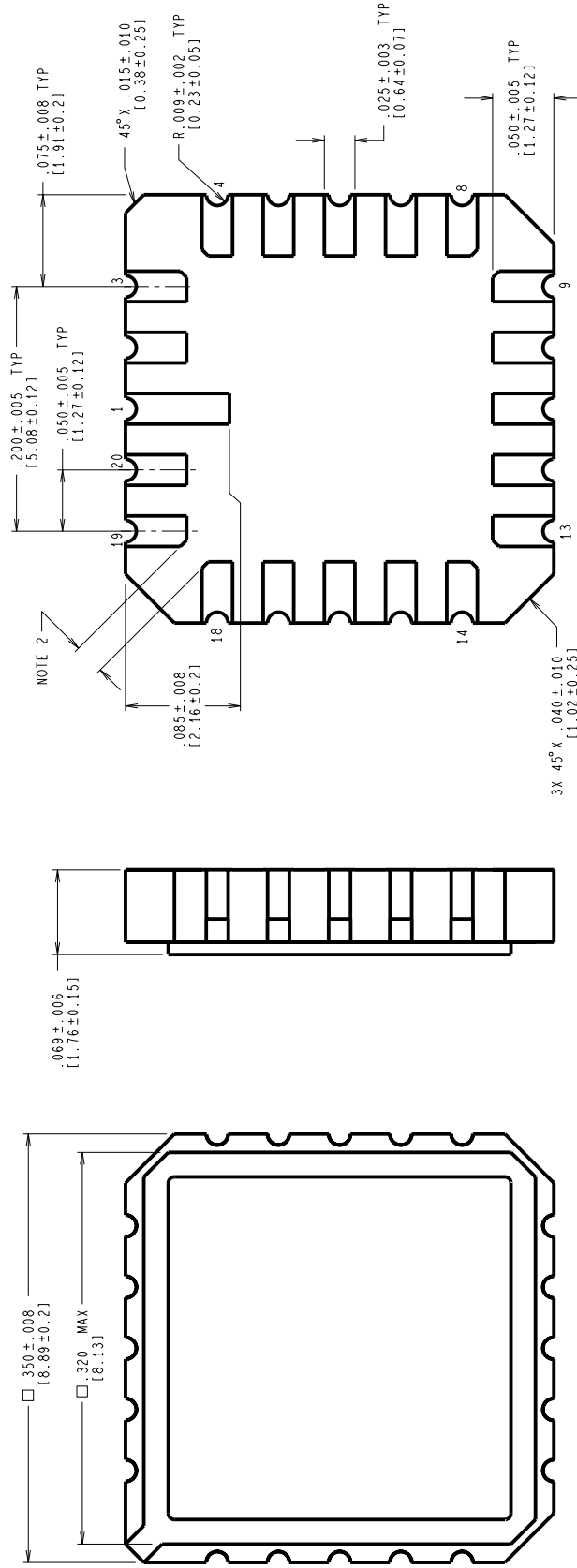
## Graphics and Diagrams

GRAPHICS#	DESCRIPTION
06142HRA3	LCC (E), TYPE C, 20 TERMINAL (B/I CKT)
08906HRB3	METAL CAN (H), 10 LEAD (B/I CKT)
09078HRB3	CERPACK (W), 10 LEAD (B/I CKT)
09641HRA2	CERDIP (J), 14 LEAD (B/I CKT)
E20ARE	LCC (E), TYPE C, 20 TERMINAL(P/P DWG)
H10CRF	METAL CAN (H), TO-100, 10LD, .230 DIA PC (P/P DWG)
J14ARH	CERDIP (J), 14 LEAD (P/P DWG)
P000182A	CERDIP (J), 14 LEAD (PINOUT)
P000196A	LCC (E), 20 LEAD (PINOUT)
P000197A	METAL CAN (H), TO-100, 10 LD, .230 DIA PC (PINOUT)
P000198A	CERPACK (W), 10 LEAD (PINOUT)
P000237A	CERAMIC SOIC (WG), 10 LEAD (PINOUT)
W10ARG	CERPACK (W), 10 LEAD (P/P DWG)
WG10ARC	CERAMIC SOIC (WG), 10 LEAD (P/P DWG)

See attached graphics following this page.

SE  
L1  
LE  
BO

REVISIONS			
LTR	DESCRIPTION	E.C.N.	DATE
E	REVISE AND REDRAW	10005	02/10/94 DEG/



CONTROLLING DIMENSION IS INCH  
VALUES IN [ ] ARE MILLIMETERS

NOTES: UNLESS OTHERWISE SPECIFIED.

- LEAD FINISH TO BE ONE OF THE FOLLOWING:
  - 50 MICRONS/12.7 MICROMETERS MINIMUM GOLD PLATING OVER 50-350 MICRONS/1.27-8.89 MICROMETERS NICKEL.
  - SOLDER DIP. SOLDER THICKNESS PER LATEST REVISION OF MIL-STD-1835.
- CORNER PADS MAY HAVE A  $45^\circ$  X  $0.20$  IN/  $0.51$  mm MAXIMUM CHAMFER TO ACCOMPLISH THE  $.015$  IN/  $0.38$  mm DIMENSION.
- REFERENCE JEDEC REGISTRATION MS-004, VARIATION CB, DATED 7/90.

MIL/AERO  
CONFIGURATION CONTROL

APPROVALS		DATE
DRN	Design	02/10/94
CHK	Eng	
CHK	Approval	

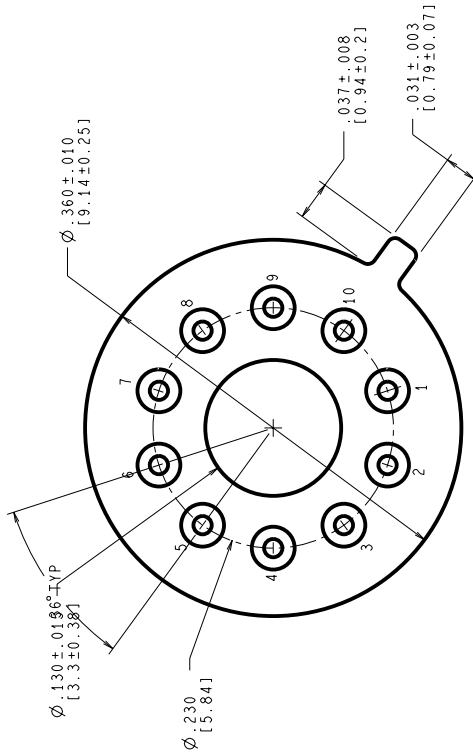
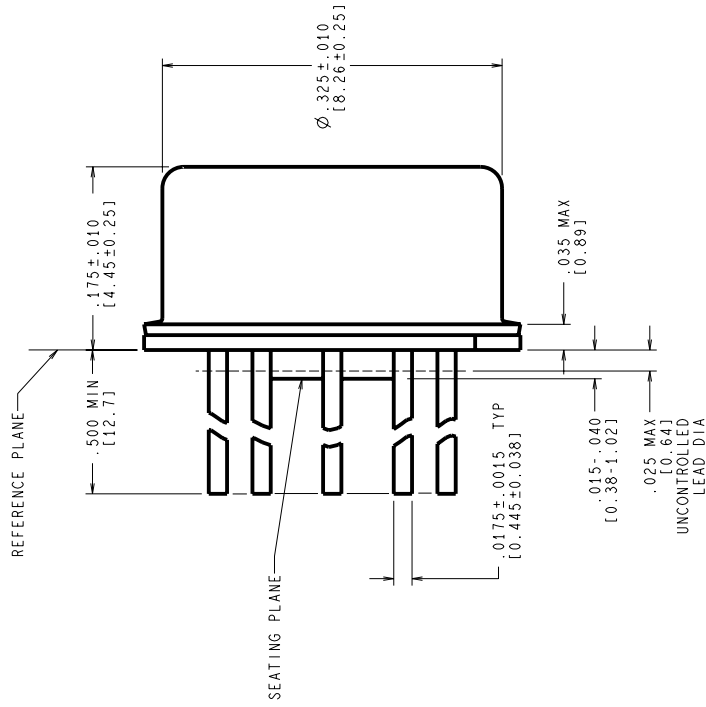
NATIONAL SEMICONDUCTOR CORPORATION		2300 Semiconductor Drive, Santa Clara, CA 95052-8090	
LEADLESS CHIP CARRIER, TYPE C, 20 TERMINAL			
SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-E20A	E

PROJECTION	
DO NOT SCALE DRAWING	SHEET 1 of 1



REVISIONS			
LTR	DESCRIPTION	E.C. N.	DATE
F	REVISE & REDRAW PER CURRENT STANDARD; UPDATE MIL/AERO STAMP & TITLE.	11003	06/26/95
			MS/



CONTROLLING DIMENSION IS INCH  
VALUES IN [ ] ARE MILLIMETERS

MIL-I-38535  
CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

- LEADS TO BE LOCATED WITHIN .007 IN/ 0.18 mm OF THEIR TRUE POSITIONS RELATIVE TO A MAXIMUM WIDTH TAB.
- STANDARD METAL CAN TYPE: SOLID BASE WITH CERAMIC STANDOFF.
- APPLIES TO MIL-AERO AND LINEAR PRODUCTS.
- REFERENCE JEDEC REGISTRATION TO-100, JEDEC PUBLICATION No. 95.

APPROVALS	DATE
DRWY: MARTA SUCHY	06/26/95
DTG: CHK.	
ENGR: CHK.	

PROJECTION		SCALE	SIZE	DRAWING NUMBER	REV
		N/A	C	MKT-H10C	F

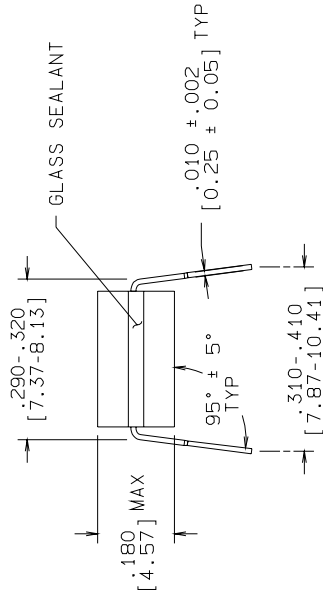
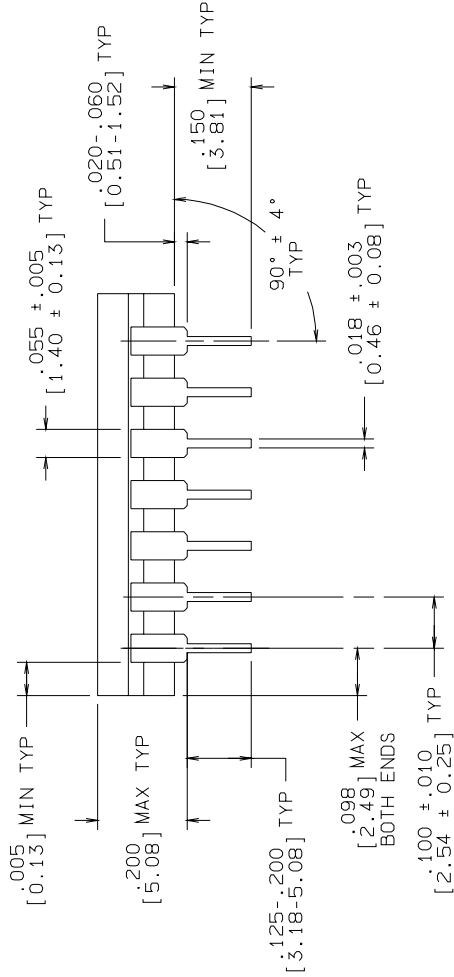
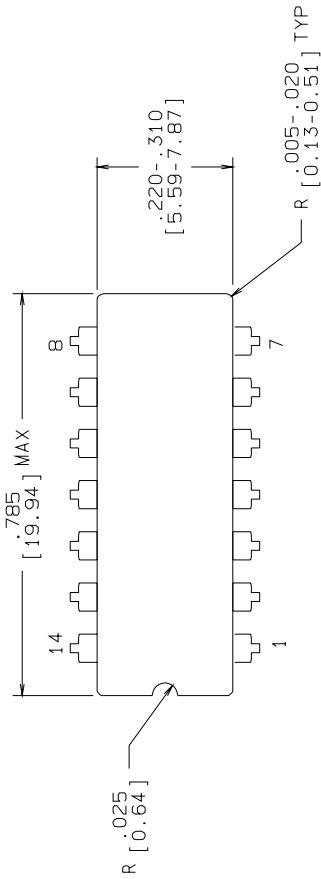
  

National Semiconductor	
2300 Semiconductor Dr., Santa Clara, CA 95052-8090	
METAL CAN	
TO-100, 10 LEAD,	
.230 DIA P.C.	

DO NOT SCALE DRAWING		SHEET 1 of 1	
----------------------	--	--------------	--

R E V I S I O N S			
LTR	DESCRIPTION	E.C.N.	DATE
H	REVISE PER CURRENT STD; REDRAW	10001	09/15/93
			BY/APP'D TL/



MIL/AERO MIL-M-38510  
 CONFIGURATION CONTROL CONFIGURATION CONTROL

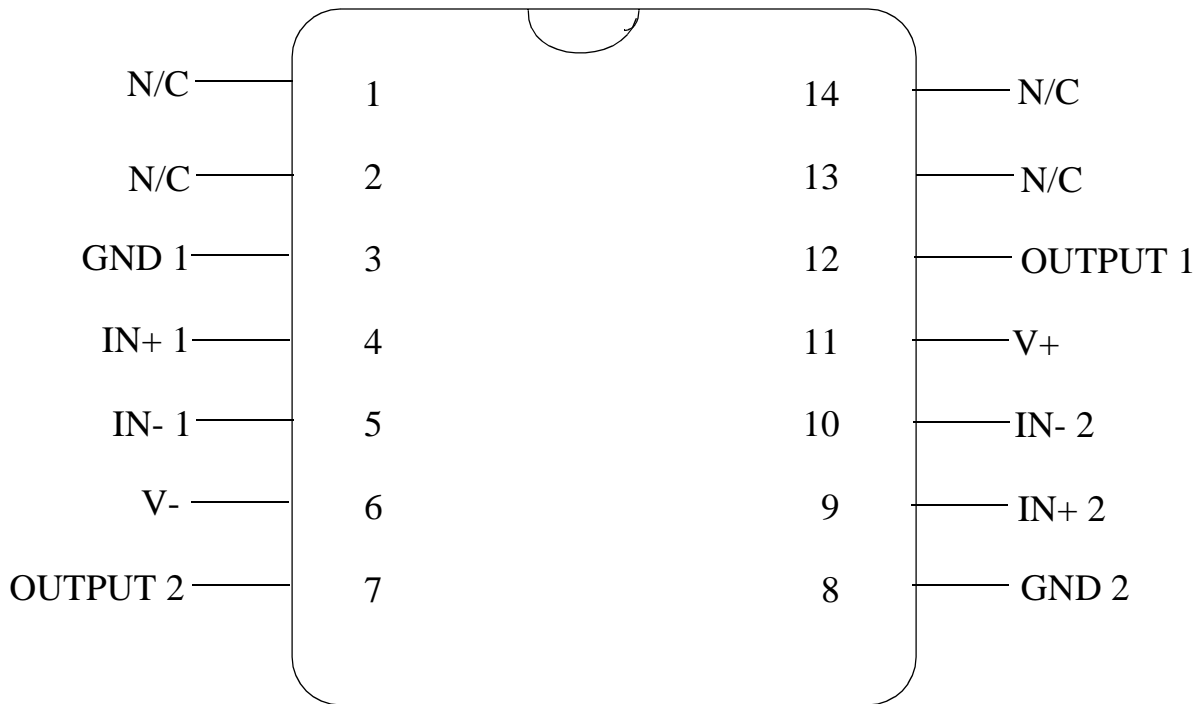
APPROVALS	DATE	NATIONAL SEMICONDUCTOR CORPORATION	
DRAWN <b>T. LEQUANG</b>	09/15/93	2900 Semiconductor Drive, Santa Clara, CA 95052-8090	
DFTG. CHK.			
ENGR. CHK.			
APPROVAL			
 PROJECTION INCH [MM]	SCALE	N/A	REV
	DRAWING NUMBER	B	H
	DO NOT SCALE DRAWING	MKT-J14A	1 OF 1

NOTES: UNLESS OTHERWISE SPECIFIED

- LEAD FINISH TO BE 200 MICRONS / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
- JEDEC REGISTRATION MO-036, VARIATION AB, DATED 04/1981.

CONTROLLING DIMENSION: INCH

CERDIP (J),  
 14 LEAD,

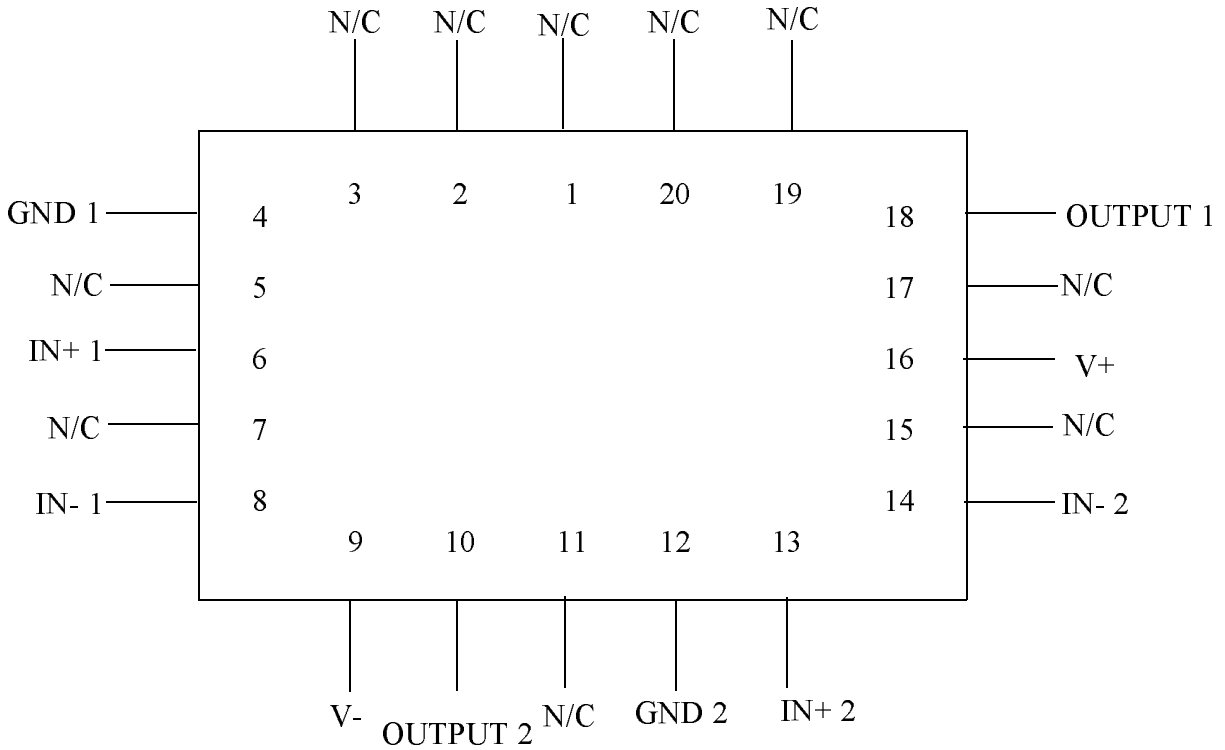


**LM119J**  
**14 - LEAD DIP**  
**CONNECTION DIAGRAM**  
**TOP VIEW**  
**P000182A**



National Semiconductor™

MIL/AEROSPACE OPERATIONS  
 2900 SEMICONDUCTOR DRIVE  
 SANTA CLARA, CA 95050

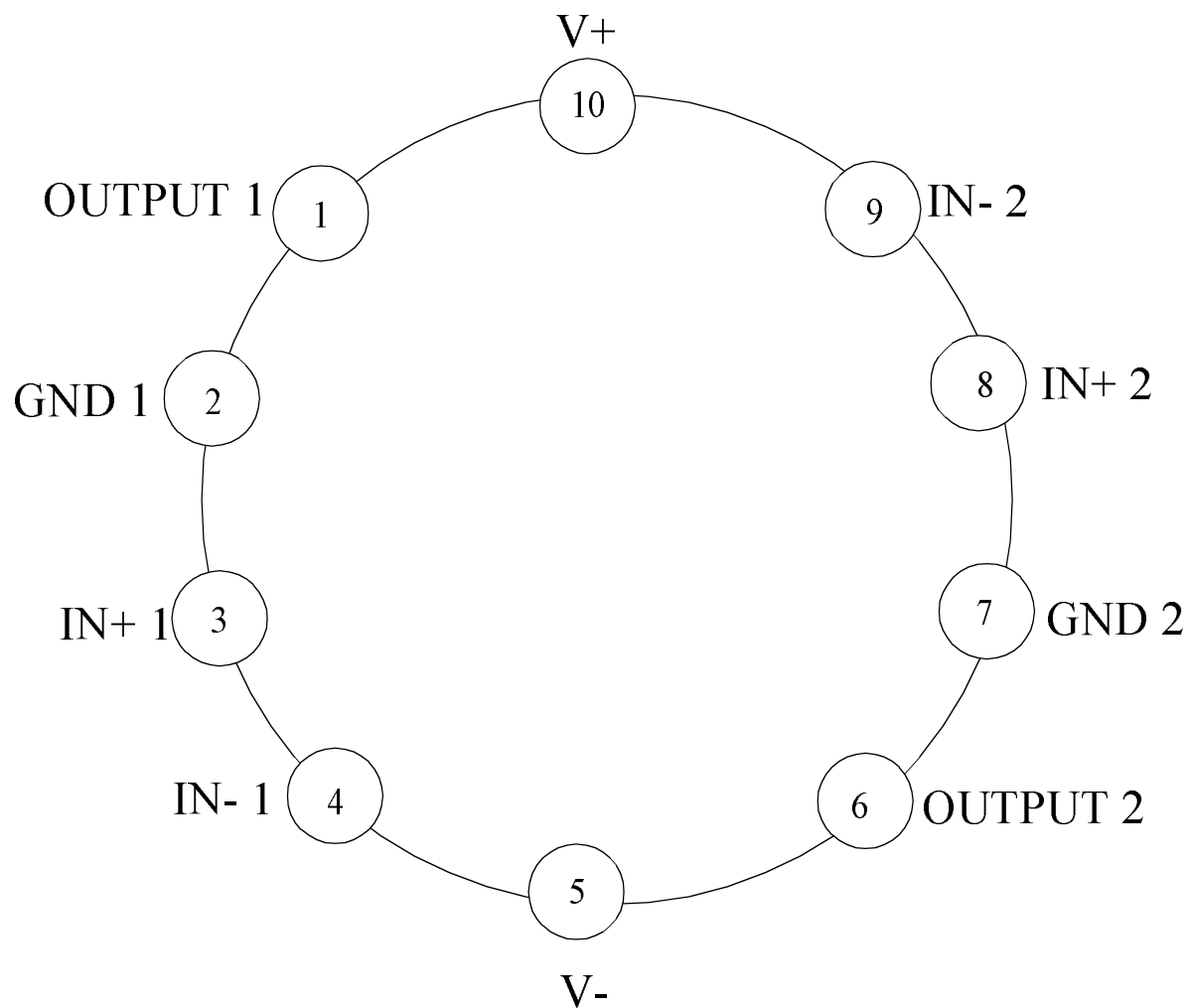


**LM119E**  
**20 - LEAD LCC**  
**CONNECTION DIAGRAM**  
**TOP VIEW**  
**P000196A**



National Semiconductor™

MIL/AEROSPACE OPERATIONS  
 2900 SEMICONDUCTOR DRIVE  
 SANTA CLARA, CA 95050

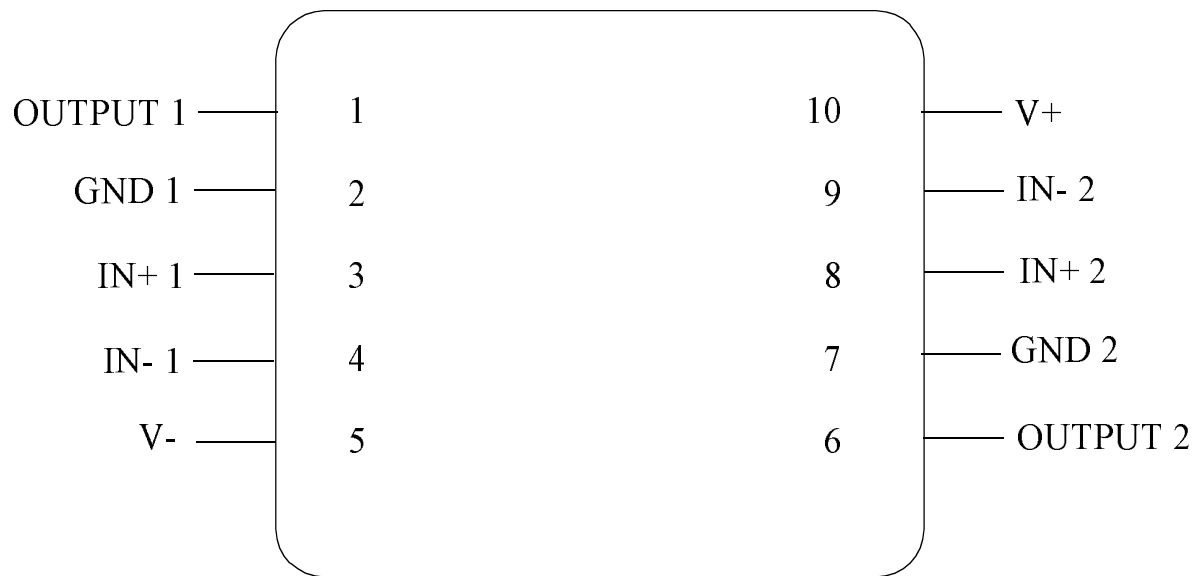


**LM119H**  
**10 - PIN METAL CAN**  
**CONNECTION DIAGRAM**  
**TOP VIEW**  
**P000197A**



National Semiconductor™

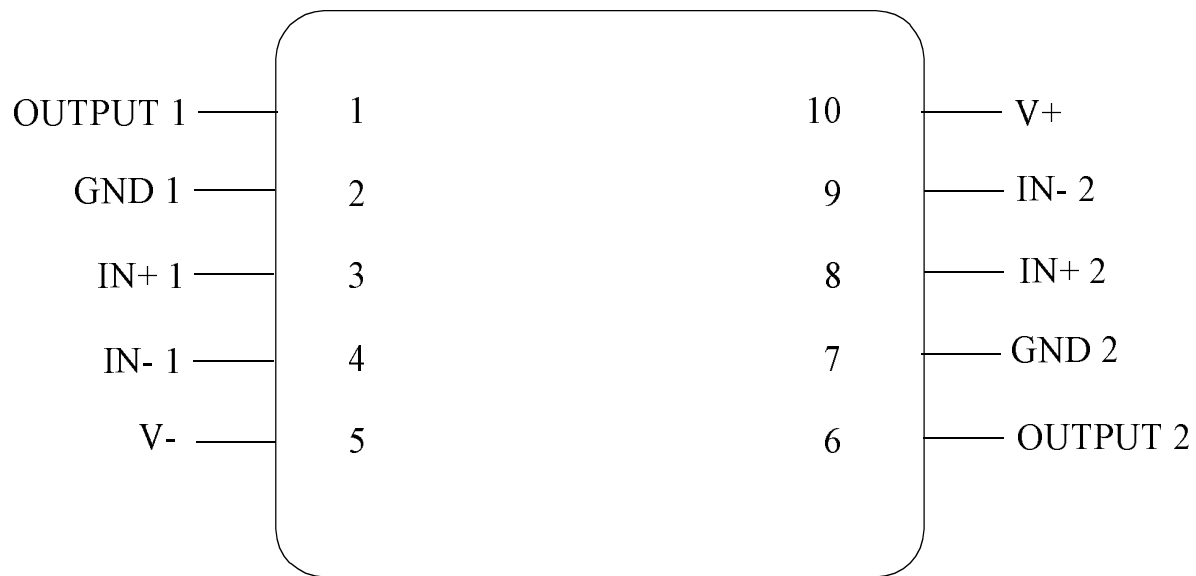
MIL/AEROSPACE OPERATIONS  
 2900 SEMICONDUCTOR DRIVE  
 SANTA CLARA, CA 95050



LM119W  
10 - LEAD CERPACK  
CONNECTION DIAGRAM  
TOP VIEW  
P000198A



National Semiconductor™  
MIL/AEROSPACE OPERATIONS  
2900 SEMICONDUCTOR DRIVE  
SANTA CLARA, CA 95050

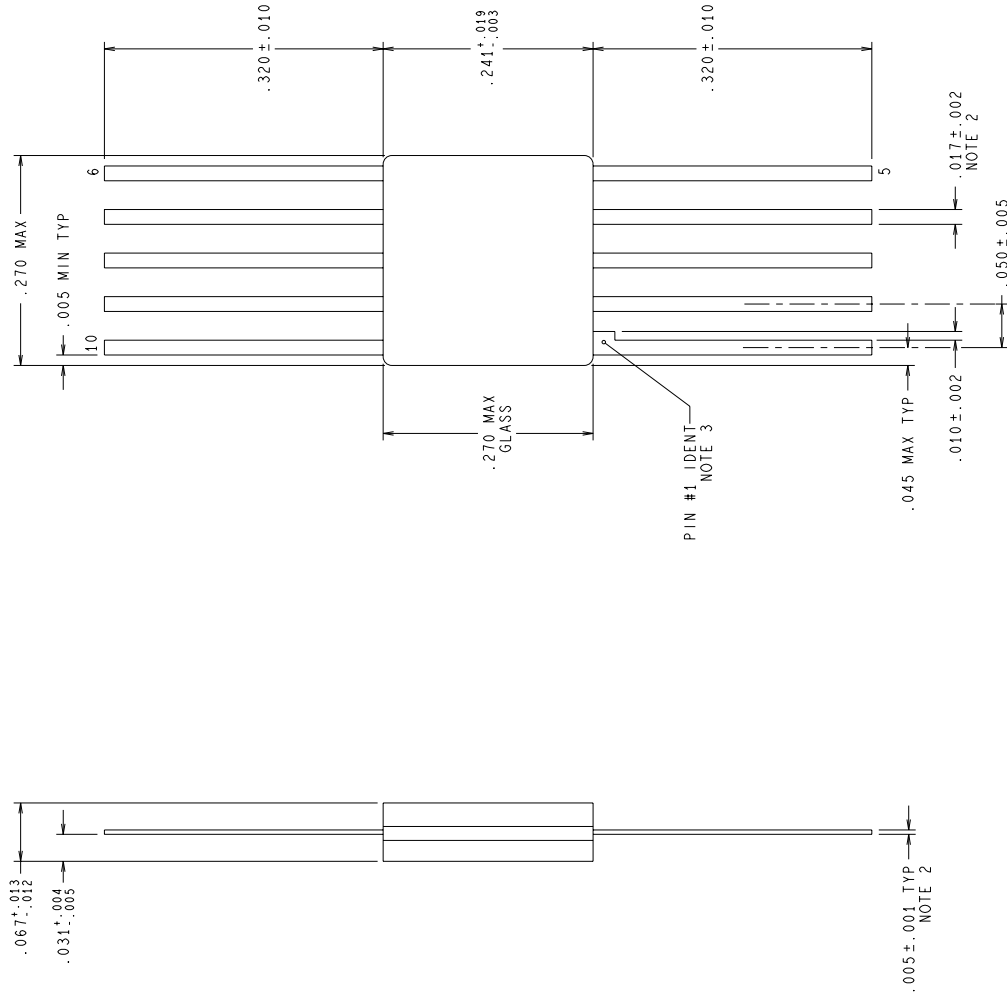


LM119WG  
10 - LEAD CERAMIC SOIC  
CONNECTION DIAGRAM  
TOP VIEW  
P000237A



National Semiconductor™  
MIL/AEROSPACE OPERATIONS  
2900 SEMICONDUCTOR DRIVE  
SANTA CLARA, CA 95050

REVISIONS			
LTR	DESCRIPTION	E.C. N.	DATE
F	REVISE AND REDRAW PER NEW STANDARD.	10510	07/28/94 DEG/AEP
G	.017±.002 WAS .017±.020.	10654	10/21/94 DEG/



NOTES: UNLESS OTHERWISE SPECIFIED.

- LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-M-38510 TO A MINIMUM THICKNESS OF 200 MICRONS. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE.
- MAXIMUM LIMIT MAY BE INCREASED BY .003 INCHES AFTER LEAD FINISH APPLIED.
- LEAD 1 IDENTIFICATION SHALL BE:
  - A NOTCH OR OTHER MARK WITHIN THIS AREA
  - A TAB ON LEAD 1, EITHER SIDE
- REFERENCE JEDEC REGISTRATION M0-003, VARIATION AG, DATED 06/01/76.

MIL/AERO  
CONFIGURATION CONTROL

MIL-M-38510  
CONFIGURATION CONTROL

APPROVALS		DATE	
DRWN	<i>D. F. Grady</i>		07/28/94
DTG. CHK.			
ENGR. CHK.			

PROJECTION			
1/8" MIN			

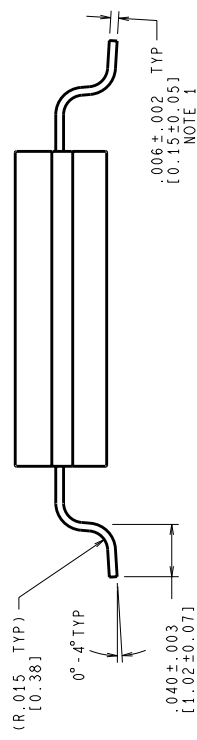
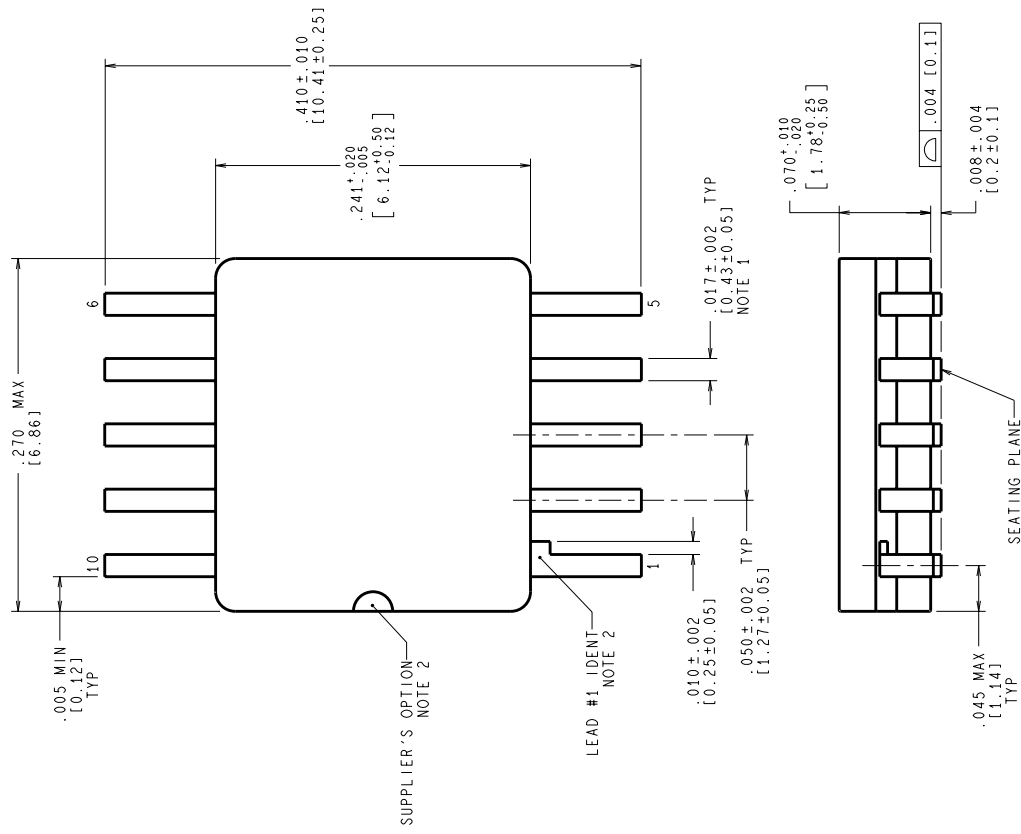
National Semiconductor			
2800 Semiconductor Dr., Santa Clara, CA 95052-8090			
SCALE		DRAWING NUMBER	
N/A		MKT-W10A	
DO NOT SCALE DRAWING		SHEET 1 of 1	

CERPACK, 10 LEAD



REVISIONS

LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	11374	02/29/1996	MS/KH
B	LD PITCH TOL WAS ±.005; CHANGE LD RADIUS TO REF DIM; REMOVE THE OTHER R.006±.002 DIM. .040±.003 WAS .037±.003	11441	04/19/1996	MS/KH
C	R .015(0.38) WAS R .006(0.15)	11838	10/08/1997	TL/



CONTROLLING DIMENSION IS INCH  
VALUES IN | ARE MILLIMETERS

MIL-PRF-38535  
CONFIGURATION CONTROL

- NOTES: UNLESS OTHERWISE SPECIFIED
- LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-PRF-38535 TO A MINIMUM THICKNESS OF 200 MICRONS/ 5.08 MICROMETERS. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE. MAXIMUM LIMIT MAY BE INCREASED BY .003 IN/ 0.08mm AFTER LEAD FINISH APPLIED.
  - LEAD 1 IDENTIFICATION SHALL BE:
    - A NOTCH OR OTHER MARK WITHIN THIS AREA
    - A TAB ON LEAD 1, EITHER SIDE
  - NO JEDEC REGISTRATION AS OF FEBRUARY 1996.

APPROVALS	DATE	SCALE	SIZE	DRAWING NUMBER	REV
DRN: MARYA SUCHY	02/29/96	N/A	C	(SC)MKT-WG10A	C
DATE: 02/29/96					
CHK: [Signature]					
CHK: [Signature]					
PROJECTION					
NATIONAL SEMICONDUCTOR 2800 Semiconductor Dr., Santa Clara, CA 95052-8090 CERPACK, 10 LEAD, GULL WING					
DO NOT SCALE DRAWING SHEET 1 of 1					

## Revision History

Rev	ECN #	Rel Date	Originator	Changes
0B0	M0001371	02/25/98	Barbara Lopez	Added Power Dissipation - Note 2 in Absolute section. Renumbered all other notes. Archive MDS - MDLM119-X Rev. 0A0. Release MDS - MDLM119-X Rev. 0B0.
0C1	M0002726	12/06/99	Barbara Lopez	Update MDS: MDLM119-X Rev. 0B0 to MDLM119-X Rev. 0C1. Added WG package to MDS. Added MKT outline, Burn-In CKT and Pinouts.
1C1	M0003596	12/06/99	Rose Malone	Archive MDLM119-X, Rev. 0C1. MDS replaced by MDLM119-X-RH, Rev. 0A0. MDS is being archived as Rev. 1C1.
2A2	M0003821	07/11/01	Rose Malone	De-Archived MDS: MDLM119-X, Re-Instate back into system at Rev. 2A2. Removed Rad Devices, MDLM119-X references Non Rad Devices ONLY. MDLM119-X, Rev. 2A2 replaces MDLM119-X-RH