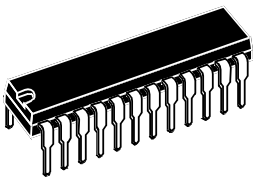
TEA6422

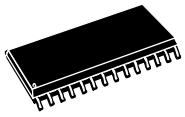
BUS-CONTROLLED AUDIO MATRIX

- 6 Stereo Inputs
- 3 Stereo Ouputs
- Gain Control 0 dB/Mute for each Output
- Cascadable (2 different addresses)
- Serial Bus Controlled
- Very Low Noise
- Very Low Distorsion
- Fully ESD Protected
- Wide Audio Dynamic Range (3 V_{RMS})



SHRINK DIP24
(Shrink Plastic Package)

ORDER CODE: TEA6422



SO28
(Plastic Monopackage)

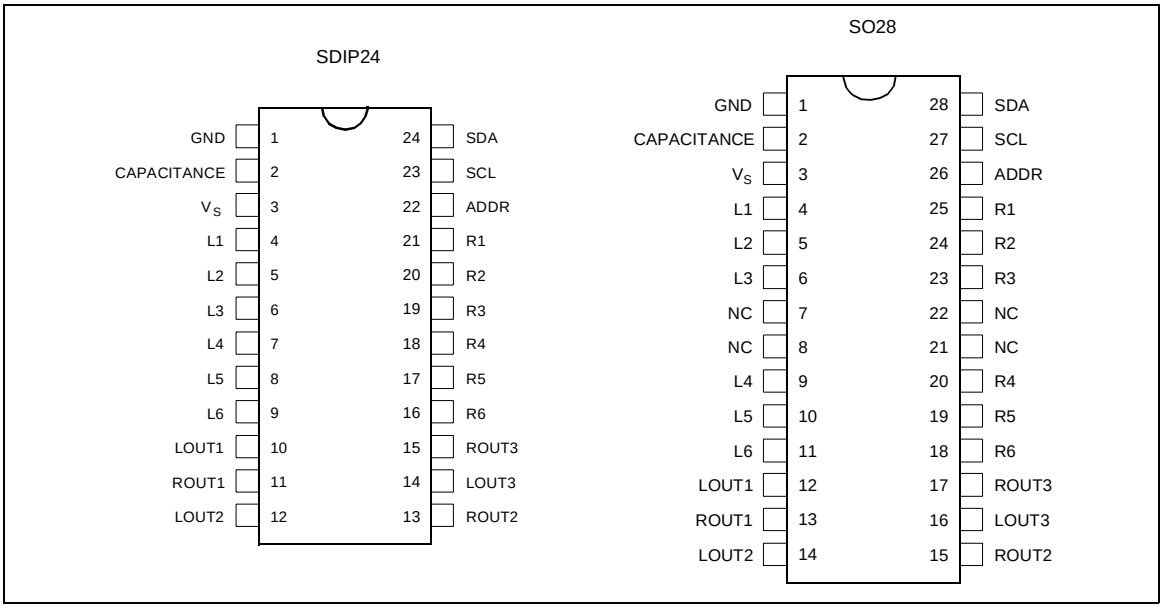
ORDER CODE: TEA6422D

DESCRIPTION

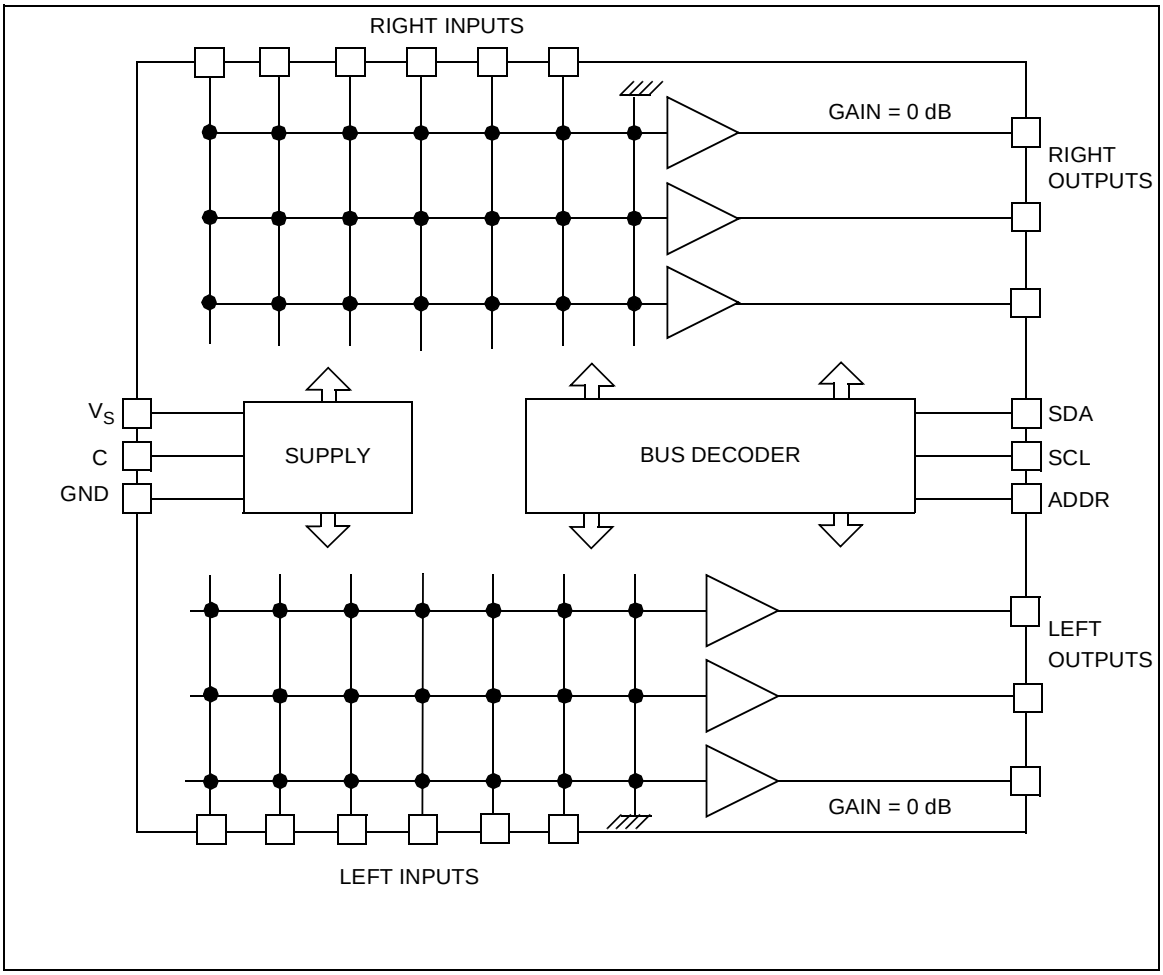
The TEA6422 switches 6 stereo audio inputs on 3 stereo outputs.

All the switching possibilities are changed through the I^2C BUS.

Figure 1. PIN CONNECTIONS



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	12	V
T_{oper}	Operating Temperature	0, + 70	^{o}C
T_{stg}	Storage Temperature	- 20, + 150	^{o}C

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th(j-a)}$	Junction - ambient Thermal Resistance	SDIP24 SO28	75 75	^{o}C/W ^{o}C/W

ELECTRICAL CHARACTERISTICS

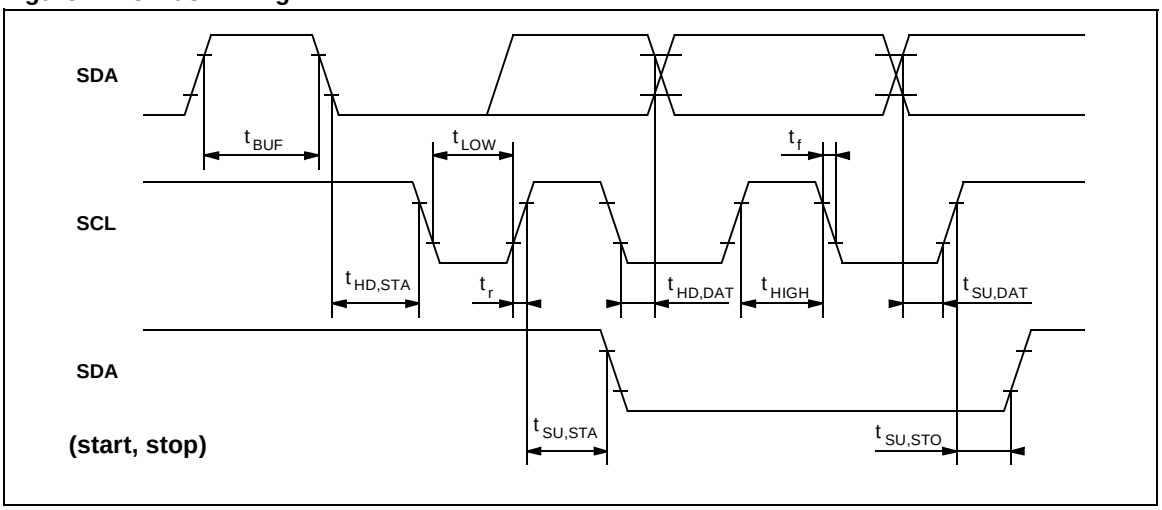
T_A = 25 °C, V_S = 9 V, R_L = 10 kΩ, R_G = 600 Ω, f = 1 kHz (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
SUPPLY						
V_S	Supply Voltage		8	10	11	V
I_S	Supply Current			3	8	mA
SVR	Ripple Rejection	V_{IN} = 500mV_{RMS}, f = 1kHz	70	80		dB
MATRIX						
V_{IN}	Input DC Level			V_{CC}/2		V
R_I	Input Resistance		30	50	100	kΩ
C_S	Channel Separation	V_{IN} = 2V_{RMS}, f = 1kHz	80	90		dB
OUTPUT BUFFER						
V_{OUT}	Output DC Level			V_{CC}/2		V
R_{OUT}	Output Resistance			50	100	Ω
e_{NI}	Input Noise	BW = 20 - 20kHz, flat		3		µV
S/N	Signal to Noise Ratio	V_{IN} = V_{OUT} = 1V_{RMS}		110		dB
G	Gain		-1	0	+ 1	dB
d	Distortion	V_{IN} = V_{OUT} = 1V_{RMS}		0.01	0.05	%
V_{CL}	Clipping Level	d = 0.3 %, V_S = 10 V	2.8	3		V_{RMS}
R_L	Output Load Resistance		2			kΩ

I²C BUS CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
SCL					
V_{IL}	Low Level Input Voltage		- 0.3	+ 1.5	V
V_{IH}	High Level Input Voltage		3.0	V_{CC} + 0.5	V
I_{LI}	Input Leakage Current	V_I = 0 to V_{CC}	- 10	+ 10	µA
f_{SCL}	Clock Frequency		0	100	kHz
t_R	Input Rise Time	1.5V to 3V		1000	ns
t_F	Input Fall Time	3V to 1.5V		300	ns
C_I	Input Capacitance			10	pF
SDA					
V_{IL}	Low Level Input Voltage		- 0.3	+ 1.5	V
V_{IH}	High Level Input Voltage		3.0	V_{CC} + 0.5	V
I_{LI}	Input Leakage Current	V_I = 0 to V_{CC}	- 10	+ 10	µA
C_I	Input Capacitance			10	pF
t_R	Input Rise Time	1.5V to 3V		1000	ns
t_F	Input Fall Time	3V to 1.5V		300	ns
V_{OL}	Low Level Output Voltage	I_{OL} = 3mA		0.4	V
t_F	Output Fall Time	3V to 1.5V		250	ns
C_L	Load Capacitance			400	pF
TIMING					
t_{LOW}	Clock Low Period		4.7		µs
t_{HIGH}	Clock High Period		4.0		µs
t_{SU}, DAT	Data Set-up Time		250		ns
t_{HD}, DAT	Data Hold Time		0	340	ns
t_{SU}, STO	Set-up Time from Clock High to Stop		4.0		µs
t_{BUF}	Start Set-up Time following a Stop		4.7		µs
t_{HD}, STA	Start Hold Time		4.0		µs
t_{SU}, STA	Start Set-up Time following Clock Low-to High Transition		4.7		µs

Figure 2. I²C Bus Timing



POWER ON RESET

After power-on reset all outputs are in mute mode

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Reset	Start of Reset	Incr. V_{CC}			2.5	V
		Decr. V_{CC}			4.2	V
	End of Reset	Incr. V_{CC}	4.5			V

SOFTWARE SPECIFICATION

1. Chip address

Address	HEX	ADDR
1001 1000	98	0
1001 1010	9A	1

2. Data bytes

Output select

X	0 0 1	0 1 0	X	X	I_2	I_1	I_0	Output 1 Output 2 Output 3

Input select

X	Q_1	Q0	X	X	0 0 0 0 1 1 1	0 0 1 1 0 0 1	0 1 0 1 0 1 0	Input 1 Input 2 Input 3 Input 4 Input 5 Input 6 Mute

X = don't care - MSB is transmitted first

Example : 010XX100 connects output 3 with input 5.

Figure 3. Distorsion Level versus Input Voltage

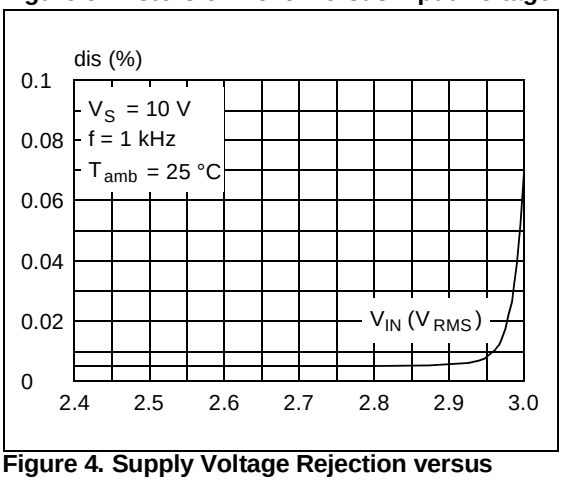


Figure 4. Supply Voltage Rejection versus Frequency (V_{IN} = 500 mV_{RMS})

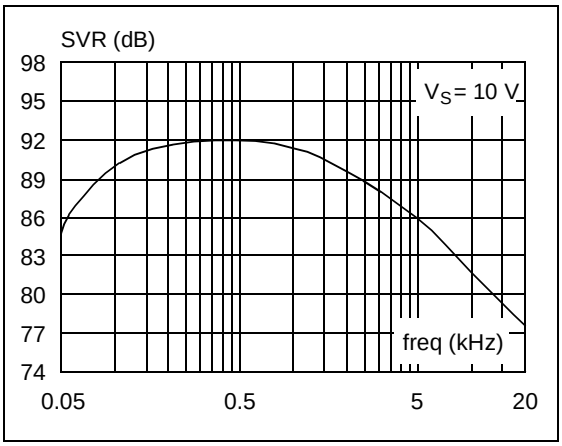
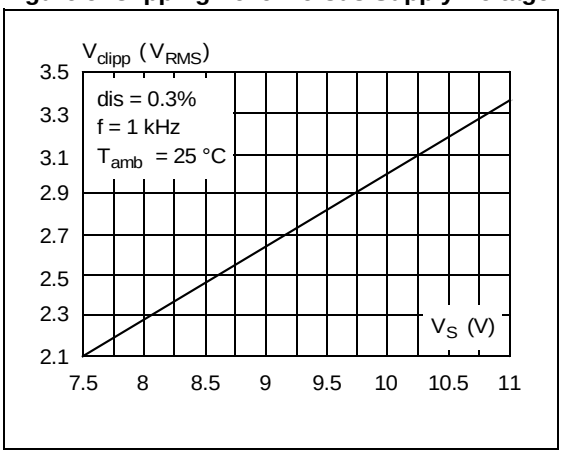


Figure 5. Clipping Level versus Supply Voltage



PIN CONFIGURATIONS (SDIP24 Package)

Figure 6. Audio IN

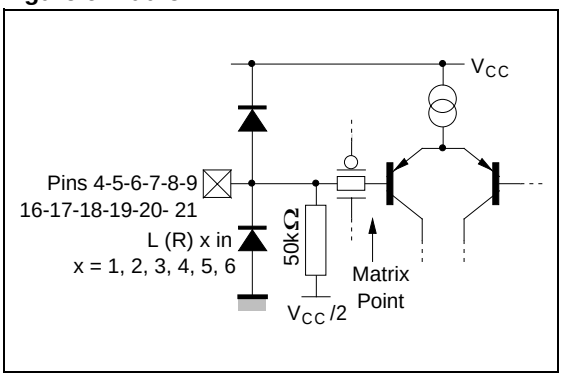


Figure 8. Audio OUT

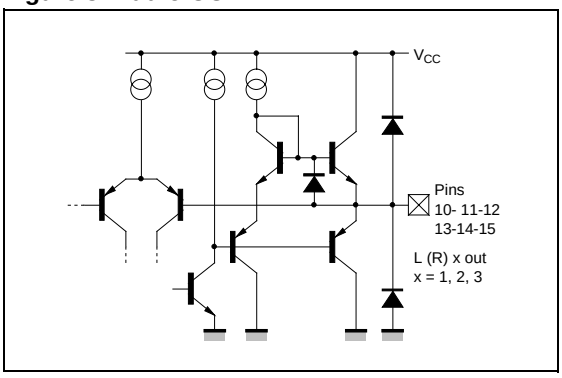


Figure 7. ADDR

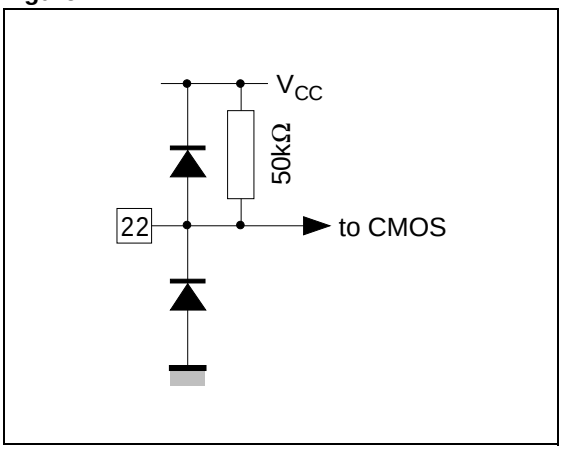


Figure 9. Bus Inputs (SDA, SCL)

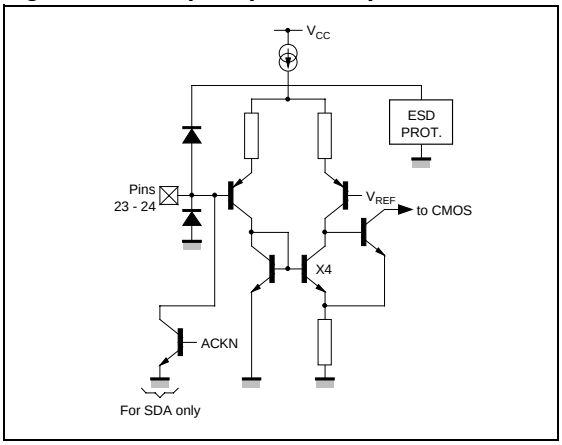
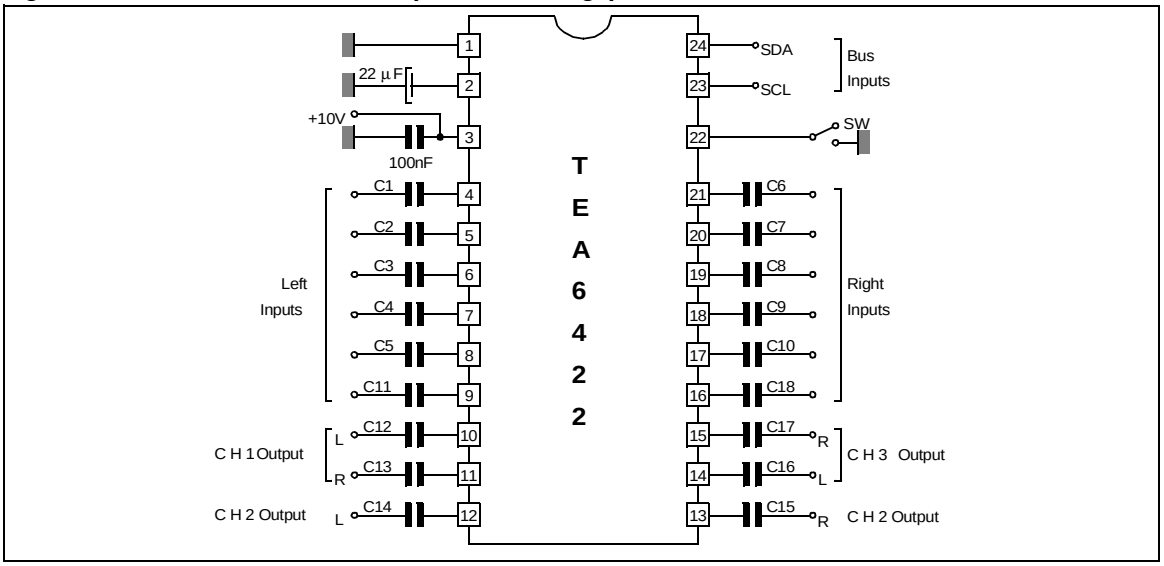


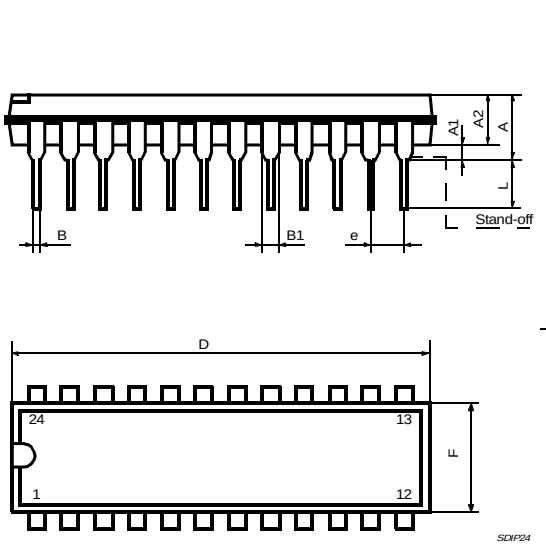
Figure 10. TYPICAL APPLICATION (SDIP24 Package)



PACKAGE MECHANICAL DATA

24 PINS - PLASTIC SHRINK

Figure 11. 24-Pin Shrink Plastic Dual In Line Package

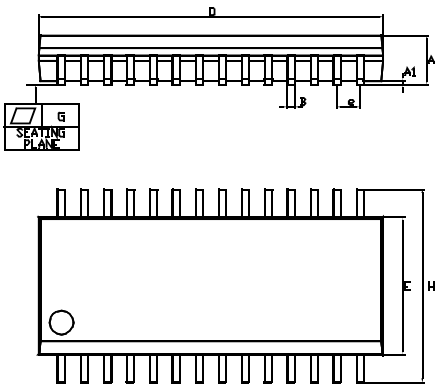


Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			5.08			0.20
A1	0.51			0.020		
A2	3.05	3.30	4.57	0.120	0.130	0.180
B	0.36	0.46	0.56	0.0142	0.0181	0.0220
B1	0.76	1.02	1.14	0.030	0.040	0.045
C	0.23	0.25	0.38	0.0090	0.0098	0.0150
D	22.61	22.86	23.11	0.890	0.90	0.910
E	7.62		8.64	0.30		0.340
E1	6.10	6.40	6.86	0.240	0.252	0.270
e		1.778			0.070	
e1		7.62			0.30	
e2			10.92			0.430
e3			1.52			0.060
	Number of Pins					
N	24					

PACKAGE MECHANICAL DATA

28 PINS - PLASTIC MICROPACKAGE

Figure 12. 28-Pin Plastic Small Outline Package, 300-mil Width



SO28

Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	2.35		2.65	0.0926		0.1043
A1	0.10		0.30	0.0040		0.0118
B	0.33		0.51	0.013		0.020
C	0.23		0.32	0.0091		0.0125
D	17.70		18.10	0.6969		0.7125
E	7.40		7.60	0.2914		0.2992
e		1.27			0.0500	
H	10.01		10.64	0.394		0.419
h	0.25		0.74	0.010		0.029
K				0°		8°
L	0.41		1.27	0.016		0.050
G			0.10			0.004
	Number of Pins					
N	28					