## **General Description**

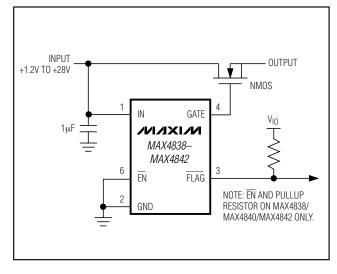
### Features

- Overvoltage Protection Up to 28V
- Preset 7.4V, 5.8V, or 4.7V Overvoltage Trip Level
- Drive Low-Cost NMOS FET
- Internal 50ms Startup Delay
- Internal Charge Pump
- Undervoltage Lockout
- 15kV ESD-Protected Input
- Voltage Fault FLAG Indicator
- 6-Pin SC70 Package

# **Ordering Information**

PART	TEMP RANGE	PIN- PACKAGE	TOP MARK
MAX4838EXT-T	-40°C to +85°C	6 SC70-6	ABW
MAX4839EXT-T	-40°C to +85°C	6 SC70-6	ABY
MAX4840EXT-T	-40°C to +85°C	6 SC70-6	ABX
MAX4841EXT-T	-40°C to +85°C	6 SC70-6	ABZ
MAX4842EXT-T	-40°C to +85°C	6 SC70-6	ACE

# Typical Operating Circuit



Pin Configuration appears at end of data sheet.

Maxim Integrated Products 1

The MAX4838-MAX4842 are overvoltage protection ICs that protect low-voltage systems against voltages of up to 28V. If the input voltage exceeds the overvoltage trip level, the MAX4838-MAX4842 turn off the low-cost external n-channel FET(s) to prevent damage to the protected components. An internal charge pump elimi-

FET gate for a simple, robust solution. The MAX4838/MAX4839 have a 7.4V overvoltage threshold, and the MAX4840/MAX4841 have a 5.8V overvoltage threshold. The MAX4842 has a 4.7V overvoltage threshold. The MAX4838-MAX4841 have an undervoltage lockout (UVLO) threshold of 3.25V while the MAX4842 has a UVLO of 3.0V. In addition to the single FET configuration, the devices can be configured with back-to-back external FETs to prevent currents from being back-driven into the adapter.

nates the need for external capacitors and drives the

On power-up, the device waits for 50ms before driving GATE high. FLAG is held low for an additional 50ms after GATE goes high before deasserting. The MAX4838/MAX4840/MAX4842 have an open-drain FLAG output, and the MAX4839/MAX4841 have a pushpull FLAG output. The FLAG output asserts immediately to an overvoltage fault.

Additional features include a 15kV ESD-protected input (when bypassed with a 1µF capacitor) and a shutdown pin (EN) to turn off the device (MAX4838/MAX4840/ MAX4842).

All devices are offered in a small 6-pin SC70 package and are specified for operation from -40°C to +85°C.

> **Cell Phones Digital Still Cameras** PDAs and Palmtop Devices **MP3** Players

## Selector Guide

Applications

PART	UVLO THRESHOLD (V)	OV TRIP LEVEL (V)	En Input	FLAG OUTPUT
MAX4838EXT-T	3.25	7.4	Yes	Open-Drain
MAX4839EXT-T	3.25	7.4	No	Push-Pull
MAX4840EXT-T	3.25	5.8	Yes	Open-Drain
MAX4841EXT-T	3.25	5.8	No	Push-Pull
MAX4842EXT-T	3.00	4.7	Yes	Open-Drain

# M/IXI/M

For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

## **ABSOLUTE MAXIMUM RATINGS**

IN to GND	0.3V to +30V
GATE to GND	0.3V to +12V
EN, FLAG to GND	0.3V to +6V
Continuous Power Dissipation ( $T_A = +70^{\circ}C$	:)
6-Pin SC70 (derate 3.1mW/°C above +70	0°C)

Operating Temperature Range	40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	65°C to +150°C
Lead Temperature (soldering, 1	0s)+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## **ELECTRICAL CHARACTERISTICS**

 $(V_{IN} = +5V (MAX4838-MAX4841), V_{IN} = +4V (MAX4842), T_A = -40^{\circ}C \text{ to } +85^{\circ}C, \text{ unless otherwise noted. Typical values are at T_A = +25^{\circ}C.) (Note 1)$ 

PARAMETER	SYMBOL			MIN	TYP	МАХ	UNITS	
Input Voltage Range	VIN			1.2		28.0	V	
	1.11.41.0		MAX4838-MAX4841	3.0	3.25	3.5	- V	
Undervoltage Lockout Threshold	UVLO	V <sub>IN</sub> falling	MAX4842	2.8	3.0	3.2		
Undervoltage Lockout Hysteresis					50		mV	
		MAX4838/MAX4839		7.0	7.4	7.8	v	
Overvoltage Trip Level	OVLO	MAX4840/MAX4841		5.5	5.8	6.1		
		MAX4842		4.4	4.7	5.0		
		MAX4838/MAX4839			100			
Overvoltage Trip Level Hysteresis		MAX4840/MAX4841			80		mV	
		MAX4842			50		1	
IN Supply Current	lusi	No load, <del>EN</del> = GND or 5.5V, V <sub>IN</sub> = 5.4V (MAX4838–MAX4841)			140	240	- μΑ	
in supply current	lin	No load, $\overline{EN} = GND$ or 4.4V, V <sub>IN</sub> = 4.3V (MAX4842)			130	220		
UVLO Supply Current		V <sub>IN</sub> = 2.9V (MAX4838–MAX4841), V <sub>IN</sub> = 2.7V (MAX4842)				150	μA	
	VGATE	IGATE sourcing 1µA	MAX4838-MAX4841	9		10		
GATE Voltage			MAX4842	7.5		8.0	V	
GATE Pulldown Current	IPD	VIN > VOVLO, VGATE	= 5.5V		60		mA	
		1.2V ≤ V <sub>IN</sub> < UVLO, Is	SINK = 50µA			0.4		
FLAG Output Low Voltage	V <sub>OL</sub>	$V_{IN} \ge OVLO, I_{SINK} = 1mA$				0.4	V	
FLAG Output High Voltage	V <sub>OH</sub>	ISOURCE = 100µA, FLAG deasserted, MAX4839/MAX4841		2.4			V	
FLAG Output High Leakage	IOH	V <sub>FLAG</sub> = 5.5V, FLAG deasserted, MAX4838/MAX4840/MAX4842				1	μA	
EN Input High Voltage	VIH	MAX4838/MAX4840/MAX4842		1.47			V	
EN Input Low Voltage	VIL	MAX4838/MAX4840/MAX4842				0.65	V	
EN Input Leakage	I <sub>LKG</sub>	MAX4838/MAX4840/MAX4842, EN = GND or 5.5V				1	μA	
IN ESD rating		CurrentuE	Human Body Model		15			
IN ESD rating		$C_{IN} \ge 1\mu F$ IEC 1000-4-2			15		kV	

2

MAX4838-MAX4842

M/X/M

# **ELECTRICAL CHARACTERISTICS (continued)**

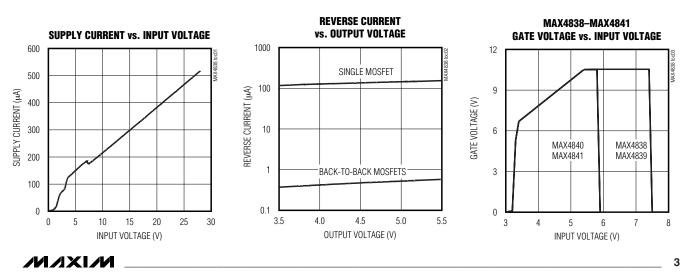
(V<sub>IN</sub> = +5V (MAX4838–MAX4841), V<sub>IN</sub> = +4V (MAX4842), T<sub>A</sub> = -40°C to +85°C, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C.) (Note 1)

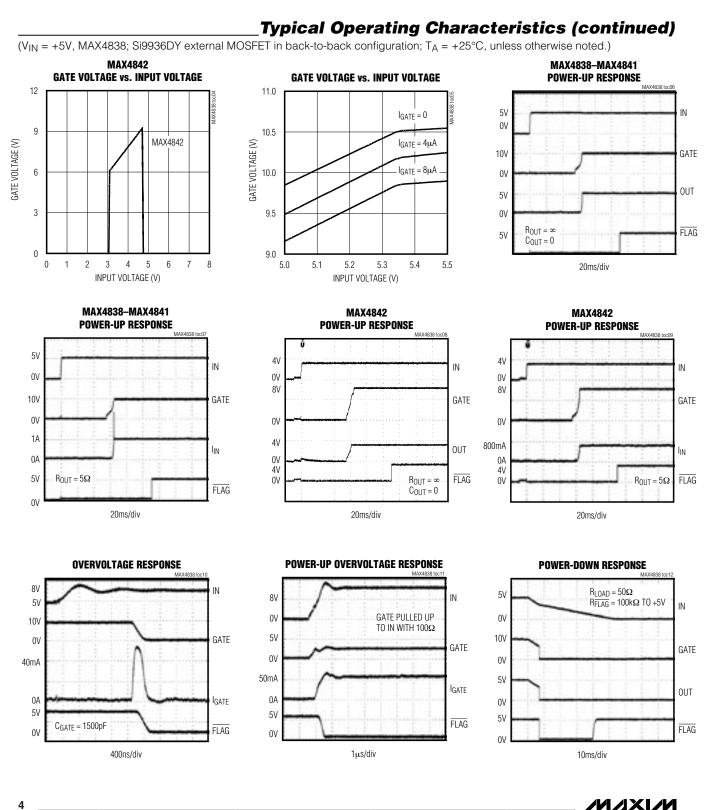
PARAMETER	PARAMETER SYMBOL CONDITIONS		MIN	ТҮР	MAX	UNITS
TIMING		•				
Startup Delay	<b>t</b> START	VIN > VUVLO, VGATE > 0.3V, Figure 1	20	50	80	ms
FLAG Blanking Time	<b>t</b> BLANK	$V_{GATE} = 0.3V, V_{FLAG} = 2.4V, Figure 1$	20	50	80	ms
GATE Turn-On Time	tgon	$V_{GATE} = 0.3V \text{ to } 8V \text{ (MAX4838-MAX4841)}, V_{GATE} = 0.3V \text{ to } 6V \text{ (MAX4842)}, C_{GATE} = 1500 \text{pF}, Figure 1$		10		ms
GATE Turn-Off Time	tGOFF	$ \begin{array}{l} V_{IN} \text{ increasing from 5V to 8V at 3V/} \mu s \\ (MAX4838-MAX4841), V_{IN} \text{ increasing from} \\ 4V to 6V at 2V/} \mu s (MAX4842), \\ V_{GATE} = 0.3V, C_{GATE} = 1500 \text{pF}, Figure 2 \\ \end{array} $	6 20			μs
FLAG Assertion Delay	tFLAG	$V_{IN}$ increasing from 5V to 8V at 3V/µs (MAX4838–MAX4841), $V_{IN}$ increasing from 4V to 6V at 2V/µs (MAX4842), $V_{FLAG}$ = 0.4V, Figure 2		5.8		μs
Initial Overvoltage Fault Delay	tovp	$V_{\rm IN}$ increasing from 0 to 8V (MAX4838–MAX4841), $V_{\rm IN}$ increasing from 0V to 6V (MAX4842), I <sub>GATE</sub> = 80% of I <sub>PD</sub> , Figure 3		100		ns
Disable Time	tDIS	VEN = 2.4V, V <sub>GATE</sub> = 0.3V, MAX4838/MAX4840/MAX4842, Figure 4	re 4 580		ns	

Note 1: All parts are 100% tested at +25°C. Electrical limits across the full temperature range are guaranteed by design and correlation.

## **Typical Operating Characteristics**

(VIN = +5V, MAX4838; Si9936DY external MOSFET in back-to-back configuration; TA = +25°C, unless otherwise noted.)

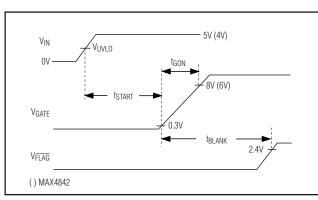


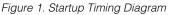


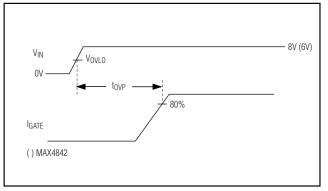
MAX4838-MAX4842

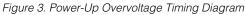
# **Pin Description**

PIN				
MAX4838/ MAX4840/ MAX4842	MAX4839/ MAX4841	NAME	FUNCTION	
1	1	IN	Input. IN is both the power-supply input and the overvoltage sense input. Bypass IN to GND with a $1\mu F$ capacitor or larger.	
2	2	GND	Ground	
3	3	FLAG	Fault Indication Output, Active Low. FLAG is asserted low during undervoltage lockout and overvoltage lockout conditions. FLAG is deasserted during normal operation. FLAG is open-drain on the MAX4838/MAX4840/MAX4842, and push-pull on the MAX4839/MAX4841.	
4	4	GATE	Gate-Drive Output. GATE is the output of an on-chip charge pump. When $V_{UVLO} < V_{IN} < V_{OVLO}$ , GATE is driven high to turn on the external N-channel MOSFET(s).	
5	5, 6	N.C.	No Connection. Can be connected to GND.	
6	_	ĒN	Device Enable Input, Active Low. Drive $\overline{\text{EN}}$ low or connect to ground to allow normal device operation. Drive $\overline{\text{EN}}$ high to turn off the external MOSFET.	











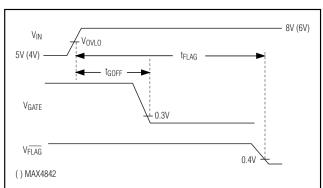
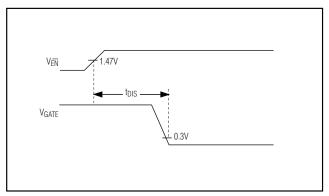
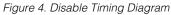


Figure 2. Shutdown Timing Diagram





# \_Timing Diagrams

MAX4838-MAX4842

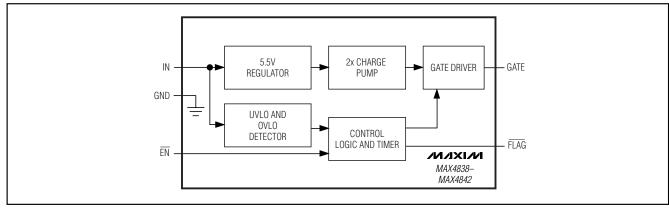


Figure 5. Functional Diagram

#### **Detailed Description**

The MAX4838–MAX4842 provide up to 28V overvoltage protection for low-voltage systems. When the input voltage exceeds the overvoltage trip level, the MAX4838–MAX4842 turn off a low-cost external n-channel FET(s) to prevent damage to the protected components. An internal charge pump (Figure 5) drives the FET gate for a simple, robust solution.

#### **Undervoltage Lockout (UVLO)**

The MAX4838–MAX4841 have a fixed 3.25V typical undervoltage lockout level (UVLO) while the MAX4842 has a 3.0V typical UVLO. When  $V_{IN}$  is less than the UVLO, the GATE driver is held low and FLAG is asserted.

#### **Overvoltage Lockout (OVLO)**

The MAX4838/MAX4839 have a 7.4V typical overvoltage threshold (OVLO), and the MAX4840/MAX4841 have a 5.8V typical overvoltage threshold. The MAX4842 has a 4.7V typical overvoltage threshold. When  $V_{IN}$  is greater than OVLO, the GATE driver is held low and FLAG is asserted.

#### **FLAG** Output

The FLAG output is used to signal the host system there is a fault with the input voltage. FLAG asserts immediately to an overvoltage fault. FLAG is held low for 50ms after GATE turns on before deasserting.

The MAX4839 and MAX4841 have a push-pull  $\overline{FLAG}$  output. The output high voltage is proportional to V<sub>IN</sub> for V<sub>IN</sub> up to 5.5V, and fixed at 5.5V when V<sub>IN</sub> > 5.5V.

The MAX4838/MAX4840/MAX4842 have an open-drain FLAG output. Connect a pullup resistor from FLAG to the logic I/O voltage of the host system.

#### **EN** Enable Input

EN is an active-low enable input on the MAX4838/ MAX4840/MAX4842 only. Drive EN low or connect to ground to enable normal device operation. Drive EN high to force the external MOSFET(s) off. EN does not override an OVLO or UVLO fault.

#### **GATE Driver**

An on-chip charge pump is used to drive GATE above IN, allowing the use of low-cost n-channel MOSFETS. The charge pump operates from the internal 5.5V regulator.

The actual GATE output voltage tracks approximately two times V<sub>IN</sub> until V<sub>IN</sub> exceeds 5.5V or the OVLO trip level is exceeded, whichever comes first. The MAX4838/MAX4839 have a 7.4V typical OVLO, therefore GATE remains relatively constant at about 10.5V for 5.5V < V<sub>IN</sub> < 7.4V. The MAX4840/MAX4841 have a 5.8V typical OVLO, but this can be as low as 5.5V. The MAX4840/MAX4841 in practice may never actually achieve the full 10.5V GATE output. The MAX4842 has a 4.7V (typ) OVLO and the GATE output voltage is 2x the input voltage. The GATE output voltage as a function of input voltage is shown in the *Typical Operating Characteristics*.

#### **Device Operation**

The MAX4838–MAX4842 have an on-board state machine to control device operation. A flowchart is shown in Figure 6. On initial power-up, if  $V_{IN}$  < UVLO or if  $V_{IN}$  > OVLO, GATE is held at 0V, and FLAG is low.

If UVLO < V<sub>IN</sub> < OVLO and  $\overline{\text{EN}}$  is low, the device enters startup after a 50ms internal delay. The internal charge pump is enabled, and GATE begins to be driven above V<sub>IN</sub> by the internal charge pump. FLAG is held low during startup until the FLAG blanking period expires, typi-



MAX4838-MAX4842

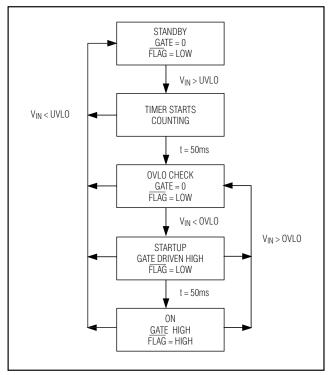


Figure 6. State Diagram

cally 50ms after the GATE starts going high. At this point the device is in its on state.

At any time if  $V_{\text{IN}}$  drops below UVLO,  $\overline{\text{FLAG}}$  is driven low and GATE is driven to ground.

#### **Applications Information**

#### **MOSFET** Configuration

The MAX4838–MAX4842 can be used with either a single MOSFET configuration as shown in the *Typical Operating Circuit*, or can be configured with a back-to-back MOSFET as shown in Figure 7.

The MAX4838–MAX4842 can drive either a single MOSFET or back-to-back MOSFETs. The back-to-back configuration has almost zero reverse current when the input supply is below the output.

If reverse current leakage is not a concern, a single MOSFET can be used. This approach has half the loss of the back-to-back configuration when used with similar MOSFET types, and is a lower cost solution. Note that if the input is actually pulled low, the output is pulled low as well due to the parasitic body diode in the

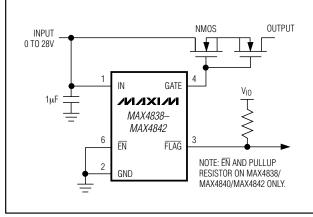


Figure 7. Back-to-Back External MOSFET Configuration

MOSFET. If this is a concern, then the back-to-back configuration should be used.

#### **MOSFET Selection**

The MAX4838–MAX4842 are designed for use with either a single n-channel MOSFET or dual back-to-back n-channel MOSFETs. In most situations, MOSFETs with RDS(ON) specified for a VGS of 4.5V work well. If the input supply is near the UVLO maximum of 3.5V consider using a MOSFET specified for a lower VGS voltage. Also the VDS should be 30V for the MOSFET to withstand the full 28V IN range of the MAX4838–MAX4842. Table 1 shows a selection of MOSFETs appropriate for use with the MAX4838–MAX4842.

#### **IN Bypass Considerations**

For most applications, bypass IN to GND with a  $1\mu$ F ceramic capacitor. If the power source has significant inductance due to long lead length, take care to prevent overshoots due to the LC tank circuit and provide protection if necessary to prevent exceeding the 30V absolute maximum rating on IN.

The MAX4838–MAX4842 provide protection against voltage faults up to 28V, but this does not include negative voltages. If negative voltages are a concern, connect a Schottky diode from IN to GND to clamp negative input voltages.

#### ESD Test Conditions

ESD performance depends on a number of conditions. The MAX4838–MAX4842 are specified for 15kV typical ESD resistance on IN when IN is bypassed to ground with a  $1\mu$ F ceramic capacitor. Contact Maxim for a reli-

PART	CONFIGURATION/ PACKAGE	V <sub>DS</sub> MAX (V)	R <sub>ON</sub> AT 4.5V (mΩ)	MANUFACTURER
Si5902DC	Dual/1206-8	30	143	Vishay Silconix www.vishay.com
Si1426DH	Single/SC70-6	30	115	402-563-6866
FDC6305N	Dual/SSOT-6	20	80	Fairchild Semiconductor
FDC6561AN	Dual/ SSOT-6	30	145	www.fairchildsemi.com
FDG315N	Single/SC70-6	30	160	207-775-8100

## Table 1. MOSFET Suggestions

ability report that documents test setup, methodology, and results.

#### Human Body Model

Figure 8 shows the Human Body Model and Figure 9 shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the device through a  $1.5k\Omega$  resistor.

#### IEC 1000-4-2

Since January 1996, all equipment manufactured and/or sold in the European community has been required to meet the stringent IEC 1000-4-2 specification. The IEC 1000-4-2 standard covers ESD testing and performance of finished equipment; it does not specifically refer to integrated circuits. The MAX4838–MAX4842 help users design equipment that meets Level 3 of IEC 1000-4-2, without additional ESD-protection components.

The main difference between tests done using the Human Body Model and IEC 1000-4-2 is higher peak current in IEC 1000-4-2. Because series resistance is lower in the IEC 1000-4-2 ESD test model (Figure 10), the ESD-withstand voltage measured to this standard is generally lower than that measured using the Human Body Model. Figure 11 shows the current waveform for the  $\pm$ 8kV IEC 1000-4-2 Level 4 ESD Contact Discharge test. The Air-Gap test involves approaching the device with a charger probe. The Contact Discharge method connects the probe to the device before the probe is energized.

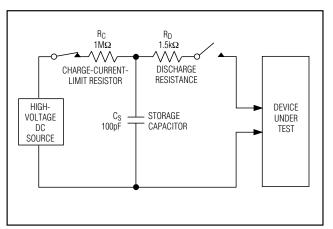
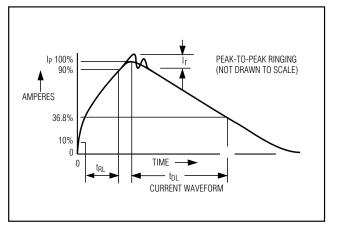


Figure 8. Human Body ESD Test Model



///XI//

Figure 9. Human Body Model Current Waveform

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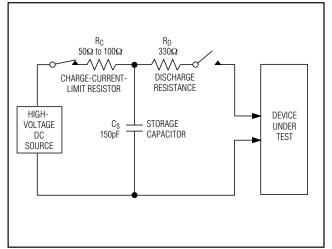


Figure 10. IEC 1000-4-2 ESD Test Model

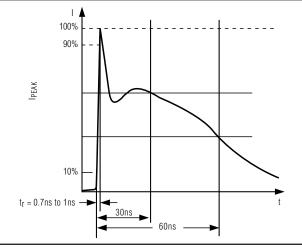
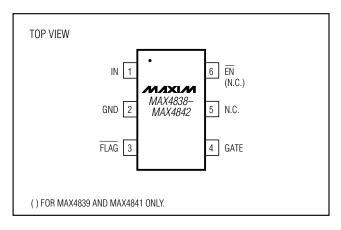


Figure 11. IEC 1000-4-2 ESD Generator Current

# **MAX4838-MAX4842**

## Pin Configuration

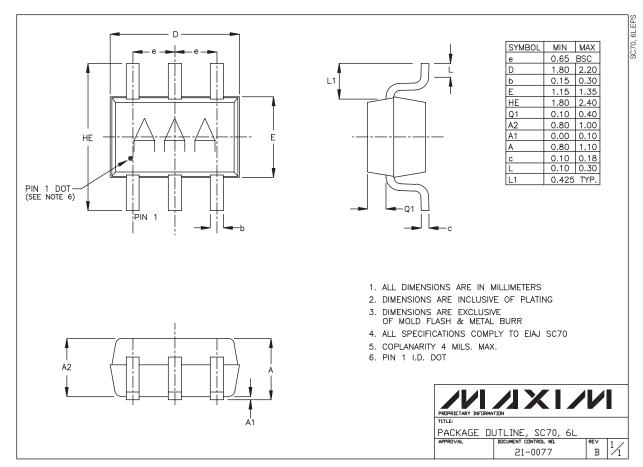


## Chip Information

TRANSISTOR COUNT: 737 PROCESS: BICMOS

## **Package Information**

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <u>www.maxim-ic.com/packages</u>.)



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