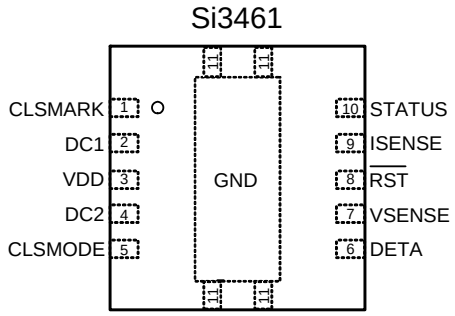
Si3461

SINGLE-PORT IEEE 802.3AT POE/POE+ PSE INTERFACE

Features

- IEEE 802.3at™ compliant PSE
- Autonomous operation requires no host processor interface
- Complete reference design available, including Si3461 controller and schematic:
  - Low-cost BOM
  - Compact PCB footprint
  - Operates directly from a +50 V isolated supply
  - Supports up to 30 W maximum output power (Class 4)
  - Robust 3-point detection algorithm eliminates false detection events
  - IEEE-compliant disconnect
  - Inrush current control
  - Short-circuit output fault protection
  - LED status signal (detect, power good, output fault)
- UNH Interoperability Test Lab report available
- Extended operating range (–40 to +85 °C)
- 11-Pin Quad Flat No-Lead (QFN) package
  - Tiny 3x3 mm PCB footprint; RoHS-compliant

Pin Assignments



11-pin QFN (3x3 mm)
Top View—Pads on bottom of package

Applications

- IEEE 802.3at endpoints and midspans
- Environment A and B PSEs
- Embedded PSEs
- Set-top boxes
- FTTH media converters
- Cable modem and DSL gateways

Description

The Si3461 is a single-port power management controller for IEEE 802.3at-compliant Power Sourcing Equipment (PSE). The Si3461 can be powered from a 50 V input using a shunt regulator, or, to save power, it can be powered from 50 V and 3.3 V power supplies. The IEEE-required Powered Device (PD) detection feature uses a robust 3-point algorithm to avoid false detection events. The Si3461's reference design kit also provides full IEEE-compliant classification and PD disconnect. Intelligent protection circuitry includes input under-voltage lockout (UVLO), classification-based current limiting, and output short-circuit protection. The Si3461 is designed to operate completely independently of host processor control. An LED status signal is provided to indicate the port status, including detection, power good, and output fault event information. The Si3461 is pin-programmable to support four available power levels, endpoint and mid-span applications, and auto-retry or restart after disconnect functions. A comprehensive reference design kit is available (Si3461-EVB), including a complete schematic and bill of materials.

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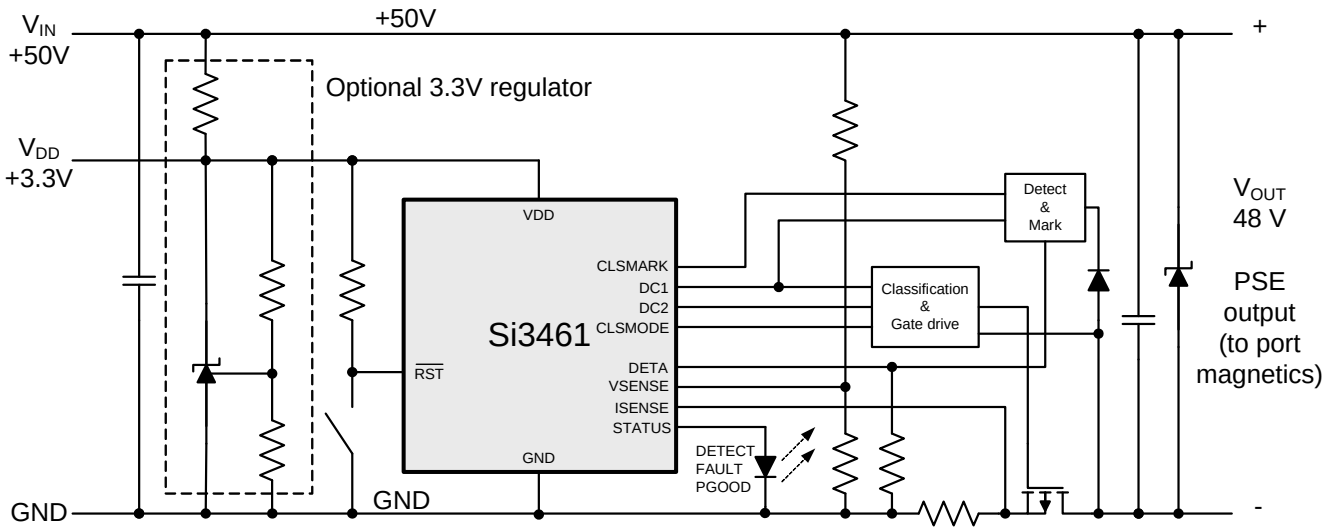
1. Typical Application Schematic



Note: Refer to the Si3461-EVB User Guide for complete schematic details

Figure 1. Si3461 Typical Application Schematic

2. Si3461 Electrical Specifications

The following specifications apply to the Si3461 controller. Refer to Tables 4 and 5 and the Si3461-EVB User's Guide and schematics for additional details about the electrical specifications of the Si3461-EVB reference design.

Table 1. Recommended Operating Conditions

Description	Symbol	Test Conditions	Min	Typ	Max	Unit
Operating Temperature Range	T_A		–40	25	+85	°C
Thermal Impedance	θ_{JA}	No airflow	—	75	—	°C/W
VDD Input Supply Voltage	VDD	During all operating modes (detect, classification, disconnect)	2.7	3.3	3.6	V

Table 2. Absolute Maximum Ratings*

Parameter	Conditions	Max Rating	Unit
Ambient Temperature Under Bias		–55 to +125	°C
Storage Temperature		–65 to +150	°C
Voltage on $\overline{\text{RST}}$ or any I/O pin with respect to GND	VDD > 2.2 V	–0.3 to 5.8	V
Voltage on VDD with respect to GND		–0.3 to 4.2	V
Maximum Total Current through VDD and GND		500	mA
Maximum Output Current into CLSMARK, DC1, DC2, CLSMODE, STATUS, ISENSE, RST, VSENSE, DETA (any I/O pin)		100	mA
ESD Tolerance	Human Body Model	–2 kV to +2 kV	V
Lead Temperature	Soldering, 10 seconds maximum	260	°C

***Note:** Stresses above those listed in this table may cause permanent device damage. This is a stress rating only, and functional operation of the devices at these or any conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 3. Electrical Characteristics*

Description	Symbol	Test Conditions	Min	Typ	Max	Unit
Digital Pins: CLSMARK, DC1, DC2, CLSMODE, STATUS (Output mode), $\overline{RST}$						
Output High Voltage	V_{OH}	I_{OH} = –3 mA I_{OH} = –10 µA	0.7 x VDD VDD – 0.1	— —	— —	V
Output Low Voltage	V_{OL}	I_{OL} = 8.5 mA I_{OL} = 10 µA	— —	— —	0.6 0.1	V
Input High Voltage	V_{IH}	Any digital pin	0.7 x VDD			V
Input Low Voltage	V_{IL}	Any digital pin	—	—	0.6	V
Input Leakage Current	I_{IL}	V_{IN} = 0 V	—	±1	—	µA
Analog Pins: ISENSE, VSENSE, DETA, STATUS (Input mode)						
Input Capacitance			—	5	—	pF
Input Leakage Current	I_{IL}		—	±1	—	µA
***Note:** VDD = 2.7 to 3.6 V, –40 to +85 °C unless otherwise specified.						

2.1. Si3461-EVB Performance Characteristics

When implemented according to the recommended external component and layout guidelines for the Si3461-EVB, the Si3461 enables the following performance specifications in single-port PSE applications. Refer to the Si3461-EVB User's Guide and schematics for details.

Table 4. Selected Electrical Specifications (Si3461-EVB)

Description	Symbol	Test Conditions	Min	Typ[1]	Max	Unit
Power Supplies						
V_{IN} Input Supply Range	V_{IN}	–40 to +85 °C ambient range	45	50	57	V
V_{IN} Input UVLO Voltage	UVLO	UVLO turn-off voltage at V_{IN}	—	42	45	V
V_{IN} Input OVLO Voltage	OVLO	OVLO turn-off voltage at V_{IN}	57	60	—	V
VDD Supply Voltage Range	V_{DD}	Si3461 supply voltage range	3.15	3.3	3.45	V
Output Supply Voltage	V_{OUT}	PSE output voltage at V_{IN} = 50 V and I_{OUT} = 350 mA	—	49	—	V
Supply Current	I_{IN}	Current into the V_{DD} node (not including shunt regulator)	—	8.0	10.5	mA
Detection Specifications						
Detection Voltage	V_{DET}	Detection point 1 Detection point 2 Detection point 3	—	4.0 8.0 4.0	—	V
Detection Current	I_{DET}	Short circuit	—	—	3	mA
Minimum Signature Resistance	R_{DETmin}		15	17	19	kΩ
Maximum Signature Resistance	R_{DETmax}		26.5	29	33	kΩ
Classification Specifications						
Classification Voltage	V_{CLASS}	0 mA < I_{CLASS} < 45 mA	15.5	—	20.5	V
Classification Current Limit	I_{CLASS}	Measured with 100 Ω across V_{OUT}	55	75	95	mA

Notes:

1. Typical specifications are based on an ambient operating temperature of 25 °C and VIN = +50 V unless otherwise specified.
2. Absolute classification current limits are configurable. See “5.2. Classification” and "5.3. Power-Up" on page 13.
3. Typical ICUT values are adjusted according to the input voltage to provide power limiting with approximately 5% margin against the 802.3 requirements. The maximum ICUT values are consistent with the IEEE requirement that Icut maximum is less than 400 mA at the minimum allowed Vout of 44 V or 684 mA for PoE+ mode at the minimum allowed Vout of 50 V.
4. Overload current is within limits, typically in less than 1 ms.

Table 4. Selected Electrical Specifications (Si3461-EVB) (Continued)

Description	Symbol	Test Conditions	Min	Typ[1]	Max	Unit
Classification Current Region	I_{CLASS_REGION}	Class 0	0	—	5	mA
		Class 1	8	—	13	mA
		Class 2	16	—	21	mA
		Class 3	25	—	31	mA
		Class 4	35	—	45	mA
Mark Voltage	V_{MARK}		7	8.5	10	V
Mark Current	I_{MARK_LIM}	Short circuit	—	—	9	mA
Protection and Current Control						
Overload Current Threshold[2,3]	I_{CUT}	Class 0 and Class 4 PoE	15,400/V_{OUT}	16,170/V_{OUT}	17,600/V_{OUT}	mA
		Class 1	4,000/V_{OUT}	4,200/V_{OUT}	4,600/V_{OUT}	mA
		Class 2	7,000/V_{OUT}	7,350/V_{OUT}	8,000/V_{OUT}	mA
		Class 3	15,400/V_{OUT}	16,170/V_{OUT}	17,600/V_{OUT}	mA
		Class 4 PoE+	30,000/V_{OUT}	31,500/V_{OUT}	34,200/V_{OUT}	mA
Overload Current Limit[4]	I_{LIM}	Class 0/1/2/3 and Class 4 PoE; Output = 100 Ω across V_{OUT}	400	425	450	mA
	I_{LIM} PoE+	Class 4 PoE+; Output = 50 Ω across V_{OUT}	684	750	825	mA
Overload Time	T_{LIM}	Class 0/1/2/3 and Class 4 PoE; Output = 100 Ω across V_{OUT}	50	60	75	ms
		Class 4 PoE+; Output = 50 Ω across V_{OUT}	14	17	20	ms
Disconnect Current	I_{MIN}	Disconnect current	5	7.5	10	mA
Efficiency						
System Efficiency	η	(P_{IN} @ V_{IN}) to (P_{OUT} @ V_{OUT})	—	93	—	%

Notes:

1. Typical specifications are based on an ambient operating temperature of 25 °C and VIN = +50 V unless otherwise specified.
2. Absolute classification current limits are configurable. See “5.2. Classification” and "5.3. Power-Up" on page 13.
3. Typical ICUT values are adjusted according to the input voltage to provide power limiting with approximately 5% margin against the 802.3 requirements. The maximum ICUT values are consistent with the IEEE requirement that Icut maximum is less than 400 mA at the minimum allowed Vout of 44 V or 684 mA for PoE+ mode at the minimum allowed Vout of 50 V.
4. Overload current is within limits, typically in less than 1 ms.

2.2. PSE Timing Characteristics

When implemented in accordance with the recommended external components and layout guidelines, the Si3461 controller enables the following typical performance characteristics in single-port PSE applications. Refer to the Si3461-EVB applications note, schematics, and user's guide for more details.

Table 5. PSE Timing

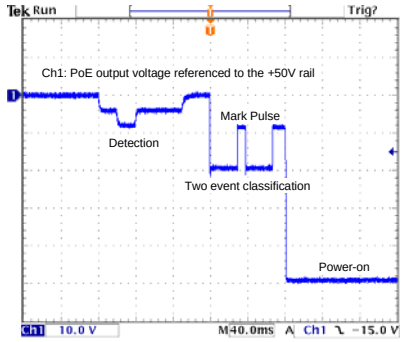
Description	Symbol	Test Conditions	Min	Typ	Max	Unit
Endpoint Detection Delay Cycle	t_{DET_CYCLE}	Time from PD connection to port to completion of detection process.	90	—	460	ms
Detection Time	t_{DETECT}	Time required to measure PD signature resistance.	—	90	—	ms
Classification Delay Cycle	t_{CLASS_CYCLE}	Class 0/1/2/3; Time from successful detect mode to classification complete.	—	60	—	ms
		Class 4, two event classification; Time from successful detect mode to classification complete.	—	99	—	ms
Classification Time	t_{CLASS}	Class 0/1/2/3 and Class 4 PoE;	—	30	—	ms
		Class 4 PoE+	—	69	—	ms
Power-Up Turn-On Delay	t_{PWRUP}	Class 0/1/2/3 and Class 4 PoE; Time from when a valid detection is completed until V_{OUT} power is applied	—	76	—	ms
		Class 4 PoE+; Time from when a valid detection is completed until V_{OUT} power is applied	—	112	—	ms
Midspan Detect Back-off Time	t_{BOM}		2.0	—	—	s
Error Delay Time	T_{ed}	Time from error to restart of detection in auto-restart mode.	2.0	—	—	s
Disconnect Delay	t_{DC_DIS}		—	350	—	ms

Note: These typical specifications are based on an ambient operating temperature of 25 °C and V_{IN} = +50 V.

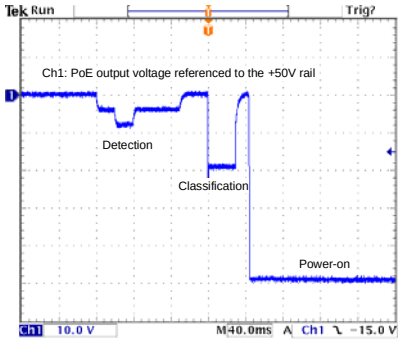
3. Typical Si3461-EVB Waveforms

Note: Voltages are negative going with respect to the positive input.

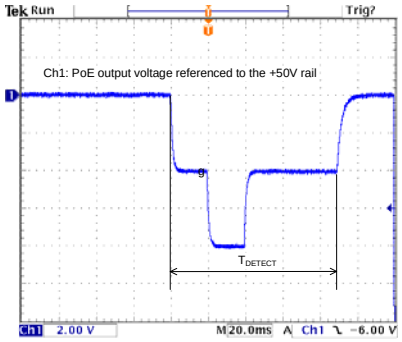
Powering a PoE+ Device



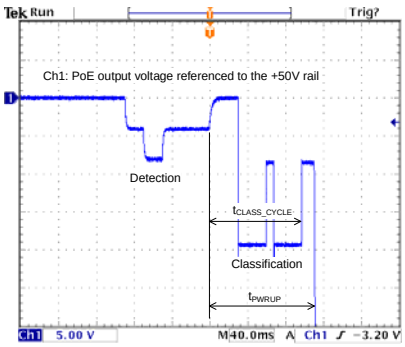
Powering a PoE Device



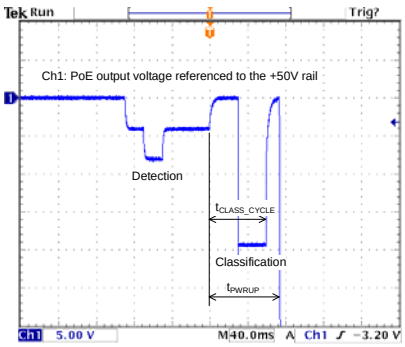
Detection Time



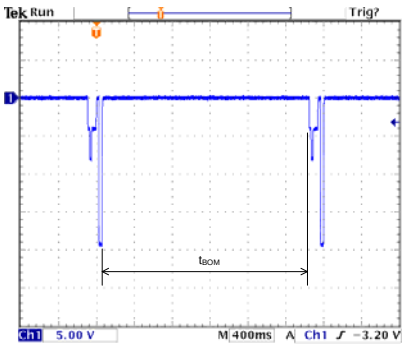
Classification and Power-up Delay PoE+



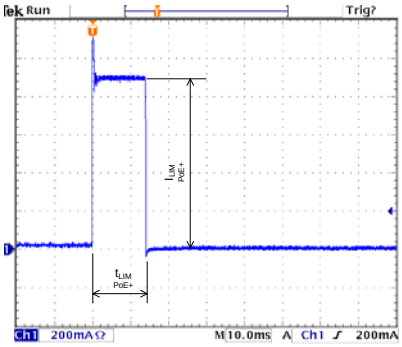
Classification and Power-up Delay PoE



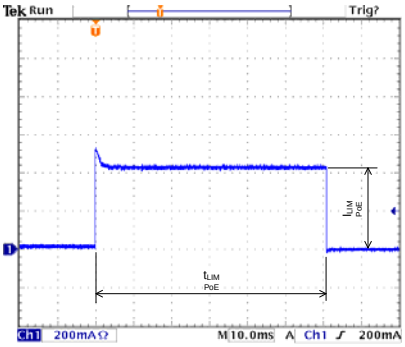
Midspan Backoff after bad Classification result



PoE+ Current Limit Response



PoE Current Limit Response



Overload During Classification

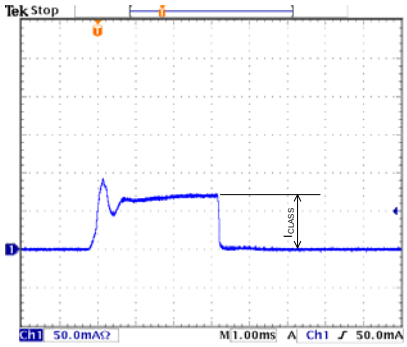


Figure 2. Typical Si3461-EVB Waveforms

4. Si3461-EVB Functional Description

In combination with low-cost external components, the Si3461 controller provides a complete PSE solution for embedded PoE applications. The Si3461-EVB reference design operates from a +50 V isolated power supply and delivers power to the powered device through a FET switch without controlling the output voltage while in the power-on state.

Refer to the Si3461-EVB User's Guide and schematics for descriptions in the following sections.

The basic sequence of applying power is shown in Figure 3. Following is the description of the function that must be performed in each phase.

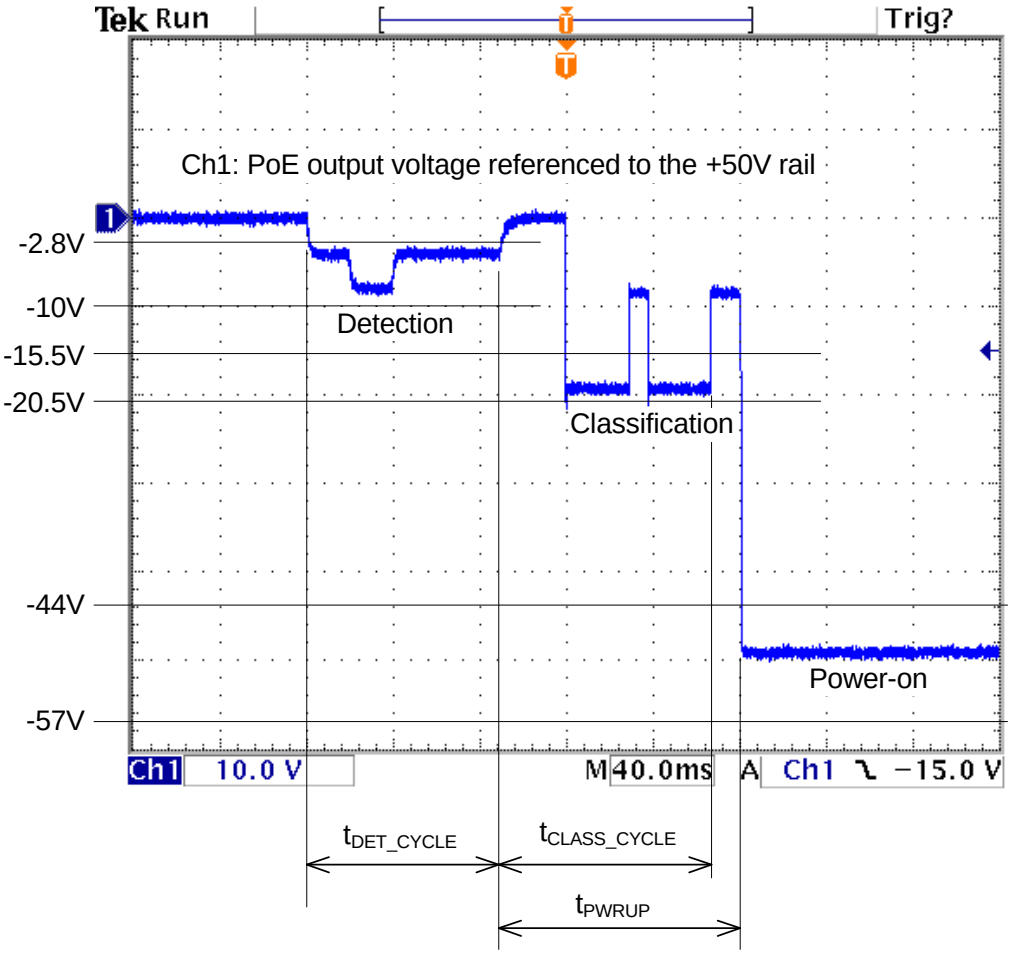


Figure 3. Basic Power-up Sequence

4.1. Reset State

At power-up or if reset is held low, the Si3461 is in an inactive state with the pass FET Q4 off.

4.2. Operating Mode Configuration

At power-up, the Si3461 reads the voltage on the STATUS pin, which is set by a DIP switch and a resistor network. The STATUS pin voltage level configures all of the Si3461's operating modes as summarized in Table 6.

Table 6. Operating Modes[1,2,3,4]

STATUS Pin Voltage (V)	Operating Mode			
	PSE Type	Midspan/ Endpoint	Restart Action on Fault or Overload Event Condition	Available Power (W)
< 0.122	1	Midspan	Restart after disconnection	4
0.122 to 0.338	1	Midspan	Restart after disconnection	7
0.338 to 0.548	1	Midspan	Restart after disconnection	15.4
0.548 to 0.756	2	Midspan	Restart after disconnection	30
0.756 to 0.961	1	Midspan	Auto restart after 2 s	4
0.961 to 1.162	1	Midspan	Auto restart after 2 s	7
1.162 to 1.366	1	Midspan	Auto restart after 2 s	15.4
1.366 to 1.575	2	Midspan	Auto restart after 2 s	30
1.575 to 1.784	1	Endpoint	Restart after disconnection	4
1.784 to 1.990	1	Endpoint	Restart after disconnection	7
1.990 to 2.196	1	Endpoint	Restart after disconnection	15.4
2.196 to 2.407	2	Endpoint	Restart after disconnection	30
2.407 to 2.618	1	Endpoint	Auto restart after 2 s	4
2.618 to 2.838	1	Endpoint	Auto restart after 2 s	7
2.838 to 3.044	1	Endpoint	Auto restart after 2 s	15.4
> 3.044	2	Endpoint	Auto restart after 2 s	30

Notes:

1. After power-up, the STATUS pin drives the base of an NPN transistor that controls an LED.
2. There is a trade-off in selecting the mode setting resistor values between voltage step accuracy and additional worst-case supply current. For high-value resistors, the base current will alter the voltage steps while low-value resistors may place higher load on the STATUS pin while driving the LED. The suggested resulting parallel resistance used by the Si3461-EVB is 2.0 kΩ.
3. Each mode setting resistor should be connected either to GND or +3.3 V through the DIP switch. Care should be taken not to short the +3.3 V supply to GND.
4. A reset is required after a DIP switch position change for the new mode to take effect.

5. Operating Mode Sequencing

5.1. Detection

After power-up the Si3461 enters the detection state with the pass FET off. Prior to turning the FET on, a valid detection sequence must take place.

According to the IEEE specifications, the detection process consists of sensing a nominal 25 kΩ signature resistance in parallel with up to 0.15 µF of capacitance. To eliminate the possibility of false detection events, the Si3461-EVB reference design performs a robust 3-point detection sequence by varying the voltage across the load that connects to the +50 V supply rail and returns to GND via D3, Q14, R26, and R37. R37 serves as a current sensing resistor, and the Si3461 monitors the voltage drop across it during the detection process.

At the beginning of the detection sequence, V_{OUT} is at zero; then, it is varied from 4 to 8 V and then back to 4 V for 20+20+50 ms at each respective level. If the PD's signature resistance is in the RGOOD range of 17 to 29 kΩ, the Si3461 proceeds to classification and power-up. If the PD resistance is not in this range, the detection sequence repeats continuously.

Detection is sequenced approximately every 400 ms for endspan and 2.2 seconds for midspan configurations and repeats until RGOOD is sensed, indicating a valid PD has been detected. The STATUS LED (D2) is flashed at a rate of about 1.5 Hz to indicate the PSE is searching for a valid PD.

5.2. Classification

After a valid PD is detected, the PSE interrogates the PD to find its power requirement. This procedure is called classification and may be carried out in different ways. The Si3461 implements the one-event classification for Type1 PDs and the two-event classification for Type2 PDs.

For one-event classification, the pass FET Q4 is turned on and programmed for an output voltage of 18 V with a current limit of 75 mA for 30 ms. For the two-event classification, the 18 V pulse is output twice with an 8.5 V amplitude mark pulse for 10 ms between the two classification pulses. The current measured at the ISENSE input during the classification process determines the class level of the PD (refer to Table 4 on page 7 for current ranges).

If the Si3461-EVB has 30 W of available power, it attempts to classify a Type2 PD first by the two-event method. If the detected class is other than Class 4 or there is less than 30 W of power available, the Si3461 tries to classify a Type1 PD using the one-event method.

If the class level of the PD is not within the supported range as set by the initial voltage on the Si3461's STATUS pin (refer to the Operating Mode Configuration section above), an error is declared, and the LED blinks rapidly at a 10 Hz rate. This is referred to as classification-based power denial. If the class level is in the supported range, the Si3461 proceeds to power-up. This is referred to as classification-based power granting.

If the classification level is at a greater power than can be supported based on the voltage read by the STATUS pin during start-up, an error condition is reported by flashing the LED at a 10 Hz rate for two seconds before the state machine goes back to the detection cycle.

5.3. Power-Up

After successful classification, the pass FET is turned on with an initial current limit of 425 mA (for all PD classes), and the respective ILIM values (indicated in Table 4) take effect after the FET is fully turned on. After power-up is complete, power is applied to V_{OUT} as long as there is not an overcurrent fault, disconnect, or input undervoltage (UVLO) or overvoltage (OVLO) condition. The STATUS LED is continuously lit when power is applied.

If the output power exceeds the level of the power requested during classification, the Si3461 will declare an error and shut down the port, flashing the LED rapidly to indicate the error. Depending on the initial voltage on the STATUS pin, the Si3461 will wait either 2.2 seconds or until the PD has been disconnected before it enters the detection phase again to look for a valid load.

5.4. Overload Protection

The Si3461 implements a two-level overload protection scheme. The output current is limited to ILIM, and the output is shut down if the current exceeds ICUT for more than 60 ms. If current limitation persists for more than 15 ms in case of PoE+ Class 4 loads, the output is shut down to protect the pass FET. Current limit values are dynamically set according to the power level granted during the classification process and the effective output voltage (refer to Table 4 on page 7 for current limit values).

A special 425 mA current limit applies until the FET is fully turned on. If the FET does not fully turn on in the first 75 ms due to an overload condition, an error is declared. The maximum time that the 425 mA inrush current is supplied is about 70 ms due to a 5 ms period to initially ramp the FET gate voltage.

The overload protection is implemented using a timer with a timeout set to 60 ms. If the output current exceeds the I_{CUT} threshold, the timer counts up; otherwise, if the output current drops below ICUT, the timer counts down towards zero at 1/16th the rate. If the timer reaches the set timeout, an overcurrent fault is declared; the channel is shut down (by turning off the external pass FET), and the status LED flashes rapidly at a rate of 10 Hz.

If the Si3461 was configured in the “automatic restart” mode during start-up, it will automatically resume the detection process after 2.2 seconds. In the “restart after disconnect” mode of operation, the status LED will flash rapidly, and the Si3461 will not resume detection until it senses a resistance higher than 150 kΩ. This condition can normally be achieved by removing the Ethernet cable from the Si3461-EVB's RJ-45 jack labeled “PoE”. Then, the detection process begins; the status LED blinks at a rate of 1.5 Hz, and the Si3461 is allowed to go into classification and power-up mode if a valid PD signature resistance is detected.

5.5. Disconnect

The Si3461 implements a robust disconnect algorithm. If the output current level drops below 7.5 mA typical for more than 350 ms, the Si3461 declares a PD disconnect event, and the pass FET is turned off. The Si3461 automatically resumes the detection process after 500 ms.

5.6. UVLO and OVLO

The Si3461-EVB reference design is optimized for 50 V nominal input voltages (44 V minimum to 57 V maximum). If the input voltage drops below 42 V, a UVLO condition is declared, which generates the error condition (LED flashing rapidly). An undervoltage event is a fault condition reported through the status LED as a rapid blinking of 10 flashes per second. In the same way, if the input voltage exceeds 60 V, an OVLO condition is declared. In both cases, the output is shut down.

The UVLO and OVLO conditions are continuously monitored in all operating states.

5.7. Status LED Function

During the normal detection sequence, the STATUS LED flashes at approximately 1.5 times per second as the detection process continues. After successful power up, the LED glows continuously. If there is an error condition (i.e., class level is beyond programmed value or a fault or over current condition has been detected), the LED flashes rapidly at 10 times per second. This occurs for two seconds for normal error delay, and the detection process will automatically start again after 2.2 s unless a “restart after disconnect condition” was set during the initial configuration. Power will not be provided until an open circuit condition is detected. Once the Si3461-EVB detects an open circuit condition, the LED blinks at 1.5 times per second.

If the Powered Device (PD) is disconnected so that a disconnect event occurs, the LED will start flashing at 1.5 times per second once the detect process resumes.

6. Design Considerations

6.1. Isolation

The Si3461-EVB's PSE output power at VOUT is not isolated from the input power source (VIN). Isolation of PSE output power requires that the input be isolated from earth ground. Typically, an ac-to-dc power supply is used to provide the 50 V power so the output of this supply is isolated from earth ground.

6.2. External Component Selection

Detailed notes on external component selection are provided in the Si3461-EVB User's Guide schematics and BOM. In general, these recommendations must be followed closely to ensure output power stability, surge protection (surge protection diode), and overall IEEE 802.3 compliance.

6.3. Input DC Supply

The Si3461-EVB reference design requires an isolated 50 V nominal dc input voltage (with a minimum of 44 V and a maximum of 57 V).

The input power supply should be rated for at least 10% higher power level than the output power level chosen. This is primarily to account for the losses in the current-sensing resistor, the pass FET, and the series protection diode of the Si3461-EVB reference design. For example, to support a Class 0 PSE, the input supply should be capable of supplying at least 16.94 W (15.4 W x 1.10 = 16.94 W).

The power supply also needs to be able to source 425 mA for 60 ms for normal operation or 885 mA for 15 ms for high power (PoE+) operation.

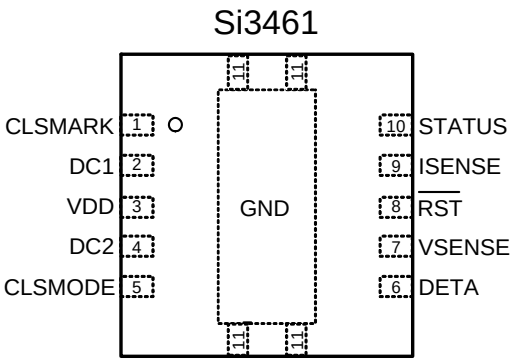
The Si3461-EVB reference design does not regulate the output voltage during the power-on state; therefore, the input dc supply should meet the ripple and noise specifications of the IEEE 802.3 standard.

The Si3461-EVB reference design includes an optional 3.3 V shunt regulator that uses the 50 V input to generate the 3.3 V supply voltage for the Si3461 controller. Alternatively, an external 3.3 V power source may be used.

7. Si3461 Pin Descriptions

Si3461 pin functionality is described in Table 7. Note that the information applies to the Si3461 device pins, while the Si3461-EVB User's Guide describes the inputs and outputs of the evaluation system.

Refer to the complete Si3461-EVB schematics and BOM listing for information about the external components needed for the complete PSE application circuit.



11-pin QFN (3x3 mm)
Top View—Pads on bottom of package

Table 7. Si3461 Pin Functionality

Pin #	Pin Name	Pin Type	Pin Function
1	CLSMARK	Digital output	Logic high on this output increases the current capability of the detection circuitry while used for mark pulse generation. Refer to the Si3461-EVB schematics.
2	DC1	Digital output	This is a PWM output providing the dc control voltage for the detection circuitry. It is also combined with the DC2 output in a ratio of 1:256 to provide the gate control voltage of the pass FET.
3	VDD	Power	3.3 V power supply input.
4	DC2	Digital output	This is a PWM output that (combined with the DC1 output) provides the gate control voltage of the pass FET with high resolution.
5	CLSMODE	Digital output	This is an open drain output. When high, it enables the feedback path controlling the 18 V classification voltage.
6	DETA	Analog input	DETA is an analog input pin. During the detection process, the DC1 pin duty cycle is varied to generate filtered dc voltages across the load, and the voltage drop across a current sensing resistor is measured through the DETA input.
7	VSENSE	Analog input	VSENSE is an analog input used for sensing the input dc voltage.
8	$\overline{\text{RST}}$	Digital input	Active low reset input. When low, it places the Si3461 device into an inactive state. When pulled high, the device begins the detection process sequence.
9	ISENSE	Analog input	ISENSE is an analog input connected to a current sense resistor for output current sensing.

Table 7. Si3461 Pin Functionality (Continued)

Pin #	Pin Name	Pin Type	Pin Function
10	STATUS	Analog in/Digital out	At power-up, the voltage on this pin is sensed to configure the PSE available power, mid span/end span timing mode and the device's restart behavior when a fault condition is detected. Refer to "4.2. Operating Mode Configuration" on page 12. After reading the voltage present at this pin at power-up, the STATUS pin becomes a digital output used to control an external LED, which indicates when a detect, power good, or output fault condition has occurred. Logic high turns the LED on, and logic low turns the LED off. Refer to "5.7. Status LED Function" on page 14.
11	GND	GND	Ground connection for the Si3461.

8. Ordering Guide

Ordering Part Number	Description	Package Information	Temperature Range (Ambient)
Si3461-E02-GM	Single-port PSE controller	11-pin, 3 x 3 mm QFN. RoHS compliant	–40 to 85 °C
Si3461-KIT	Si3461 evaluation board and reference design kit	Evaluation board	N/A

Notes:
1. Add R to part number to denote tape-and-reel option (e.g., Si3461-E02-GMR).
2. The ordering part number above is not the same as the device mark. See "9.3. Marking Specification" on page 22 for more information.

9. Package Outline: 11-Pin QFN

Figure 4 illustrates the package details for the Si3461. Table 8 lists the values for the dimensions shown in the illustration. The Si3461 is packaged in an industry-standard, 3x3 mm, RoHS-compliant, 11-pin QFN package.

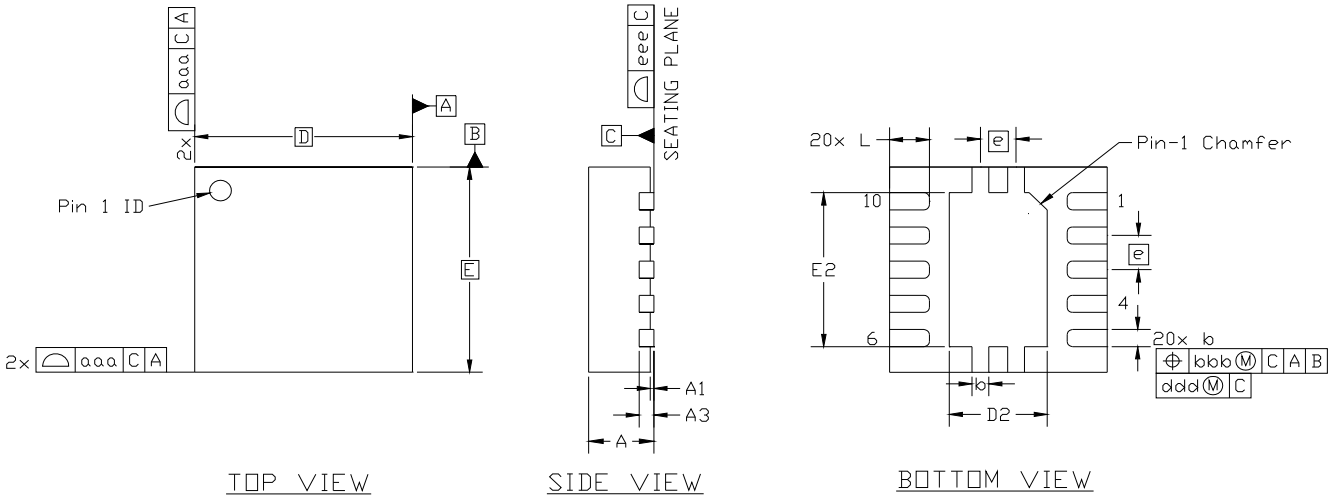


Figure 4. QFN-11 Package Drawing

Table 8. Package Diagram Dimensions

Dimension	Min	Nom	Max
A	0.80	0.90	1.00
A1	0.03	0.07	0.11
A3		0.25 REF	
b	0.18	0.25	0.30
D		3.00 BSC.	
D2	1.30	1.35	1.40
e		0.50 BSC.	
E		3.00 BSC.	
E2	2.20	2.25	2.30
L	.45	.55	.65
aaa	—	—	0.15
bbb	—	—	0.15
ddd	—	—	0.05
eee	—	—	0.08

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MO-243, variation VEED except for custom features D2, E2, and L which are toleranced per supplier designation.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

9.1. Solder Paste Mask

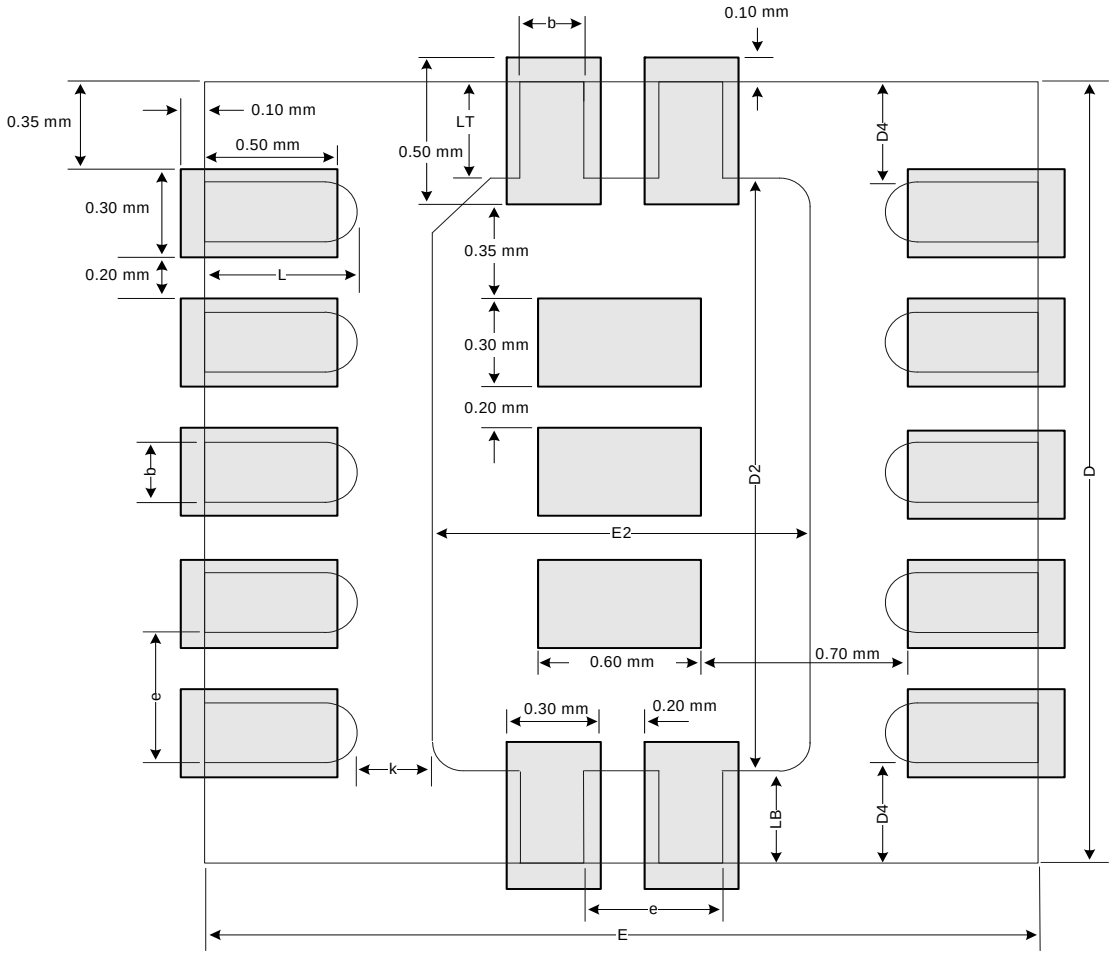


Figure 5. Solder Paste Mask

9.2. PCB Landing Pattern

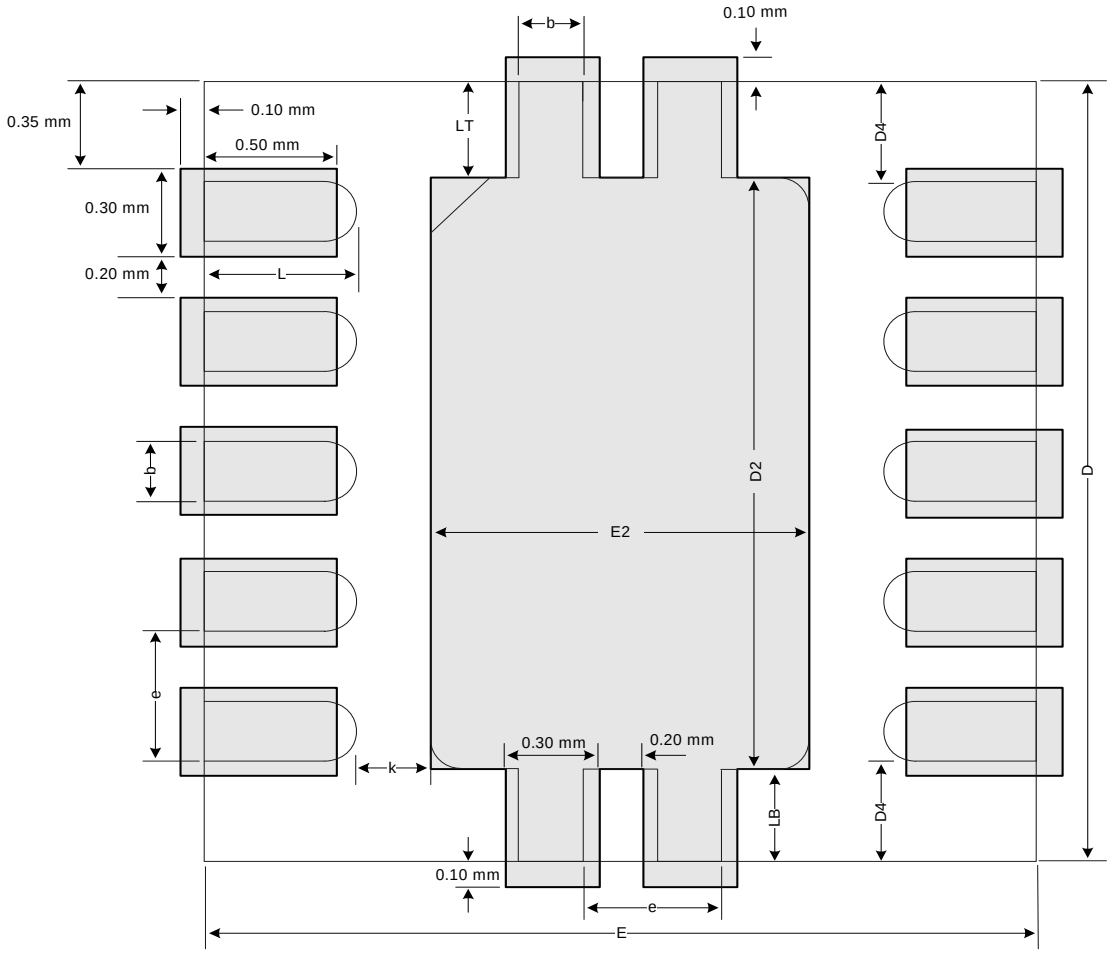


Figure 6. Typical QFN-11 Landing Diagram

9.3. Marking Specification

The top of the Si3461 package is marked as shown in Figure 7.

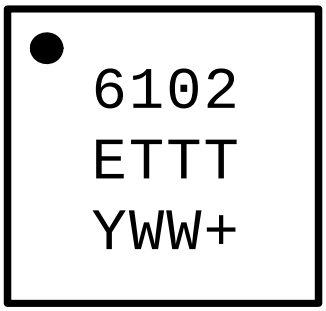


Figure 7. QFN 11 Top Marking

Table 9. Top Marking Explanation

Line 1 Marking:	Pin 1 Identifier	Circle = 0.25 mm Diameter
	Product ID	6102 61 = Si3461; 02 = Firmware Revision 02
Line 2 Marking:	ETTT = Trace Code	Assembly trace code E = Product revision TTT = Assembly trace code
Line 3 Marking:	YWW = Date Code	Assigned by the Assembly contractor. Y = Last Digit of Current Year (ex: 2009 = 9) WW = Current Work Week
	Lead-Free Designator	+

DOCUMENT CHANGE LIST

Revision 0.1 to Revision 0.2

- Updated "9.3. Marking Specification" on page 22.

Revision 0.2 to Revision 0.3

- Updated "8. Ordering Guide" on page 18.

Revision 0.3 to Revision 1.0

- Updated firmware revision to 02.
- Updated Table 3 on page 6
  - Made consistent with firmware revision 02.
  - Corrected previous errors for I_{OH} and V_{IL} values.
- Updated Table 4 on page 7
  - Added min OVLO and max UVLO limits.
  - Updated I_{IN} so as not to include the shunt regulator current.
  - Updated I_{CUT} values to be consistent with IEEE specification.
- Updated Table 6 on page 12.
  - Update suggested parallel resistance at status pin in Note 2.

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