

MC10EL32, MC100EL32

5V ECL ÷2 Divider

Description

The MC10EL/100EL32 is an integrated ÷2 divider. The differential clock inputs and the V_{BB} allow a differential, single-ended or AC coupled interface to the device. The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μ F capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

The reset pin is asynchronous and is asserted on the rising edge. Upon power-up, the internal flip-flop will attain a random state; the reset allows for the synchronization of multiple EL32's in a system.

The 100 Series contains temperature compensation.

Features

- 510 ps Propagation Delay
- 3.0 GHz Toggle Frequency
- ESD Protection: > 1 kV Human Body Model, > 100 V Machine Model
- PECL Mode Operating Range: $V_{CC} = 4.2$ V to 5.7 V with $V_{EE} = 0$ V
- NECL Mode Operating Range: $V_{CC} = 0$ V with $V_{EE} = -4.2$ V to -5.7 V
- Internal Input Pulldown Resistors on CLK(s) and R.
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL 94 V-0 @ 0.125 in, Oxygen Index: 28 to 34
- Transistor Count = 82 devices
- Pb-Free Packages are Available



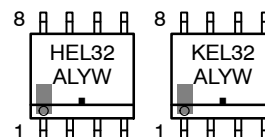
ON Semiconductor®

<http://onsemi.com>

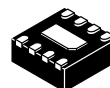
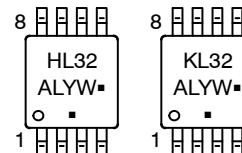
MARKING DIAGRAMS*



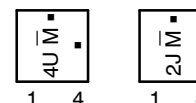
SOIC-8
D SUFFIX
CASE 751



TSSOP-8
DT SUFFIX
CASE 948R



DFN8
MN SUFFIX
CASE 506AA



H = MC10	L = Wafer Lot
K = MC100	Y = Year
4U = MC10	W = Work Week
2J = MC100	M̄ = Date Code
A = Assembly Location	▪ = Pb-Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

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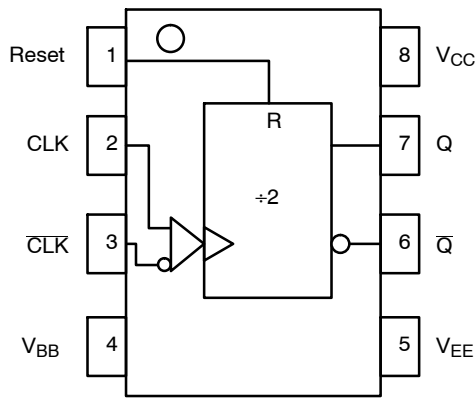


Figure 1. Logic Diagram and Pinout Assignment

Table 1. PIN DESCRIPTION

PIN	FUNCTION
CLK, $\overline{\text{CLK}}$	ECL Clock Inputs*
Reset	ECL Asynch Reset*
Q, $\overline{\text{Q}}$	ECL Data Outputs
V_{BB}	Reference Voltage Output
V_{CC}	Positive Supply
V_{EE}	Negative Supply
EP	(DFN8 only) Thermal exposed pad must be connected to a sufficient thermal conduit. Electrically connect to the most negative supply (GND) or leave unconnected, floating open.

*Pins will default low when left open.

Table 2. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	PECL Mode Power Supply	$V_{\text{EE}} = 0 \text{ V}$		8	V
V_{EE}	NECL Mode Power Supply	$V_{\text{CC}} = 0 \text{ V}$		-8	V
V_{I}	PECL Mode Input Voltage NECL Mode Input Voltage	$V_{\text{EE}} = 0 \text{ V}$ $V_{\text{CC}} = 0 \text{ V}$	$V_{\text{I}} \leq V_{\text{CC}}$ $V_{\text{I}} \geq V_{\text{EE}}$	6 -6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
T_{A}	Operating Temperature Range			-40 to +85	$^{\circ}\text{C}$
T_{stg}	Storage Temperature Range			-65 to +150	$^{\circ}\text{C}$
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	SOIC-8 SOIC-8	190 130	$^{\circ}\text{C}/\text{W}$ $^{\circ}\text{C}/\text{W}$
θ_{JC}	Thermal Resistance (Junction-to-Case)	Standard Board	SOIC-8	41 to 44	$^{\circ}\text{C}/\text{W}$
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	TSSOP-8 TSSOP-8	185 140	$^{\circ}\text{C}/\text{W}$ $^{\circ}\text{C}/\text{W}$
θ_{JC}	Thermal Resistance (Junction-to-Case)	Standard Board	TSSOP-8	41 to 44 $\pm 5\%$	$^{\circ}\text{C}/\text{W}$
T_{sol}	Wave Solder	<2 to 3 sec @ 248 $^{\circ}\text{C}$		265	$^{\circ}\text{C}$
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	DFN8 DFN8	129 84	$^{\circ}\text{C}/\text{W}$ $^{\circ}\text{C}/\text{W}$
T_{sol}	Wave Solder	Pb Pb-Free <2 to 3 sec @ 248 $^{\circ}\text{C}$ <2 to 3 sec @ 260 $^{\circ}\text{C}$		265 265	$^{\circ}\text{C}$
θ_{JC}	Thermal Resistance (Junction-to-Case)	(Note 1)	DFN8	35 to 40	$^{\circ}\text{C}/\text{W}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. JEDEC standard multilayer board – 2S2P (2 signal, 2 power)

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Table 3. 10EL SERIES PECL DC CHARACTERISTICS $V_{CC} = 5.0\text{ V}$; $V_{EE} = 0\text{ V}$ (Note 2)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		25	30		25	30		25	30	mA
V_{OH}	Output HIGH Voltage (Note 6)	3920	4010	4110	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 3)	3050	3200	3350	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	3770		4110	3870		4190	3940		4280	mV
V_{IL}	Input LOW Voltage (Single-Ended)	3050		3500	3050		3520	3050		3555	mV
V_{BB}	Output Voltage Reference	3.57		3.7	3.65		3.75	3.69		3.81	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 4)	2.5		4.6	2.5		4.6	2.5		4.6	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.3			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

2. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +0.25 V / -0.5 V.

3. Outputs are terminated through a 50 Ω resistor to $V_{CC} - 2.0\text{ V}$.

4. V_{IHCMR} min varies 1:1 with V_{EE} . V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{ppmin} and 1 V.

Table 4. 10EL SERIES NECL DC CHARACTERISTICS $V_{CC} = 0\text{ V}$; $V_{EE} = -5.0\text{ V}$ (Note 5)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		25	30		25	30		25	30	mA
V_{OH}	Output HIGH Voltage (Note 6)	-1080	-990	-890	-980	-895	-810	-910	-815	-720	mV
V_{OL}	Output LOW Voltage (Note 6)	-1950	-1800	-1650	-1950	-1790	-1630	-1950	-1773	-1595	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	-1230		-890	-1130		-810	-1060		-720	mV
V_{IL}	Input LOW Voltage (Single-Ended)	-1950		-1500	-1950		-1480	-1950		-1445	mV
V_{BB}	Output Voltage Reference	-1.43		-1.30	-1.35		-1.25	-1.31		-1.19	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 7)	-2.5		-0.4	-2.5		-0.4	-2.5		-0.4	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.3			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

5. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +0.25 V / -0.5 V.

6. Outputs are terminated through a 50 Ω resistor to $V_{CC} - 2.0\text{ V}$.

7. V_{IHCMR} min varies 1:1 with V_{EE} . V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{ppmin} and 1 V.

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Table 5. 100EL SERIES PECL DC CHARACTERISTICS $V_{CC} = 5.0\text{ V}$; $V_{EE} = 0\text{ V}$ (Note 8)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		25	30		25	30		29	35	mA
V_{OH}	Output HIGH Voltage (Note 9)	3915	3995	4120	3975	4045	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 9)	3170	3305	3445	3190	3295	3380	3190	3295	3380	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	3835		4120	3835		4120	3835		4120	mV
V_{IL}	Input LOW Voltage (Single-Ended)	3190		3525	3190		3525	3190		3525	mV
V_{BB}	Output Voltage Reference	3.62		3.74	3.62		3.74	3.62		3.74	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 10)	2.5		4.6	2.5		4.6	2.5		4.6	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

8. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +0.8 V / -0.5 V.

9. Outputs are terminated through a 50 Ω resistor to $V_{CC} - 2.0\text{ V}$.

10. V_{IHCMR} min varies 1:1 with V_{EE} , V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{ppmin} and 1 V.

Table 6. 100EL SERIES NECL DC CHARACTERISTICS $V_{CC} = 0\text{ V}$; $V_{EE} = -5.0\text{ V}$ (Note 11)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		25	30		25	30		29	35	mA
V_{OH}	Output HIGH Voltage (Note 12)	-1085	-1005	-880	-1025	-955	-880	-1025	-955	-880	mV
V_{OL}	Output LOW Voltage (Note 12)	-1830	-1695	-1555	-1810	-1705	-1620	-1810	-1705	-1620	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	-1165		-880	-1165		-880	-1165		-880	mV
V_{IL}	Input LOW Voltage (Single-Ended)	-1810		-1475	-1810		-1475	-1810		-1475	mV
V_{BB}	Output Voltage Reference	-1.38		-1.26	-1.38		-1.26	-1.38		-1.26	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 13)	-2.5		-0.4	-2.5		-0.4	-2.5		-0.4	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

11. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +0.8 V / -0.5 V.

12. Outputs are terminated through a 50 Ω resistor to $V_{CC} - 2$ volts.

13. V_{IHCMR} min varies 1:1 with V_{EE} , V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{ppmin} and 1 V.

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Table 7. AC CHARACTERISTICS $V_{CC} = 5.0\text{ V}$; $V_{EE} = 0\text{ V}$ or $V_{CC} = 0\text{ V}$; $V_{EE} = -5.0\text{ V}$ (Note 14)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{\max}	Maximum Toggle Frequency	2.2	3.0		2.6	3.0		2.6	3.0		GHz
t_{PLH} t_{PHL}	Propagation Delay CLK to Q Reset to Q	360 390	500 540	640 690	420 440	510 540	600 640	450 450	540 550	630 650	ps
V_{PP}	Input Swing (Note 15)	150		1000	150		1000	150		1000	mV
t_{JITTER}	Cycle-to-Cycle Jitter		TBD			TBD			TBD		ps
t_r t_f	Output Rise/Fall Times Q (20% - 80%)	100	225	350	100	225	350	100	225	350	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

14. 10 Series: V_{EE} can vary +0.25 V / -0.5 V.

100 Series: V_{EE} can vary +0.8 V / -0.5 V.

15. $V_{\text{PP}}(\text{min})$ is minimum input swing for which AC parameters guaranteed. The device has a DC gain of ≈ 40 .

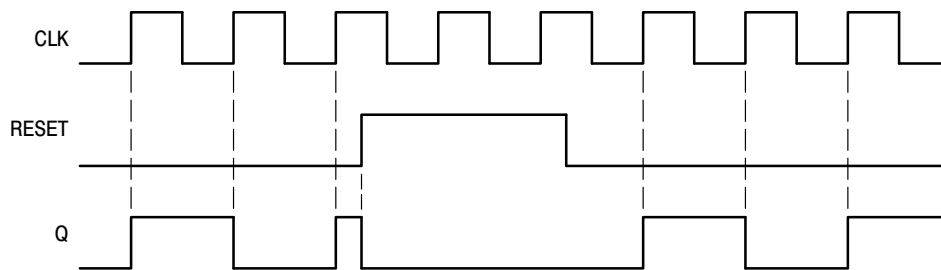


Figure 2. Timing Diagram

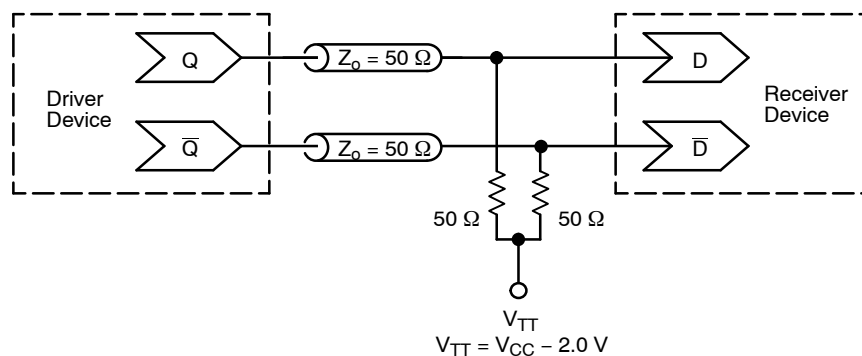


Figure 3. Typical Termination for Output Driver and Device Evaluation
(See Application Note AND8020/D – Termination of ECL Logic Devices.)

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ORDERING INFORMATION

Device	Package	Shipping [†]
MC10EL32D	SOIC-8	98 Units / Rail
MC10EL32DG	SOIC-8 (Pb-Free)	98 Units / Rail
MC10EL32DR2	SOIC-8	2500 / Tape & Reel
MC10EL32DR2G	SOIC-8 (Pb-Free)	2500 / Tape & Reel
MC10EL32DT	TSSOP-8	100 Units / Rail
MC10EL32DTG	TSSOP-8 (Pb-Free)	100 Units / Rail
MC10EL32DTR2	TSSOP-8	2500 / Tape & Reel
MC10EL32DTR2G	TSSOP-8 (Pb-Free)	2500 / Tape & Reel
MC10EL32MNR4	DFN8	1000 / Tape & Reel
MC10EL32MNR4G	DFN8 (Pb-Free)	1000 / Tape & Reel
MC100EL32D	SOIC-8	98 Units / Rail
MC100EL32DG	SOIC-8 (Pb-Free)	98 Units / Rail
MC100EL32DR2	SOIC-8	2500 / Tape & Reel
MC100EL32DR2G	SOIC-8 (Pb-Free)	2500 / Tape & Reel
MC100EL32DT	TSSOP-8	100 Units / Rail
MC100EL32DTG	TSSOP-8 (Pb-Free)	100 Units / Rail
MC100EL32DTR2	TSSOP-8	2500 / Tape & Reel
MC100EL32DTR2G	TSSOP-8 (Pb-Free)	2500 / Tape & Reel
MC100EL32MNR4	DFN8	1000 / Tape & Reel
MC100EL32MNR4G	DFN8 (Pb-Free)	1000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

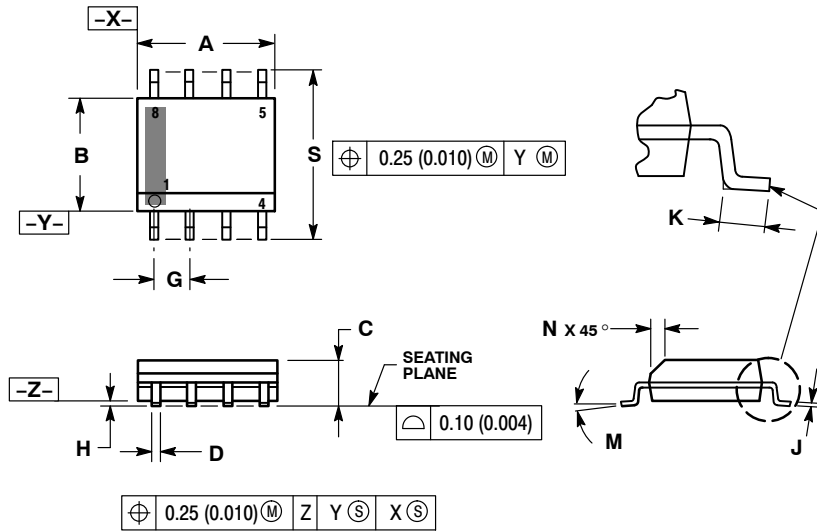
Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPICE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

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PACKAGE DIMENSIONS

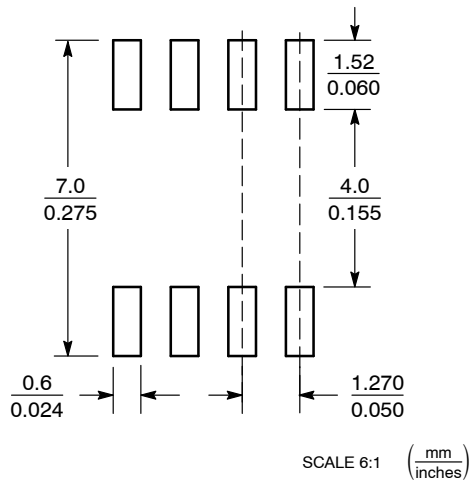
SOIC-8 NB
CASE 751-07
ISSUE AH



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*

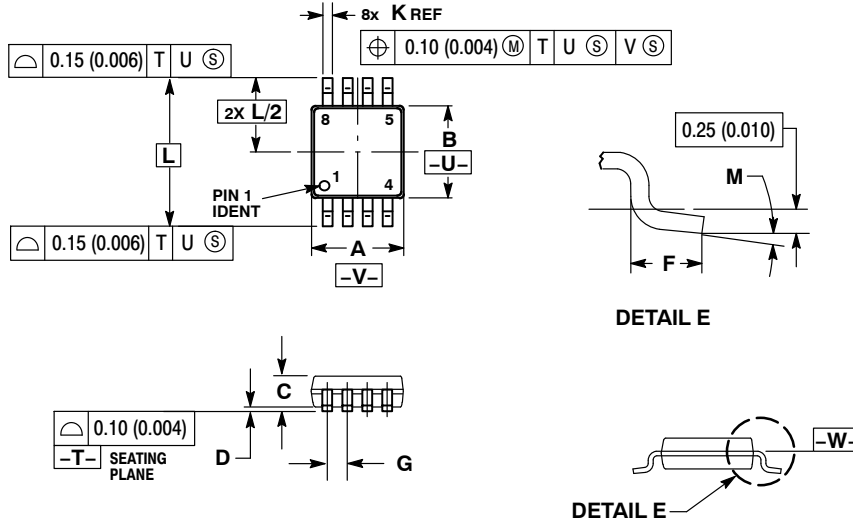


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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PACKAGE DIMENSIONS

TSSOP-8
DT SUFFIX
 PLASTIC TSSOP PACKAGE
 CASE 948R-02
 ISSUE A



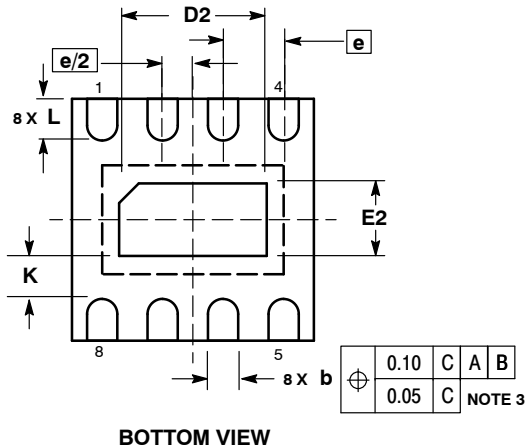
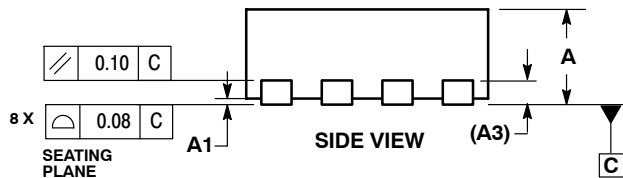
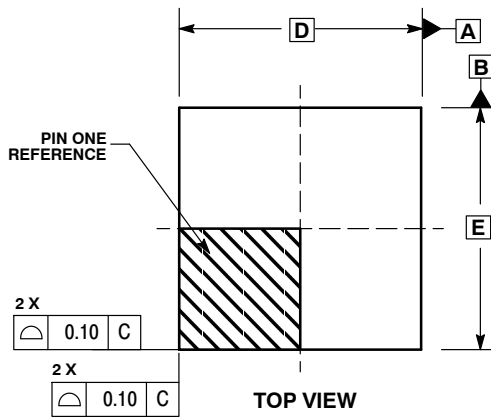
- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
 5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
 6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	0.80	1.10	0.031	0.043
D	0.05	0.15	0.002	0.006
F	0.40	0.70	0.016	0.028
G	0.65 BSC		0.026 BSC	
K	0.25	0.40	0.010	0.016
L	4.90 BSC		0.193 BSC	
M	0°	6°	0°	6°

MC10EL32, MC100EL32

PACKAGE DIMENSIONS

DFN8
CASE 506AA-01
ISSUE D



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994 .
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	2.00 BSC	
D2	1.10	1.30
E	2.00 BSC	
E2	0.70	0.90
e	0.50 BSC	
K	0.20	---
L	0.25	0.35

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