Si5310

PRECISION CLOCK MULTIPLIER/REGENERATOR IC

Features

Complete precision clock multiplier and clock regenerator device:

- Performs clock multiplication to one of two frequency ranges: 150–167 MHz or 600–668 MHz
- Jitter generation as low as 0.5 ps_{rms} for 622 MHz output
- Accepts input clock from 9.4–668 MHz
- Regenerates a "clean", jitter-attenuated version of input clock
- DSPLL™ technology provides superior jitter performance
- Small footprint: 4 x 4 mm
- Low power: 310 mW typical
- ROHS-compliant Pb-free packaging option available

Ordering Information:

See page 21.

Applications

- SONET/SDH systems
- Terabit routers
- Digital cross connects
- Optical transceiver modules
- Gigabit Ethernet systems
- Fibre channel

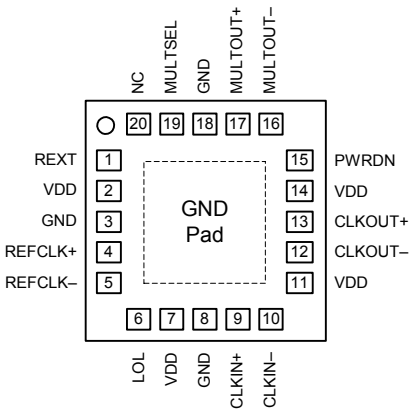
Description

The Si5310 is a fully integrated low-power clock multiplier and clock regenerator IC. The clock multiplier generates an output clock that is an integer multiple of the input clock. The clock regenerator operates simultaneously, creating a "clean" version of the input clock by using the clock synthesis phase-locked loop (PLL) to remove unwanted jitter and square up the input clock's rising and falling edges. The Si5310 uses Silicon Laboratories patented DSPLL® architecture to achieve superior jitter performance while eliminating the analog loop filter found in traditional PLL designs with a digital signal-processing algorithm.

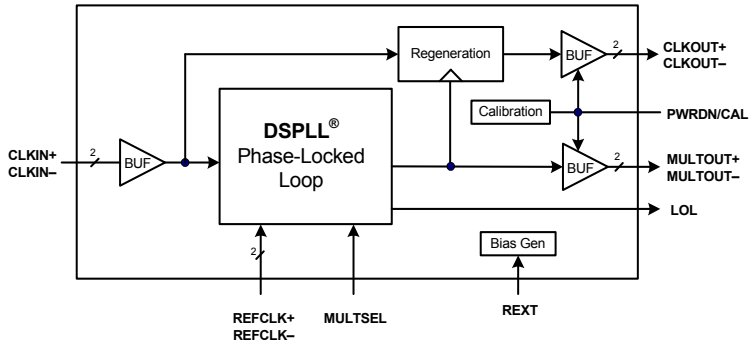
The Si5310 represents a new standard in low jitter, small size, low power, and ease-of-use for clock devices. It operates from a single 2.5 V supply over the industrial temperature range (–40 to 85 °C).

Pin Assignments

Si5310



Functional Block Diagram



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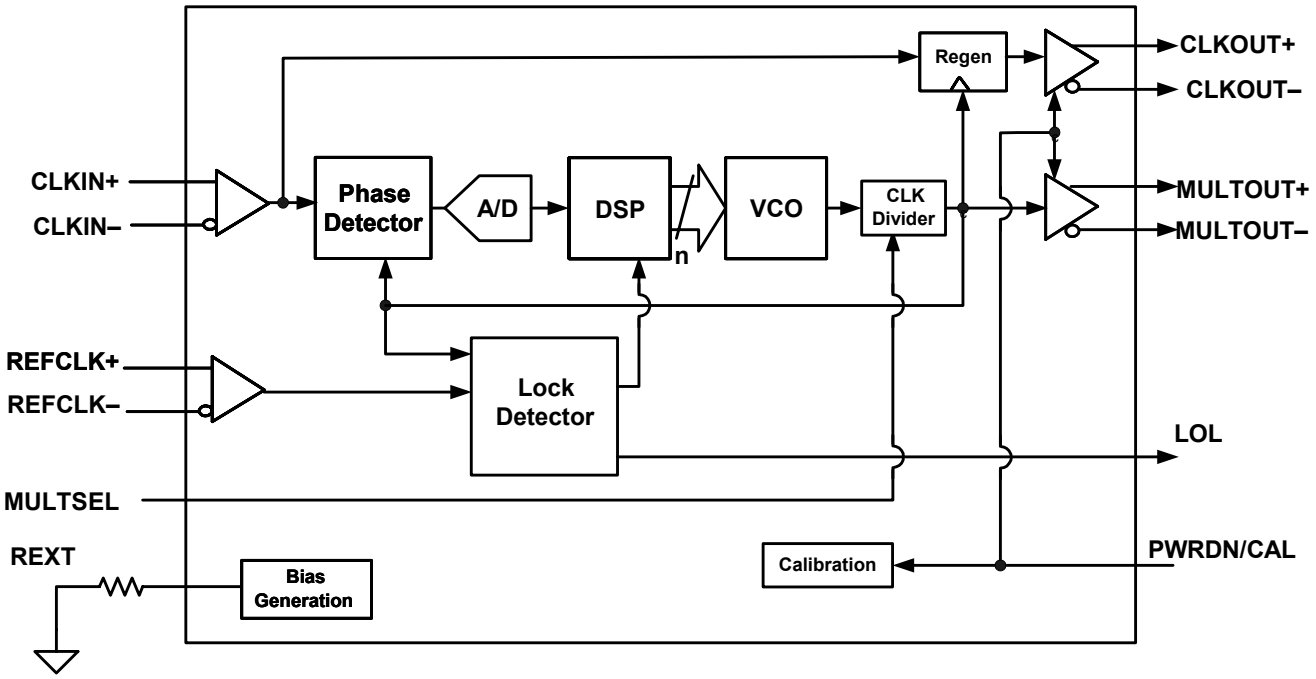
1. Detailed Block Diagram



2. Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min[1]	Typ	Max[1]	Unit
Ambient Temperature	T_A		–40	25	85	°C
Si5310 Supply Voltage[2]	V_{DD}		2.375	2.5	2.625	V

Notes:
1. All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise stated.
2. The Si5310 specifications are guaranteed when using the recommended application circuit (including component tolerance) of "3. Typical Application Circuit" on page 11.

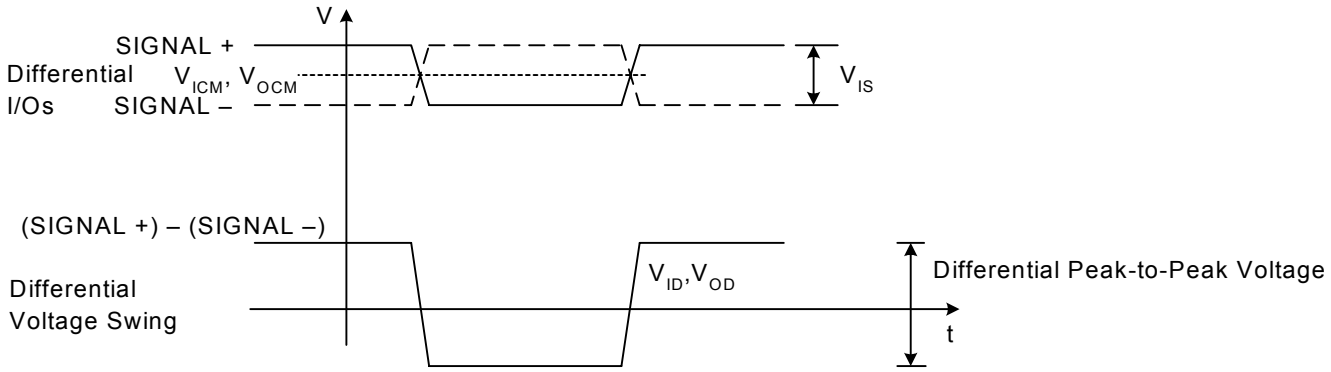


Figure 1. Differential Voltage Measurement (CLKIN, REFCLK, CLKOUT, MULTOUT)

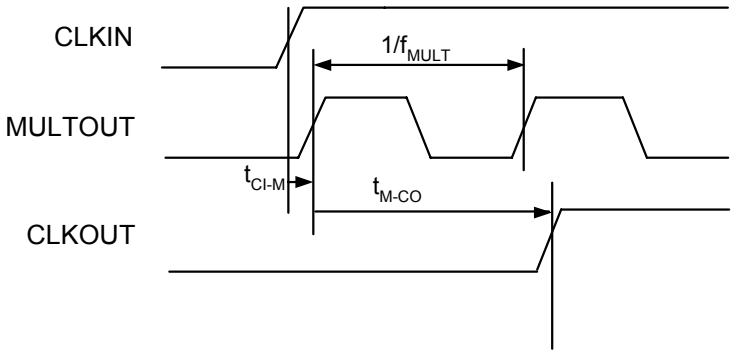


Figure 2. CLKIN to CLKOUT, MULTOUT Phase Relationship

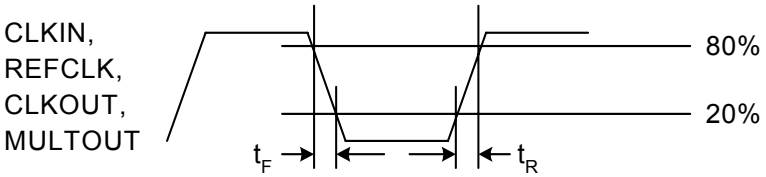


Figure 3. Differential Clock Input and Output Rise/Fall Times

Table 2. DC Characteristics, V_{DD} = 2.5 V, 622 Mbps (MULTSEL = 0)

(V_{DD} = 2.5 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Current MULTSEL = 0 MULTSEL = 1	I_{DD}		 — —	 117 124	 127 134	mA
Power Dissipation MULTSEL = 0 MULTSEL = 1	P_D		 — —	 293 310	 333 352	mW
Common Mode Input Voltage (CLKIN, REFCLK)	V_{ICM}	See Figure 1	—	.80 x V_{DD}	—	V
Input Voltage Range* (CLKIN+, CLKIN–, REFCLK+, REFCLK–)	V_{IS}	See Figure 1	200	—	750	mV
Differential Input Voltage Swing* (CLKIN, REFCLK)	V_{ID}	See Figure 1	200	—	1500	mV_{PP}
Input Impedance (CLKIN, REFCLK)	R_{IN}	Line-to-Line	84	100	116	Ω
Differential Output Voltage Swing (CLKOUT)	V_{OD}	100 Ω Load Line-to-Line	780	970	1260	mV_{PP}
Differential Output Voltage Swing (MULTOUT)	V_{OD}	100 Ω Load Line-to-Line	780	970	1260	mV_{PP}
Output Common Mode Voltage (CLKOUT, MULTOUT)	V_{OCM}	100 Ω Load Line-to-Line	—	V_{DD} – 0.23	—	V
Output Impedance (CLKOUT, MULTOUT)	R_{OUT}	Single-ended	84	100	116	Ω
Output Short to GND (CLKOUT, MULTOUT)	$I_{SC(–)}$		—	25	31	mA
Output Short to V_{DD} (CLKOUT, MULTOUT)	$I_{SC(+)}$		–17.5	–14.5	—	mA
Input Voltage Low (LVTTL Inputs)	V_{IL}		—	—	.8	V
Input Voltage High (LVTTL Inputs)	V_{IH}		2.0	—	—	V
Input Low Current (LVTTL Inputs)	I_{IL}		—	—	10	µA
Input High Current (LVTTL Inputs)	I_{IH}		—	—	10	µA
Output Voltage Low (LVTTL Outputs)	V_{OL}	I_O = 2 mA	—	—	0.4	V
Output Voltage High (LVTTL Outputs)	V_{OH}	I_O = 2 mA	2.0	—	—	V
Input Impedance (LVTTL Inputs)	R_{IN}		10	—	—	kΩ
PWRDN/CAL Internal Pulldown Current	I_{PWRDN}	$V_{PWRDN} \geq 0.8$ V	15	25	45	µA

***Note:** The CLKIN and REFCLK inputs may be driven differentially or single-endedly. When driving single-endedly, the voltage swing of the signal applied to the active input must exceed the specified minimum Differential Input Voltage Swing (V_{ID} min) and the unused input must be ac-coupled to ground. When driving differentially, the difference between the positive and negative input signals must exceed V_{ID} min. (Each individual input signal needs to swing only half of this range.) In either case, the voltage applied to any individual pin (CLKIN+, CLKIN–, REFCLK+, or REFCLK–) must not exceed the specified maximum Input Voltage Range (V_{IS} max).

Table 3. AC Characteristics
(V_{DD} = 2.5 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
CLKIN Frequency Range*			9.375	—	668	MHz
CLKIN Duty Cycle			40	—	60	%
REFCLK Range*			9.375	—	167	MHz
REFCLK Duty Cycle	C_{DUTY}		40	50	60	%
REFCLK Frequency Tolerance	C_{TOL}		–100	—	100	ppm
MULTOUT Clock Rate MULTOUT = 0 MULTOUT = 1	f_{MULT}		 600 150	 — —	 668 167	MHz
Output Rise/Fall Time (differential) (CLKOUT, MULTOUT)	t_R, t_F	Figure 3	—	80	110	ps
Input Rise/Fall Time (differential) (CLKIN, REFCLK)	t_R, t_F	Figure 3	—	—	50	ns
CLKIN to MULTOUT Delay MULTSEL = 0 MULTSEL = 1	t_{CI-M}	Figure 2	 –670 2.4	 130 3.4	 930 4.4	 ps ns
MULTOUT to CLKOUT Delay MULTSEL = 0 MULTSEL = 1	t_{M-CO}	Figure 2	 $1/f_{MULT}$ + 100 780	 $1/f_{MULT}$ + 140 870	 $1/f_{MULT}$ + 180 960	 ps ps
Input Return Loss		100 kHz–1 GHz	—	20	—	dB

***Note:** See Table 9.

Table 4. AC Characteristics (PLL Performance Characteristics)
(V_{DD} = 2.5 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Jitter Tolerance (MULTSEL = 0, MULTOUT = 600 to 668 MHz)	$J_{TOL(PP)}$	See Table 5				
Jitter Tolerance (MULTSEL = 1, MULTOUT = 150 to 167 MHz)	$J_{TOL(PP)}$	See Table 6				
Jitter Generation (MULTOUT, CLKOUT) (MULTSEL = 0, MULTOUT = 600 to 668 MHz)* (measurement BW = 12kHz to 1MHz)	$J_{GEN(rms)}$	Clock Input (MHz) = 37.500 to 41.750	—	2.5	5.4	ps_{rms}
		Clock Input (MHz) = 75.000 to 83.500	—	1.6	3.1	ps_{rms}
		Clock Input (MHz) = 150.000 to 167.000	—	0.9	1.6	ps_{rms}
		Clock Input (MHz) = 300.000 to 334.000	—	0.6	1.3	ps_{rms}
		Clock Input (MHz) = 600.000 to 668.000	—	0.4	0.8	ps_{rms}
Jitter Generation (MULTOUT, CLKOUT) (MULTSEL = 1, MULTOUT = 150 to 167 MHz)* (measurement BW = 12kHz to 1MHz)	$J_{GEN(rms)}$	Clock Input (MHz) = 9.375 to 10.438	—	8.5	34.0	ps_{rms}
		Clock Input (MHz) = 18.750 to 20.875	—	5.0	19.7	ps_{rms}
		Clock Input (MHz) = 37.500 to 41.750	—	3.7	15.2	ps_{rms}
		Clock Input (MHz) = 75.000 to 83.500	—	2.3	15.2	ps_{rms}
		Clock Input (MHz) = 150.000 to 167.000	—	1.1	3.0	ps_{rms}
Jitter Transfer Bandwidth (MULTSEL = 0, MULTOUT = 600 to 668 MHz)*	J_{BW}	Clock Input (MHz) = 37.500 to 41.750	—	75	105	kHz
		Clock Input (MHz) = 75.000 to 83.500	—	150	210	kHz
		Clock Input (MHz) = 150.000 to 167.000	—	300	420	kHz
		Clock Input (MHz) = 300.000 to 334.000	—	600	840	kHz
		Clock Input (MHz) = 600.000 to 668.000	—	1200	1680	kHz

***Note:** See PLL Performance section of this document for test descriptions.

Table 4. AC Characteristics (PLL Performance Characteristics) (Continued)
(V_{DD} = 2.5 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Jitter Transfer Bandwidth (MULTSEL = 1, MULTOUT = 150 to 167 MHz)*	J_{BW}	Clock Input (MHz) = 9.375 to 10.438	—	19	26	kHz
		Clock Input (MHz) = 18.750 to 20.875	—	38	53	kHz
		Clock Input (MHz) = 37.500 to 41.750	—	75	105	kHz
		Clock Input (MHz) = 75.000 to 83.500	—	150	210	kHz
		Clock Input (MHz) = 150.000 to 167.000	—	300	420	kHz
Jitter Transfer Peaking (MULTSEL = 0, MULTOUT = 600 to 668 MHz)*	J_P	Clock Input (MHz) = 37.500 to 41.750	—	0.12	0.4	dB
		Clock Input (MHz) = 75.000 to 83.500	—	0.06	0.2	dB
		Clock Input (MHz) = 150.000 to 167.000	—	0.03	0.1	dB
		Clock Input (MHz) = 300.000 to 334.000	—	0.02	0.066	dB
		Clock Input (MHz) = 600.000 to 668.000	—	0.01	0.033	dB
Jitter Transfer Peaking (MULTSEL = 1, MULTOUT = 150 to 167 MHz)*	J_P	Clock Input (MHz) = 9.375 to 10.438	—	0.12	0.4	dB
		Clock Input (MHz) = 18.750 to 20.875	—	0.06	0.2	dB
		Clock Input (MHz) = 37.500 to 41.750	—	0.03	0.1	dB
		Clock Input (MHz) = 75.000 to 83.500	—	0.02	0.066	dB
		Clock Input (MHz) = 150.000 to 167.000	—	0.01	0.033	dB
Acquisition Time	T_{AQ}	After falling edge of PWRDN/CAL	1.45	1.5	1.7	ms
		From the return of valid CLKIN	40	60	150	µs
Frequency Difference at which PLL goes out of Lock (REFCLK compared to the divided down VCO clock)	LOL		450	600	750	ppm
Frequency Difference at which PLL goes into Lock (REFCLK compared to the divided down VCO clock)	LOCK		150	300	450	ppm

***Note:** See PLL Performance section of this document for test descriptions.

Table 5. Minimum Jitter Tolerance in Nanoseconds* (MULTSEL = 0, MULTOUT = 600 to 668 MHz)

Frequency (Hz)	37.5–41.75 MHz Clock Input	75–83.5 MHz Clock Input	150–167 MHz Clock Input	300–334 MHz Clock Input
< 300	25.0	25.0	25.0	25.0
25K	1.6	3.2	6.5	16
250K	1.6	3.2	3.0	3.2
> 1M	0.3	0.3	0.5	0.5
***Note:** Measured using sinusoidal jitter at stated Test Condition frequency.				

Table 6. Minimum Jitter Tolerance in Nanoseconds* (MULTSEL = 1, MULTOUT = 150 to 167 MHz)

Frequency (Hz)	9.375–10.438 MHz Clock Input	18.75–20.875 MHz Clock Input	37.5–41.75 MHz Clock Input	75–83.5 MHz Clock Input
< 300	66.7	66.7	66.7	66.7
6.5K	6.4	13.0	29.0	33.3
65K	1.2	1.9	1.9	4.8
325K	1.2	1.9	1.9	2.6
> 1M	1.2	1.9	1.9	1.9
***Note:** Measured using sinusoidal jitter at stated Test Condition frequency.				

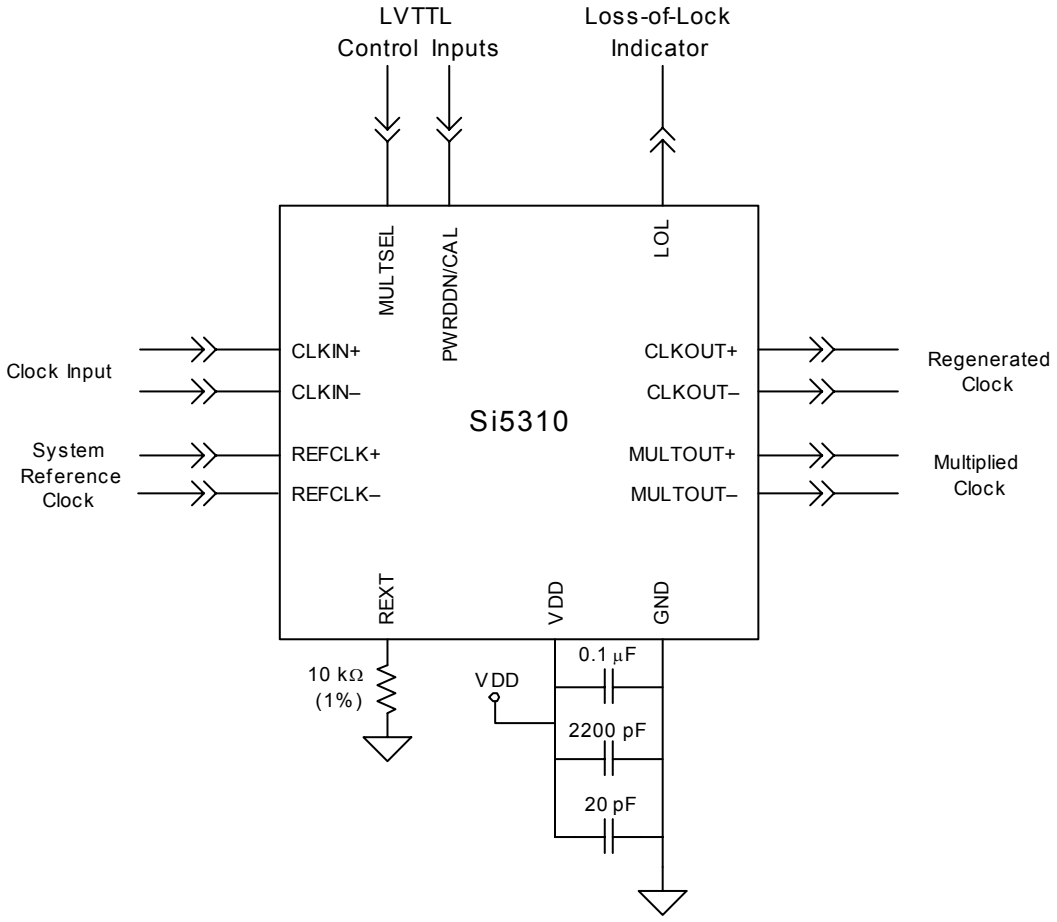
Table 7. Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	–0.5 to 2.8	V
LVTTL Input Voltage	V_{DIG}	–0.3 to 3.6	V
Differential Input Voltages	V_{DIF}	–0.3 to (V_{DD}+ 0.3)	V
Maximum Current any output PIN		±50	mA
Operating Junction Temperature	T_{JCT}	–55 to 150	°C
Storage Temperature Range	T_{STG}	–55 to 150	°C
ESD HBM Tolerance (100 pf, 1.5 kΩ) CLKIN+, CLKIN–, REFCLK+, REFCLK–, All other pins	 — —	 1 1.5	 kV kV
Note: Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.			

Table 8. Thermal Characteristics

Parameter	Symbol	Test Condition	Value	Unit
Thermal Resistance Junction to Ambient	φ_{JA}	Still Air	38	°C/W

3. Typical Application Circuit



4. Functional Description

The Si5310 is an integrated clock multiplier and clock regenerator device based on SIlicon Laboratories DSPLL™ technology. The DSPLL phase locks to the clock input signal (CLKIN) and generates a phase-locked output clock (MULTOUT) at a multiple of the input clock frequency. The DSPLL is also employed to regenerate an output clock (CLKOUT) that is a jitter-attenuated version of the input clock with clean rising and falling edges.

The MULTOUT output is configured to operate in either the 150–167 MHz or the 600–668 MHz frequency range using the MULTSEL control input. A reference clock input signal (REFCLK) is used by the DSPLL as a reference for determination of the PLL lock status. For convenience, REFCLK can be provided at any one of five frequencies, each a multiple of the CLKIN frequency. The REFCLK rate is automatically detected, so no control inputs are needed for configuration. The REFCLK input can be synchronous or asynchronous with respect to the CLKIN input. The operating ranges for the CLKIN, CLKOUT, MULTOUT, and REFCLK signals are indicated in Table 9. Typical values for several applications are presented in Table 10.

Table 9. CLKIN, CLKOUT, MULTOUT, REFCLK Operating Ranges

MULTSEL	CLKIN Range (MHz)	REFCLK = 2^n x CLKIN ±100 ppm (See Note 1)	CLKOUT	MULTOUT
0 (MULTOUT = 600–668 MHz)	37.500–41.750	n = –2, –1, 0, 1, 2	1xCLKIN	16xCLKIN
	75.000–83.500	n = –3, –2, –1, 0, 1	1xCLKIN	8xCLKIN
	150.000–167.000	n = –4, –3, –2, –1, 0	1xCLKIN	4xCLKIN
	300.000–334.000	n = –5, –4, –3, –2, –1	1xCLKIN	2xCLKIN
	600.000–668.000	n = –6, –5, –4, –3, –2	See Note 2	1xCLKIN
1 (MULTOUT = 150–167 MHz)	9.375–10.438	n = 0, 1, 2, 3, 4	1xCLKIN	16xCLKIN
	18.750–20.875	n = –1, 0, 1, 2, 3	1xCLKIN	8xCLKIN
	37.500–41.750	n = –2, –1, 0, 1, 2	1xCLKIN	4xCLKIN
	75.000–83.500	n = –3, –2, –1, 0, 1	1xCLKIN	2xCLKIN
	150.000–167.000	n = –4, –3, –2, –1, 0	See Note 2	1xCLKIN

Note:
1. The REFCLK input can be set to any one of the five CLKIN multiples indicated. The REFCLK input can be asynchronous to the CLKIN input, but must be within ±100 ppm of the stated CLKIN multiple.
2. The CLKOUT output is not valid for MULTOUT:CLKIN ratios of 1:1 (MULTOUT = 1 x CLKIN.)

Table 10. Clock Values for Typical Applications

	CLKIN (MHz)	REFCLK Input (MHz)	MULTSEL	CLKOUT (MHz)	MULTOUT output (MHz)
SONET/SDH	9.72	9.72	1	9.72	155.52
	19.44	19.44	1	19.44	155.52
	38.88	38.88	1	38.88	155.52
			0	38.88	622.08
	77.76	77.76	1	77.76	155.52
			0	77.76	622.08
	155.52	155.52	1	—	155.52
			0	155.52	622.08
	311.04	9.72, 19.44, 38.88, 77.76, or 155.52	0	311.04	622.08
	622.08	9.72, 19.44, 38.88, 77.76, or 155.52	0	—	622.08
Gigabit Ethernet	9.77	9.77	1	9.77	156.25
	19.53	19.53	1	19.53	156.25
	39.06	39.06	1	39.06	156.25
			0	39.06	625
	78.125	78.125	1	78.125	156.25
			0	78.125	625
	156.25	156.25	1	—	156.25
			0	156.25	625
	312.5	9.77, 19.53, 39.06, 78.125, or 156.25	0	312.5	625
	625	9.77, 19.53, 39.06, 78.125, or 156.25	0	—	625.00
SONET/SDH FEC (15/14)	10.41	10.41	1	10.41	166.63
	20.83	20.83	1	20.83	166.63
	41.66	41.66	1	41.66	166.63
			0	41.66	666.51
	83.31	83.31	1	83.31	166.63
			0	83.31	666.51
	166.63	166.63	1	—	166.63
			0	166.63	666.51
	333.26	10.41, 20.83, 41.66, 83.31, or 166.63	0	333.26	666.51
	666.51	10.41, 20.83, 41.66, 83.31, or 166.63	0	—	666.51

4.1. DSPLL®

The PLL structure (shown in Figure 1 on page 5) utilizes Silicon Laboratories' DSPLL® technology to produce superior jitter performance while eliminating the need for external loop filter components found in traditional PLL implementations. This is achieved by using a digital signal processing (DSP) algorithm to replace the loop filter commonly found in analog PLL designs. This algorithm processes the phase detector error term and generates a digital control value to adjust the frequency of the voltage-controlled oscillator (VCO). The technology produces clocks with less jitter than is generated using traditional methods. In addition, because external loop filter components are not required, sensitive noise entry points are eliminated, thus making the DSPLL less susceptible to board-level noise sources.

4.2. Clock Multiplier

The DSPLL phase locks to the clock input signal (CLKIN) and generates an output clock (MULTOUT) at a multiple of the input clock frequency. The MULTOUT output is configured to operate in either the 150–167 MHz frequency range or in the 600–668 MHz frequency range using the MULTSEL control input as indicated in Table 9. Values for typical applications are given in Table 10.

The amount of jitter present in the MULTOUT output is a function of the DSPLL jitter transfer function and jitter generation characteristic. Details are provided in the PLL Performance section of this document. (See Figures 4 and 5.) The amount of jitter that the DSPLL can tolerate on the CLKIN input is specified in Tables 5 and 6.

The DSPLL implementation in the Si5310 is insensitive to the duty cycle of the CLKIN input. The MULTOUT output will continue to exhibit a very good duty cycle characteristic even when the CLKIN input duty cycle is degraded.

4.3. 1x Multiplication

The Si5310 Clock Multiplier function may also be utilized as a 1x multiplier in order to provide jitter attenuation and duty cycle correction without multiplication of the input clock frequency.

Note: When the Si5310 is configured as a 1:1 multiplier, the CLKOUT output is not valid.

4.4. Clock Regeneration

The DSPLL is used to regenerate a jitter-attenuated version of the CLKIN input, resulting in a “clean” CLKOUT output with sharp rising and falling edges. The CLKOUT output is a resampled version of the CLKIN input with all CLKOUT transitions occurring synchronously with the rising edges of the MULTOUT output. The rising edges of CLKOUT are insensitive to the location of the falling edges of the CLKIN input. Thus the period of CLKOUT, measured rising edge to rising edge, is not affected by the CLKIN duty cycle or by jitter on the falling edge of CLKIN.

The falling edges of CLKOUT may be affected by the location of the CLKIN falling edges as follows: If the duty cycle error of CLKIN is significant relative to the period of MULTOUT, then

1. The CLKOUT duty cycle may deviate from 50% (the falling edge of CLKOUT will be time quantized to the nearest rising edge of MULTOUT.)
2. Jitter on the falling edges of CLKIN may result in a CLKOUT duty cycle that alternates between two discrete values.

Note: When the Si5310 is configured as a 1:1 multiplier, the CLKOUT output is not valid.

4.5. Reference Clock

The Si5310 CMU requires an external reference clock applied to the REFCLK input for normal device operation. When REFCLK is absent, the LOL alarm will always be asserted when it has been determined that no activity exists on REFCLK, indicating the lock status of the PLL is unknown. Additionally, the reference clock input is used to center the DSPLL and also to act as a reference for determination of the PLL lock status. REFCLK is a multiple of the CLKIN frequency, and can be provided in any one of five frequency ranges (9.375–10.438 MHz, 18.78–20.875 MHz, 37.500–41.750 MHz, 75.00–83.50 MHz, or 150–167.00 MHz). The REFCLK rate is automatically detected by the Si5310, so no control inputs are needed for REFCLK frequency selection. The REFCLK input may be synchronous or asynchronous with respect to the CLKIN input. The frequency relationship between REFCLK and CLKIN is indicated in Table 9. In many applications, it may be desirable to tie REFCLK and CLKIN together and drive them from the same clock source. The Si5310 is insensitive to the phase relationship between CLKIN and REFCLK, so these differential inputs may be driven in phase or 180° out of phase if this simplifies board layout. Values for typical applications are given in Table 10.

4.6. DSPLL Lock Detection (Loss-of-Lock)

The Si5310 provides lock-detect circuitry that indicates whether the DSPLL has achieved frequency lock with the incoming CLKIN signal. The circuit compares the frequency of a divided down version of the multiplier

output with the frequency of the supplied reference clock. If the divided multiplier output frequency deviates from that of the reference clock by the amount specified in Table 4 on page 8, the PLL is declared out of lock, and the loss-of-lock (LOL) pin is asserted high. In this state, the PLL will periodically try to reacquire lock with the input clock (CLKIN). During reacquisition, the multiplier output clock (MULTOUT) may drift over a ±600 ppm range relative to the applied reference clock and the LOL output alarm may toggle until the PLL has reacquired frequency lock. Due to the low noise and stability of the DSPLL, under the condition where the input clock is removed from the inputs, there is the possibility that the PLL will not drift enough to render an out-of-lock condition.

If REFCLK is removed, the LOL output alarm will always be asserted when it has been determined that no activity exists on REFCLK, indicating the frequency lock status of the PLL is unknown.

Note: LOL is not asserted during PWRDN/CAL.

4.7. PLL Performance

The Si5310 DSPLL circuitry is designed to provide low jitter generation, high jitter tolerance, and a well-controlled jitter transfer function with low peaking. Each of these key performance parameters is described more fully in the following sections.

4.7.1. Jitter Tolerance

Jitter tolerance for the Si5310 is defined as the maximum peak-to-peak sinusoidal jitter that can be added to the incoming clock before the PLL exceeds its allowable operating range and loses lock. The tolerance is a function of the jitter frequency, the incoming clock rate, and the MULTSEL setting.

The jitter tolerance for specified jitter frequencies and input clock rates is given in Tables 5 and 6.

4.7.2. Jitter Transfer

Jitter transfer is defined as the ratio of output signal jitter to input signal jitter for a specified jitter frequency. The jitter transfer characteristic determines the amount of input clock jitter that will be passed on to the Si5310 CLKOUT and MULTOUT outputs. The DSPLL technology used in the Si5310 provides a tightly controlled jitter transfer curve because many of the PLL gain parameters are determined by digital signal processing algorithms which do not vary over supply voltage, process, and temperature. In a system application, a well-controlled transfer curve minimizes the output clock jitter variation from board to board, providing more consistent system level jitter performance.

The jitter transfer characteristic is a function of the MULTSEL setting and the input clock rate. Higher input clock rates produce higher bandwidth transfer functions with lower jitter peaking. Table 4 gives the 3 dB bandwidth and peaking values for specified input clock rates and MULTSEL settings. Figures 4 and 5 show a family of jitter transfer curves for different input clock rates.

4.7.3. Jitter Generation

Jitter generation is defined as the amount of jitter produced at the output of the device with a jitter free input clock. Generated jitter arises from sources within the VCO and other PLL components. Jitter generation is a function of MULTSEL setting and input clock frequency. For clock multiplier applications, the higher the multiplier ratio desired, the larger the jitter generation. Table 4 gives the jitter generation values for specified MULTSEL settings and input clock rates.

4.8. Device Powerdown

The Si5310 PWRDN/CAL input can be used to hold the device in a power-down state when not in use. When the PWRDN/CAL input is asserted (set high), the CLKOUT and MULTOUT output drivers are disabled and the positive and negative terminals of the CLKOUT and MULTOUT outputs are each tied to VDD through 100 Ω on-chip resistors. This feature is useful in reducing power consumption in applications that employ redundant clock sources. When PWRDN/CAL is released (set to low) the digital logic is reset to a known initial condition and the DSPLL circuitry is recalibrated and will begin to lock to the incoming clock.

4.9. PLL Self-Calibration

Si5310 device provides an internal self-calibration function that optimizes the loop gain parameters within the internal DSPLL. Self-calibration is initiated by a high-to-low transition of the PWRDN/CAL signal while a valid reference clock is supplied to the REFCLK input.

For optimal jitter performance, the supply voltage should be stable at 2.5 V ±10% when calibration is initiated. The PWRDN/CAL signal should be held high for at least 1 μS after the supply has stabilized before transitioning low to initiate self-calibration. See Silicon Laboratories application note AN42 for suggested methods of generating the PWRDN/CAL signal for initiation of self-calibration.

4.10. Device Grounding

The Si5310 uses the GND pad on the bottom of the 20-pin micro leaded package (MLP) for device ground. This pad should be connected directly to the analog supply ground. See Figures 11 and 12 for the ground (GND) pad location.

4.11. Bias Generation Circuitry

The Si5310 makes use of an external resistor to set internal bias currents. The external resistor allows precise generation of bias currents which significantly reduces power consumption compared with traditional implementations that use an internal resistor. The bias generation circuitry requires a 10 kΩ (1%) resistor connected between REXT and GND.

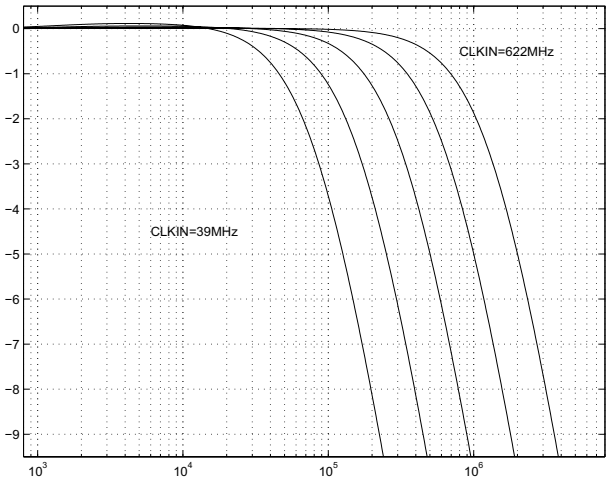


Figure 4. PLL Jitter Transfer Functions, MULTSEL = 0 (MULTOUT = 600–668 MHz)

4.12. Differential Input Circuitry

The Si5310 provides differential inputs for both the input clock (CLKIN) and the reference clock (REFCLK) inputs. An example termination for these inputs is shown in Figure 6. In applications where direct dc coupling is possible, the 0.1 μF capacitors may be omitted. The CLKIN and REFCLK input amplifiers require input signals with minimum differential peak-to-peak voltages as specified in Table 2 on page 6.

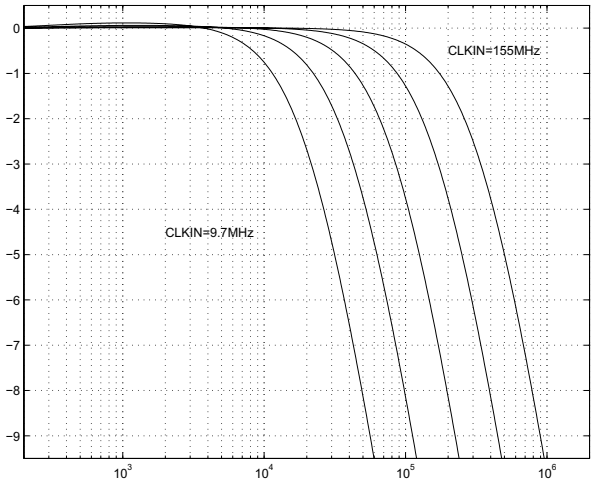


Figure 5. PLL Jitter Transfer Functions, MULTSEL = 1 (MULTOUT = 150–167 MHz)

4.13. Differential Output Circuitry

The Si5310 utilizes a current mode logic (CML) architecture to output both the regenerated clock (CLKOUT) and the multiplied clock (MULTOUT). An example of output termination with ac coupling is shown in Figure 10. For applications in which direct dc coupling is possible, the 0.1 μF capacitors may be omitted. The differential peak-to-peak voltage swing of the CML is listed in Table 2 on page 6.

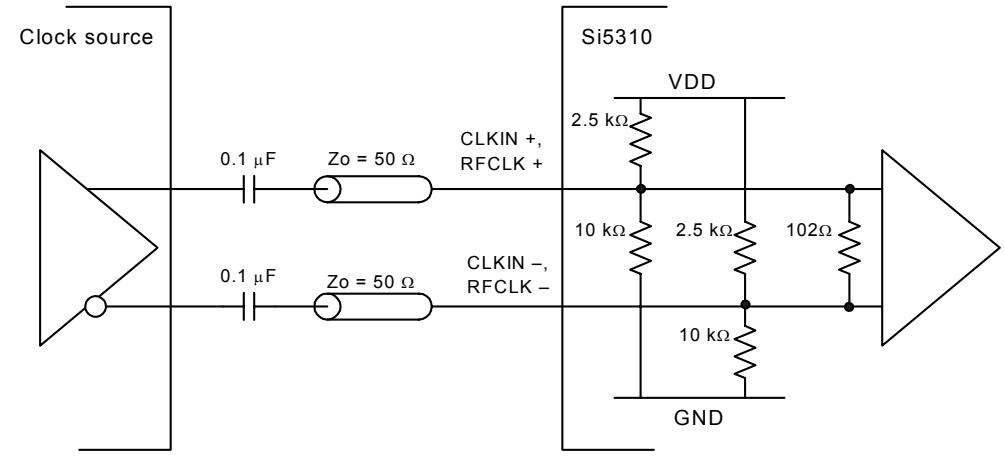


Figure 6. Input Termination for CLKIN and REFCLK (ac-coupled)

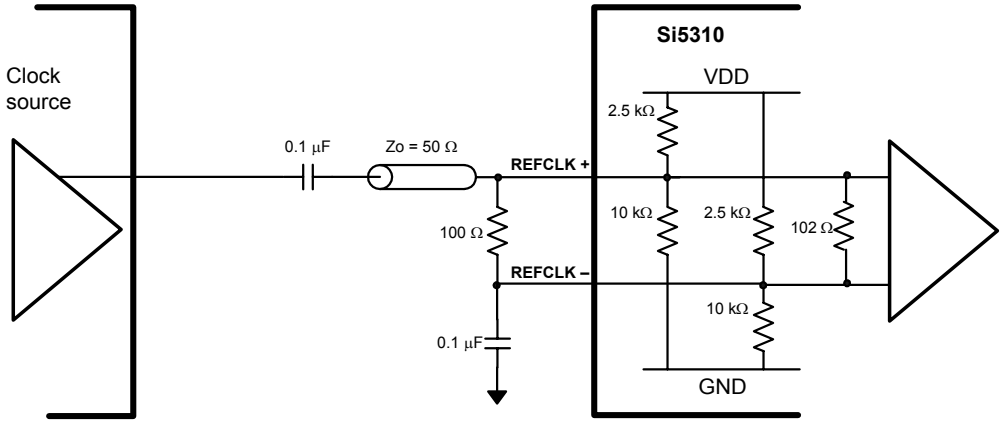


Figure 7. Single-Ended Input Termination for REFCLK (ac-coupled)

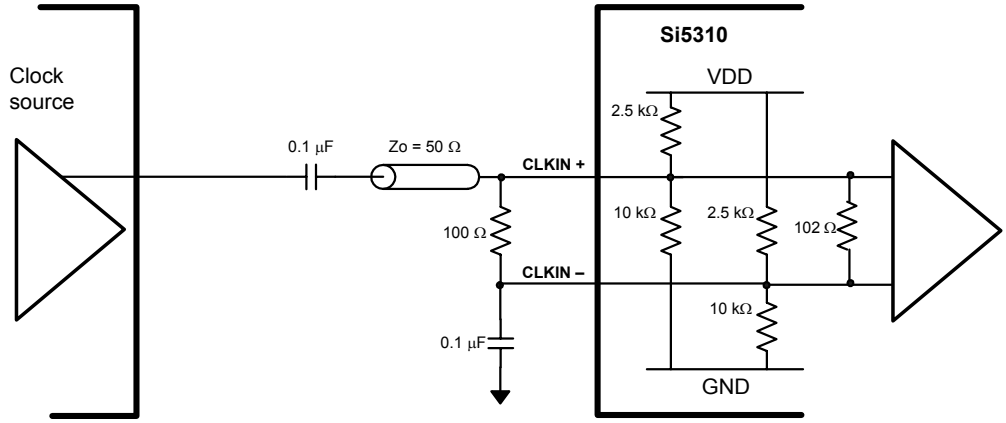


Figure 8. Single-Ended Input Termination for CLKIN (ac-coupled)

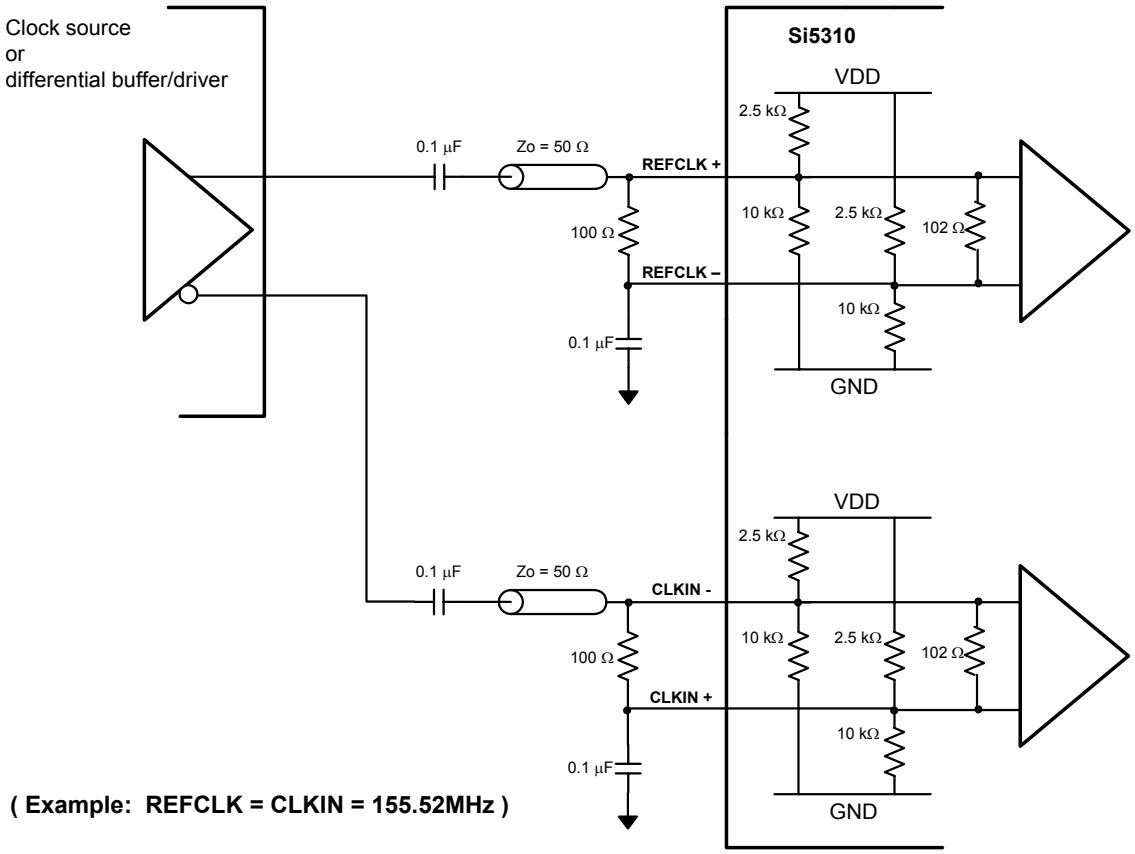


Figure 9. Single-Ended Input Termination for REFCLK & CLKIN (ac-coupled)

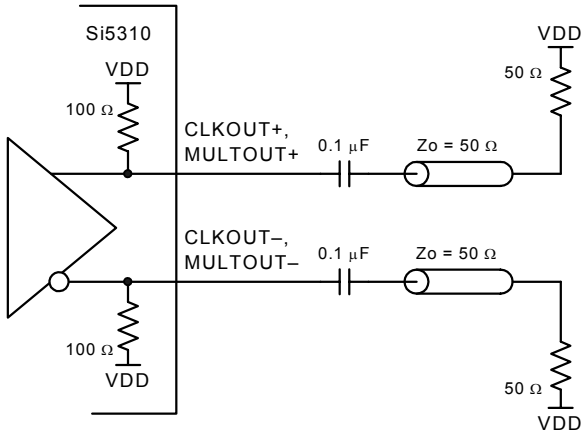
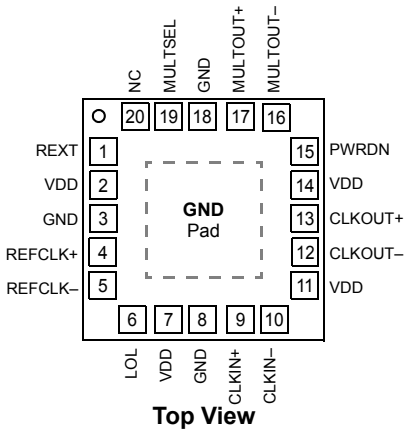


Figure 10. Output Termination for CLKOUT and MULTOUT (ac-coupled)

5. Pin Descriptions: Si5310



Top View

Figure 11. Si5310 Pin Configuration

Table 11. Si5310 Pin Descriptions

Pin #	Pin Name	I/O	Signal Level	Description
1	REXT			**External Bias Resistor.** This resistor is used by onboard circuitry to establish bias currents within the device. This pin must be connected to GND through a 10 kΩ (1%) resistor.
2, 7, 11, 14	VDD		2.5 V	**Supply Voltage.** Nominally 2.5 V.
3, 8, 18, and GND Pad	GND		GND	**Supply Ground.** Nominally 0.0 V. The GND pad found on the bottom of the 20-pin micro leaded package (see Figure 12) must be connected directly to supply ground.
4, 5	REFCLK+, REF-CLK–	I	See Table 2	**Differential Reference Clock.** The reference clock sets the initial operating frequency used by the onboard PLL for clock regeneration and multiplication. Additionally, the reference clock is used as a reference in generation of the LOL output and to bound the frequency drift of MULTOUT when CLKIN is not present.
6	LOL	O	LVTTL	**Loss of Lock.** This output is driven high when a divided version of the clock multiplier output deviates from the reference clock frequency by the amount specified in Table 4 on page 8.
9, 10	CLKIN+, CLKIN–	I	See Table 2	**Differential Clock Input.** Differential input clock from which MULTOUT is derived.

Table 11. Si5310 Pin Descriptions (Continued)

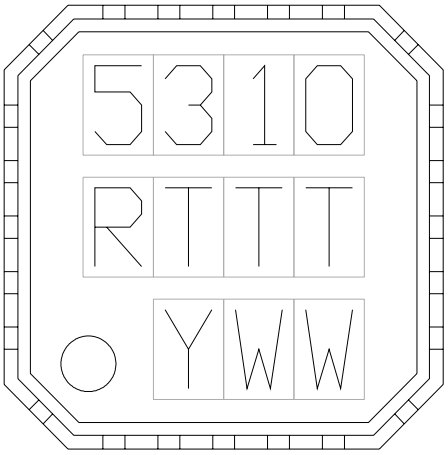
Pin #	Pin Name	I/O	Signal Level	Description
12, 13	CLKOUT–, CLKOUT+	O	CML	**Differential Clock Output.** The clock output signal is a regenerated version of the input clock signal present on CLKIN. It is phase aligned with MULTOUT and is updated on the rising edge of MULTOUT. **Note:** Connection of an improperly terminated transmission line to the CLKOUT output can cause reflections that may adversely affect the performance of the MULTOUT output. If the CLKOUT output is not used, these pins should be either tied to V_{DD} (recommended), left unconnected, or connected to a properly terminated transmission line.
15	PWRDN/CAL	I	LVTTL	**Power Down.** To shut down the high-speed outputs and reduce power consumption, hold this pin high. For normal operation, hold this pin low. **Calibration.** To initiate an internal self-calibration, force a high-to-low transition on this pin. (See "4.9. PLL Self-Calibration" on page 15.) **Note:** This input has a weak internal pulldown.
16, 17	MULTOUT–, MULTOUT+	O	CML	**Differential Multiplier Output.** The multiplier output is generated from the signal present on CLKIN. In the absence of CLKIN, the REFCLK is used to bound the frequency of MULTOUT according to Table 4 on page 8. **Note:** Connection of an improperly terminated transmission line to the MULTOUT output can cause reflections that may adversely affect the CLKOUT output. If the MULTOUT output is not used, these pins should be either tied to V_{DD} (recommended), left unconnected, or connected to a properly terminated transmission line.
19	MULTSEL	I	LVTTL	**Multiplier Rate Select.** This pin configures the onboard PLL-based clock multiplier for clock generation at one of two user selectable clock rates. **Note:** This input has a weak internal pulldown.
20	NC			**No Connect.**

6. Ordering Guide

Part Number	Package	Voltage	Pb-Free	Temperature
Si5310-X-GM	20-Lead QFN	2.5	Yes	–40 to 85 °C

1. “X” denotes product revision.
2. Add an “R” at the end of the device to denote tape and reel option; 2500 quantity per reel.
3. These devices use a NiPdAu pre-plated finish on the leads that is fully RoHS6 compliant while being fully compatible with both leaded and lead-free card assembly processes.

7. Top Mark



Part Number	Die Revision (R)	Assembly Date (YWW)
Si5310-C-GM	C	Y = Last digit of current year WW = Work week

8. Package Outline

Figure 12 illustrates the package details for the Si5310. Table 12 lists the values for the dimensions shown in the illustration.

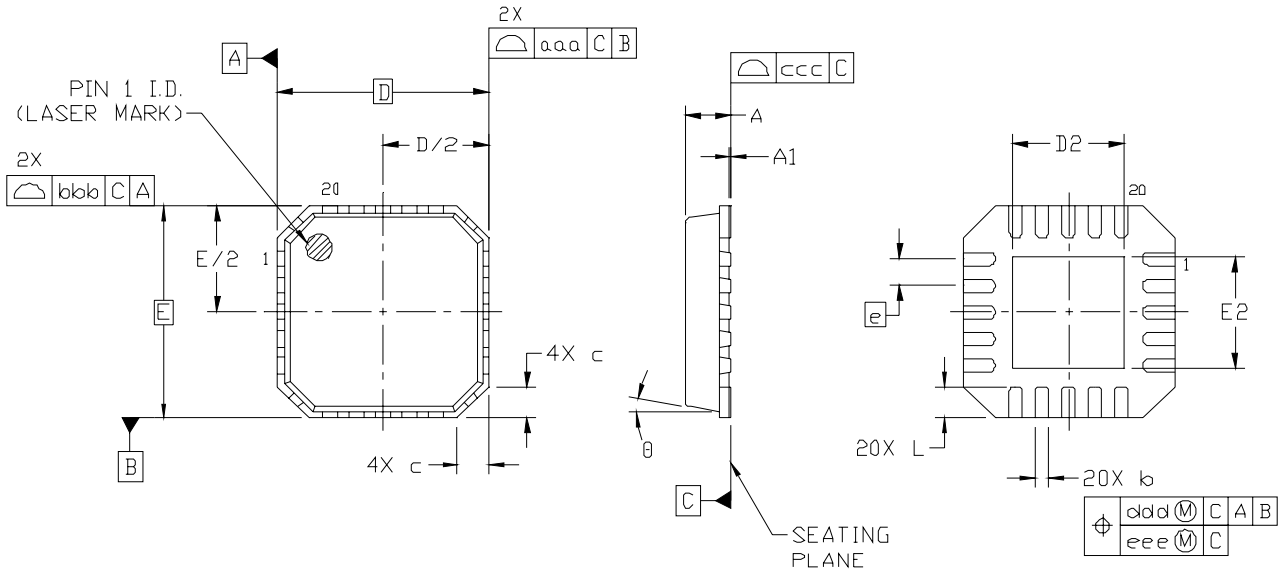


Figure 12. 20-pin Quad Flat No-Lead (QFN)

Table 12. Package Dimensions

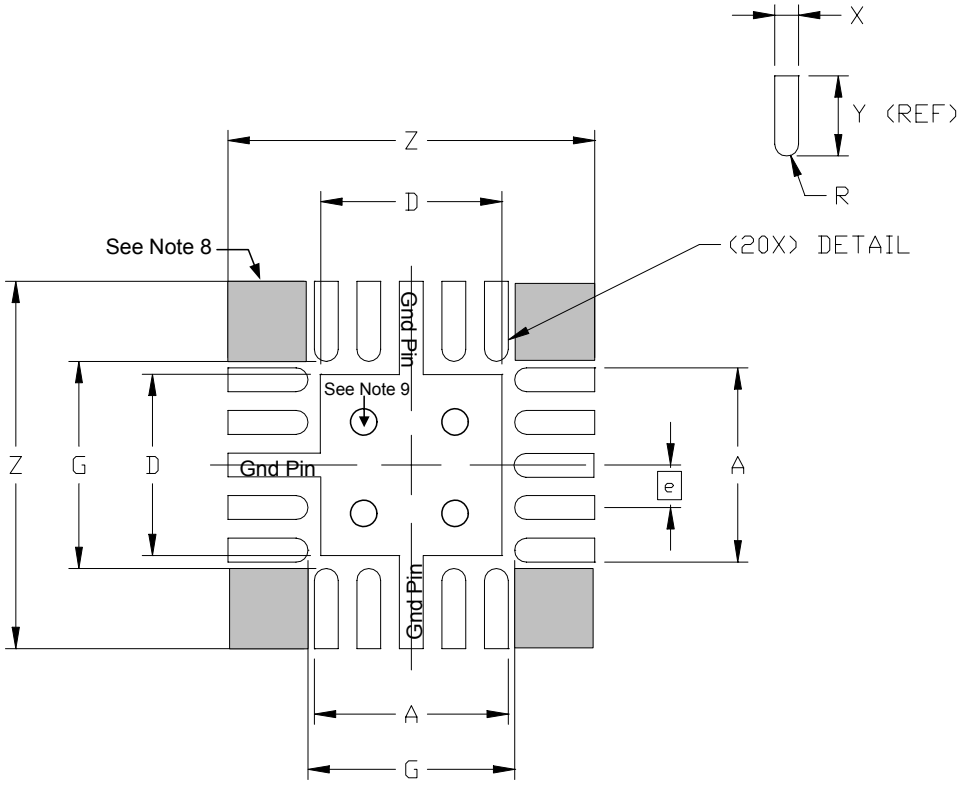
Symbol	Millimeters		
	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
c	—	—	0.60
D		4.00 BSC	
D2	1.95	2.10	2.25
e		0.50 BSC	
E		4.00 BSC	

Symbol	Millimeters		
	Min	Nom	Max
E2	1.95	2.10	2.25
L	0.50	0.60	0.70
θ	0°	—	12°
aaa		0.10	
bbb		0.10	
ccc		0.08	
ddd		0.10	
eee		0.05	

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MO-220, variation VGGD-1.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

9. 4x4 mm 20L QFN Recommended PCB Layout



Symbol	Parameter	Dimensions		
		Min	Nom	Max
A	Pad Row/Column Width/Length	2.23	2.25	2.28
D	Thermal Pad Width/Height	2.03	2.08	2.13
e	Pad Pitch	—	0.50 BSC	—
G	Pad Row/Column Separation	2.43	2.46	2.48
R	Pad Radius	—	0.12 REF	—
X	Pad Width	0.23	0.25	0.28
Y	Pad Length	—	0.94 REF	—
Z	Pad Row/Column Extents	4.26	4.28	4.31

Notes:

1. All dimensions listed are in millimeters (mm).
2. The perimeter pads are to be Non-Solder Mask Defined (NSMD). Solder mask openings should be designed to leave 60-75 mm separation between solder mask and pad metal, all the way around the pad.
3. The center thermal pad is to be Solder Mask Defined (SMD).
4. Thermal/Ground vias placed in the center pad should be no less than 0.2 mm (8 mil) diameter and tented from the top to prevent solder from flowing into the via hole.
5. The stencil aperture should match the pad size (1:1 ratio) for the perimeter pads. A 3x3 array of 0.5 mm square stencil openings, on a 0.65 mm pitch, should be used for the center thermal pad.
6. A stencil thickness of 5 mil is recommended. The stencil should be laser cut and electropolished, with trapezoidal walls to facilitate paste release.
7. A “No-Clean”, Type 3 solder paste should be used for assembly. Nitrogen purge during reflow is recommended.
8. Do not place any signal or power plane vias in these “keep out” regions.
9. Suggest four 0.38 mm (15 mil) vias to the ground plane.

Document Change List

Revision 1.0 to Revision 1.1

- Added "7. Top Mark" on page 21.
- Updated "8. Package Outline" on page 22.
- Added "9. 4x4 mm 20L QFN Recommended PCB Layout" on page 23.

Revision 1.1 to Revision 1.2

- Added Pb-free packaging option in "6. Ordering Guide" on page 21.

Revision 1.2 to Revision 1.3

- Added "7. Top Mark" on page 21.
- Updated "6. Ordering Guide" on page 21.
- Updated "8. Package Outline" on page 22.

NOTES:

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