

3.3V Low Skew 1-to-4 Crystal/LVCMOS to LVDS Fanout Buffer

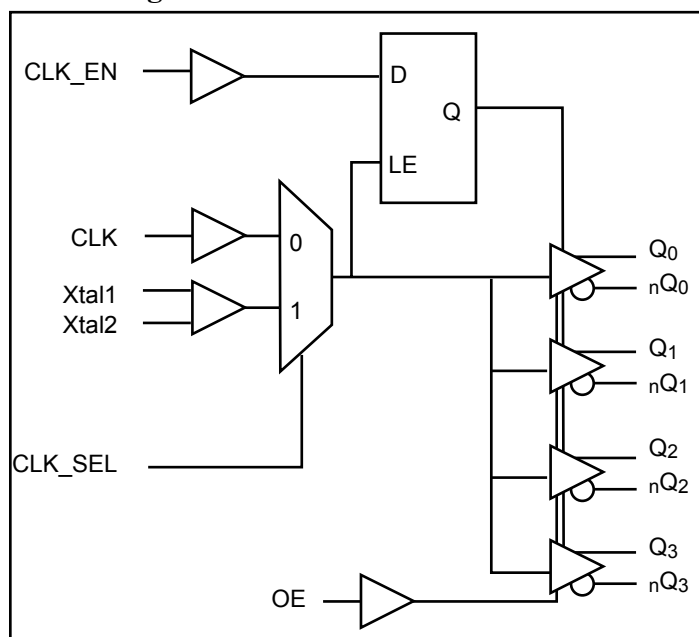
Features

- Maximum operation frequency: 650 MHz
- 4 pair of differential LVDS outputs
- Selectable CLK and crystal inputs
- CLK accepts LVCMOS, LVTTL input level
- Output Skew: 40ps (maximum)
- Part-to-part skew: 300ps (maximum)
- Propagation delay: 2.2ns (maximum)
- 3.3V power supply
- Operating Temperature: -40°C to 85°C
- Packaging (Pb-free & Green):
- 20-pin TSSOP (L)

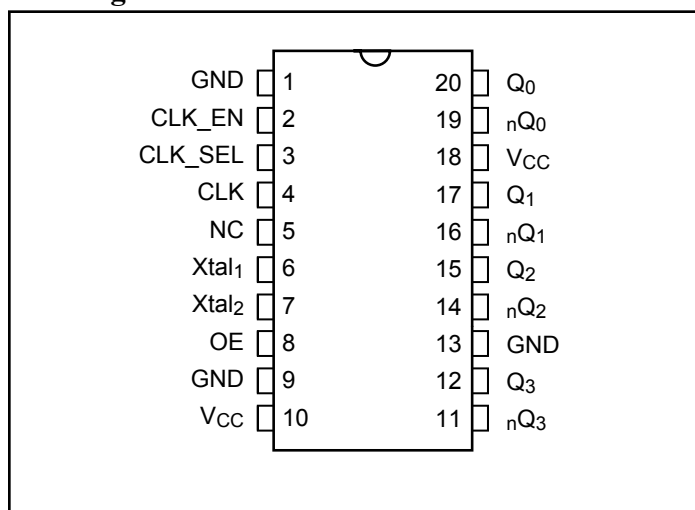
Description

The PI6C48545-11 is a high-performance low-skew LVDS fanout buffer. PI6C48545-11 features selectable single-ended clock or crystal inputs and translates to four LVDS outputs. The CLK input accepts LVCMOS or LVTTL signals. The outputs are synchronized with input clock during asynchronous assertion /deassertion of CLK_EN pin. PI6C48545-11 is ideal for crystal or LVCMOS/LVTTL to LVDS translation. Typical clock translation and distribution applications are Data Communications and Telecommunications.

Block Diagram



Pin Diagram



Pin Description

Name	Pin #	Type	Description
GND	1, 9, 13	P	Connect to Ground
CLK_EN	2	I_PU	Synchronizing clock enable. When high, clock outputs follow clock input. When low, Q _x outputs are forced low, _n Q _x outputs are forced high. LVCMOS/LVTTL level with 80KΩ pull up.
CLK_SEL	3	I_PD	Clock select input. When high, selects CLK ₁ input. When low, selects CLK ₀ input. LVCMOS/LVTTL level with 80kΩ pull down.
CLK	4	I_PD	LVCMOS / LVTTL clock input
Xtal1, Xtal2	6, 7		Crystal input and output
NC	5		No internal connection.
OE	8	I_PU	Output Enable. Controls outputs Q ₀ , _n Q ₀ through Q ₃ , _n Q ₃ .
V _{CC}	10, 13, 18	P	Connect to 3.3V
Q ₃ , _n Q ₃	11, 12	O	Differential output pair, LVDS interface level.
Q ₂ , _n Q ₂	14, 15	O	Differential output pair, LVDS interface level.
Q ₁ , _n Q ₁	16, 17	O	Differential output pair, LVDS interface level.
Q ₀ , _n Q ₀	19, 20	O	Differential output pair, LVDS interface level.

Notes:

1. I = Input, O = Output, P = Power supply connection, I_PD = Input with pull down, I_PU = Input with pull up

Pin Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
C _{IN}	Input Capacitance			6		pF
R _{pullup}	Input Pullup Resistance			80		KΩ
R _{pulldown}	Input Pulldown Resistance			80		

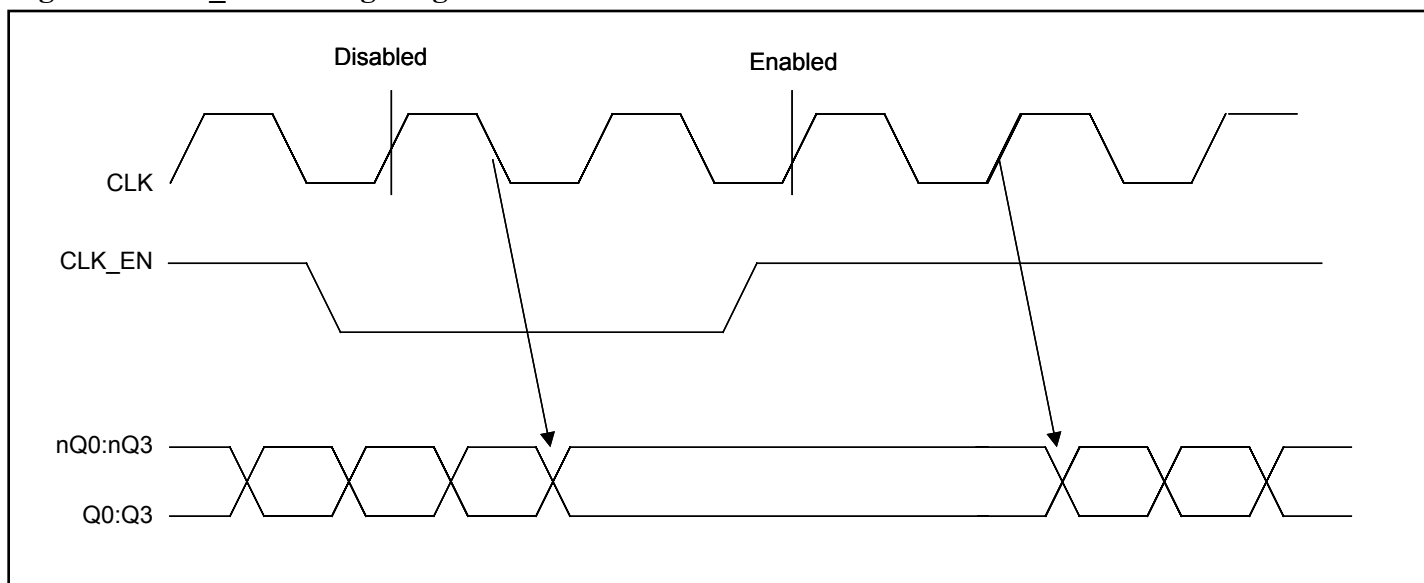
Control Input Function Table

Inputs				Outputs	
OE	CLK_EN	CLK_SEL	Selected Source	Q ₀ :Q ₃	_n Q ₀ : _n Q ₃
1	0	0	CLK	Diabld: Low	Diabld: High
1	0	1	Xtal1, Xtal2	Disabled: Low	Disabled: High
1	1	0	CLK	Enabled	Enabled
1	1	1	Xtal1, Xtal2	Enabled	Enabled
0	x	x		HiZ	HiZ

Notes:

1. After CLK_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock edge as show below.

Figure 1. CLK_EN Timing Diagram



Clock Input Function Table

Inputs	Outputs	
CLK	Q ₀ :Q ₃	nQ ₀ :nQ ₃
0	LOW	HIGH
1	HIGH	LOW

Absolute Maximum Ratings

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V _{CC}	Supply voltage	Referenced to GND			4.6	V
V _{IN}	Input voltage	Referenced to GND	-0.5		V _{CC} +0.5V	
V _{OUT}	Output voltage	Referenced to GND	-0.5		V _{CC} +0.5V	
T _{STG}	Storage temperature		-65		150	°C

Notes:

- Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only and correct functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Operating Conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V _{CC}	Power Supply Voltage		3.135	3.3	3.465	V
T _A	Ambient Temperature		-40		85	°C
I _{CC}	Power Supply Current				60	mA

LVCMOS/LVTTL DC Characteristics ($T_A = -40^{\circ}\text{C}$ to 85°C , $V_{CC} = 3.135\text{V}$ to 3.465V unless otherwise stated below.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units	
V_{IH}	Input High Voltage		2		$V_{CC}+0.3$	V	
V_{IL}	Input Low Voltage		-0.3		0.8		
I_{IH}	Input High Current	CLK, CLK_SEL	$V_{IN} = V_{CC} = 3.465\text{V}$			150	μA
		CLK_EN, OE	$V_{IN} = V_{CC} = 3.465\text{V}$			5	
I_{IL}	Input Low Current	CLK, CLK_SEL	$V_{IN} = 0\text{V}, V_{CC} = 3.465\text{V}$	-5			
		CLK_EN, OE	$V_{IN} = 0\text{V}, V_{CC} = 3.465\text{V}$	-150			

LVDS DC Characteristics ($T_A = -40^{\circ}\text{C}$ to 85°C , $V_{CC} = 3.135\text{V}$ to 3.465V unless otherwise stated below.)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{OD}	Differential Output Voltage		200	280	360	mV
ΔV_{OD}	V_{OD} Magnitude Change			0	40	
V_{OS}	Offset Voltage		1.125	1.25	1.375	V
ΔV_{OS}	V_{OS} Magnitude Change			5	25	mV
I_{OZ}	High Impedance Leakage Current		-10		+10	μA
I_{OFF}	Power OFF Leakage		-20	± 1	+20	
I_{OSD}	Differential Output Short Circuit Current			-3.5	-5	mA
I_{OS}	Output Short Circuit Current			-3.5	-5	
V_{OH}	Output Voltage High			1.34	1.6	V
V_{OL}	Output Voltage Low		0.9	1.06		

Crystal Characteristics

Parameter	Min.	Typ.	Max.	Units
Mode of Oscillation	Fundamental			
Frequency Range	14		25	MHz
Equivalent Series Resistance (ESR)			70	Ω
Shunt Capacitance			7	pF

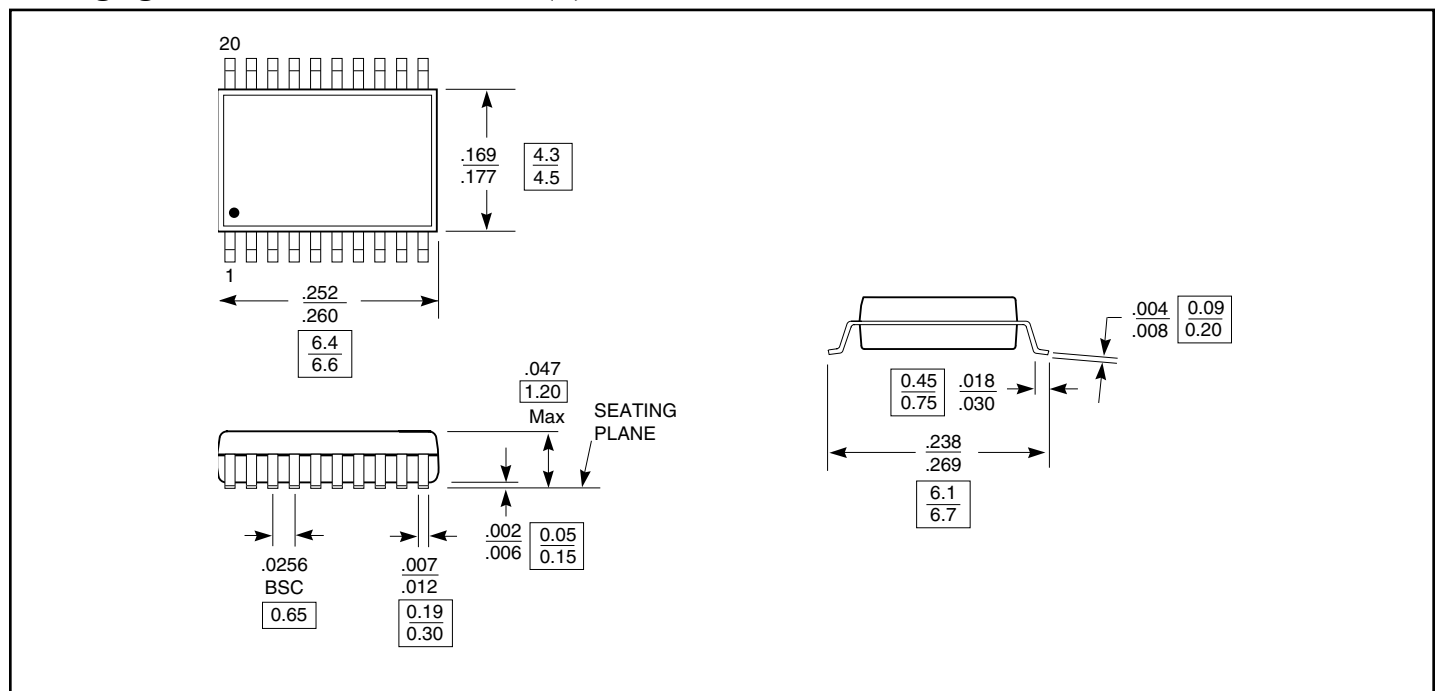
AC Characteristics ($T_A = -40^{\circ}\text{C}$ to 85°C , $V_{CC} = 3.135\text{V}$ to 3.465V)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
f_{\max}	Output Frequency				650	MHz
t_{pd}	Propagation Delay ⁽¹⁾		0.8		2.2	ns
$T_{sk(o)}$	Output-to-output Skew ⁽²⁾				40	ps
$T_{sk(pp)}$	Part-to-part Skew ⁽³⁾				150	
t_r/t_f	Output Rise/Fall time	20% - 80%	100		300	
odc	Output duty cycle		48		52	%
Osc	Crystal Tolerance				1000	ppm

Notes:

1. Measured from the $V_{CC}/2$ of the input to the differential output crossing point
2. Defined as skew between outputs at the same supply voltage and with equal load condition. Measured at the outputs differential crossing point.
3. Defined as skew between outputs on different parts operating at the same supply voltage and with equal load condition. Measured at the outputs differential crossing point.
4. All parameters are measured at 500MHz unless noted otherwise

Packaging Mechanical: 20-Pin TSSOP (L)



Ordering Information

Ordering Code	Package Code	Package Description
PI6C48545-11LE	L	Pb-free & Green 20-pin 173-mil wide TSSOP

Notes:

1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
2. Number of Transistors = TBD