SPL505YC256BT/ SPL505YC256BS

Clock Generator for Intel® Bearlake Chipset

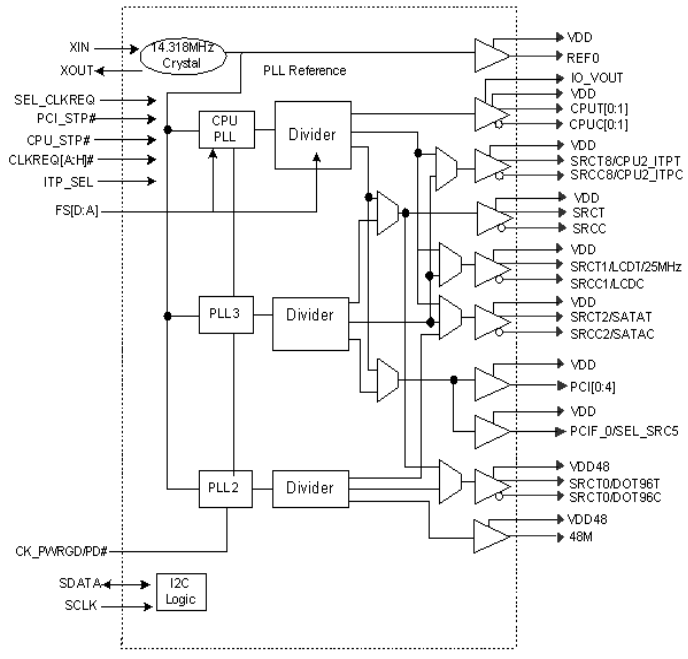
Features

- Compliant to Intel® CK505
- Selectable CPU frequencies
- Differential CPU clock pairs
- 100 MHz Differential SRC clocks
- 100 MHz Differential LCD clock
- 96 MHz Differential Dot clock
- 48 MHz USB clocks
- 33 MHz PCI clock
- 25 MHz WOL or PATA clock
- 27 MHz non-spread Video Clock
- Buffered Reference Clock 14.318 MHz
- Low-voltage frequency select input
- I^2C support with readback capabilities
- Triangular Spread Spectrum profile for maximum electromagnetic interference (EMI) reduction
- 3.3V Power supply/0.7V for Diff IOs
- 56-pin TSSOP and SSOP package

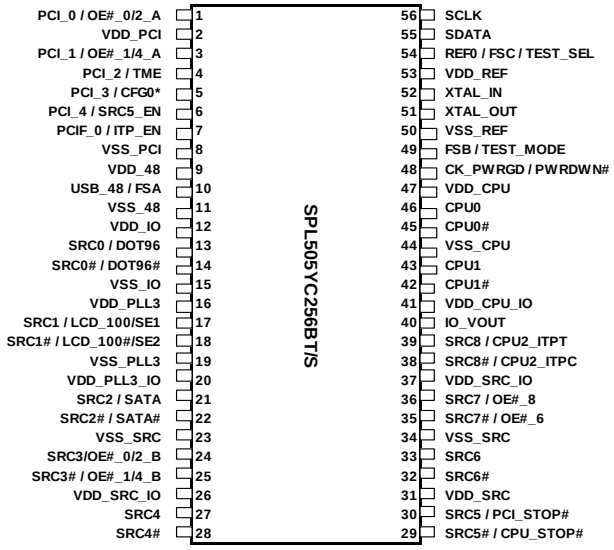
Table 1. Output Configuration Table

CPU	SRC	PCI	REF	DOT96	USB_48M	LCD
x2/x3	x8/12	x6	x 1	x 1	x 1	x1

Block Diagram



Pin Configuration



* Internal Pull-Down

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Pin Definitions

Pin No.	Name	Type	Description
1	PCI_0/OE#_0/2_A	I/O, SE	33 MHz clock/3.3V OE# Input mappable via I2C to control either SRC 0 or SRC 2. Default PCI0
2	VDD_PCI	PWR	3.3V Power supply for PCI PLL.
3	PCI_1/OE#_1/4_A	I/O, SE	33 MHz clock/3.3V OE# Input mappable via I2C to control either SRC 1 or SRC 4. Default PCI1.
4	PCI_2/TME	I/O, SE	3.3V tolerance input for overclocking enable pin 33 MHz clock. *Refer to DC Electrical Specifications table for Vil_FS and Vih_FS specifications.*
5	PCI_3/CFG0	I/O, SE, PD	3.3V tolerant input for CPU frequency selection/33 MHz clock. *Refer to DC Electrical Specifications table for Vil_PCI3/CFG0 and Vih_PCI3/CFG0 specifications*.
6	PCI_4/SRC5_SEL	I/O, SE	3.3V tolerant input to enable SRC5/33 MHz clock output. (sampled on the CK_PWRGD assertion) 1 = SRC5, 0 = CPU_STOP#
7	PCIF_0/ITP_EN	I/O, SE	3.3V LVTTL input to enable SRC8 or CPU2_ITP/33 MHz clock output. (sampled on the CK_PWRGD assertion) 1 = CPU2_ITP, 0 = SRC8
8	VSS_PCI	GND	Ground for outputs.
9	VDD_48	PWR	3.3V Power supply for outputs and PLL.
10	USB_48/FSA	I/O	3.3V tolerant input for CPU frequency selection/fixed 48 MHz clock output. *Refer to DC Electrical Specifications table for Vil_FS and Vih_FS specifications.*
11	VSS_48	GND	Ground for outputs.
12	VDD_IO	PWR	0.7V Power supply for outputs.
13	SRC0/DOT96	O, DIF	100 MHz Differential serial reference clocks/Fixed 96 MHz clock output. Selected via I2C default is SRC0.
14	SRC0#/DOT96#	O, DIF	100 MHz Differential serial reference clocks/Fixed 96 MHz clock output. Selected via I2C default is SRC0.
15	VSS_IO	GND	Ground for PLL2.
16	VDD_PLL3	PWR	3.3V Power supply for PLL3
17	SRC1/LCD_100/SE1	O, DIF, SE	100 MHz Differential serial reference clocks/100 MHz LCD video clock/SE1 and SE2 clocks. Default SRC1
18	SRC1#/LCD_100#/SE2	O, DIF, SE	100 MHz Differential serial reference clocks/100 MHz LCD video clock/SE1 and SE2 clocks. Default SRC1
19	VSS_PLL3	GND	Ground for PLL3.
20	VDD_PLL3_IO	PWR	0.7V Power supply for PLL3 outputs.
21	SRC2/SATA	O, DIF	100 MHz Differential serial reference clocks / 100MHz SATA clock
22	SRC2#/SATA#	O, DIF	100 MHz Differential serial reference clocks / 100MHz SATA clock
23	VSS_SRC	GND	Ground for outputs.
24	SRC3/OE#_0/2_B	I/O, Dif	100-MHz Differential serial reference clocks / 3.3V OE#_0/2_B, input, mappable via I2C to control either SRC 0 or SRC 2
25	SRC3#/OE#_1/4_B	I/O, Dif	100-MHz Differential serial reference clocks / 3.3V OE#_1/4_B input, mappable via I2C to control either SRC 1 or SRC 4. Default SRC3
26	VDD_SRC_IO	PWR	0.7V power supply for SRC outputs.
27	SRC4	O, DIF	100 MHz Differential serial reference clocks.
28	SRC4#	O, DIF	100 MHz Differential serial reference clocks.
29	SRC5#/PCI_STOP#	I/O, Dif	3.3V tolerant input for stopping PCI and SRC outputs /100 MHz Differential serial reference clocks.

Pin Definitions (continued)

Pin No.	Name	Type	Description
30	SRC5/CPU_STOP#	I/O, Dif	3.3V tolerant input for stopping CPU outputs/100 MHz Differential serial reference clocks.
31	VDD_SRC	PWR	3.3V Power supply for SRC PLL.
32	SRC6#	O, DIF	100 MHz Differential serial reference clocks.
33	SRC6	O, DIF	100 MHz Differential serial reference clocks.
34	VSS_SRC	GND	Ground for outputs.
35	SRC7#/OE#_6	I/O, Dif	100 MHz Differential serial reference clocks/3.3V OE#6 Input controlling SRC6. Default SRC7.
36	SRC7/OE#_8	I/O, Dif	100 MHz Differential serial reference clocks/3.3V OE#8 Input controlling SRC8. Default SRC7.
37	VDD_SRC_IO	PWR	0.7V power supply for SRC outputs.
38	SRC8#/CPUT2_ITP#	O, DIF	Selectable differential CPU or SRC clock output. ITP_EN = 0 @ CK_PWRGD assertion = SRC8 ITP_EN = 1 @ CK_PWRGD assertion = CPU2 *Note: CPU2 is an iAMT clock in iAMT mode depending on the configuration set in Byte 11 Bit3:2.*
39	SRC8/CPUC2_ITP	O, DIF	Selectable differential CPU or SRC clock output. ITP_EN = 0 @ CK_PWRGD assertion = SRC8 ITP_EN = 1 @ CK_PWRGD assertion = CPU2 *Note: CPU2 is an iAMT clock in iAMT mode depending on the configuration set in Byte 11 Bit3:2.*
40	IO_VOUT	O	Integrated Linear Regulator Control.
41	VDD_CPU_IO	PWR	0.7V Power supply for CPU outputs.
42	CPU1#	O, DIF	Differential CPU clock outputs. *Note: CPU1 is an iAMT clock in iAMT mode depending on the configuration set in Byte 11 Bit3:2.*
43	CPU1	O, DIF	Differential CPU clock outputs. *Note: CPU1 is an iAMT clock in iAMT mode depending on the configuration set in Byte 11 Bit3:2.*
44	VSS_CPU	GND	Ground for outputs.
45	CPU0#	O, DIF	Differential CPU clock outputs.
46	CPU0	O, DIF	Differential CPU clock outputs.
47	VDD_CPU	PWR	3.3V Power supply for CPU PLL.
48	CK_PWRGD/PWRDWN#	I	3.3V LVTTL input. This pin is a level sensitive strobe used to latch the FS_A, FS_B, FS_C, FS_D, SRC5_SEL, and ITP_EN. After CK_PWRGD (active HIGH) assertion, this pin becomes a real-time input for asserting power down (active LOW).
49	FSB/TEST_MODE	I	3.3V tolerant input for CPU frequency selection. Selects Ref/N or Tri-state when in test mode 0 = Tri-state, 1 = Ref/N. *Refer to DC Electrical Specifications table for Vil_FS and Vih_FS specifications.*
50	VSS_REF	GND	Ground for outputs.
51	XOUT	O, SE	14.318 MHz Crystal output.
52	XIN	I	14.318 MHz Crystal input.
53	VDD_REF	PWR	3.3V Power supply for outputs and also maintains SMBUS registers during power-down.
54	REF0/FSC/TEST_SEL	I/O	3.3V tolerant input for CPU frequency selection/fixed 14.318 clock output. Selects test mode if pulled to V_{IHFS_C} when CK_PWRGD is asserted HIGH. *Refer to DC Electrical Specifications table for* V_{ILFS_C}, V_{IMFS_C}, V_{IHFS_C} *specifications.*
55	SMB_DATA	I/O	SMBus compatible SDATA.
56	SMB_CLK	I	SMBus compatible SCLOCK.

Frequency Select Pin (FSA, FSB, and FSC)

To achieve host clock frequency selection, apply the appropriate logic levels to FS_A, FS_B, and FS_C, inputs before CK_PWRGD assertion (as seen by the clock synthesizer). When CK_PWRGD is sampled HIGH by the clock chip (indicating processor CK_PWRGD voltage is stable), the clock chip samples the FS_A, FS_B, and FS_C, input values. For all logic levels of FS_A, FS_B, and FS_C CK_PWRGDemploys a one-shot functionality, in that once a valid HIGH on CK_PWRGD has been sampled, all further CK_PWRGD FS_A, FS_B, and FS_C, transitions will be ignored, except in test mode.

Frequency Select Pin (FSA, FSB, and FSC)

Input Conditions			Output Frequency						
FSC	FSB	FSA	CPU (MHz)	SRC (MHz)	SATA (MHz)	DOT96 (MHz)	USB (MHz)	PCI (MHz)	REF (MHz)
FSEL_2	FSEL_1	FSEL_0							
1	0	1	100	100	100	96	48	33.3	14.318
0	0	1	133						
0	1	1	166						
0	1	0	200						
0	0	0	266						
1	0	0	333						
1	1	0	400						
1	1	1	200						

Serial Data Interface

To enhance the flexibility and function of the clock synthesizer, a two-signal serial interface is provided. Through the Serial Data Interface, various device functions, such as individual clock output buffers, can be individually enabled or disabled. The registers associated with the Serial Data Interface initialize to their default setting upon power-up, and therefore use of this interface is optional. Clock device register changes are normally made upon system initialization, if any are required. The interface cannot be used during system operation for power management functions.

Data Protocol

The clock driver serial protocol accepts byte write, byte read, block write, and block read operations from the controller. For block write/read operation, the bytes must be accessed in sequential order from lowest to highest byte (most significant bit first) with the ability to stop after any complete byte has been transferred. For byte write and byte read operations, the system controller can access individually indexed bytes. The offset of the indexed byte is encoded in the command code, as described in *Table 2*.

The block write and block read protocol is outlined in *Table 3* while *Table 4* outlines the corresponding byte write and byte read protocol. The slave receiver address is 11010010 (D2h)
.

Table 2. Command Code Definition

Bit	Description
7	0 = Block read or block write operation, 1 = Byte read or byte write operation
(6:0)	Byte offset for byte read or byte write operation. For block read or block write operations, these bits should be '0000000'

Table 3. Block Read and Block Write Protocol

Block Write Protocol		Block Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
8:2	Slave address–7 bits	8:2	Slave address–7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
18:11	Command Code–8 bits	18:11	Command Code–8 bits
19	Acknowledge from slave	19	Acknowledge from slave
27:20	Byte Count–8 bits (Skip this step if I^2C_EN bit set)	20	Repeat start
28	Acknowledge from slave	27:21	Slave address–7 bits
36:29	Data byte 1–8 bits	28	Read = 1
37	Acknowledge from slave	29	Acknowledge from slave
45:38	Data byte 2–8 bits	37:30	Byte Count from slave–8 bits
46	Acknowledge from slave	38	Acknowledge
....	Data Byte/Slave Acknowledges	46:39	Data byte 1 from slave–8 bits
....	Data Byte N–8 bits	47	Acknowledge
....	Acknowledge from slave	55:48	Data byte 2 from slave–8 bits
....	Stop	56	Acknowledge
		....	Data bytes from slave/Acknowledge
		....	Data Byte N from slave–8 bits
		....	NOT Acknowledge
		....	Stop

Table 4. Byte Read and Byte Write Protocol

Byte Write Protocol		Byte Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
8:2	Slave address–7 bits	8:2	Slave address–7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
18:11	Command Code–8 bits	18:11	Command Code–8 bits
19	Acknowledge from slave	19	Acknowledge from slave
27:20	Data byte–8 bits	20	Repeated start
28	Acknowledge from slave	27:21	Slave address–7 bits
29	Stop	28	Read
		29	Acknowledge from slave
		37:30	Data from slave–8 bits
		38	NOT Acknowledge
		39	Stop

Control Registers

Byte 0: Control Register 0

Bit	@Pup	Name	Description

Byte 0: Control Register 0

7	HW	FS_C	CPU Frequency Select Bit, set by HW
6	HW	FS_B	CPU Frequency Select Bit, set by HW
5	HW	FS_A	CPU Frequency Select Bit, set by HW
4	0	iAMT_EN	Set via SMBus or by combination of PWRDWN, CPU_STP, and PCI_STP 0 = Legacy Mode, 1 = iAMT Enabled, Sticky 1
3	0	RESERVED	RESERVED
2	0	SRC_MAIN_SEL	Select source for SRC clock, 0 = SRC_MAIN = PLL1, PLL3_CFB Table applies 1 = SRC_MAIN = PLL3, PLL3_CFB Table does not apply
1	0	SATA_SEL	Select source of SATA clock 0 = SATA SRC_MAIN, 1= SATA PLL2
0	1	PD_Restore	Save Config. In powerdown 0 = Config. Cleared, 1 = Config. Saved

Byte 1: Control Register 1

Bit	@Pup	Name	Description
7	0	SRC0_SEL	Select for SRC0 or DOT96, 0 = SRC0, 1 = DOT96
6	0	PLL1_SS_DC	Select for down or center SS, 0 = Down spread, 1 = Center spread
5	0	PLL3_SS_DC	Select for down or center SS, 0 = Down spread, 1 = Center spread
4	0	PLL3_CFB3	Bit 4:1 only apply when SRC_SEL=0 0000 = PLL3 Disable Default PLL3 OFF, SRC1 = SRC_MAIN 0001 = 100 MHz 0.5% SSC Stby PLL3 ON, SRC1 = SRC_MAIN 0010 = 100 MHz 0.5% SSC Only SRC1 sourced from PLL3 0011 = 100 MHz 1.0% SSC Only SRC1 sourced from PLL3 0100 = 100 MHz 1.5% SSC Only SRC1 sourced from PLL3 0101 = 100 MHz 2.0% SSC Only SRC1 sourced from PLL3 0110 = RESERVED 0111 = RESERVED 1000 = RESERVED 1001 = RESERVED 1010 = RESERVED 1011 = 27MHz_NSS on SE1 and SE2 1100 = 25MHz on SE1 and SE2 1101 = 25MHz on SE1 and SE2 Disabled *(set whenPCI3/CFB0 is set high to config to HW mode 3)* 1110 = RESERVED 1111 = RESERVED *Note: SE clocks required to be enabled through Byte 8 Bit1:0*
3	0	PLL3_CFB2	
2	0	PLL3_CFB1	
1	1	PLL3_CFB0	
0	1	PCI_SEL	Select PCI Clock source from PLL1 or SRC_MAIN 0 = PLL1, 1 = SRC_MAIN

Byte 2: Control Register 2

Bit	@Pup	Name	Description
7	1	REF_OE	Output enable for REF 0 = Output Disabled, 1 = Output Enabled
6	1	USB_OE	Output enable for USB 0 = Output Disabled, 1 = Output Enabled
5	1	PCIF0_OE	Output enable for PCIF0 0 = Output Disabled, 1 = Output Enabled
4	1	PCI4_OE	Output enable for PCI4, 0 = Output Disabled, 1 = Output Enabled
3	1	PCI3_OE	Output enable for PCI3, 0 = Output Disabled, 1 = Output Enabled

Byte 2: Control Register 2 (continued)

Bit	@Pup	Name	Description
2	1	PCI2_OE	Output enable for PCI2, 0 = Output Disabled, 1 = Output Enabled
1	1	PCI1_OE	Output enable for PCI1, 0 = Output Disabled, 1 = Output Enabled
0	1	PCI0_OE	Output enable for PCI0, 0 = Output Disabled, 1 = Output Enabled

Byte 3: Control Register 3

Bit	@Pup	Name	Description
7	1	SRC11_OE	Output enable for SRC11, 0 = Output Disabled, 1 = Output Enabled
6	1	SRC10_OE	Output enable for SRC10, 0 = Output Disabled, 1 = Output Enabled
5	1	SRC9_OE	Output enable for SRC9, 0 = Output Disabled, 1 = Output Enabled
4	1	SRC8/ITP_OE	Output enable for SRC8 or ITP, 0 = Output Disabled, 1 = Output Enabled
3	1	SRC7_OE	Output enable for SRC7, 0 = Output Disabled, 1 = Output Enabled
2	1	SRC6_OE	Output enable for SRC6, 0 = Output Disabled, 1 = Output Enabled
1	1	SRC5_OE	Output enable for SRC5, 0 = Output Disabled, 1 = Output Enabled
0	1	SRC4_OE	Output enable for SRC4, 0 = Output Disabled, 1 = Output Enabled

Byte 4: Control Register 4

Bit	@Pup	Name	Description
7	1	SRC3_OE	Output enable for SRC3, 0 = Output Disabled, 1 = Output Enabled
6	1	SRC2/SATA_OE	Output enable for SATA/SRC2, 0 = Output Disabled, 1 = Output Enabled
5	1	SRC1_OE	Output enable for SRC, 0 = Output Disabled, 1 = Output Enabled
4	1	SRC0/DOT96_OE	Output enable for SRC0/DOT96 0 = Output Disabled, 1 = Output Enabled
3	1	CPU1_OE	Output enable for CPU1, 0 = Output Disabled, 1 = Output Enabled
2	1	CPU0_OE	Output enable for CPU0, 0 = Output Disabled, 1 = Output Enabled
1	1	PLL1_SS_EN	Enable PLL1's spread modulation, 0 = Spread Disabled 1 = Spread Enabled
0	1	PLL3_SS_EN	Enable PLL3's spread modulation 0 = Spread Disabled, 1 = Spread Enabled

Byte 5: Control Register 5

Bit	@Pup	Name	Description
7	0	OE#_0/2_EN_A	Enable OE#_0/2 (clk req) 0 = Disabled OE#_0/2, 1 = Enabled OE#_0/2,
6	0	OE#_0/2_SEL_A	Set OE#_0/2 → SRC0 or SRC2 0 = OE#_0/2→SRC0, 1 = OE#_0/2→SRC2
5	0	OE#_1/4_EN_A	Enable OE#_1/4 (clk req) 0 = Disabled OE#_1/4, 1 = Enabled OE#_1/4,
4	0	OE#_1/4_SEL_A	Set OE#_1/4 → SRC1 or SRC4 0 = OE#_1/4→SRC1, 1 = OE#_1/4→SRC4
3	0	OE#_0/2_EN_B	Enable OE#_0/2 (clk req) 0 = Disabled OE#_0/2 1 = Enabled OE#_0/2
2	0	OE#_0/2_SEL_B	Set OE#_0/2 → SRC0 or SRC2 0 = OE#_0/2→SRC0, 1 = OE#_0/2→SRC2
1	0	OE#_1/4_EN_B	Enable OE#_1/4 (clk req) 0 = Disabled OE#_1/4, 1 = Enabled OE#_1/4,
0	0	OE#_1/4_SEL_B	Set OE#_1/4 → SRC1 or SRC4 0 = OE#_1/4→SRC1, 1 = OE#_1/4→SRC4

Byte 6: Control Register 6

Bit	@Pup	Name	Description
7	0	OE#_6_EN	Enable OE#_6 (clk req) → SRC6
6	0	OE#_8_EN	Enable OE#_8 (clk req) → SRC8
5	0	OE#_9_EN	Enable OE#_9 (clk req) → SRC9
4	0	OE#_10_EN	Enable OE#_10 (clk req) → SRC10
3	0	RESERVED	RESERVED
2	0	RESERVED	RESERVED
1	0	LCD_100_STP_CTRL	Allows control of LCD_100 with assertion of PCI_STOP# 0 = Free runningLCD_100, 1 = Stopped with PCI_STOP#
0	0	SRC_STP_CTRL	Allows control of SRC with assertion of PCI_STOP# 0 = Free running SRC 1 = Stopped with PCI_STOP#

Byte 7: Vendor ID

Bit	@Pup	Name	Description
7	0	Rev Code Bit 3	Revision Code Bit 3
6	0	Rev Code Bit 2	Revision Code Bit 2
5	0	Rev Code Bit 1	Revision Code Bit 1
4	1	Rev Code Bit 0	Revision Code Bit 0
3	1	Vendor ID bit 3	Vendor ID Bit 3
2	0	Vendor ID bit 2	Vendor ID Bit 2
1	0	Vendor ID bit 1	Vendor ID Bit 1
0	0	Vendor ID bit 0	Vendor ID Bit 0

Byte 8: Control Register 8

Bit	@Pup	Name	Description
7	0	Device_ID3	0000 = CK505 Yellow Cover Device, 56-pin TSSOP 0001 = CK505 Yellow Cover Device, 64-pin TSSOP 0010 = CK505 Yellow Cover Device, 48-pin QFN (reserved) 0011 = CK505 Yellow Cover Device, 56-pin QFN (reserved) 0100 = CK505 Yellow Cover Device, 64-pin QFN (reserved) 0101 = CK505 Yellow Cover Device, 72-pin QFN (reserved) 0110 = CK505 Yellow Cover Device, 48-pin SSOP (reserved) 0111 = CK505 Yellow Cover Device, 56-pin SSOP (reserved) 1000 = Reserved 1001 = Reserved 1010 = Reserved 1011 = Reserved 1100 = Reserved 1101 = Reserved 1110 = Reserved 1111 = Reserved
7	0	Device_ID2	
5	0	Device_ID1	
4	0	Device_ID0	
3	0	RESERVED	RESERVED
2	0	RESERVED	RESERVED
1	0	SE1_OE	SE1 Output enable 0 = Output Disabled, 1 = Output Enabled
0	0	SE2_OE	SE2 Output enable 0 = Output Disabled, 1 = Output Enabled

Byte 9 Control Register 9

Bit	@Pup	Name	Description

Byte 9 Control Register 9

7	0	PCIF0_STP_CTRL	Allows control of PCIF0 with assertion of PCI_STOP# 0 = Free running PCIF, 1 = Stopped with PCI_STOP#
6	HW_Pin	TME_STRAP	Trusted mode enable strap status, 0 = normal, 1 = no overclocking
5	1	REF_DSC1	REF drive strength control, *See Byte 18 for more setting* 0 = Low, 1 = High
4	0	TEST_MODE_SEL	Mode select either REF/N or tri-state 0 = All output tri-state, 1 = All output REF/N
3	0	TEST_MODE_ENTRY	Allow entry into test mode 0=Normal operation, 1=Enter test mode
2	1	IO_VOUT2	IO_VOUT[2,1,0] 000 = 0.3V 001 = 0.4V 010 = 0.5V 011 = 0.6V 100 = 0.7V 101 = 0.8V, *Default* 110 = 0.9V 111 = 1.0V
1	0	IO_VOUT1	
0	1	IO_VOUT0	

Byte 10 Control Register 10

Bit	@Pup	Name	Description
7	HW	SRC5_EN_STRAP	Read only bit for SRC5_EN_STRAP 0 = CPU/PCI_STOP enabled, 1 = SRC5 pair enabled
6	1	PLL3_EN	PLL3 Enabled 0 = PLL3 disabled, 1 = PLL3 enabled
5	1	PLL2_EN	PLL2 Enabled 0 = PLL2 disabled, 1 = PLL2 enabled
4	1	SRC_DIV_EN	SRC Divider Enabled 0 = SRC Divider disabled, 1 = SRC Divider enabled
3	1	PCI_DIV_EN	PCI Divider Enabled 0 = PCI Divider disabled, 1 = PCI Divider enabled
2	1	CPU_DIV_EN	CPU Divider Enabled 0 = CPU Divider disabled, 1 = CPU Divider enabled
1	1	CPU1_STP_CRTL	Allow control of CPU1 with assertion of CPU_STOP# 0 = Free running, 1 = Stopped with CPU_STOP#
0	1	CPU0_STP_CRTL	Allow control of CPU0 with assertion of CPU_STOP# 0 = Free running, 1 = Stopped with CPU_STOP#

Byte 11 Control Register 11

Bit	@Pup	Name	Description
7	HW	PCI3_CFG1	
6	HW	PCI3_CFG0	
5	0	25MHz_EN_SE1	25MHz Output Enabled applies to Powerdown / M1 *(Only applies when PCI3/CGFG0 strap is set high to enter HW mode 3)* 0 = 25MHz disabled in Powerdown / M1 1 = 25MHz enabled in Powerdown / M1; Sticky 1
4	1	RESERVED	RESERVED

PCI3/ CGF1	PCI3/ CGF0	Mode	PLL1		PLL2		PLL3	
			Output	SSC	Output	SSC	Output	SSC
0	0	0 -Def	CPU / SRC / PCI33	Down	USB	NA	--	--
0	1	1	CPU	Down	USB	NA	SRC/PCI33	Down
1	0	2	CPU	Center	USB	NA	SRC/PCI33	Down
1	1	3	CPU	Center	USB/25M	NA	SRC/PCI33	Down

Byte 11 Control Register 11

3	0	CPU2_AMT_EN	
2	1	CPU1_AMT_EN	
1	HW	PCI-E_GEN2	PCI-E_Gen2 Compliant 0 = non Gen2, 1= Gen2 Compliant
0	1	CPU2_STP_CRTL	Allow control of CPU2 with assertion of CPU_STOP# 0 = Free running, 1 = Stopped with CPU_STOP#

PCIF0/ITP_EN	AMT_EN	CPU2_AMT_EN	CPU1_AMT_EN	Description
x	1	0	0	Reserved
x	1	0	1	CPU1 = M1 Clock
1	1	1	0	CPU2 - M1 Clock
1	1	1	1	CPU1 and CPU2 = M1 Clock

Byte 12 Byte Count

Bit	@Pup	Name	Description
7	0	RESERVED	RESERVED
6	0	RESERVED	RESERVED
5	0	BC5	Byte count
4	0	BC4	Byte count
3	1	BC3	Byte count
2	1	BC2	Byte count
1	0	BC1	Byte count
0	1	BC0	Byte count

Byte 13 Control Register 13

Bit	@Pup	Name	Description
7	1	USB_DSC1	USB drive strength control, *See Byte 18 for more setting* 0 = Low, 1= High
6	1	PCI/PCIF_DSC1	PCI drive strength control, *See Byte 18 for more setting* 0 = Low, 1 = High
5	0	RESERVED	RESERVED
4	0	SATA_SS_EN	Enable SATA spread modulation, 0 = Spread Disabled 1 = Spread Enabled
3	1	EN_CFG0_SET	By defalult CFG0 pin strap sets the SMBus initial values to select the HW mode. When this bit is written0, subsequent SMBus accesses is the Lathes Open state, can overwrite the CFG0 pin setting into the SMBus bits and set the mode before the M0 state: specifically B0b2, B1b[6,4,3], B9b1, B11b5
2	1	SE1/SE2_DSC1	SE1 and SE2 drive strength control, *See Byte 18 for more setting* 0 = Low, 1 = High
1	1	RESERVED	RESERVED
0	1	SW_PCI	SW PCI_STP# Function 0 = SW PCI_STP assert, 1 = SW PCI_STP deassert When this bit is set to 0, all STOPPABLE PCI, PCIF and SRC outputs will be stopped in a synchronous manner with no short pulses. When this bit is set to 1, all STOPPED PCI, PCIF and SRC outputs will resume in a synchronous manner with no short pulses.

Byte 14 Control Register 14

Bit	@Pup	Name	Description

Byte 14 Control Register 14

7	0	CPU_DAF_N7	If Prog_CPU_EN is set, the values programmed in CPU_DAF_N[8:0] and CPU_DAF_M[6:0] will be used to determine the CPU output frequency. The setting of the FS_Override bit determines the frequency ratio for CPU and other output clocks. When it is cleared, the same frequency ratio stated in the Latched FS[C:A] register will be used. When it is set, the frequency ratio stated in the FSEL[2:0] register will be used
6	0	CPU_DAF_N6	
5	0	CPU_DAF_N5	
4	0	CPU_DAF_N4	
3	0	CPU_DAF_N3	
2	0	CPU_DAF_N2	
1	0	CPU_DAF_N1	
0	0	CPU_DAF_N0	

Byte 15 Control Register 15

Bit	@Pup	Name	Description
7	0	CPU_DAF_N8	See Byte 14 for description
6	0	CPU_DAF_M6	If Prog_CPU_EN is set, the values programmed are in CPU_FSEL_N[8:0] and CPU_FSEL_M[6:0] will be used to determine the CPU output frequency. The setting of the FS_Override bit determines the frequency ratio for CPU and other output clocks. When it is cleared, the same frequency ratio stated in the Latched FS[C:A] register will be used. When it is set, the frequency ratio stated in the FSEL[2:0] register will be used
5	0	CPU_DAF_M5	
4	0	CPU_DAF_M4	
3	0	CPU_DAF_M3	
2	0	CPU_DAF_M2	
1	0	CPU_DAF_M1	
0	0	CPU_DAF_M0	

Byte 16 Control Register 16

Bit	@Pup	Name	Description
7	0	PCI-E_N7	If Prog_SRC_EN is set, the values programmed in SRC_DAF_N[7:0] will be used to determine the SRC output frequency.
6	0	PCI-E_N6	
5	0	PCI-E_N5	
4	0	PCI-E_N4	
3	0	PCI-E_N3	
2	0	PCI-E_N2	
1	0	PCI-E_N1	
0	0	PCI-E_N0	

Byte 17 Control Register 17

Bit	@Pup	Name	Description
7	0	SMSW_EN	Enable Smooth Switching, 0 = Disabled, 1= Enabled
6	0	SMSW_SEL	Smooth switch select, 0 = CPU_PLL, 1 = SRC_PLL
5	0	RESERVED	RESERVED
4	0	Prog_PCI-E_EN	Programmable PCI-E frequency enable 0 = Disabled, 1= Enabled
3	0	Prog_CPU_EN	Programmable CPU frequency enable 0 = Disabled, 1= Enabled
2	0	RESERVED	RESERVED
1	0	RESERVED	RESERVED
0	0	RESERVED	RESERVED

Byte 18 Control Register 18

Bit	@Pup	Name	Description
7	0	PCI_DSC2	Drive Strength Control - DSC[2:0]
6	1	PCI_DSC0	
5	0	USB_DSC2	
4	0	USB_DSC0	
3	0	SE1/SE2_DSC2	
2	0	SE1/SE2_DSC0	
1	0	REF_DSC2	
0	0	REF_DSC0	

	DSC_2 (Byte18)	DSC_1 (Various Bytes)	DSC_0 (Byte 18)	Buffer Strength
	1	1	1	Strongest
	1	1	0	
	1	0	1	
	1	0	0	
Default PCI	0	1	1	
Default REF/Usb	0	1	0	
	0	0	1	
	0	0	0	Weakest

Table 5. Crystal Recommendations

Frequency (Fund)	Cut	Loading	Load Cap	Drive (max.)	Shunt Cap (max.)	Motional (max.)	Tolerance (max.)	Stability (max.)	Aging (max.)
14.31818 MHz	AT	Parallel	20 pF	0.1 mW	5 pF	0.016 pF	35 ppm	30 ppm	5 ppm

The SPL505YC256BT/ SPL505YC256BS requires a parallel resonance crystal. Substituting a series resonance crystal causes the SPL505YC256BT/ SPL505YC256BS to operate at the wrong frequency and violate the ppm specification. For most applications there is a 300-ppm frequency shift between series and parallel crystals due to incorrect loading.

Crystal Loading

Crystal loading plays a critical role in achieving low ppm performance. To realize low ppm performance, the total capacitance the crystal sees must be considered to calculate the appropriate capacitive loading (CL).

Figure 1 shows a typical crystal configuration using the two trim capacitors. An important clarification for the following discussion is that the trim capacitors are in series with the crystal not parallel. The common misconception that load capacitors are in parallel with the crystal and should be approximately equal to the load capacitance of the crystal is not true.

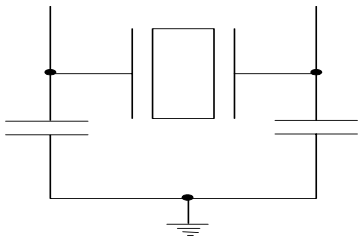


Figure 1. Crystal Capacitive Clarification

Calculating Load Capacitors

In addition to the standard external trim capacitors, trace capacitance and pin capacitance must also be considered to correctly calculate crystal loading. As mentioned previously, the capacitance on each side of the crystal is in series with the crystal. This means the total capacitance on each side of the crystal must be twice the specified crystal load capacitance (CL). While the capacitance on each side of the crystal is in series with the crystal, trim capacitors (Ce1,Ce2) should be calculated to provide equal capacitive loading on both sides.

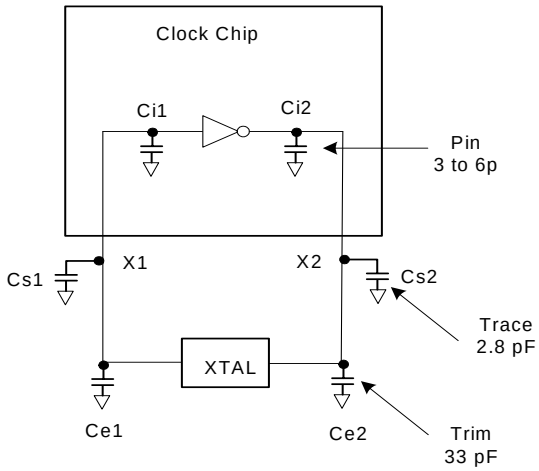


Figure 2. Crystal Loading Example

Use the following formulas to calculate the trim capacitor values for Ce1 and Ce2.

Load Capacitance (each side)

$$Ce = 2 * CL - (Cs + Ci)$$

Total Capacitance (as seen by the crystal)

$$CLe = \frac{1}{\left(\frac{1}{Ce1 + Cs1 + Ci1} + \frac{1}{Ce2 + Cs2 + Ci2}\right)}$$

CL ..... Crystal load capacitance

CLe .....Actual loading seen by crystal using standard value trim capacitors

Ce .....External trim capacitors

Cs ..... Stray capacitance (terraced)

Ci ..... Internal capacitance (lead frame, bond wires etc.)

Dial-A-Frequency (CPU & PCIEX)

This feature allows users to over-clock their systems by slowly stepping up the CPU or SRC frequency. When the programmable output frequency feature is enabled, the CPU and SRC frequencies are determined by the following equation:

Fcpu = G * N/M or Fcpu=G2 * N, where G2 = G/M.

'N' and 'M' are the values programmed in Programmable Frequency Select N-Value Register and M-Value Register, respectively. 'G' stands for the PLL Gear Constant, which is determined by the programmed value of FS[E:A]. See *Frequency Table* for the Gear Constant for each Frequency selection. The PCI Express only allows user control of the N register, the M value is fixed and documented in the *Frequency Select Table*.

In this mode, the user writes the desired N and M value into the DAF I2C registers. The user cannot change only the M value and must change both the M and the N values at the same time, if they require a change to the M value. The user may change only the required N value.

Associated Register Bits

CPU_DAF Enable – This bit enables CPU DAF mode. By default, it is not set. When set, the operating frequency is determined by the values entered into the CPU_DAF_N register. Note that the CPU_DAF_N and M register must contain valid values before CPU_DAF is set. Default = 0, (No DAF).

CPU_DAF_N – There are nine bits (for 512 values) to linearly change the CPU frequency (limited by VCO range). Default = 0, (0000). The allowable values for N are detailed in the *Frequency Select Table*.

CPU DAF M – There are 7 bits (for 128 values) to linearly change the CPU frequency (limited by VCO range). Default = 0, the allowable values for M are detailed in the *Frequency Select Table*.

SRC_DAF Enable – This bit enables SRC DAF mode. By default, it is not set. When set, the operating frequency is determined by the values entered into the SRC_DAF_N register. Note that the SRC_DAF_N register must contain valid values before SRC_DAF is set. Default = 0, (No DAF).

SRC_DAF_N – There are nine bits (for 512 values) to linearly change the CPU frequency (limited by VCO range). Default = 0, (0000). The allowable values for N are detailed in the *Frequency Select Table*.

Smooth Switching

The device contains 1 smooth switch circuit that is shared by the CPU PLL and SRC PLL. The smooth switch circuit ensures that when the output frequency changes by overclocking, the transition from the old frequency to the new frequency is a slow, smooth transition containing no glitches. The rate of change of output frequency when using the smooth switch circuit is less than 1 MHz/0.667 µs. The frequency overshoot and undershoot is less than 2%.

The Smooth Switch circuit can be assigned as auto or manual. In Auto mode, clock generator will assign smooth switch automatically when the PLL does overclocking. For manual mode, the smooth switch circuit can be assigned to either PLL via SMBus. By default the smooth switch circuit is set to auto mode. Either PLL can still be over-clocked when it does not have control of the smooth switch circuit but it is not guaranteed to transition to the new frequency without large frequency glitches.

It is not recommended to enable over-clocking and change the N values of both PLLs in the same SMBUS block write and use smooth switch mechanism on spread spectrum on/off.

PD# Clarification

The CK_PWRGD/PD# pin is a dual-function pin. During initial power-up, the pin functions as CK_PWRGD. Once CK_PWRGD has been sampled HIGH by the clock chip, the pin assumes PD# functionality. The PD# pin is an asynchronous active LOW input used to shut off all clocks cleanly prior to shutting off power to the device. This signal is synchronized internal to the device prior to powering down the clock synthesizer. PD# is also an asynchronous input for powering up the system. When PD# is asserted LOW, all clocks need to be driven to a LOW value and held prior to turning off the VCOs and the crystal oscillator.

PD Assertion

When PS is sampled HIGH by two consecutive rising edges of CPUC, all single-ended outputs will be held LOW on their next HIGH-to-LOW transition and differential clocks must held LOW. In the event that PD mode is desired as the initial power-on state, PD must be asserted HIGH in less than 10 µs after asserting CK_PWRGD.

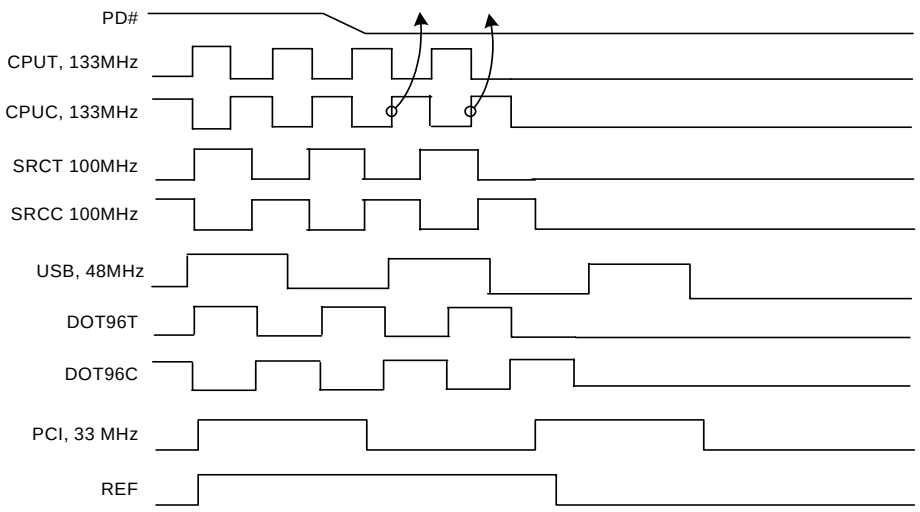
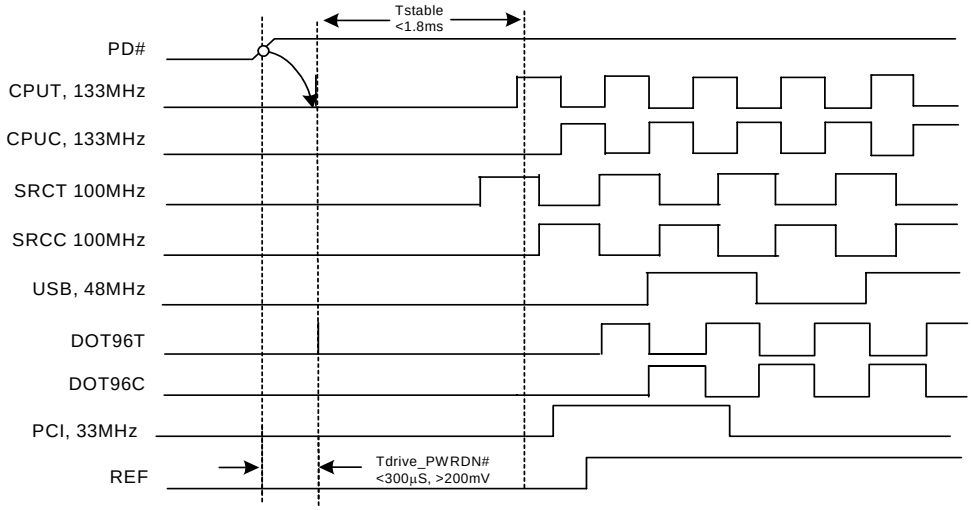


Figure 3. PD Assertion Timing Waveform

PD# Deassertion

The power-up latency is less than 1.8 ms. This is the time from the deassertion of the PD# pin or the ramping of the power supply until the time that stable clocks are output from the clock chip. All differential outputs stopped in a three-state condition resulting from power down will be driven high in less than 300 μs of PD# deassertion to a voltage greater than 200 mV. After the clock chip's internal PLL is powered up and locked, all outputs will be enabled within a few clock cycles of each other. Below is an example showing the relationship of clocks coming up.



PD Deassertion Timing Waveform

CPU_STP# Assertion

The CPU_STP# signal is an active LOW input used to synchronously stop and start the CPU output clocks while the rest of the clock generator continues to function. When the CPU_STP# pin is asserted, all CPU outputs that are set with the SMBus configuration to be stoppable via assertion of CPU_STP# are stopped within two to six CPU clock periods after being sampled by two rising edges of the internal CPUC clock. The final states of the stopped CPU signals are CPUT = HIGH and CPUC = LOW.

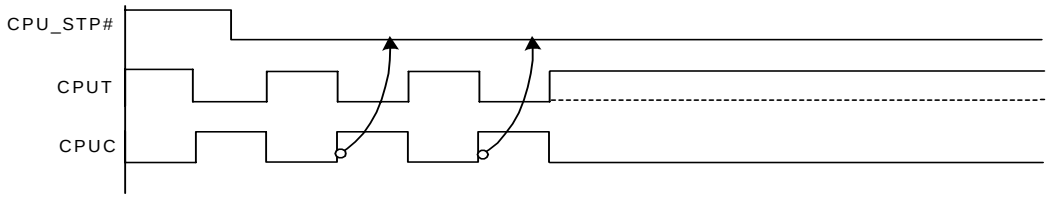
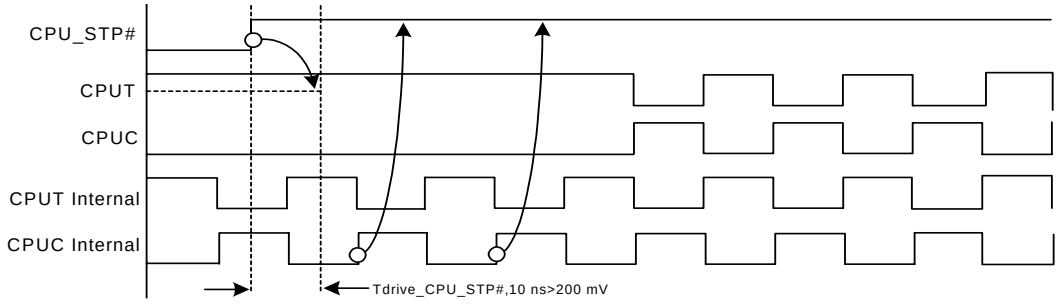


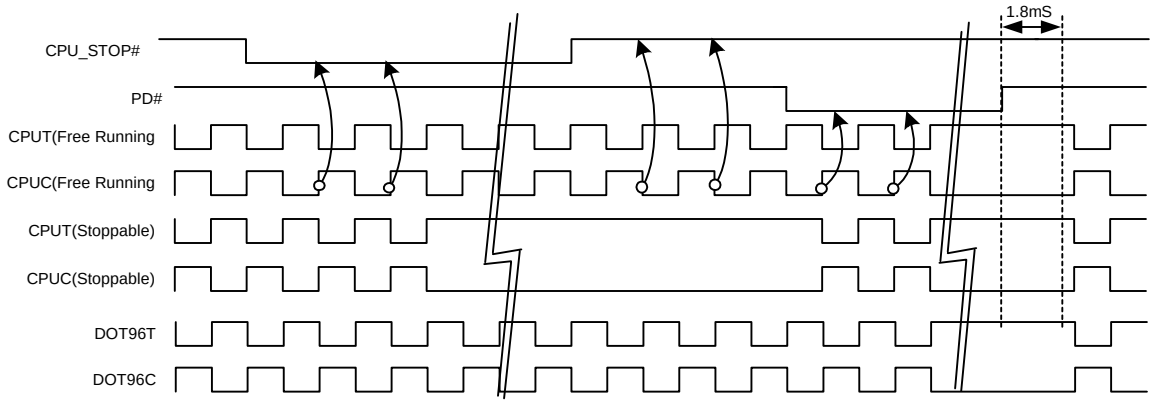
Figure 4. CPU_STP# Assertion Waveform

CPU_STP# Deassertion

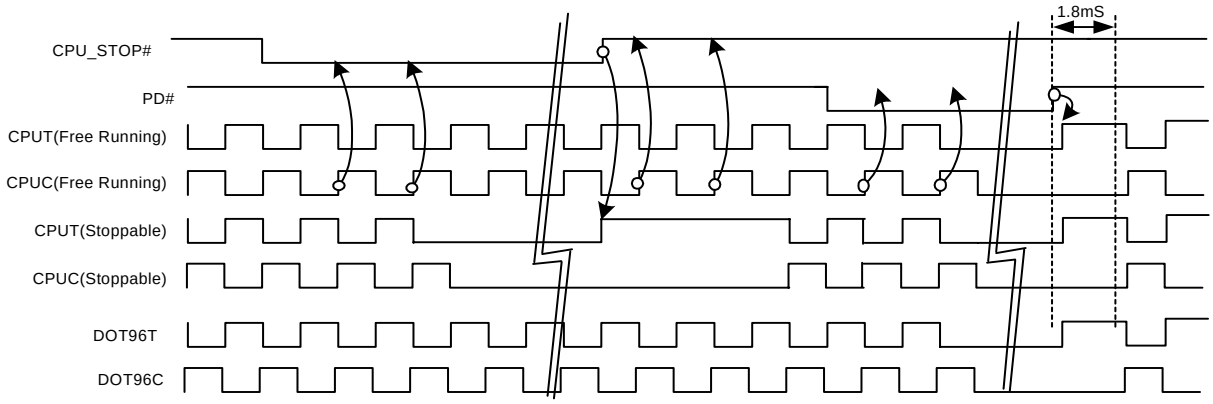
The deassertion of the CPU_STP# signal will cause all CPU outputs that were stopped to resume normal operation in a synchronous manner, synchronous manner meaning that no short or stretched clock pulses will be produce when the clock resumes. The maximum latency from the deassertion to active outputs is no more than two CPU clock cycles.



CPU_STP# Deassertion Waveform



CPU_STP# = Driven, CPU_PD = Driven, DOT_PD = Driven



CPU_STP# = Tri-state, CPU_PD = Tri-state, DOT_PD = Tri-state

PCI_STP# Assertion

The PCI_STP# signal is an active LOW input used to synchronously stop and start the PCI outputs while the rest of the clock generator continues to function. The set-up time for capturing PCI_STP# going LOW is 10 ns (t_{SU}). (See *Figure 5*.) The PCIF clocks will not be affected by this pin if their corresponding control bit in the SMBus register is set to allow them to be free running.

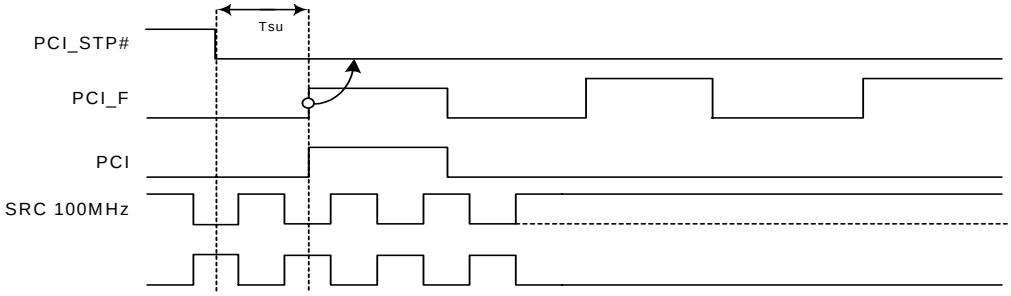


Figure 5. PCI_STP# Assertion Waveform

PCI_STP# Deassertion

The deassertion of the PCI_STP# signal causes all PCI and stoppable PCIF clocks to resume running in a synchronous manner within two PCI clock periods after PCI_STP# transitions to a HIGH level.

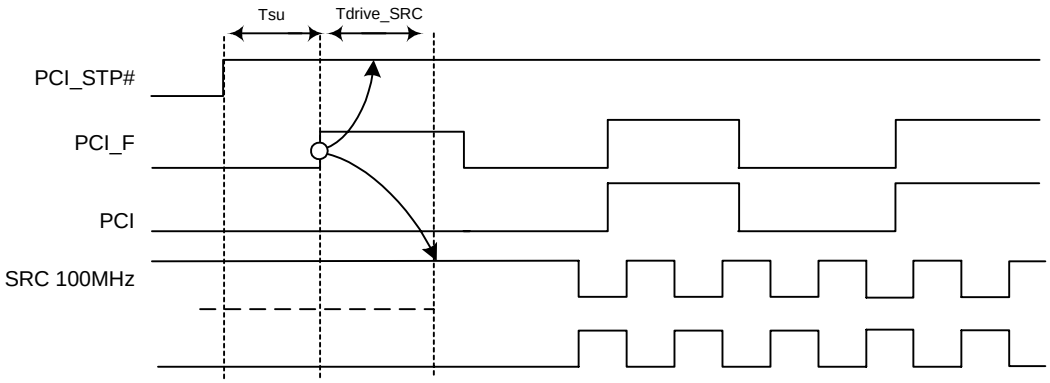


Figure 6. PCI_STP# Deassertion Waveform

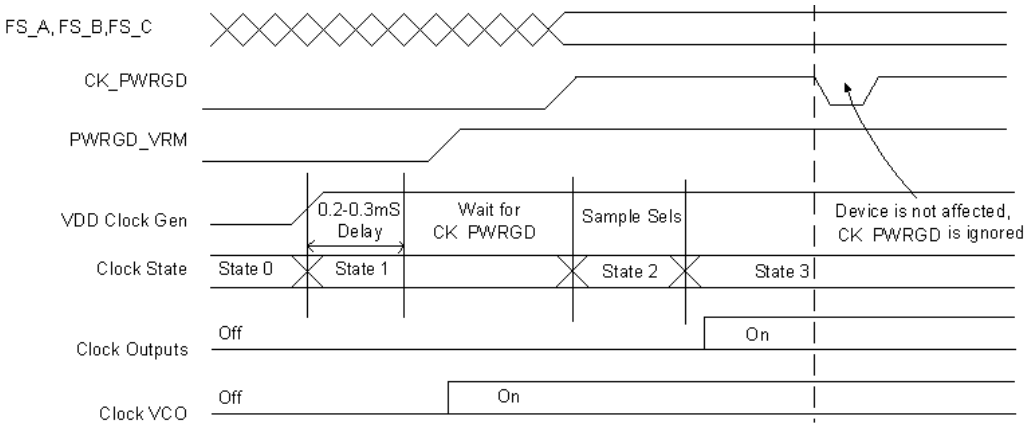


Figure 7. CK_PWRGD Timing Diagram

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Table 6. Output Driver Status during PCI-STOP# and CPU-STOP#

		PCI_STOP# Asserted	CPU_STOP# Asserted	SMBus OE Disabled
Single-ended Clocks	Stoppable	Driven Low	Running	Driven Low
	Non Stoppable	Running	Running	
Differential Clocks	Stoppable	Clock Drive High Clock# Driven Low	Clock Drive High Clock# Driven Low	Driven Low or 20K pulldown
	Non Stoppable	Running	Running	

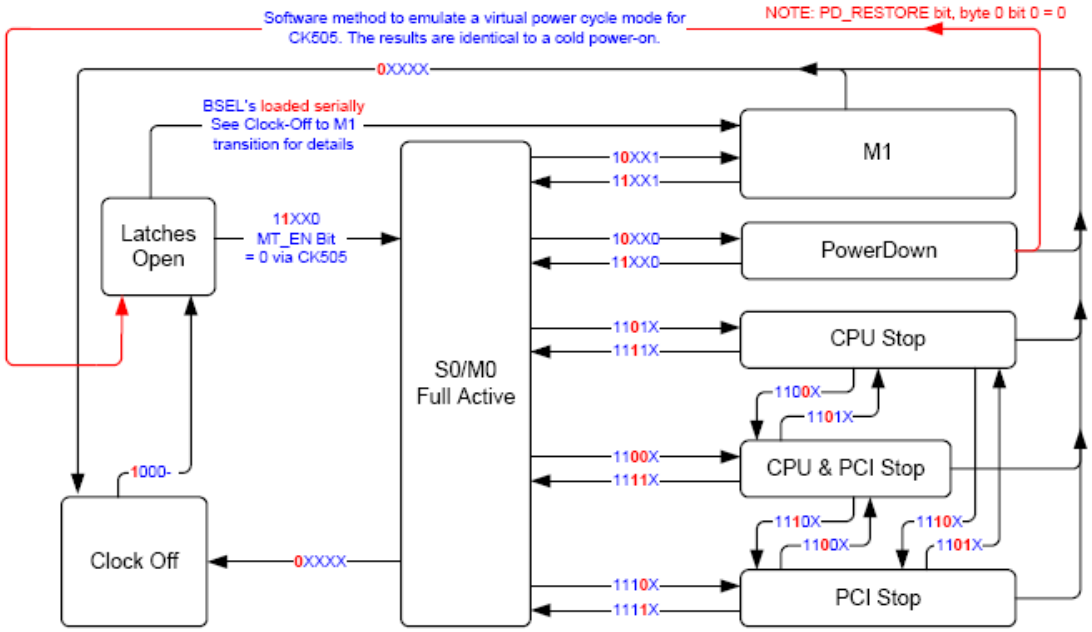
Table 7. Output Driver Status

	All Single-ended Clocks		All Differential Clocks except CPU1		CPU1	
	w/o Strap	**w/Strap**	**Clock**	**Clock#**	**Clock**	**Clock#**
Latches Open State	Low	Hi-Z	Low or 20K pulldown	Low	Low or 20K pulldown	Low
Powerdown	Low	Hi-Z	Low or 20K pulldown	Low	Low or 20K pulldown	Low
M1	Low	Hi-Z	Low or 20K pulldown	Low	Running	Running

PD_RESTORE

If a '0' is set for Byte 0 bit 0 then, upon assertion of PWRDWN# LOW, the CY505 will initiate a full reset. The results of this will be that the clock chip will emulate a cold power on start and go to the 'Latches Open' state. If the PD_RESTORE bit is set to a '1' then the configuration is stored upon PWRDWN# asserted LOW. Note that if the iAMT bit, Byte 0 bit 3, is set to a '1' then the PD_RESTORE bit must be ignored. In other words, in Intel iAMT mode, PWRDWN# reset is not allowed.

Figure 8. Clock Generator Power-up/Run State Diagram



State Diagram Logic Legend

Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Vdd_Main	CKPWRGD / PWRDWN#	CPU_STOP#	PCI_STOP#	MT_EN

Absolute Maximum Conditions

Parameter	Description	Condition	Min.	Max.	Unit
V_{DD}	Core Supply Voltage		–0.5	4.6	V
V_{DD_A}	Analog Supply Voltage		–0.5	4.6	V
V_{DD_IO}	IO Supply Voltage			1.5	V
V_{IN}	Input Voltage	Relative to V_{SS}	–0.5	4.6	V_{DC}
T_S	Temperature, Storage	Non-functional	–65	150	°C
T_A	Temperature, Operating Ambient	Functional	0	85	°C
T_J	Temperature, Junction	Functional	–	150	°C
$Ø_{JC}$	Dissipation, Junction to Case	Mil-STD-883E Method 1012.1	–	20	°C/W
$Ø_{JA}$	Dissipation, Junction to Ambient	JEDEC (JESD 51)	–	60	°C/W
ESD_{HBM}	ESD Protection (Human Body Model)	MIL-STD-883, Method 3015	2000	–	V
UL-94	Flammability Rating	At 1/8 in.	V–0		
MSL	Moisture Sensitivity Level		1		

Multiple Supplies: The Voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.

DC Electrical Specifications

Parameter	Description	Condition	Min.	Max.	Unit
VDD core	3.3V Operating Voltage	3.3 ± 5%	3.135	3.465	V
V_{IH}	3.3V Input High Voltage (SE)		2.0	V_{DD} + 0.3	V
V_{IL}	3.3V Input Low Voltage (SE)		V_{SS}–0.3	0.8	V
V_{IHI2C}	Input High Voltage	SDATA, SCLK	2.2	–	V
V_{ILI2C}	Input Low Voltage	SDATA, SCLK	–	1.0	V
V_{IH_FS}	FS_[A,B] Input High Voltage		0.7	1.5	V
V_{IL_FS}	FS_[A,B] Input Low Voltage		V_{SS}–0.3	0.35	V
$V_{IHFS\_C\_TEST}$	FS_C Input High Voltage		2	V_{DD} + 0.3	V
$V_{IMFS\_C\_NORMAL}$	FS_C Input Middle Voltage		0.7	1.5	V
$V_{ILFS\_C\_NORMAL}$	FS_C Input Low Voltage		V_{SS}–0.3	0.35	V
$PCI3/CFG0_{\_HIGH}$	PCI3/CFG0 Input High Voltage	Typ. 2.75V	2.40	VDD	V
$PCI3/CFG0_{\_MID}$	PCI3/CFG0 Input Mid Voltage	Typ. 1.65V	1.30	2.00	V
$PCI3/CFG0_{\_LOW}$	PCI3/CFG0 Input Low Voltage	Typ. 0.550V	0	0.900	V
I_{IH}	Input High Leakage Current	except internal pull-down resistors, $0< V_{IN}<V_{DD}$	–	5	µA
I_{IL}	Input Low Leakage Current	except internal pull-up resistors, $0 < V_{IN} < V_{DD}$	–5	–	µA
V_{OH}	3.3V Output High Voltage (SE)	I_{OH} = –1 mA	2.4	–	V
V_{OL}	3.3V Output Low Voltage (SE)	I_{OL} = 1 mA	–	0.4	V
VDD IO	Low Voltage IO Supply Voltage		0.72	0.88	
V_{OH}	3.3V Input High Voltage (DIFF)		0.70	0.90	V
V_{OL}	3.3V Input Low Voltage (DIFF)			0.40	V
I_{OZ}	High-impedance Output Current		–10	10	µA
C_{IN}	Input Pin Capacitance		1.5	5	pF
C_{OUT}	Output Pin Capacitance			6	pF
L_{IN}	Pin Inductance		–	7	nH
V_{XIH}	Xin High Voltage		$0.7V_{DD}$	V_{DD}	V
V_{XIL}	Xin Low Voltage		0	$0.3V_{DD}$	V
$I_{DD3.3V}$	Dynamic Supply Current		–	250	mA

AC Electrical Specifications

Parameter	Description	Condition	Min.	Max.	Unit
Crystal					
T_{DC}	XIN Duty Cycle	The device will operate reliably with input duty cycles up to 30/70 but the REF clock duty cycle will not be within specification	47.5	52.5	%
T_{PERIOD}	XIN Period	When XIN is driven from an external clock source	69.841	71.0	ns
T_R/T_F	XIN Rise and Fall Times	Measured between $0.3V_{DD}$ and $0.7V_{DD}$	–	10.0	ns
T_{CCJ}	XIN Cycle to Cycle Jitter	As an average over 1-µs duration	–	500	ps
L_{ACC}	Long-term Accuracy		–	300	ppm
CPU at 0.7V					
T_{DC}	CPUT and CPUC Duty Cycle	Measured at 0V differential @ 0.1s	45	55	%
T_{PERIOD}	100 MHz CPUT and CPUC Period	Measured at 0V differential @ 0.1s	9.99900	10.0100	ns
T_{PERIOD}	133 MHz CPUT and CPUC Period	Measured at 0V differential @ 0.1s	7.49925	7.50075	ns
T_{PERIOD}	166 MHz CPUT and CPUC Period	Measured at 0V differential @ 0.1s	5.99940	6.00060	ns
T_{PERIOD}	200 MHz CPUT and CPUC Period	Measured at 0V differential @ 0.1s	4.99950	5.00050	ns
T_{PERIOD}	266 MHz CPUT and CPUC Period	Measured at 0V differential @ 0.1s	3.74963	3.75038	ns
T_{PERIOD}	333 MHz CPUT and CPUC Period	Measured at 0V differential @ 0.1s	2.99970	3.00030	ns
T_{PERIOD}	400 MHz CPUT and CPUC Period	Measured at 0V differential @ 0.1s	2.49975	2.50025	ns
$T_{PERIODSS}$	100 MHz CPUT and CPUC Period, SSC	Measured at 0V differential @ 0.1s	10.02406	10.02607	ns
$T_{PERIODSS}$	133 MHz CPUT and CPUC Period, SSC	Measured at 0V differential @ 0.1s	7.51804	7.51955	ns
$T_{PERIODSS}$	166 MHz CPUT and CPUC Period, SSC	Measured at 0V differential @ 0.1s	6.01444	6.01564	ns
$T_{PERIODSS}$	200 MHz CPUT and CPUC Period, SSC	Measured at 0V differential @ 0.1s	5.01203	5.01303	ns
$T_{PERIODSS}$	266 MHz CPUT and CPUC Period, SSC	Measured at 0V differential @ 0.1s	3.75902	3.75978	ns
$T_{PERIODSS}$	333 MHz CPUT and CPUC Period, SSC	Measured at 0V differential @ 0.1s	3.00722	3.00782	ns
$T_{PERIODSS}$	400 MHz CPUT and CPUC Period, SSC	Measured at 0V differential @ 0.1s	2.50601	2.50652	ns
$T_{PERIODAbs}$	100 MHz CPUT and CPUC Absolute period	Measured at 0V differential @ 1 clock	9.91400	10.0860	ns
$T_{PERIODAbs}$	133 MHz CPUT and CPUC Absolute period	Measured at 0V differential @ 1 clock	7.41425	7.58575	ns
$T_{PERIODAbs}$	166 MHz CPUT and CPUC Absolute period	Measured at 0V differential @ 1 clock	5.91440	6.08560	ns
$T_{PERIODAbs}$	200 MHz CPUT and CPUC Absolute period	Measured at 0V differential @ 1 clock	4.91450	5.08550	ns
$T_{PERIODAbs}$	266 MHz CPUT and CPUC Absolute period	Measured at 0V differential @ 1 clock	3.66463	3.83538	ns
$T_{PERIODAbs}$	333 MHz CPUT and CPUC Absolute period	Measured at 0V differential @ 1 clock	2.91470	3.08530	ns
$T_{PERIODAbs}$	400 MHz CPUT and CPUC Absolute period	Measured at 0V differential @ 1 clock	2.41475	2.58525	ns
$T_{PERIODSSAbs}$	100 MHz CPUT and CPUC Absolute period, SSC	Measured at 0V differential @ 1 clock	9.91406	10.1362	ns
$T_{PERIODSSAbs}$	133 MHz CPUT and CPUC Absolute period, SSC	Measured at 0V differential @ 1 clock	7.41430	7.62340	ns
$T_{PERIODSSAbs}$	166 MHz CPUT and CPUC Absolute period, SSC	Measured at 0V differential @ 1 clock	5.91444	6.11572	ns
$T_{PERIODSSAbs}$	200 MHz CPUT and CPUC Absolute period, SSC	Measured at 0V differential @ 1 clock	4.91453	5.11060	ns
$T_{PERIODSSAbs}$	266 MHz CPUT and CPUC Absolute period, SSC	Measured at 0V differential @ 1 clock	3.66465	3.85420	ns
$T_{PERIODSSAbs}$	333 MHz CPUT and CPUC Absolute period, SSC	Measured at 0V differential @ 1 clock	2.91472	3.10036	ns
$T_{PERIODSSAbs}$	400 MHz CPUT and CPUC Absolute period, SSC	Measured at 0V differential @ 1 clock	2.41477	2.59780	ns
T_{CCJ}	CPUT/C Cycle to Cycle Jitter	Measured at 0V differential	–	85	ps
T_{CCJ2}	CPU2_ITP Cycle to Cycle Jitter	Measured at 0V differential	–	125	ps
L_{ACC}	Long-term Accuracy	Measured at 0V differential	–	100	ppm
T_{SKEW2}	CPU2_ITP to CPU0 Clock Skew	Measured at 0V differential	–	100	ps
T_{SKEW2}	CPU2_ITP to CPU0 Clock Skew	Measured at 0V differential	–	150	ps

AC Electrical Specifications (continued)

Parameter	Description	Condition	Min.	Max.	Unit
T_R/T_F	CPUT and CPUC Rise and Fall Time	Measured differentially from ±150 mV	2.5	8	V/ns
T_{RFM}	Rise/Fall Matching	Measured single-endedly from ±75 mV	–	20	%
V_{HIGH}	Voltage High			1.15	V
V_{LOW}	Voltage Low		–0.3	–	V
V_{OX}	Crossing Point Voltage at 0.7V Swing		300	550	mV
SRC					
T_{DC}	SRCT and SRCC Duty Cycle	Measured at 0V differential	45	55	%
T_{PERIOD}	100 MHz SRCT and SRCC Period	Measured at 0V differential @ 0.1s	9.99900	10.0010	ns
$T_{PERIODSS}$	100 MHz SRCT and SRCC Period, SSC	Measured at 0V differential @ 0.1s	10.02406	10.02607	ns
$T_{PERIODAbs}$	100 MHz SRCT and SRCC Absolute Period	Measured at 0V differential @ 1 clock	9.87400	10.1260	ns
$T_{PERIODSSAbs}$	100 MHz SRCT and SRCC Absolute Period, SSC	Measured at 0V differential @ 1 clock	9.87406	10.1762	ns
$T_{SKEW(window)}$	Any SRCT/C to SRCT/C Clock Skew from the earliest bank to the latest bank	Measured at 0V differential	–	3.0	ns
T_{CCJ}	SRCT/C Cycle to Cycle Jitter	Measured at 0V differential	–	125	ps
L_{ACC}	SRCT/C Long Term Accuracy	Measured at 0V differential	–	100	ppm
T_R/T_F	SRCT and SRCC Rise and Fall Time	Measured differentially from ±150 mV	2.5	8	V/ns
T_{RFM}	Rise/Fall Matching	Measured single-endedly from ±75 mV	–	20	%
V_{HIGH}	Voltage High			1.15	V
V_{LOW}	Voltage Low		–0.3	–	V
V_{OX}	Crossing Point Voltage at 0.7V Swing		300	550	mV
DOT					
T_{DC}	DOT96T and DOT96C Duty Cycle	Measured at 0V differential	45	55	%
T_{PERIOD}	DOT96T and DOT96C Period	Measured at 0V differential @ 0.1s	10.4156	10.4177	ns
$T_{PERIODAbs}$	DOT96T and DOT96C Absolute Period	Measured at 0V differential @ 0.1s	10.1656	10.6677	ns
T_{CCJ}	DOT96T/C Cycle to Cycle Jitter	Measured at 0V differential @ 1 clock	–	250	ps
L_{ACC}	DOT96T/C Long Term Accuracy	Measured at 0V differential @ 1 clock	–	300	ppm
T_R/T_F	DOT96T and DOT96C Rise and Fall Time	Measured differentially from ±150 mV	2.5	8	V/ns
T_{RFM}	Rise/Fall Matching	Measured single-endedly from ±75 mV	–	20	%
V_{HIGH}	Voltage High			1.15	V
V_{LOW}	Voltage Low		–0.3	–	V
V_{OX}	Crossing Point Voltage at 0.7V Swing		300	550	mV
LCD_100_SSC					
T_{DC}	SSCT and SSCC Duty Cycle	Measured at 0V differential	45	55	%
T_{PERIOD}	100 MHz SSCT and SSCC Period	Measured at 0V differential @ 0.1s	9.99900	10.0010	ns
$T_{PERIODSS}$	100 MHz SSCT and SSCC Period, SSC	Measured at 0V differential @ 0.1s	10.02406	10.02607	ns
$T_{PERIODAbs}$	100 MHz SSCT and SSCC Absolute Period	Measured at 0V differential @ 1 clock	9.87400	10.1260	ns
$T_{PERIODSSAbs}$	100 MHz SRCT and SRCC Absolute Period, SSC	Measured at 0V differential @ 1 clock	9.87406	10.1762	ns
T_{CCJ}	SSCT/C Cycle to Cycle Jitter	Measured at 0V differential	–	250	ps
L_{ACC}	SSCT/C Long Term Accuracy	Measured at 0V differential	–	300	ppm
T_R/T_F	SSCT and SSCC Rise and Fall Time	Measured differentially from ±150 mV	2.5	8	V/ns
T_{RFM}	Rise/Fall Matching	Measured single-endedly from ±75 mV	–	20	%
V_{HIGH}	Voltage High			1.15	V
V_{LOW}	Voltage Low		–0.3	–	V

AC Electrical Specifications (continued)

Parameter	Description	Condition	Min.	Max.	Unit
V_{OX}	Crossing Point Voltage at 0.7V Swing		300	550	mV
PCI/PCIF					
T_{DC}	PCI Duty Cycle	Measurement at 1.5V	45	55	%
T_{PERIOD}	Spread Disabled PCIF/PCI Period	Measurement at 1.5V	29.99100	30.00900	ns
$T_{PERIODSS}$	Spread Enabled PCIF/PCI Period, SSC	Measurement at 1.5V	30.08421	30.23459	ns
$T_{PERIODAbs}$	Spread Disabled PCIF/PCI Period	Measurement at 1.5V	29.49700	30.50300	ns
$T_{PERIODSSAbs}$	Spread Enabled PCIF/PCI Period, SSC	Measurement at 1.5V	29.56617	30.58421	ns
T_{HIGH}	PCIF and PCI high time	Measurement at 2.4V	12.0	–	ns
T_{LOW}	PCIF and PCI low time	Measurement at 0.4V	12.0	–	ns
T_R/T_F	PCIF/PCI rising and falling Edge Rate	Measured between 0.8V and 2.0V	1.0	4.0	V/ns
T_{SKEW}	Any PCI clock to Any PCI clock Skew	Measurement at 1.5V	–	1000	ps
T_{CCJ}	PCIF and PCI Cycle to Cycle Jitter	Measurement at 1.5V	–	500	ps
L_{ACC}	PCIF/PCI Long Term Accuracy	Measurement at 1.5V	–	100	ppm
48_M					
T_{DC}	Duty Cycle	Measurement at 1.5V	45	55	%
T_{PERIOD}	Period	Measurement at 1.5V	20.83125	20.83542	ns
$T_{PERIODAbs}$	Absolute Period	Measurement at 1.5V	20.48125	21.18542	ns
T_{HIGH}	48_M High time	Measurement at 2.4V	8.216563	11.15198	ns
T_{LOW}	48_M Low time	Measurement at 0.4V	7.816563	10.95198	ns
T_R/T_F	Rising and Falling Edge Rate	Measured between 0.8V and 2.0V	1.0	2.0	V/ns
T_{CCJ}	Cycle to Cycle Jitter	Measurement at 1.5V	–	350	ps
L_{ACC}	48M Long Term Accuracy	Measurement at 1.5V	–	100	ppm
25_M					
T_{DC}	Duty Cycle	Measurement at 1.5V	45	55	%
T_{PERIOD}	Period	Measurement at 1.5V	39.996	40.004	ns
T_R/T_F	Rising and Falling Edge Rate	Measured between 0.8V and 2.0V	1.0	4.0	V/ns
T_{CCJ}	Cycle to Cycle Jitter	Measurement at 1.5V	–	500	ps
L_{ACC}	25M Long Term Accuracy	Measurement at 1.5V	–	50	ppm
27_M					
T_{DC}	Duty Cycle	Measurement at 1.5V	45	55	%
T_{PERIOD}	Period	Measurement at 1.5V	37.03594	37.03813	ns
T_R/T_F	Rising and Falling Edge Rate	Measured between 0.8V and 2.0V	1.0	4.0	V/ns
T_{CCJ}	Cycle to Cycle Jitter	Measurement at 1.5V	–	500	ps
L_{ACC}	27M Long Term Accuracy	Measurement at 1.5V	–	30	ppm
T_{LTJ} @ 1 µs	27M Long Term Jitter @ 10 µs	Measurement at 1.5V @ 1 µs	–	500	ps
REF					
T_{DC}	REF Duty Cycle	Measurement at 1.5V	45	55	%
T_{PERIOD}	REF Period	Measurement at 1.5V	69.82033	69.86224	ns
$T_{PERIODAbs}$	REF Absolute Period	Measurement at 1.5V	68.83429	70.84826	ns
T_{HIGH}	REF High time	Measurement at 2V	29.97543	38.46654	ns
T_{LOW}	REF Low time	Measurement at 0.8V	29.57543	38.26654	ns
T_R/T_F	REF Rising and Falling Edge Rate	Measured between 0.8V and 2.0V	1.0	4.0	V/ns
T_{SKEW}	REF Clock to REF Clock	Measurement at 1.5V	–	500	ps
T_{CCJ}	REF Cycle to Cycle Jitter	Measurement at 1.5V	–	1000	ps

AC Electrical Specifications (continued)

Parameter	Description	Condition	Min.	Max.	Unit
L_{ACC}	Long Term Accuracy	Measurement at 1.5V	–	100	ppm
ENABLE/DISABLE and SET-UP					
T_{STABLE}	Clock Stabilization from Power-up		–	1.8	ms
T_{SS}	Stopclock Set-up Time		10.0	–	ns

Test and Measurement Set-up

For PCI Single-ended Signals and Reference

The following diagram shows the test load configurations for the single-ended PCI, USB, and REF output signals.

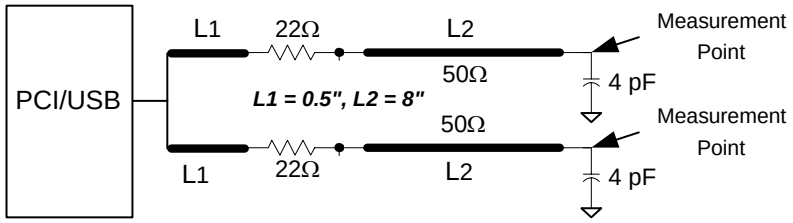


Figure 9. Single-ended PCI and USB Double Load Configuration

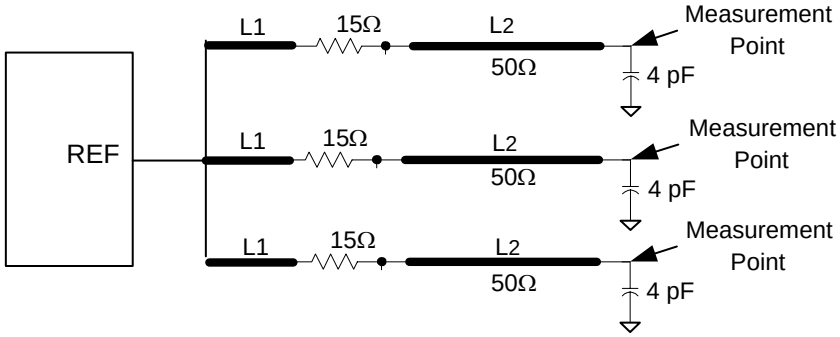


Figure 10. Single-ended REF Triple Load Configuration

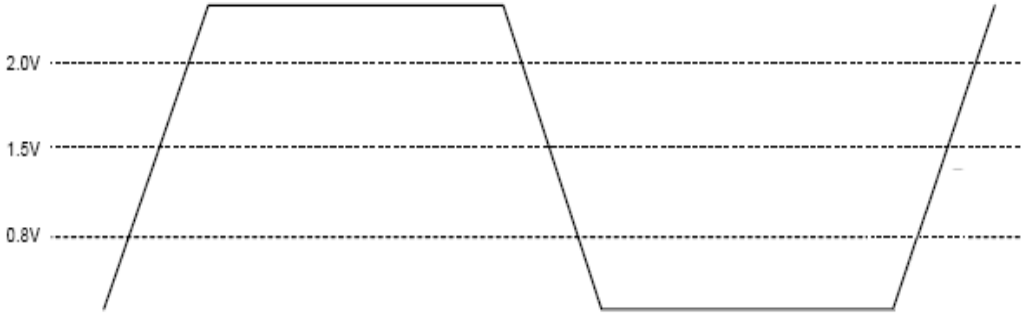


Figure 11. Single-ended Output Signals (for AC Parameters Measurement)

For CPU, SRC, and DOT96 Signals and Reference

The following diagram shows the test load configuration for the differential CPU and SRC outputs.

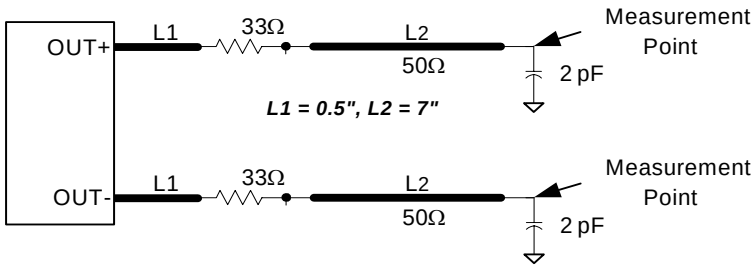


Figure 12. 0.7V Differential Load Configuration

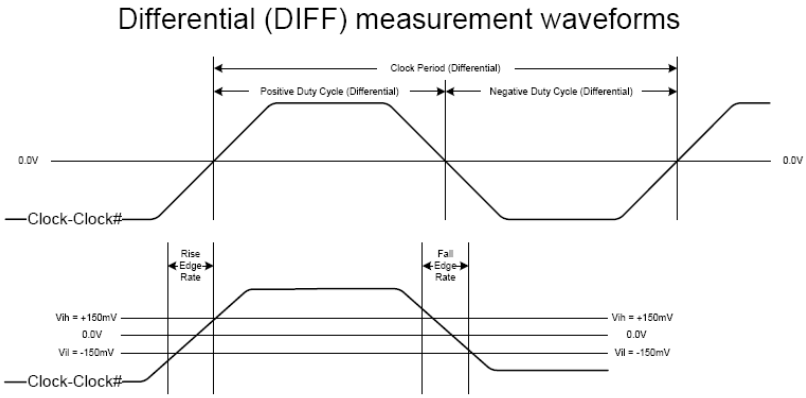


Figure 13. Differential Measurement for Differential Output Signals (for AC Parameters Measuremement

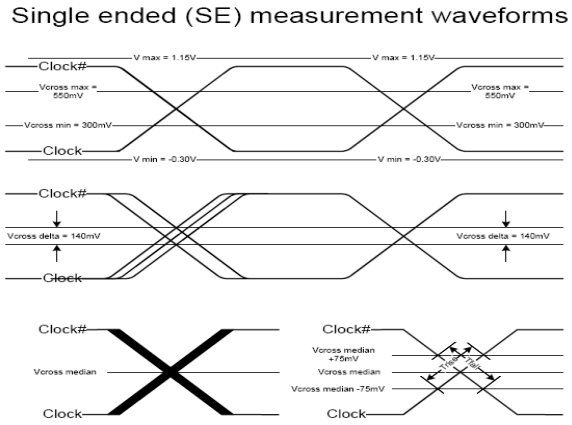


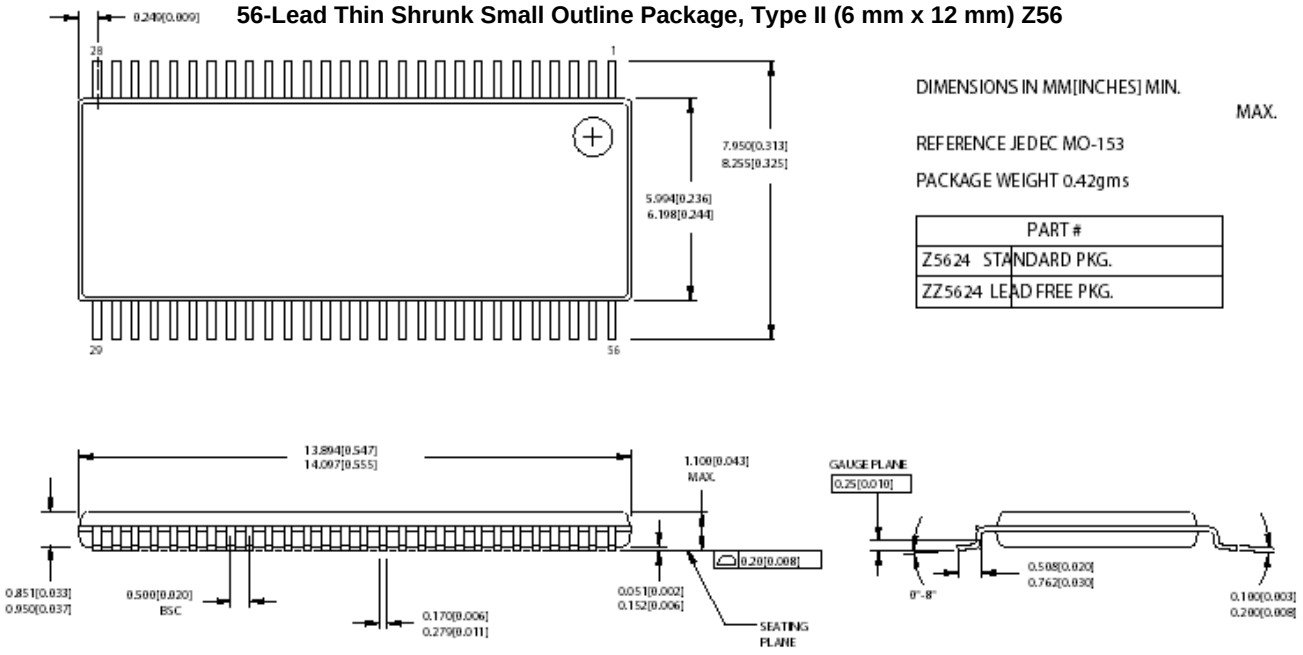
Figure 14. Single-ended Measurement for Differential Output Signals (for AC Parameters Measurement)

Ordering Information

Part Number	Package Type	Product Flow
Lead-free		
SPL505YC256BT	56-pin TSSOP	Commercial, 0° to 85°C
SPL505YC256BTT	56-pin TSSOP–Tape and Reel	Commercial, 0° to 85°C
SPL505YC256BS	56-pin SSOP	Commercial, 0° to 85°C
SPL505YC256BST	56-pin SSOP–Tape and Reel	Commercial, 0° to 85°C

Package Diagram

56-Lead Thin Shrunk Small Outline Package, Type II (6 mm x 12 mm) Z56



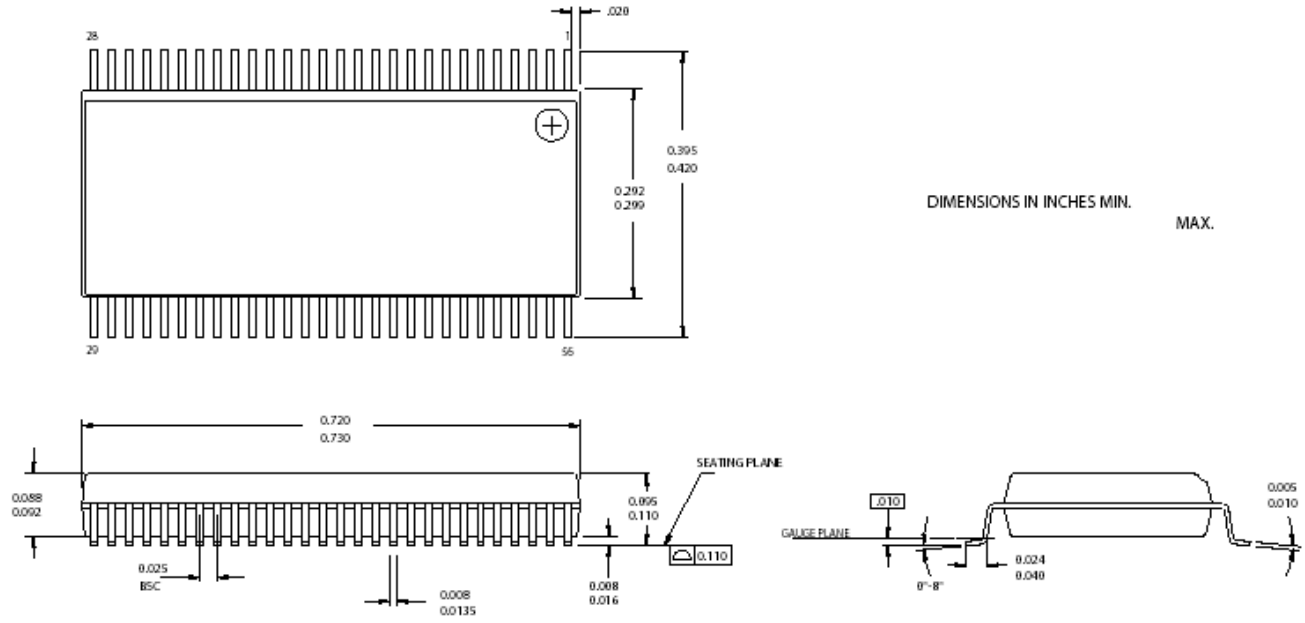
DIMENSIONS IN MM[INCHES] MIN.
MAX.

REFERENCE JEDEC MO-153

PACKAGE WEIGHT 0.42gms

PART #
Z5624 STANDARD PKG.
ZZ5624 LEAD FREE PKG.

56-Lead Shrunk Small Outline Package O56



DIMENSIONS IN INCHES MIN.
MAX.

Document History Page

Document Title: SPL505YC256BT/ SPL505YC256BS Clock Generator for Intel® Bearlake Chipset			
REV.	**Issue Date**	**Orig. of Change**	**Description of Change**
1.0	12/13/06	JMA	New data sheet
1.1	1/30/07	JMA	1. Added SE1/SE2 to pinout in pinout diagram 2. Added clarifications to Byte 11 3. Added new definitions to Byte 13 4. Added PCI3/CFG0 voltage requirements in DC parameters
1.2	2/06/07	JMA	1. Changed Byte11 Bit 0 from 1 to 0; CPU2 to Stopped with CPU_STP# 2. Changed Byte 13 Bit 4 from 1 to 0; SATA spread default off 3. Changed Byte 13 Bit 2 from 0 to 1; SE drive strength default tohigh 4. Changed Byte 13 Bit 1 from 0 to 1; Reserved bit 6. Changed 1394A ppm from +/-100ppm to +/-30ppm 5. Added 1394B 6. Added CPU0 to CPU1 100ps skew spec 7. 25M typo on 1394A removed 8. FSD in overclocking description removed.
1.3	3/06/07	JMA	1. Part number changes due to part revision 2. Revision ID changed from 0000 to 0001 in Byte 7[7:4] 3. Added Byte 18 for additional single-ended drive strength control
1.4	3/21/07	JMA	1. Specified Triangular Spread Spectrum Profile 2. Removed IEEE clocks 3. RESERVED Byte 13 Bit5 - Engineering spread percentage -0.47%