Direct Rambus™ Clock Generator

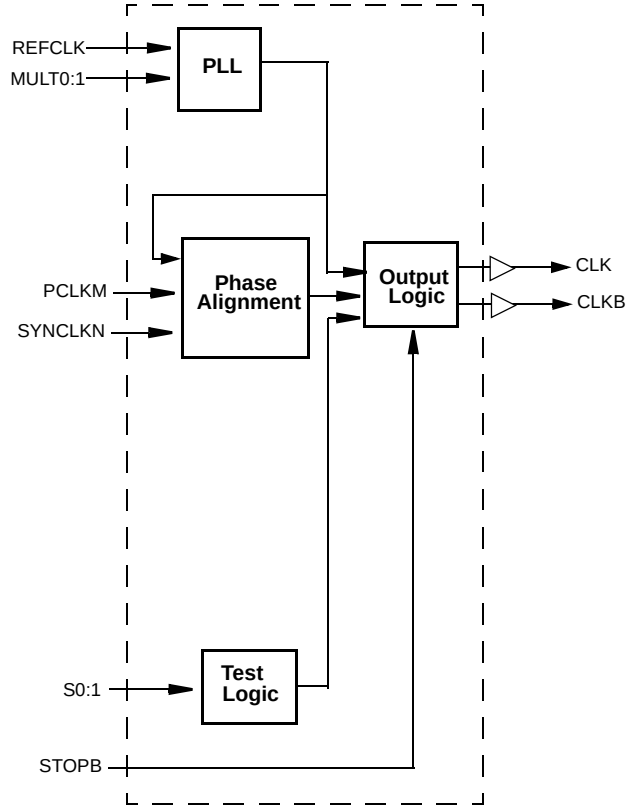
Features

- **Differential clock source for Direct Rambus™ memory subsystem for up to 800-MHz data transfer rate**
- **Provide synchronization flexibility: the Rambus® Channel can optionally be synchronous to an external system or processor clock**
- **Power-managed output allows Rambus Channel clock to be turned off to minimize power consumption for mobile applications**
- **Works with Cypress CY2210, W133, W158, W159, W161, and W167 to support Intel® architecture platforms**
- **Low-power CMOS design packaged in a 24-pin QSOP (150-mil SSOP) package**

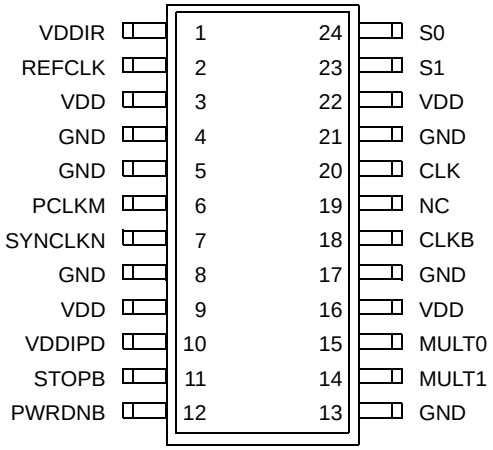
Description

The Cypress W134M/W134S provides the differential clock signals for a Direct Rambus memory subsystem. It includes signals to synchronize the Direct Rambus Channel clock to an external system clock but can also be used in systems that do not require synchronization of the Rambus clock.

Block Diagram



Pin Configuration



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Pin Definitions

Pin Name	No.	Type	Description
REFCLK	2	I	**Reference Clock Input**. Reference clock input, normally supplied by a system frequency synthesizer (Cypress W133).
PCLKM	6	I	**Phase Detector Input**. The phase difference between this signal and SYNCLKN is used to synchronize the Rambus Channel Clock with the system clock. Both PCLKM and SYNCLKN are provided by the Gear Ratio Logic in the memory controller. If Gear Ratio Logic is not used, this pin would be connected to Ground.
SYNCLKN	7	I	**Phase Detector Input**. The phase difference between this signal and PCLKM is used to synchronize the Rambus Channel Clock with the system clock. Both PCLKM and SYNCLKN are provided by the Gear Ratio Logic in the memory controller. If Gear Ratio Logic is not used, this pin would be connected to Ground.
STOPB	11	I	**Clock Output Enable**. When this input is driven to active LOW, it disables the differential Rambus Channel clocks.
PWRDNB	12	I	**Active LOW Power-down**. When this input is driven to active LOW, it disables the differential Rambus Channel clocks and places the W134M/W134S in power-down mode.
MULT 0:1	15, 14	I	**PLL Multiplier Select**. These inputs select the PLL prescaler and feedback dividers to determine the multiply ratio for the PLL for the input REFCLK. MULT0 / MULT1 / W134M PLL/REFCLK / W134S PLL/REFCLK 0 / 0 / 4.5 / 4 0 / 1 / 6 / 6 1 / 1 / 8 / 8 1 / 0 / 5.333 / 5.333
CLK, CLKB	20, 18	O	**Complementary Output Clock**. Differential Rambus Channel clock outputs.
S0, S1	24, 23	I	**Mode Control Input**. These inputs control the operating mode of the W134M/W134S. S0 / S1 / MODE 0 / 0 / Normal 0 / 1 / Output Enable Test 1 / 0 / Bypass 1 / 1 / Test
NC	19	–	**No Connect**
VDDIR	1	RefV	**Reference for REFCLK**. Voltage reference for input reference clock.
VDDIPD	10	RefV	**Reference for Phase Detector**. Voltage reference for phase detector inputs and StopB.
VDD	3, 9, 16, 22	P	**Power Connection**. Power supply for core logic and output buffers. Connected to 3.3V supply.
GND	4, 5, 8, 13, 17, 21	G	**Ground Connection**. Connect all ground pins to the common system ground plane.

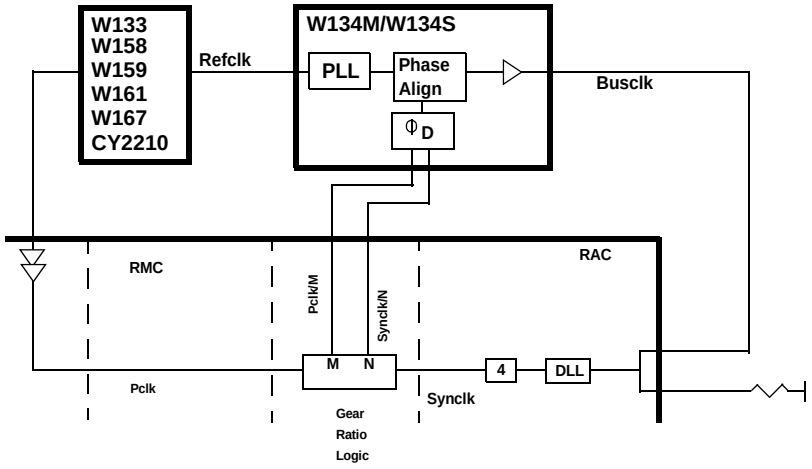


Figure 1. DDLL System Architecture

Key Specifications

Supply Voltage: ..... V_{DD} = 3.3V±0.165V
Operating Temperature: ..... 0°C to +70°C
Input Threshold: ..... 1.5V typical
Maximum Input Voltage: ..... V_{DD}+0.5V
Maximum Input Frequency: ..... 100 MHz
Output Duty Cycle: ..... 40/60% worst case
Output Type: ..... Rambus signaling level (RSL)

DDLL System Architecture and Gear Ratio Logic

Figure 1 shows the Distributed Delay Lock Loop (DDLL) system architecture, including the main system clock source, the Direct Rambus clock generator (DRCG), and the core logic that contains the Rambus Access Cell (RAC), the Rambus Memory Controller (RMC), and the Gear Ratio Logic. (This diagram abstractly represents the differential clocks as a single Busclk wire.)

The purpose of the DDLL is to frequency-lock and phase-align the core logic and Rambus clocks (Pclk and Synclk) at the RMC/RAC boundary in order to allow data transfers without incurring additional latency. In the DDLL architecture, a PLL is used to generate the desired Busclk frequency, while a distributed loop forms a DLL to align the phase of Pclk and Synclk at the RMC/RAC boundary.

The main clock source drives the system clock (Pclk) to the core logic, and also drives the reference clock (Refclk) to the DRCG. For typical Intel architecture platforms, Refclk will be half the CPU front side bus frequency. A PLL inside the DRCG multiplies Refclk to generate the desired frequency for Busclk, and Busclk is driven through a terminated transmission line (Rambus Channel). At the mid-point of the channel, the RAC senses Busclk using its own DLL for clock alignment, followed by a fixed divide-by-4 that generates Synclk.

Pclk is the clock used in the memory controller (RMC) in the core logic, and Synclk is the clock used at the core logic interface of the RAC. The DDLL together with the Gear Ratio Logic enables users to exchange data directly from the Pclk domain to the Synclk domain without incurring additional latency for synchronization. In general, Pclk and Synclk can be of different frequencies, so the Gear Ratio Logic must select the appropriate M and N dividers such that the frequencies of Pclk/M and Synclk/N are equal. In one interesting example, Pclk = 133 MHz, Synclk = 100 MHz, and M = 4 while N = 3, giving Pclk/M = Synclk/N = 33 MHz. This example of the clock waveforms with the Gear Ratio Logic is shown in *Figure 2*.

The output clocks from the Gear Ratio Logic, Pclk/M, and Synclk/N, are output from the core logic and routed to the DRCG Phase Detector inputs. The routing of Pclk/M and Synclk/N must be matched in the core logic as well as on the board.

After comparing the phase of Pclk/M vs. Synclk/N, the DRCG Phase Detector drives a phase aligner that adjusts the phase of the DRCG output clock, Busclk. Since everything else in the distributed loop is fixed delay, adjusting Busclk adjusts the phase of Synclk and thus the phase of Synclk/N. In this manner the distributed loop adjusts the phase of Synclk/N to match that of Pclk/M, nulling the phase error at the input of the DRCG Phase Detector. When the clocks are aligned, data can be exchanged directly from the Pclk domain to the Synclk domain.

Table 1 shows the combinations of Pclk and Busclk frequencies of greatest interest, organized by Gear Ratio.

Table 1. Supported Pclk and Busclk Frequencies, by Gear Ratio

Pclk	Gear Ratio and Busclk			
	2.0	1.5	1.33	1.0
67 MHz				267 MHz
100 MHz			300 MHz	400 MHz
133 MHz	267 MHz	356 MHz	400 MHz	
150 MHz		400 MHz		
200 MHz	400 MHz			

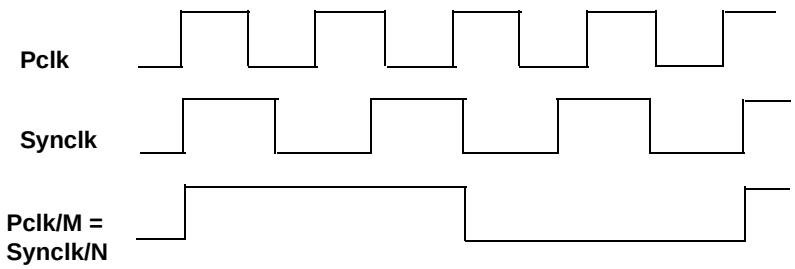


Figure 2. Gear Ratio Timing Diagram

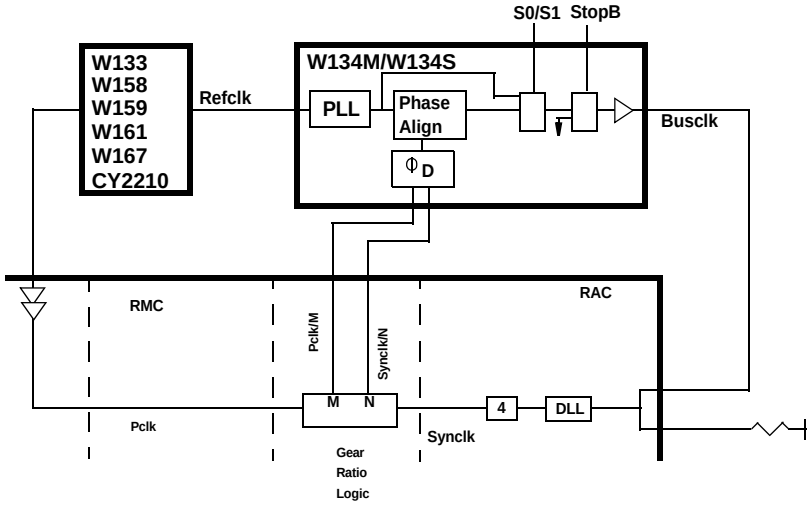


Figure 3. DDLL Including Details of DRCG

Figure 3 shows more details of the DDLL system architecture, including the DRCG output enable and bypass modes.

Phase Detector Signals

The DRCG Phase Detector receives two inputs from the core logic, PclkM (Pclk/M) and SynclkN (Synclk/N). The M and N dividers in the core logic are chosen so that the frequencies of PclkM and SynclkN are identical. The Phase Detector detects the phase difference between the two input clocks, and drives the DRCG Phase Aligner to null the input phase error through the distributed loop. When the loop is locked, the input phase error between PclkM and SynclkN is within the specification $t_{ERR,PD}$ given in the Device Characteristics table after the lock time given in the State Transition Section.

The Phase Detector aligns the rising edge of PclkM to the rising edge of SynclkN. The duty cycle of the phase detector input clocks will be within the specification $DC_{IN,PD}$ given in the Operating Conditions table. Because the duty cycles of the two phase detector input clocks will not necessarily be identical, the falling edges of PclkM and SynclkN may not be aligned when the rising edges are aligned.

The voltage levels of the PclkM and SynclkN signals are determined by the controller. The pin VDDIPD is used as the voltage reference for the phase detector inputs and should be connected to the output voltage supply of the controller. In some applications, the DRCG PLL output clock will be used directly, by bypassing the Phase Aligner. If PclkM and SynclkN are not used, those inputs must be grounded.

Selection Logic

Table 2 shows the logic for selecting the PLL prescaler and feedback dividers to determine the multiply ratio for the PLL from the input Refclk. Divider A sets the feedback and divider B sets the prescaler, so the PLL output clock frequency is set by: PLLclk = Refclk*A/B.

Table 2. PLL Divider Selection

Mult0	Mult1	W134M		W134S	
		A	B	A	B
0	0	9	2	4	1
0	1	6	1	6	1
1	1	8	1	8	1
1	0	16	3	16	3

Table 3 shows the logic for enabling the clock outputs, using the StopB input signal. When StopB is HIGH, the DRCG is in its normal mode, and Clk and ClkB are complementary outputs following the Phase Aligner output (PAclk). When StopB is LOW, the DRCG is in the Clk Stop mode, the output clock drivers are disabled (set to Hi-Z), and the Clk and ClkB settle to the DC voltage $V_{X,STOP}$ as given in the Device Characteristics table. The level of $V_{X,STOP}$ is set by an external resistor network.

Table 3. Clock Stop Mode Selection

Mode	StopB	Clk	ClkB
Normal	1	PAclk	PAclkB
Clk Stop	0	$V_{X,STOP}$	$V_{X,STOP}$

Table 4 shows the logic for selecting the Bypass and Test modes. The select bits, S0 and S1, control the selection of these modes. The Bypass mode brings out the full-speed PLL output clock, bypassing the Phase Aligner. The Test mode brings the Refclk input all the way to the output, bypassing both the PLL and the Phase Aligner. In the Output Test mode (OE), both the Clk and ClkB outputs are put into a high-impedance state (Hi-Z). This can be used for component testing and for board-level testing.

Table 4. Bypass and Test Mode Selection

Mode	S0	S1	Bypclk (int.)	Clk	ClkB
Normal	0	0	Gnd	PAclk	PAclkB
Output Test (OE)	0	1	–	Hi-Z	Hi-Z
Bypass	1	0	PLLclk	PLLclk	PLLclkB
Test	1	1	Refclk	Refclk	RefclkB

Table 5 shows the logic for selecting the Power-down mode, using the PwrDnB input signal. PwrDnB is active LOW (enabled when 0). When PwrDnB is disabled, the DRCG is in its normal mode. When PwrDnB is enabled, the DRCG is put into a powered-off state, and the Clk and ClkB outputs are three-stated.

Table 5. Power-down Mode Selection

Mode	PwrDnB	Clk	ClkB
Normal	1	PAclk	PAclkB
Power-down	0	GND	GND

Table of Frequencies and Gear Ratios

Table 6 shows several supported Pclk and Busclk frequencies, the corresponding A and B dividers required in the DRCG PLL, and the corresponding M and N dividers in the gear ratio logic. The column Ratio gives the Gear Ratio as defined Pclk/Synclk (same as M and N). The column F@PD gives the divided down frequency (in MHz) at the Phase Detector, where F@PD = Pclk/M = Synclk/N.

State Transitions

The clock source has three fundamental operating states. *Figure 4* shows the state diagram with each transition labelled A through H. Note that the clock source output may NOT be glitch-free during state transitions.

Upon powering up the device, the device can enter any state, depending on the settings of the control signals, PwrDnB and StopB.

In Power-down mode, the clock source is powered down with the control signal, PwrDnB, equal to 0. The control signals S0 and S1 must be stable before power is applied to the device, and can only be changed in Power-down mode (PwrDnB = 0). The reference inputs, V_{DDR} and V_{DDPD}, may remain on or may be grounded during the Power-down mode.

Table 6. Examples of Frequencies, Dividers, and Gear Ratios

Pclk	Refclk	Busclk	Synclk	A	B	M	N	Ratio	F@PD
67	33	267	67	8	1	2	2	1.0	33
100	50	300	75	6	1	8	6	1.33	12.5
100	50	400	100	8	1	4	4	1.0	25
133	67	267	67	4	1	4	2	2.0	33
133	67	400	100	6	1	8	6	1.33	16.7

The control signals Mult0 and Mult1 can be used in two ways. If they are changed during Power-down mode, then the Power-down transition timings determine the settling time of the DRCG. However, the Mult0 and Mult1 control signals can also be changed during Normal mode. When the Mult control signals are “hot-swapped” in this manner, the Mult transition timings determine the settling time of the DRCG.

In Normal mode, the clock source is on, and the output is enabled.

Table 7 lists the control signals for each state.

Table 7. Control Signals for Clock Source States

State	PwrDnB	StopB	Clock Source	Output Buffer
Power-down	0	X	OFF	Ground
Clock Stop	1	0	ON	Disabled
Normal	1	1	ON	Enabled

Figure 5 shows the timing diagrams for the various transitions between states, and *Table 8* specifies the latencies of each state transition. Note that these transition latencies assume the following.

Refclk input has settled and meets specification shown in the Operating Conditions table.

The Mult0, Mult1, S0 and S1 control signals are stable.

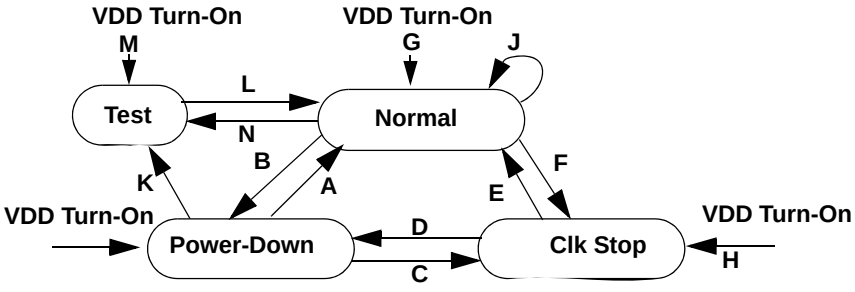
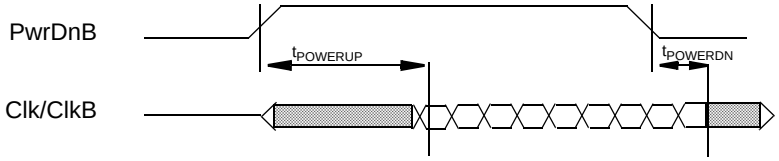


Figure 4. Clock Source State Diagram

Timing Diagrams

Power-down Exit and Entry



Output Enable Control

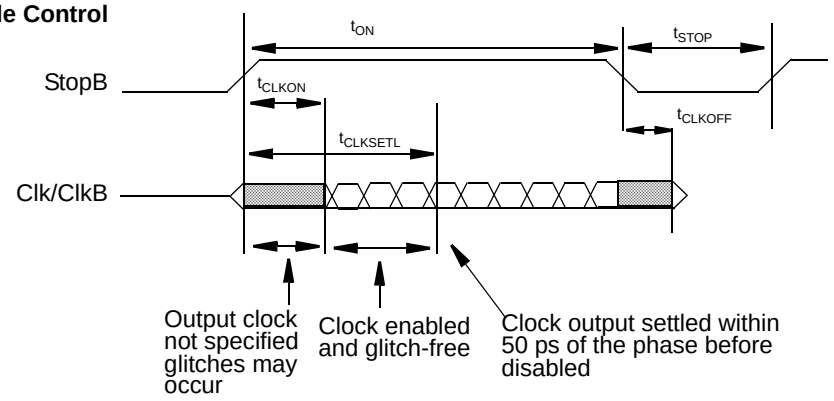


Figure 5. State Transition Timing Diagrams

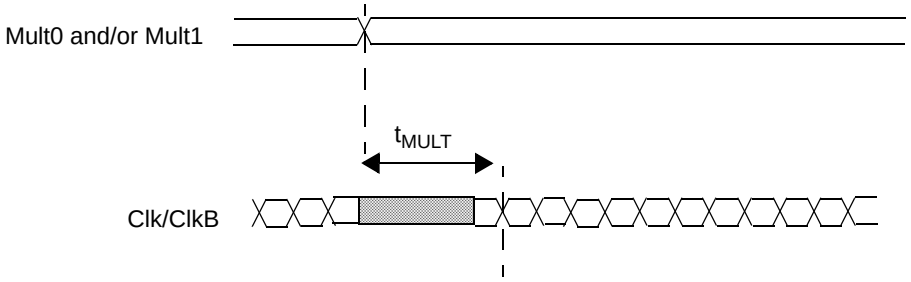


Figure 6. Multiply Transition Timing

Table 8. State Transition Latency Specifications

Transition	From	To	Transition Latency		Description
			Parameter	Max.	
A	Power-down	Normal	$t_{POWERUP}$	3 ms	Time from PwrDnB to Clk/ClkB output settled (excluding $t_{DISTLOCK}$).
C	Power-down	Clk Stop	$t_{POWERUP}$	3 ms	Time from PwrDnB until the internal PLL and clock has turned ON and settled.
K	Power-down	Test	$t_{POWERUP}$	3 ms	Time from PwrDnB to Clk/ClkB output settled (excluding $t_{DISTLOCK}$).
G	V_{DD} ON	Normal	$t_{POWERUP}$	3 ms	Time from V_{DD} is applied and settled until Clk/ClkB output settled (excluding $t_{DISTLOCK}$).
H	V_{DD} ON	Clk Stop	$t_{POWERUP}$	3 ms	Time from V_{DD} is applied and settled until internal PLL and clock has turned ON and settled.
M	V_{DD} ON	Test	$t_{POWERUP}$	3 ms	Time from V_{DD} is applied and settled until internal PLL and clock has turned ON and settled.
J	Normal	Normal	t_{MULT}	1 ms	Time from when Mult0 or Mult1 changed until Clk/ClkB output resettled (excluding $t_{DISTLOCK}$).

Table 8. State Transition Latency Specifications (continued)

Transition	From	To	Transition Latency		Description
			Parameter	Max.	
E	Clk Stop	Normal	t_{CLKON}	10 ns	Time from StopB until Clk/ClkB provides glitch-free clock edges.
E	Clk Stop	Normal	$t_{CLKSETL}$	20 cycles	Time from StopB to Clk/ClkB output settled to within 50 ps of the phase before CLK/CLKB was disabled.
F	Normal	Clk Stop	t_{CLKOFF}	5 ns	Time from StopB to Clk/ClkB output disabled.
L	Test	Normal	t_{CTL}	3 ms	Time from when S0 or S1 is changed until CLK/CLKB output has resettled (excluding $t_{DISTLOCK}$).
N	Normal	Test	t_{CTL}	3 ms	Time from when S0 or S1 is changed until CLK/CLKB output has resettled (excluding $t_{DISTLOCK}$).
B,D	Normal or Clk Stop	Power-down	$t_{POWERDN}$	1 ms	Time from PwrDnB to the device in Power-down.

Figure 5 shows that the Clk Stop to Normal transition goes through three phases. During t_{CLKON}, the clock output is not specified and can have glitches. For $t_{CLKON} < t < t_{CLKSETL}$, the clock output is enabled and must be glitch-free. For $t > t_{CLKSETL}$, the clock output phase must be settled to within 50 ps of the phase before the clock output was disabled. At this time, the clock output must also meet the voltage and timing specifications of the Device Characteristics table. The outputs are in a high-impedance state during the Clk Stop mode.

Table 9. Distributed Loop Lock Time Specification

Parameter	Description	Min.	Max.	Unit
$t_{DISTLOCK}$	Time from when Clk/ClkB output is settled to when the phase error between SynclkN and PclkM falls within the $t_{ERR,PD}$ spec in *Table* .		5	ms

Table 10.Supply and Reference Current Specification

Parameter	Description	Min.	Max.	Unit
$I_{POWERDOWN}$	“Supply” current in Power-down state (PwrDnB 1 = 0)	–	250	µA
$I_{CLKSTOP}$	“Supply” current in Clk Stop state (StopB = 0)	–	65	mA
I_{NORMAL}	“Supply” current in Normal state (StopB = 1, PwrDnB = 1)	–	100	mA
$I_{REF,PWDN}$	Current at VDDIR or VDDIPD reference pin in Power-down state (PwrDnB = 0)	–	50	µA
$I_{REF,NORM}$	Current at VDDIR or VDDIPD reference pin in Normal or Clk Stop state (PwrDnB = 1)	–	2	mA

Absolute Maximum Conditions[1]

Parameter	Description	Min.	Max.	Unit
$V_{DD, ABS}$	Max. voltage on V_{DD} with respect to ground	–0.5	4.0	V
$V_{I, ABS}$	Max. voltage on any pin with respect ground	–0.5	V_{DD} + 0.5	V

External Component Values[2]

Parameter	Description	Min.	Max.	Unit
R_S	Serial Resistor	39	±5%	Ω
R_P	Parallel Resistor	51	±5%	Ω
C_F	Edge Rate Filter Capacitor	4–15[3]	±10%	pF
C_{MID}	AC Ground Capacitor	470 pF	0.1 µF	±20%

Operating Conditions[4]

Parameter	Description	Min.	Max.	Unit
V_{DD}	Supply Voltage	3.135	3.465	V
T_A	Ambient Operating Temperature	0	70	°C
$t_{CYCLE,IN}$	Refclk Input Cycle Time	10	40	ns
$t_{J,IN}$	Input Cycle-to-Cycle Jitter[5]	–	250	ps
DC_{IN}	Input Duty Cycle over 10,000 Cycles	40	60	$\%t_{CYCLE}$
FM_{IN}	Input Frequency of Modulation	30	33	kHz
PM_{IN}[6]	Modulation Index for Triangular Modulation	–	0.6	%
	Modulation Index for Non-Triangular Modulation	–	0.5[8]	%
$t_{CYCLE,PD}$	Phase Detector Input Cycle Time at PclkM & SynclkN	30	100	ns
$t_{ERR,INIT}$	Initial Phase error at Phase Detector Inputs	–0.5	0.5	$t_{CYCLE,PD}$
$DC_{IN,PD}$	Phase Detector Input Duty Cycle over 10,000 Cycles	25	75	$t_{CYCLE,PD}$
$t_{I,SR}$	Input Slew Rate (measured at 20%-80% of input voltage) for PclkM, SynclkN, and Refclk	1	4	V/ns
$C_{IN,PD}$	Input Capacitance at PclkM, SynclkN, and Refclk[7]	–	7	pF
$DC_{IN,PD}$	Input Capacitance matching at PclkM and SynclkN[7]	–	0.5	pF
$C_{IN,CMOS}$	Input Capacitance at CMOS pins (excluding PclkM, SynclkN, and Refclk)[7]	–	10	pF
V_{IL}	Input (CMOS) Signal Low Voltage	–	0.3	VDD
V_{IH}	Input (CMOS) Signal High Voltage	0.7	–	VDD
$V_{IL,R}$	Refclk input Low Voltage	–	0.3	V_{DDIR}
$V_{IH,R}$	Refclk input High Voltage	0.7	–	V_{DDIR}
$V_{IL,PD}$	Input Signal Low Voltage for PD Inputs and StopB	–	0.3	V_{DDIPD}
$V_{IH,PD}$	Input Signal High Voltage for PD Inputs and StopB	0.7	–	V_{DDIPD}
V_{DDIR}	Input Supply Reference for Refclk	1.235	3.465	V
V_{DDIPD}	Input Supply Reference for PD Inputs	1.235	2.625	V

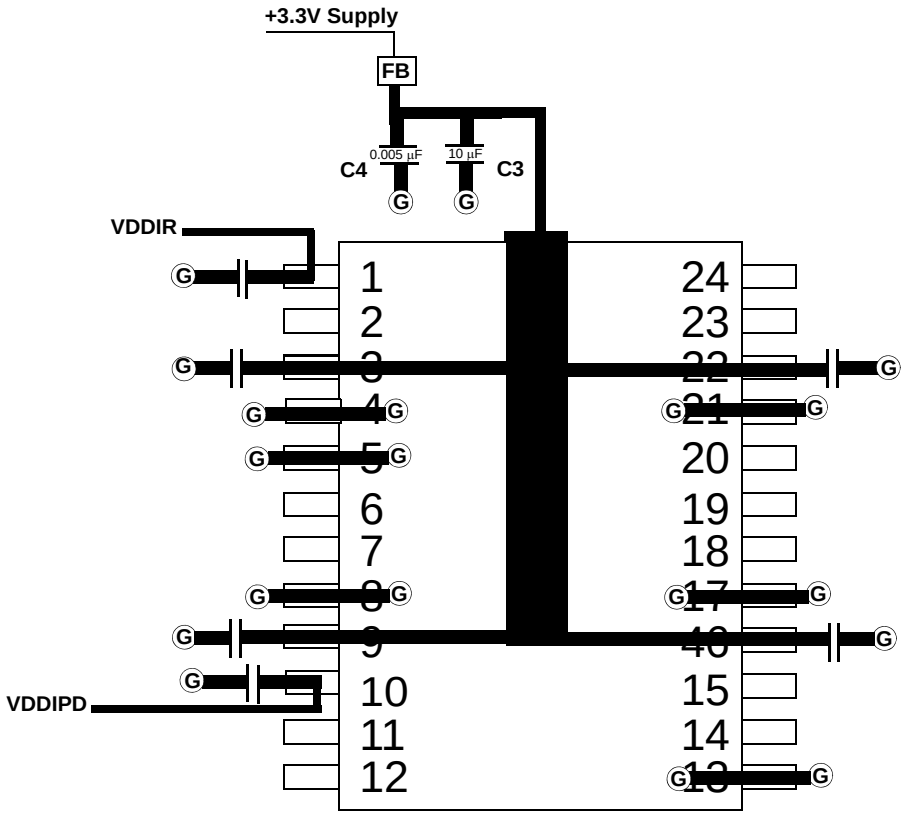
Notes:
1. Represents stress ratings only, and functional operation at the maximums is not guaranteed.
2. Gives the nominal values of the external components and their maximum acceptable tolerance, assuming Z_{CH} = 28Ω.
3. Do not populate C_F. Leave pads for future use.
4. Multiple Supplies: The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.
5. Refclk jitter measured at V_{DDIR} (nom)/2.
6. If input modulation is used: input modulation is allowed but not required.
7. Capacitance measured at Freq=1 MHz, DC bias = 0.9V and V_{AC} < 100 mV.
8. The amount of allowed spreading for any non-triangular modulation is determined by the induced downstream tracking skew, which cannot exceed the skew generated by the specified 0.6% triangular modulation. Typically, the amount of allowed non-triangular modulation is about 0.5%.

Device Characteristics

Parameter	Description	Min.	Max.	Unit
t_{CYCLE}	Clock Cycle Time	2.5	3.75	ns
t_J	Cycle-to-Cycle Jitter at Clk/ClkB[9]	–	60	ps
	Total Jitter over 2, 3, or 4 Clock Cycles[9]	–	100	ps
	266-MHz Cycle-to-Cycle Jitter[10]	–	100	ps
	266-MHz Total Jitter over 2, 3, or 4 Clock Cycles[10]	–	160	ps
t_{STEP}	Phase Aligner Phase Step Size (at Clk/ClkB)	1	–	ps
$t_{ERR,PD}$	Phase Detector Phase Error for Distributed Loop Measured at PclkM-SynclkN (rising edges) (does not include clock jitter)	–100	100	ps
$t_{ERR,SSC}$	PLL Output Phase Error when Tracking SSC	–100	100	ps
$V_{X,STOP}$	Output Voltage during Clk Stop (StopB=0)	1.1	2.0	V
V_X	Differential Output Crossing-Point Voltage	1.3	1.8	V
V_{COS}	Output Voltage Swing (p-p single-ended)[11]	0.4	0.6	V
V_{OH}	Output High Voltage	–	2.0	V
V_{OL}	Output Low voltage	1.0	–	V
r_{OUT}	Output Dynamic Resistance (at pins)[12]	12	50	Ω
I_{OZ}	Output Current during Hi-Z (S0 = 0, S1 = 1)	–	50	µA
$I_{OZ,STOP}$	Output Current during Clk Stop (StopB = 0)	–	500	µA
DC	Output Duty Cycle over 10,000 Cycles	40	60	$\%t_{CYCLE}$
$t_{DC,ERR}$	Output Cycle-to-Cycle Duty Cycle Error	–	50	ps
t_R, t_F	Output Rise and Fall Times (measured at 20%–80% of output voltage)	250	500	ps
$t_{CR,CF}$	Difference between Output Rise and Fall Times on the Same Pin of a Single Device (20%–80%)	–	100	ps

Notes:
9. Output Jitter spec measured at t_{CYCLE} = 2.5 ns.
10. Output Jitter Spec measured at t_{CYCLE} = 3.75 ns.
11. $V_{COS} = V_{OH} – V_{OL}$.
12. $r_{OUT} = DV_O / D I_O$. This is defined at the output pins.

Layout Example



Internal Power Supply Plane

FB = Dale ILB1206 - 300 (300Ω @ 100 MHz)

Ⓖ = VIA to GND plane layer

All Bypass cap = 0.1 Ceramic XR7

Ordering Information

Ordering Code	Package Type
W134H	24-pin QSOP (150 mils, SSOP)
W134HT	24-pin QSOP (150 mils, SSOP) – Tape and Reel
W134SH	24-pin QSOP (150 mils, SSOP)
W134SHT	24-pin QSOP (150 mils, SSOP) – Tape and Reel
Lead-free	
CYW134MOXC	24-pin QSOP (150 mils, SSOP)
CYW134MOXCT	24-pin QSOP (150 mils, SSOP), Tape and Reel
CYW134SOXC	24-pin QSOP (150 mils, SSOP)
CYW134SOXCT	24-pin QSOP (150 mils, SSOP), Tape and Reel

Package Diagram

24-Lead Quarter Size Outline Q13