Title	***Reference Design Report for a 5 W Dimmable Power Factor Corrected LED Driver (Non-Isolated) Using LinkSwitch™-PL LNK457DG***
Specification	90 VAC – 265 VAC, >0.9 PF Input; 12 V – 18 V, 350 mA ±8% Output
Application	LED Driver for A19 Incandescent Lamp Replacement
Author	Applications Engineering Department
Document Number	RDR-251
Date	February 15, 2011
Revision	1.92

Summary and Features

- Single stage power factor correction and accurate constant current (CC) output
- Low cost, low component count and small PCB footprint solution
- Superior performance and end user experience
  - >100:1 dimming range even with low cost leading edge TRIAC dimmers
  - Clean monotonic start-up – no output blinking
  - Fast start-up (<300 ms) – no perceptible delay
  - Consistent dimming performance unit to unit
- Highly energy efficient
  - >73% at 115 VAC / 230 VAC (dimmable configuration)
  - >78% at 115 VAC / 230 VAC (non-dimmable configuration)
- Integrated protection and reliability features
  - Output open-circuit protected / output short-circuit protected with auto-recovery
  - Auto-recovering thermal shutdown with large hysteresis protects both components and printed circuit board
  - No damage during brown out conditions
  - Extended pin creepage distance between device DRAIN pin and other pins for reliable operation in high pollution and humid environments
- Meets IEC ringwave and EN55015 conducted EMI
- PF >0.9 at 115 VAC / 230 VAC
- %ATHD <10% at 115 VAC and <15% at 230 VAC
- Meets EN61000-3-2 harmonics contents

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Table of Contents

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Important Note:
This board is designed for non-isolated application and the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

This document is an engineering report describing a non-isolated LED driver (power supply) utilizing a LNK457DG from the LinkSwitch-PL family of devices.

The RD-251 provides a single constant current output of 350 mA over an LED string voltage of 12 V and 18 V. The output current can be reduced using a standard AC mains TRIAC dimmer down to 1% (3 mA) without instability and flickering of the LED load. The board is compatible with both low cost leading edge and more sophisticated trailing edge dimmers.

The board was optimized to operate over the universal AC input voltage range (85 VAC to 265 VAC, 47 Hz to 63 Hz) but suffers no damage over an input range of 0 VAC to 300 VAC. This increases field reliability and lifetime during line sags and swells. LinkSwitch-PL based designs provide a high power factor (>0.9) meeting current international requirements and enabling a single design to be used worldwide.

The form factor of the board was chosen to meet the requirements for standard pear shaped (A19) LED replacement lamps. The output is non-isolated and requires the mechanical design of the enclosure to isolate the output of the supply and the LED load from the user.

The document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data.

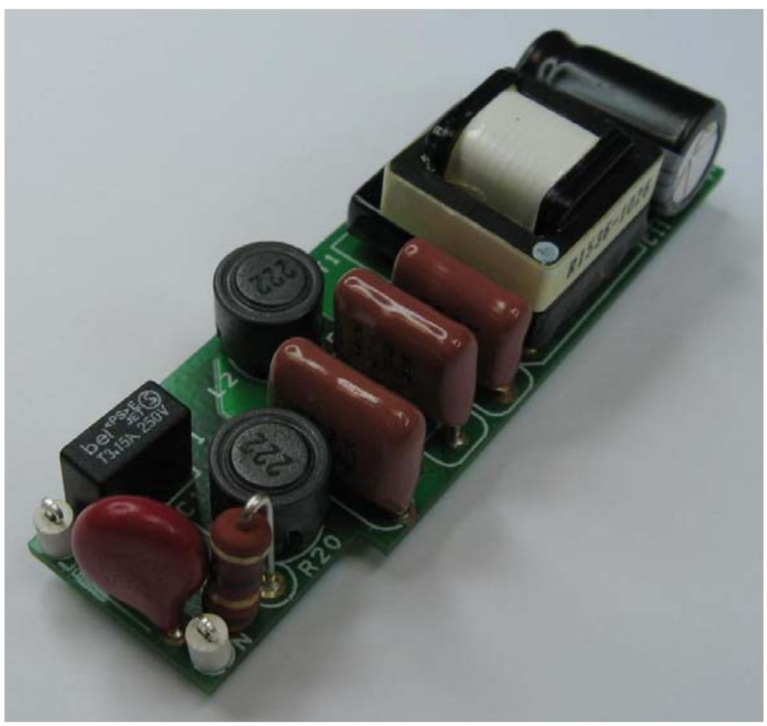

Figure 1 – Populated Circuit Board Photograph (Top).

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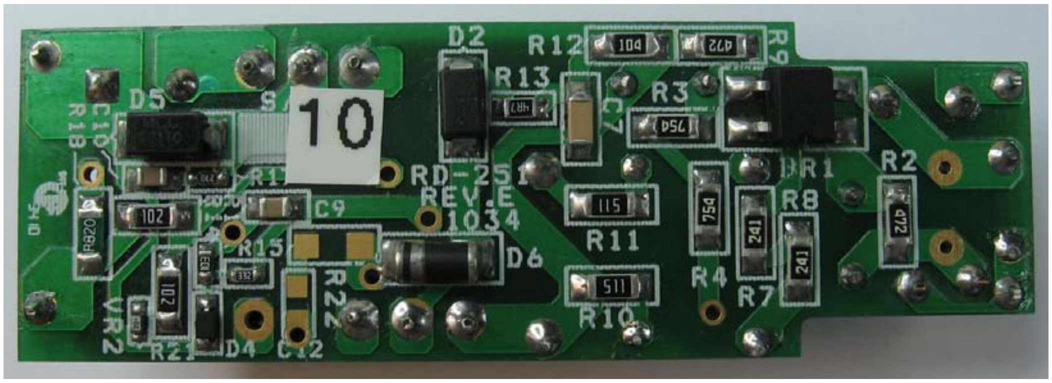

Figure 2 – Populated Circuit Board Photograph (Bottom).

Figure 3 – Example of RD-251 Used in an A19 LED Replacement Lamp (board removed from housing).

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	$V_{IN(NOM)}$		115/230		VAC	Nominal line voltages
	$V_{IN(EXT)}$	90		265	VAC	Normal operating range
	$V_{IN(ND)}$	0		300	VAC	Voltage range over which no damage to the supply shall occur
Frequency	f_{LINE}	47	50/60	63	Hz	
Output						
Output Voltage	V_{OUT}	12	15	18	V	Thermal results were verified with 15 V LED string
Output Current	$I_{OUT(N)}$	322	350	378	mA	(+/-8%) at $V_{IN(NOM)}$ after reaching thermal equilibrium
	$I_{OUT(E)}$	315	350	385	mA	(+/-10%) Extended 90-265 VAC Input, -20 °C to 80 °C
Output Power	P_{OUT}		5		W	
Efficiency						
Dimmable configuration	η		73		%	Measured at P_{OUT} 25 °C
Non-dimmable configuration			78			
Environmental						
Conducted EMI		Meets CISPR22B / EN55015				Mounted into A19 metal finned enclosure and measured on ground plane (to simulate end application)
%ATHD 230 V		< 18				
Safety		Non-isolated				
Line Surge Differential Mode (L1-L2)				500	V	1.2/50 µs surge, IEC 1000-4-5, Series Impedance: Differential Mode: 2 Ω
Ring Wave (100 kHz) Differential Mode (L1-L2)				2500	V	200 A short-circuit Series Impedance: Differential Mode
Dimensions						0.83” (20.86 mm) x 2.52” (63.9 mm)
Board Level Ambient Temperature	T_{AMB}	-20		80	°C	Free convection, sea level

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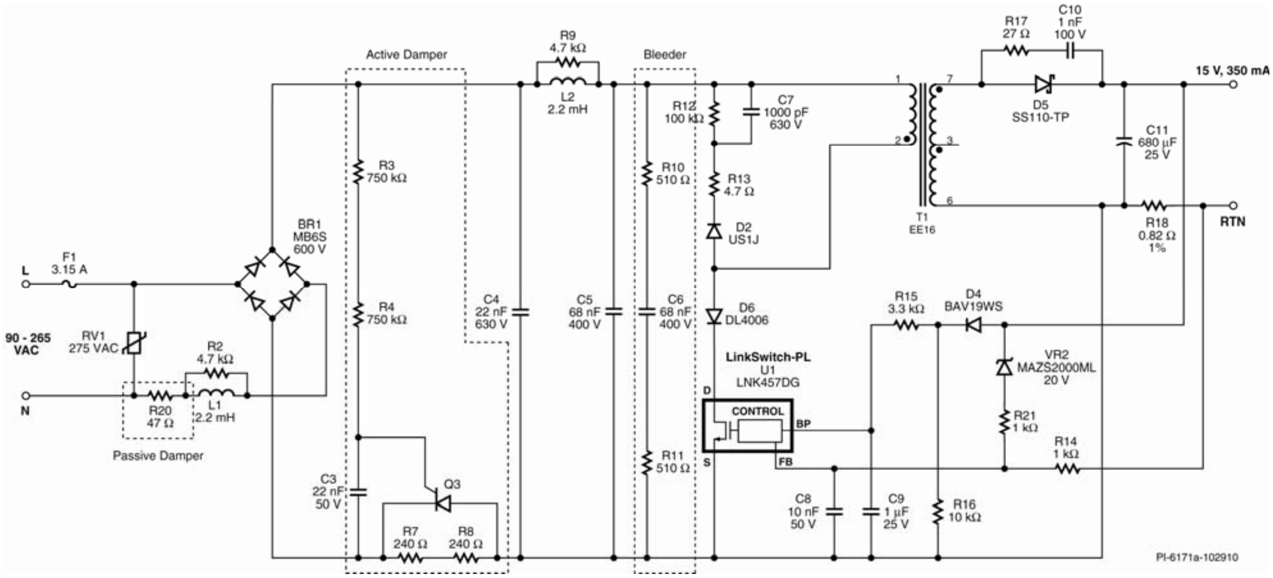
3 Schematic



Note:

C1, R22 and C12 are not populated.

For non-dimming application, the Active Damper and Bleeder blocks can be removed allowing the following parts can be deleted: Q3, R20, R3, R4, R10, R11 C6 and C3. Replace 0Ω for the following locations: R7, R8, and R20.

For high line only application and to match high leakage dimmer such as REV 300 W, Busch 2250 (600 W) or alike the following parts can be tuned. Replace F1 to 47 Ω / 2 W fusible resistors, R7 and R8 to 20Ω, C6 to 220 nF, R10 and R11 to 510 Ω / 0.5 W minimum, C3 to 150nF and R16 to 1 kΩ / 0.25 W.

Figure 4 – Schematic (highlighted blocks may be removed for non-dimming applications.)

4 Circuit Description

This circuit is configured as non-isolated discontinuous flyback converter designed to drive LED strings at voltages of 12 V to 18 V with an output current of 350 mA. The driver is guaranteed to operate across a wide range input voltage range and provide high power factor. The circuit meets both line surge and EMI requirements and the low component count allows board dimensions required for LED bulb replacement applications.

4.1 Dimming Performance Circuit Design Considerations

The requirement to provide output dimming with low cost, TRIAC base, leading edge phase dimmers introduces a number of trade offs in the design.

Due to the much lower power consumed by LED based lighting the line current drawn by the overall lamp is typically below the holding current of the TRIAC within the dimmer. This causes undesirable behaviors such as limited dim range and/or flickering. The relatively large impedance the LED driver presents to the line allows significant ringing to occur when the TRIAC turns on. At the instant the TRIAC conducts, a large inrush current flows into the input capacitance of the driver, exciting the line inductance and causing current ringing. This too can cause similar undesirable behavior as the ringing may cause the TRIAC current to fall to zero and turn off, also generating flicker.

To overcome these issues the circuit includes two circuit blocks labeled active damper and bleeder. The drawback of these blocks is increased dissipation and therefore reduced efficiency of the supply.

The values used for the damper and bleeder in this design allow correct operation of a single board with the widest range of ≤600 W dimmer models including low cost leading edge TRIAC models across the full input voltage range. The trade off decision was to give flicker free operation for a single lamp connected to a dimmer operating at high line.

A single lamp operating at high line results in the lowest current drawn from the line and the highest inrush current (when the TRIAC fires) and represents the worst case. As a result the active damper and bleeder networks were designed to be aggressive; lower impedance for the bleeder and higher impedance for the damper. This increases dissipation and therefore lowers efficiency of the driver and efficacy of the overall system.

Requiring multiple lamps to be connected to a single dimmer for correct operation reduces the current required through the bleeder, allowing increasing the values of R10 and R11 and reducing the value of C6.

Limiting operation to low line only (85 VAC to 132 VAC) allows the values of R7 and R8 to be reduced as the peak currents that occur when a leading edge dimmer TRIAC fires are significantly lower.

Both changes reduce dissipation and improve efficiency.

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For non-dimming application these components can simply be omitted and jumpers used to replace R7 and R8 giving higher efficiency with no change in other performance characteristics.

4.2 Input EMI Filtering and Input Rectification

The EMI filter was optimized to minimize the impact on dimming performance. Resistor R20 is a fusible resistor. Fusible types are selected to fail open-circuit should a component failure cause excessive input current. Film types (vs. wirewound) are acceptable compared to a non or passive PFC solution. This reduces the instantaneous dissipation as the input capacitance charges, however, a 2 w rating is recommended for designed that operate at high line. In addition they limit the inrush current caused when a phase leading TRIAC dimmer turns on and capacitors C4 and C5 charge. The worst case condition (maximum inrush current) occurs when the TRIAC turns on at 90 or 270 degrees, which correspond to the peaks of the AC waveform. Finally they act to damp any current ringing between the AC line impedance and the input stage of the supply again caused by the inrush current when leading edge TRIAC dimmers turn on.

Two differential pi (π) filter EMI stages are used with C1, R2, L1 and C2 forming one stage and C4, L2, R9 and C5 the second. It was found during testing that C1 was not required to meet conducted EMI limits and was therefore not populated.

The incoming AC is rectified by BR1 and filtered by C4 and C5. The total effective input capacitance, the sum of C4, C5 and C6, was selected to assure correct zero crossing detection of the AC input by the LinkSwitch-PL device, necessary correct operation and best performance during dimming.

4.3 Active Damper

The active damper network is used to limit the inrush current, associated voltage spikes and ringing when the TRIAC within a dimmer turns on. This connects a resistance (R7 and R8) in series with the input rectifier for a short period of each AC half-cycle, it is then bypassed for the remainder of the AC cycle by a parallel SCR (Q3). Resistor R3, R4 and C3 determines the delay before the turn-on of Q3.

4.4 Bleeder

Resistor R10, R11 and C6 form a bleeder network which ensures the initial input current is high enough meet the TRIAC holding current requirement, especially during small TRIAC conduction angles.

For non-dimming application, both the active damper and bleeder network may be removed. To achieve this, the following parts can be deleted: Q3, R20, R3, R4, R10, R11, C6 and C3. Replace 0Ω for the following locations: R7, R8, and R20.

4.5 LinkSwitch-PL Primary

The LNK457DG device (U1) incorporates the power switching device, oscillator, output constant current control, start-up, and protection functions. The integrated 725 V MOSFET provides extended voltage margin and ensures high reliability even during line surge events. The device is powered from the BYPASS pin via the decoupling capacitor C9. At start-up, C9 is charged by U1 from an internal current source via the DRAIN pin and then during normal operation it is supplied by the output via R15 and D4.

The rectified and filtered input voltage is applied to one end of the primary winding of T1. The other side of the transformer's primary winding is driven by the integrated MOSFET in U1. The leakage inductance drain voltage spike is limited by an RCD-R clamp consisting of D2, R13, R12, and C7.

Diode D6 is used to protect the IC from negative ringing (drain voltage ringing below source voltage) when the MOSFET is off due to the reflected output voltage exceeding the DC bus voltage, the result of minimal input capacitance to give high power factor.

4.6 Output Rectification

The secondary of the transformer is rectified by D5 and filtered by C11. A Schottky barrier type was selected for higher efficiency. As C11 provides energy storage during AC zero crossings its value determines the magnitude of the line frequency output ripple (2 x f_L due to full wave rectification). The value may therefore be adjusted based on the desired output ripple. For the 680 μF value shown the output ripple is ±50% of I_O. Resistor R17 and C10 damp high frequency ringing and improve conducted and radiated EMI.

4.7 Output Feedback

The CC mode set-point is determined by the voltage drop that appears across R18 which is then fed to the FB pin of U1. Output overvoltage protection is provided by VR2 and R14 (the effect of R14 on the current sense signal in negligible and can be ignored).

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5 PCB Layout

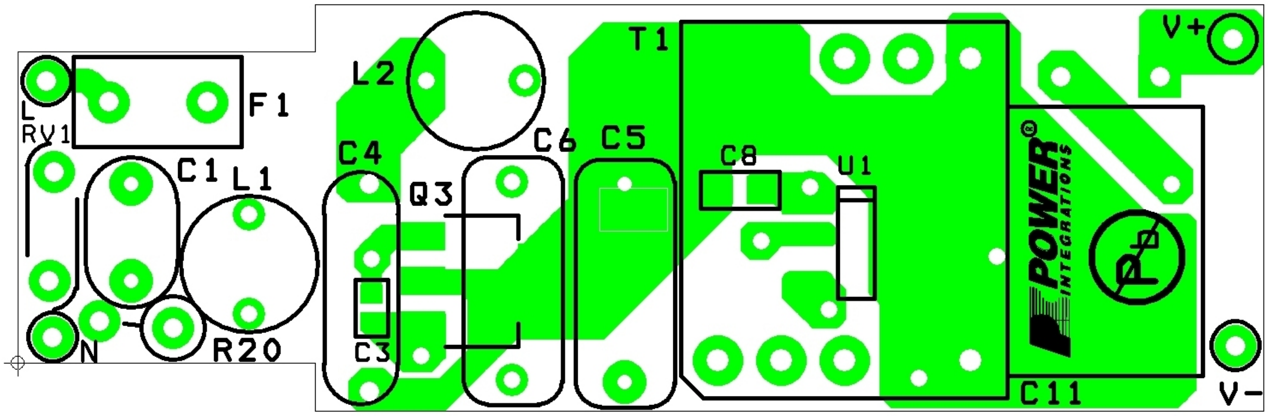

Figure 5 – Top Printed Circuit Layout 0.83" (20.86 mm) x 2.52" (63.9 mm).

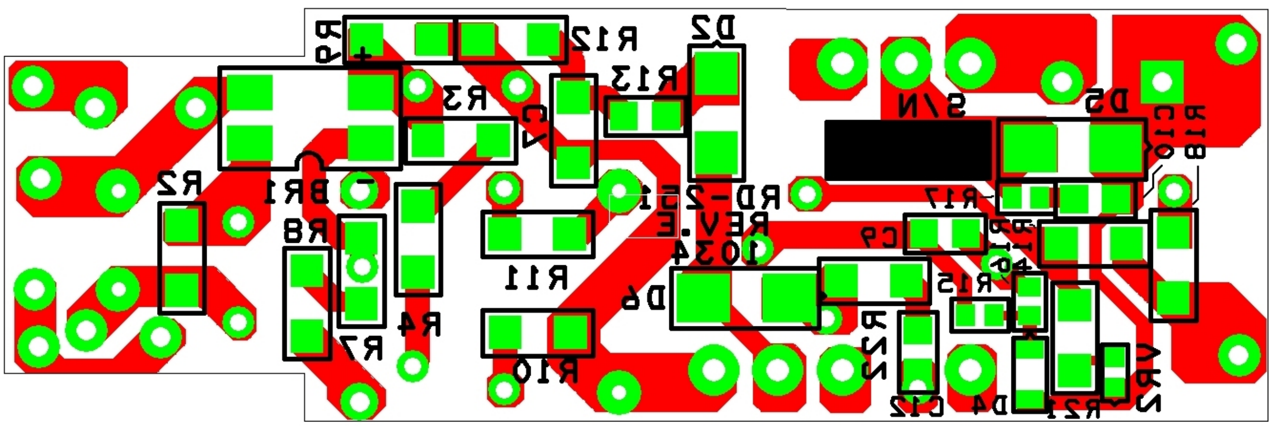

Figure 6 – Bottom Printed Circuit Layout.

6 Bill of Materials

Item	Qty	Ref Des	Description	Manufacturer P/N	Manufacturer
1	1	BR1	Bridge Rectifier Diode MBS GPP 0.8A 1000V	B10S-G	Comchip Technology
		BR1 (sub)	600 V, 0.5 A, Bridge Rectifier, SMD, MBS-1, 4-SOIC	MB6S-TP	Micro Commercial
2	1	C3	22 nF, 50 V, Ceramic, Y5V, 0603	ECJ-1VF1H223Z	Panasonic
3	1	C4	22 nF, 630V, Film	ECQ-E6223KZ	Panasonic
4	1	C5 C6	68 nF, 400 V, Film	ECQ-E4683KF	Panasonic
5	1	C7	1000 pF, 630 V, Ceramic, X7R, 1206	ECJ-3FB2J102K	Panasonic
6	1	C8	10 nF, 50 V, Ceramic, X7R, 0805	ECJ-2VB1H103K	Panasonic
7	1	C9	1 μF, 25 V, Ceramic, X7R, 0805	ECJ-2FB1E105K	Panasonic
8	1	C10	1 nF, 100 V, Ceramic, X7R, 0805	ECJ-2VB2A102K	Panasonic
9	1	C11	680 μF, 25 V, Electrolytic, Very Low ESR, 32 mΩ, (10 x 16)	25ZLH680MEFC10X16	Rubycon
10	0	C1	Do not mount (unstalled/optional location only)		
11	0	C12	Do not mount (unstalled/optional location only)		
12	1	D4	100 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV19WS-7-F	Diode Inc.
13	1	D2	DIODE ULTRA FAST, SW 600V, 1A, SMA	US1J-13-F	Diodes, Inc
14	1	D5	100 V, 1 A, Schottky, DO-214AC (SMA)	SS110-TP	Micro commercial
15	1	D6	800 V, 1 A, Rectifier, Glass Passivated, DO-213AA (MELF)	DL4006-13-F	Diodes Inc
		D6 (sub)	200 V, 1 A, Fast Recovery, 150ns, SMA	RS1D-13-F	Diodes Inc
16	1	F1	3.15 A, 250V, Slow, RST	507-1181	Belfuse
17	2	L1 L2	2.2 mH, 0.15 A, Ferrite Core	CTSCH875DF – 222K	CTParts
18	1	Q3	SCR, 400 V, 0.8 A, SMD, SOT-223	P0102DN 5AA4	ST Microelectroics
19	2	R2 R9	4.7 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ472V	Panasonic
20	2	R3 R4	750 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ754V	Panasonic
21	2	R7 R8	240 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ241V	Panasonic
22	2	R10 R11	510 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ511V	Panasonic
23	1	R12	100 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ104V	Panasonic
24	1	R13	4.7 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ4R7V	Panasonic
25	1	R14 R21	1 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ102V	Panasonic
26	1	R15	3.3 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ332V	Panasonic
27	1	R16	10 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ103V	Panasonic
28	1	R17	27 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ270V	Panasonic
29	1	R18	0.82 Ω, 1%, 1/2 W, Thick Film, 1206	RL1632R-R820-F	Susumu Co Ltd
30	2	R19 R20	47 Ω, 5%, 2 W, MF Fusible	NFR0200004709JR500	Vishay/BC Components
31	0	R22	Do not mount (unstalled/optional location only)		
32	1	RV1	275 V, 23 J, 7 mm, RADIAL	V275LA4P	Littlefuse
33	1	T1	Custom transformer, EE16. See report for specifications	SNX-R1536	Santronics
34	1	U1	LinkSwitch-PL, LNK457DG, SO-8C	LNK457DG	Power Integrations
35	1	VR2	20 V, 5%, 150 mW, SSMINI-2	MAZS2000ML	Panasonic-SSG
36	1	J1 J2	Test point, WHT, Miniature THRU-HOLE MOUNT	5002	Keystone
37	1	J3	Test point, RED, Miniature THRU-HOLE MOUNT	5000	Keystone
38	1	J4	Test point, BLK, Miniature THRU-HOLE MOUNT	5001	Keystone

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7 Transformer Design Spreadsheet

ACDC_LinkSwitch-PL-Flb_042910; Rev.1.0; Copyright Power Integrations 2010	**INPUT**	**INFO**	**OUTPUT**	**UNIT**	**ACDC_LinkSwitch-PL_Flb_042910; LinkSwitch-PL Flyback Transformer Design Spreadsheet**
ENTER APPLICATION VARIABLES					5 W Dimmable Power Factor Corrected LED Driver (Non-Isolated) Using LinkSwitch-PL LNK457DG
VACMIN	85		85	V	Minimum AC input voltage
VACMAX	265		265	V	Maximum AC input voltage
FL	50		50	Hz	Minimum line frequency
VO_MAX	18		18	V	Maximum Output Voltage
VO_MIN			10.0	V	Minimum output voltage before device operates in cycle skipping at VACMAX
IO	0.35		0.350	A	Average output current
N	0.7		0.7	%/100	Total power supply efficiency
Z	0.7		0.7		Loss allocation factor. Larger value of Z means losses are more on secondary side, smaller value of Z means more losses on primary side.
Enclosure	Open Frame		Open Frame		Enclosure selections determines thermal conditions and maximum power
PO			6.30	W	Average output power
VD			0.7	V	Output diode forward voltage drop
LinkSwitch-PL DESIGN VARIABLES					
Device	LNK457		LNK457		Chose device PO max in Open Frame: 7.357W, PO Max in Retrofit Lamp: 6.893125 W.
VOR			120.7	V	Reflected output voltage
Turns Ratio			6.5		Primary to secondary turns ratio
TON			3.27	us	Expected on-time of MOSFET at low line and PO
FSW			122.1	kHz	Expected switching frequency at low line and PO
Duty Cycle			39.9	%	Expected operating duty cycle at low line and PO
VDRAIN			620	V	Estimated drain voltage
IRMS			0.154	A	Primary RMS current
IPK			0.595	A	Peak primary current

ACDC_LinkSwitch-PL-Flb_042910; Rev.1.0; Copyright Power Integrations 2010	INPUT	INFO	OUTPUT	UNIT	ACDC_LinkSwitch-PL_Flb_042910; LinkSwitch-PL Flyback Transformer Design Spreadsheet
ILIM_MAX			0.910	A	Device peak current
KDP			1.51		Ratio between off-time of switch and reset time of core
LinkSwitch-PL EXTERNAL COMPONENT CALCULATIONS					
RSENSE			0.829	Ohms	Output current sense resistor
Standard RSENSE			0.83	Ohms	Closest 1% value for RSENSE
PSENSE			0.102	W	Power dissipated by RSENSE
ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					
Core Type	EE16		EE16		Core Type
Core Part Number			PC40EE16-Z		Core Part Number (if Available)
Bobbin Part Number			BE-16-118CPH		Bobbin Part Number (if available)
AE			19.20	mm^2	Core Effective Cross Sectional Area
LE			35.00	mm	Core Effective Path Length
AL			1140	nH/T^2	Ungapped Core Effective Inductance
BW			8.6	mm	Bobbin Physical Winding Width
L			3		Number of primary winding layers
NS			20	Turns	Number of Secondary Turns
TRANSFORMER PRIMARY DESIGN PARAMETERS					
LP			0.660	mH	Primary Inductance
LP Tolerance			10	%	Tolerance of Primary Inductance
NP			130	Turns	Primary Winding Number of Turns
ALG			39	nH/T^2	Gapped Core Effective Inductance
BM			1574	Gauss	Maximum (BM < 3000 G)
BAC			787	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
BP_TARGET	2650		2650	Gauss	Target Peak Flux density. Recommended value of BP_TARGET < 3700 G.
BP			2647	Gauss	Peak Flux Density (BP < 3700 G)

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ACDC_LinkSwitch-PL-Flb_042910; Rev.1.0; Copyright Power Integrations 2010	INPUT	INFO	OUTPUT	UNIT	ACDC_LinkSwitch-PL_Flb_042910; LinkSwitch-PL Flyback Transformer Design Spreadsheet
LG			0.618	mm	Gap Length (Lg > 0.1 mm)
BWE			25.8	mm	Effective Bobbin Width
OD			0.20	mm	Maximum Primary Wire Diameter including insulation
INS			0.04	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA			0.16	mm	Bare conductor diameter
AWG			35	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM			32	Cmils	Bare conductor effective area in circular mils
CMA			208	Cmils/Amp	Primary Winding Current Capacity (200 < CMA < 500)
Primary Current Density (J)			9.61	A/ mm^2	Primary Winding Current density (3.8 < J < 9.75 A/mm^2)
SECONDARY DESIGN PARAMETERS					
ISP			3.87	A	Peak Secondary Current
ISRMS			0.91	A	Secondary RMS current
IO			0.35	A	Output Current
PIVS			83.6	V	Peak Inverse Voltage experienced by the output diode with added 10% margin added for reverse recovery voltage spike
CMS1			183	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS			27	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS			0.36	mm	Minimum Bare Conductor Diameter
ODS			1.29	mm	Maximum Outside Diameter for Triple Insulated Wire

8 Transformer Specification

8.1 Electrical Diagram

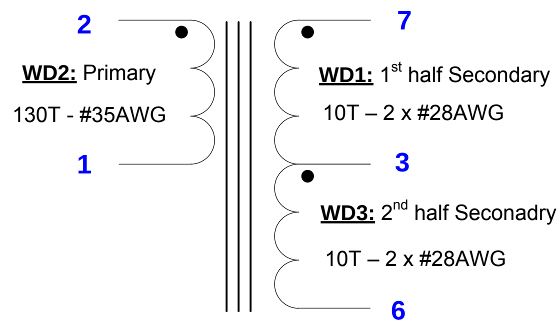

Figure 7 – Transformer Electrical Diagram.

8.2 Electrical Specifications

Electrical Strength	3 second, 60 Hz, from pins 1-2 to pins 6-7	500 VAC
Primary Inductance	Pins 1-2, all other windings open, measured at 100 kHz, 0.4 VRMS	660 μH, ±10 %
Resonant Frequency	Pins 1-2, all other windings open	1200 kHz (Min.)
Primary Leakage Inductance	Pins 1-2, with pins 7-9 shorted, measured at 100 kHz, 0.4 VRMS	15 μH (Max.)

8.3 Materials

Item	Description
[1]	Core: EE16/PC40
[2]	Bobbin: EE16, Horizontal, 10 pins, (5/5), TF1613 (Taiwan Shulin) or equivalent.
[3]	Magnet wire: #28 AWG double coated.
[4]	Magnet wire: #35 AWG double coated.
[5]	Tape: 3M 1298 Polyester Film, 8.0 mm wide, 2.0mils thick or equivalent.
[6]	Varnish.

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8.4 Transformer Build Diagram

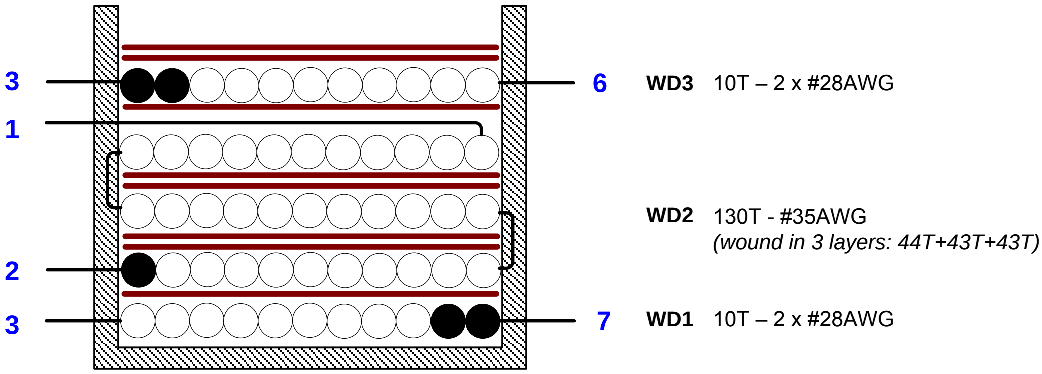

Figure 8 – Transformer Build Diagram.

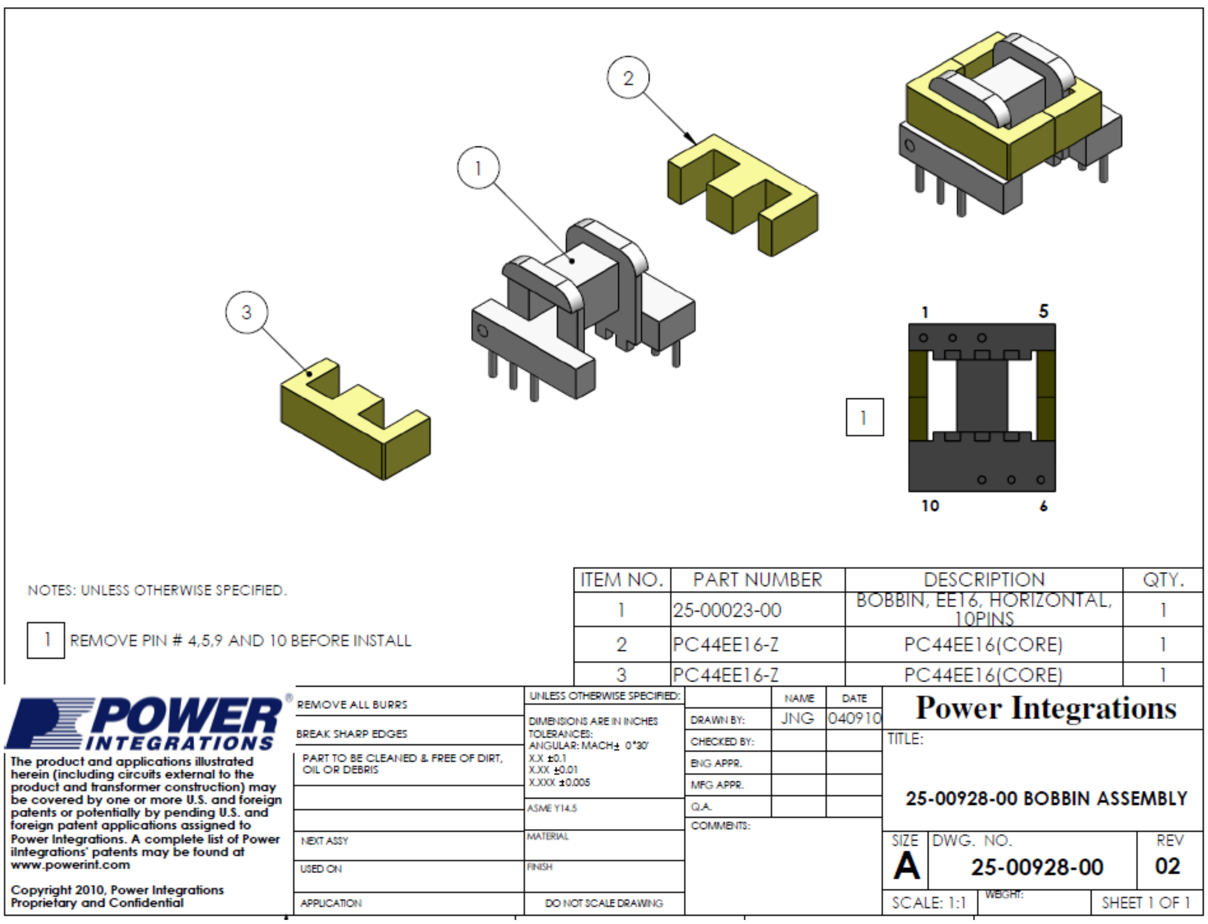

Figure 9 – Transformer Assembly.

8.5 Transformer Construction

Winding Preparation	Place bobbin on the mandrel such that primary on the left and secondary on the right. Winding direction is clock-wise direction.
WD1 1st Half of Secondary	Start at pin 7, wind 10 bifilar turns of wire item [3] from right to left, and terminate at pin 3.
Insulation	1 layer of tape item [5].
WD2 Primary	Start at pin 2, wind 130 turns of wire item [4] in 3 layers: 44T+43T+43T, place 2 layers of tape item [5] between layers, see fig.7 above, and terminate at pin 1.
Insulation	1 layer of tape item [5].
WD3 2nd Half of Secondary	Start at pin 3, wind 10 bifilar turns of wire item [3] from left to right, and terminate at pin 6.
Insulation	2 layers of tape item [5].
Finish	Grind core halves to get 660 μH assemble with tape. Varnish.

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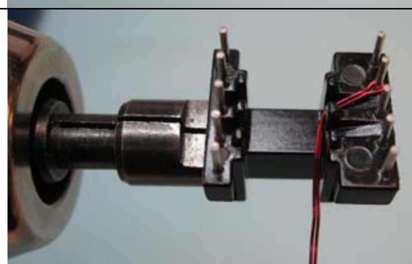
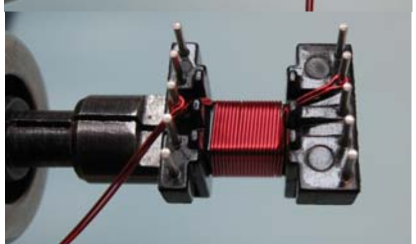
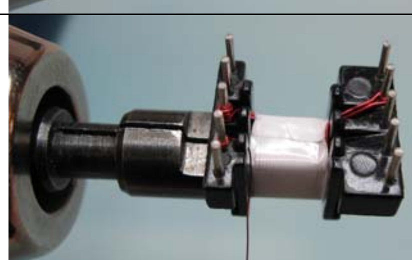
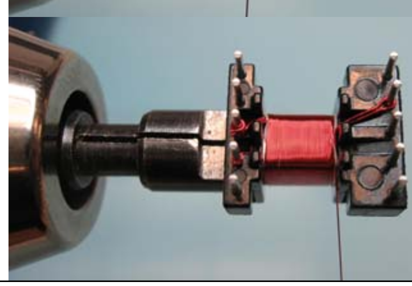
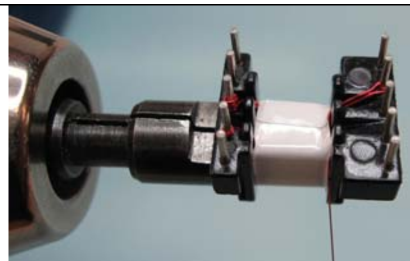
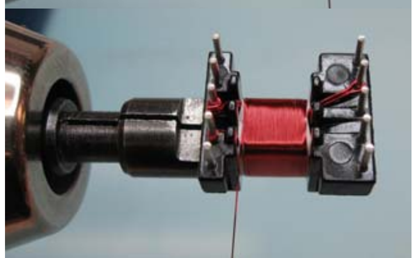
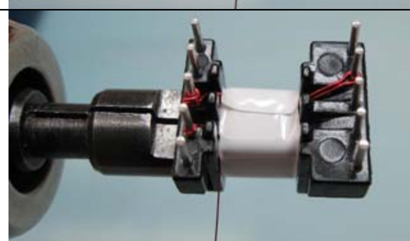
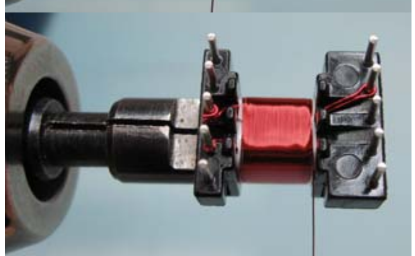
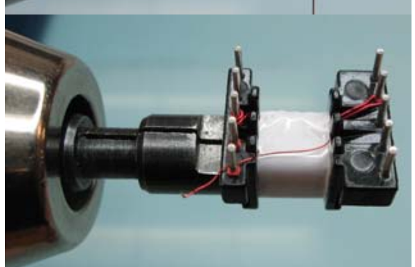
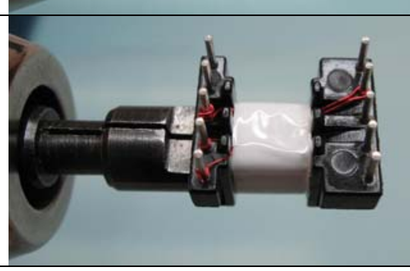
8.6 Winding Illustrations

Winding Preparation		Place bobbin on the mandrel such that primary on the left and secondary on the right. Winding direction is clock-wise direction.
WD1 **1st Half of Secondary**	 	Start at pin 7, wind 10 bifilar turns of wire item [3] from right to left, and terminate at pin 3.
Insulation		1 layer of tape item [5].
WD2 **Primary**	 	Start at pin 2, wind 130 turns of wire item [4] in 3 layers: 44T+43T+43T, place 2 layers of tape item [5] between layers,

	 	
WD2 Primary (Cont'd)	  	Refer to fig.7 above, and terminate at pin 1.
Insulation		1 layer of tape item [5].

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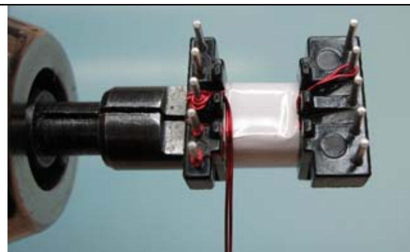
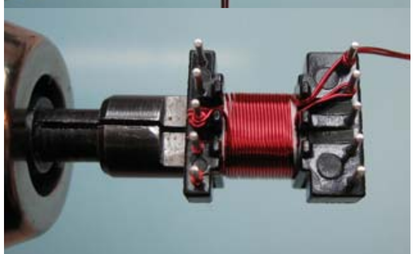
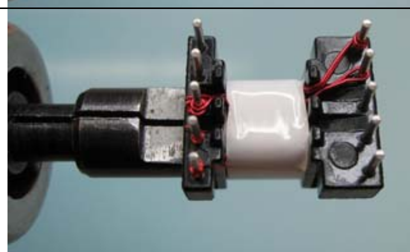
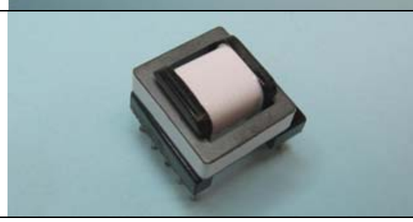
WD3 **2nd Half of Secondary**	 	Start at pin 3, wind 10 bifilar turns of wire item [3] from left to right, and terminate at pin 6.
Insulation		2 layers of tape item [5].
Finish		Grind core halves to get 660μH, between cores see figure.3, and assemble with tape. Varnish.

Figure 10 – Transformer Construction.

9 Performance Data

All measurements performed at room temperature otherwise specified.

9.1 Active Mode Efficiency

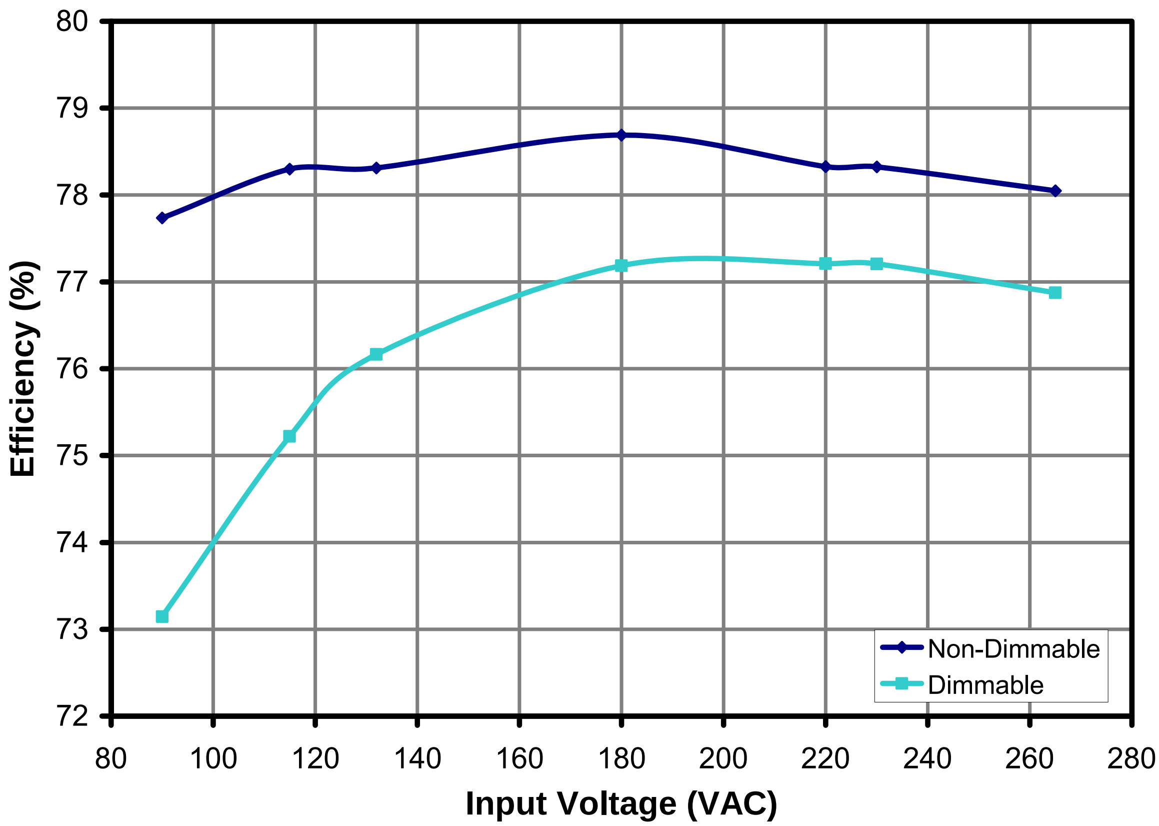


Figure 11 – Full Load (15 V, 350 mA) Efficiency with Respect to Line Input Voltage and Dimming or Non-Dimming Configuration (active damper and bleeder removed).

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9.2 Non-Dimmable Configuration

Active Damper and Bleeder components removed.

Input		Input Measurement				Load Measurement			Efficiency (%)
VAC (V_{RMS})	Freq (Hz)	I_{IN} (mA_{RMS})	P_{IN} (W)	PF	%THD	V_O (V_{DC})	I_O (mA_{DC})	Po (W)	
90	47	75.020	6.728	0.9973	6.6400	15.12	342.80	5.23	77.73
115	60	61.030	6.981	0.9950	8.36	15.17	358.10	5.47	78.30
132	60	53.870	7.054	0.9924	10.09	15.17	361.90	5.52	78.31
180	50	39.540	7.010	0.9853	12.02	15.15	361.10	5.52	78.69
220	50	32.160	6.902	0.9755	12.35	15.13	354.60	5.41	78.33
230	50	31.040	6.934	0.9717	12.21	15.13	356.20	5.43	78.32
265	63	27.800	6.915	0.9384	12.07	15.13	354.80	5.40	78.05
230	50	29.932	6.676	0.9700	12.53	15.08	343.50	5.22	78.21
220	50	30.723	6.577	0.9731	12.59	15.07	339.60	5.16	78.39
180	50	37.740	6.682	0.9839	12.37	15.08	345.10	5.25	78.51
132	60	50.848	6.653	0.9914	10.77	15.08	343.90	5.22	78.40
115	60	58.278	6.665	0.9945	8.7100	15.08	343.80	5.22	78.24
90	47	74.710	6.700	0.9973	6.67	15.06	342.80	5.21	77.73

9.3 Dimmable

Input		Input Measurement				Load Measurement			Efficiency (%)
VAC (V_{RMS})	Freq (Hz)	I_{IN} (mA_{RMS})	P_{IN} (W)	PF	%THD	V_O (V_{DC})	I_O (mA_{DC})	Po (W)	
90	47	81.250	7.29	0.9974	6.0100	15.13	349.10	5.33	73.14
115	60	65.400	7.47	0.9941	7.18	15.18	368.00	5.62	75.22
132	60	55.980	7.31	0.9895	9.6	15.16	364.90	5.57	76.16
180	50	41.920	7.35	0.9746	12.23	15.16	371.20	5.67	77.19
220	50	34.910	7.30	0.9507	13.43	15.15	369.20	5.64	77.21
230	50	33.690	7.30	0.9423	13.09	15.14	369.30	5.64	77.21
265	63	30.110	7.09	0.8886	22.46	15.11	359.00	5.45	76.88
230	50	31.986	6.89	0.9370	13.85	15.07	350.00	5.31	77.12
220	50	33.249	6.91	0.9448	13.71	15.07	351.60	5.34	77.25
180	50	39.671	6.94	0.9719	12.7	15.07	352.10	5.35	77.07
132	60	52.683	6.87	0.9877	10.57	15.05	346.60	5.25	76.42
115	60	63.186	7.22	0.9938	7.3500	15.08	358.40	5.44	75.34
90	47	79.780	7.15	0.9974	5.98	15.03	345.50	5.24	73.22

Table 1 – Full Load Characteristic, Verified with 5 White LED Series String.

9.4 Harmonics

Meets EN61000-3-2 Harmonics contents standards.

Order	Input Current Harmonics (mA)				EN 61000-3-2
	Non-Dimmable		Dimmable		
	115 V	230 V	115 V	230 V	
1	61.87	32.40	62.19	32.52	
3	1.45	1.25	1.92	1.51	P
5	3.72	1.26	3.22	1.57	P
7	0.81	1.61	1.51	1.72	P
9	0.29	1.55	0.84	1.64	P
11	1.69	1.58	1.02	1.63	P
13	0.79	1.61	0.17	1.55	P
15	0.65	1.30	0.69	1.31	P
17	0.90	0.81	1.37	1.05	P
19	1.08	0.69	1.50	0.73	P
21	0.58	0.30	0.81	0.99	P
23	0.81	0.22	1.00	0.53	P
25	0.61	0.13	0.62	0.66	P
27	0.64	0.11	0.34	0.50	P
29	0.67	0.15	0.52	0.45	P
31	0.70	0.14	0.59	0.36	P
33	0.53	0.11	0.57	0.30	P
35	0.43	0.12	0.57	0.39	P
37	0.33	0.12	0.55	0.35	P
39	0.20	0.12	0.43	0.36	P
41	0.06	0.14	0.24	0.28	
43	0.13	0.15	0.21	0.24	
45	0.20	0.09	0.12	0.27	
47	0.15	0.11	0.24	0.18	
49	0.10	0.13	0.27	0.15	

Table 2 – Harmonics Contents

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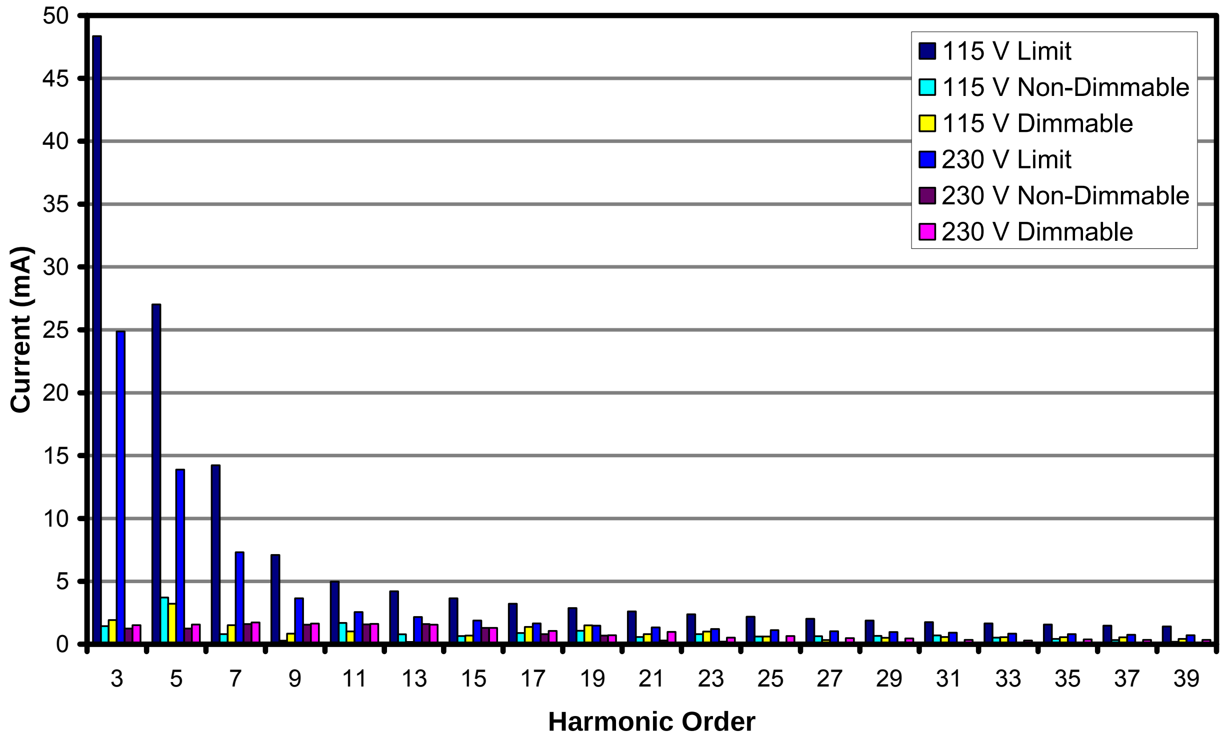

Figure 12 – UUT Harmonic content**.**

9.5 Power Factor

Line voltage was swept from minimum to maximum and back. The difference seen is due to the hysteresis between operating states of the internal controller and is deterministic.

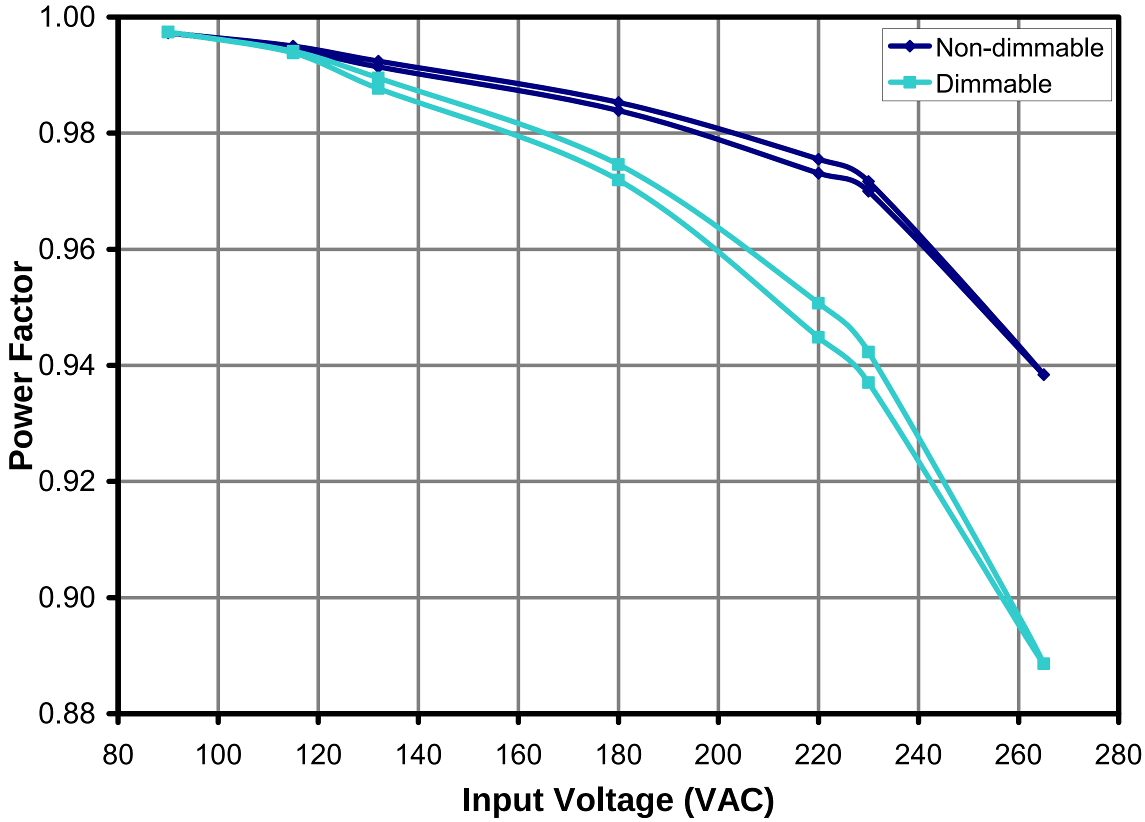

Figure 13 – Power Factor with Respect to AC Input at Full Load.

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9.6 Line Regulation

Line voltage was swept from minimum to maximum and back. The difference seen is due to the hysteresis between the operating states of the internal controller and is deterministic.

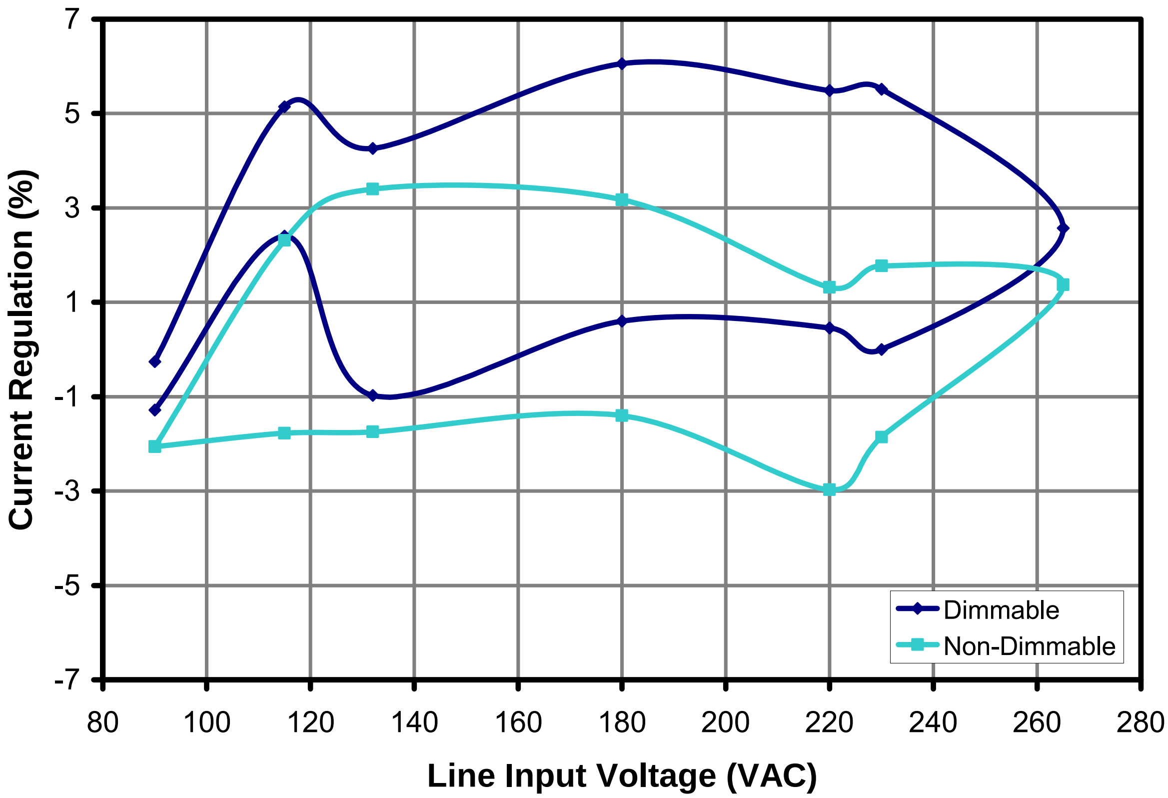

Figure 14 – Line Regulation, Room Temperature, Full Load.

9.7 Dimming Performance

9.7.1 Dimming Range

The design was characterized using a programmable AC source to simulate a leading edge TRIAC dimmer. Data was taken in 1 degree phase angle steps.

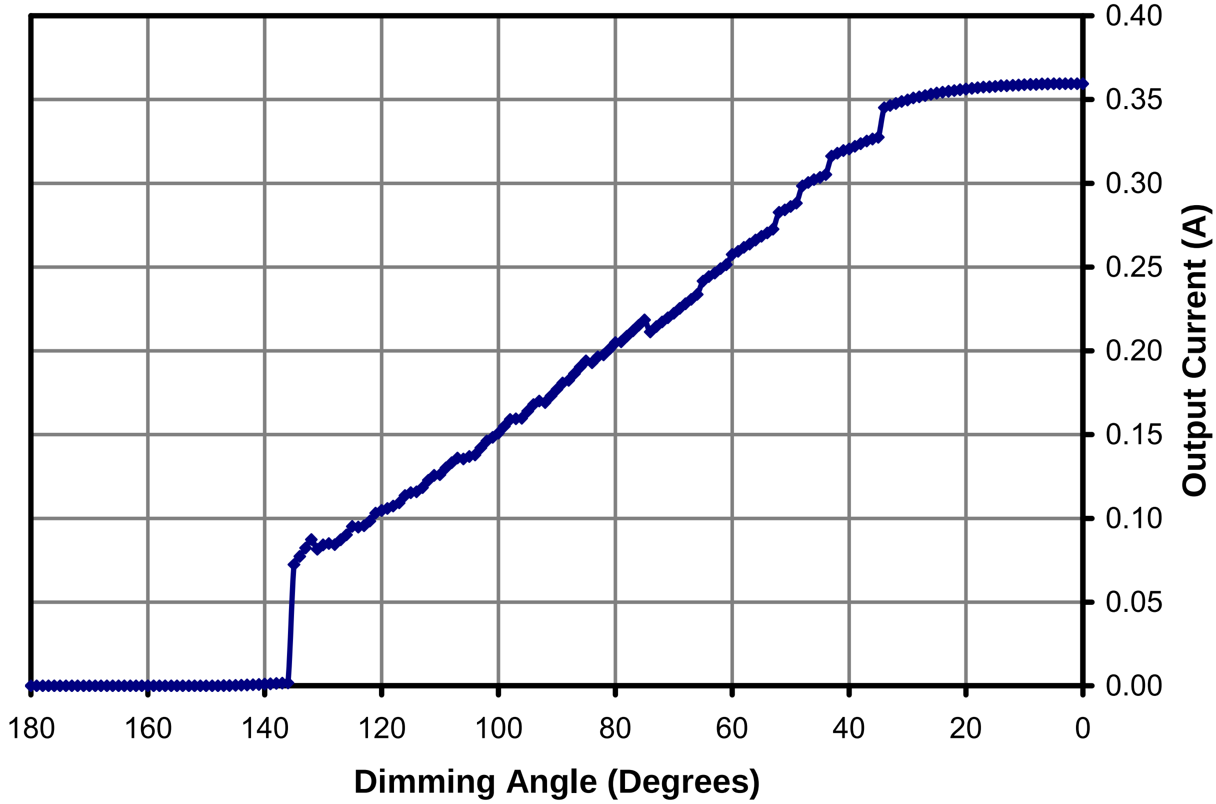

Figure 15 – 115 V Phase Angle Dimming Characteristic (Increasing Output Current).

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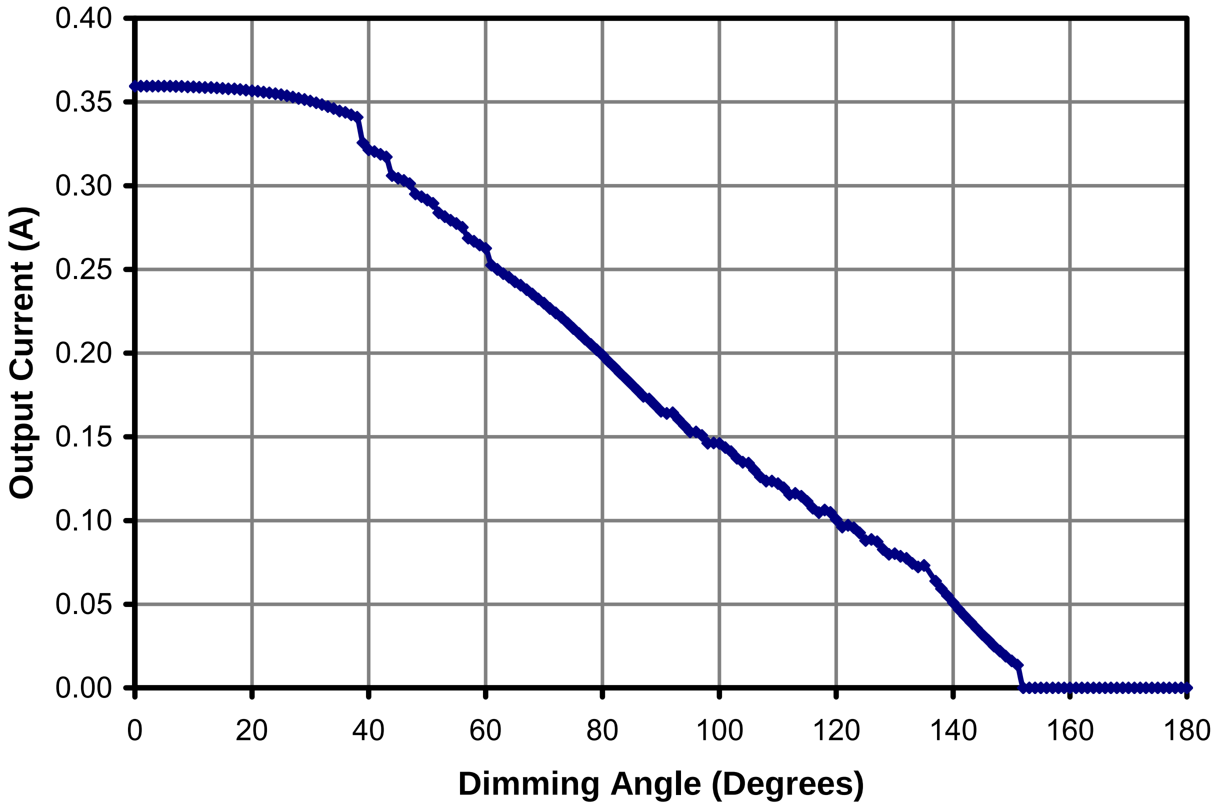

Figure 16 – 115 V Phase Angle Dimming Characteristic (Decreasing Output Current).

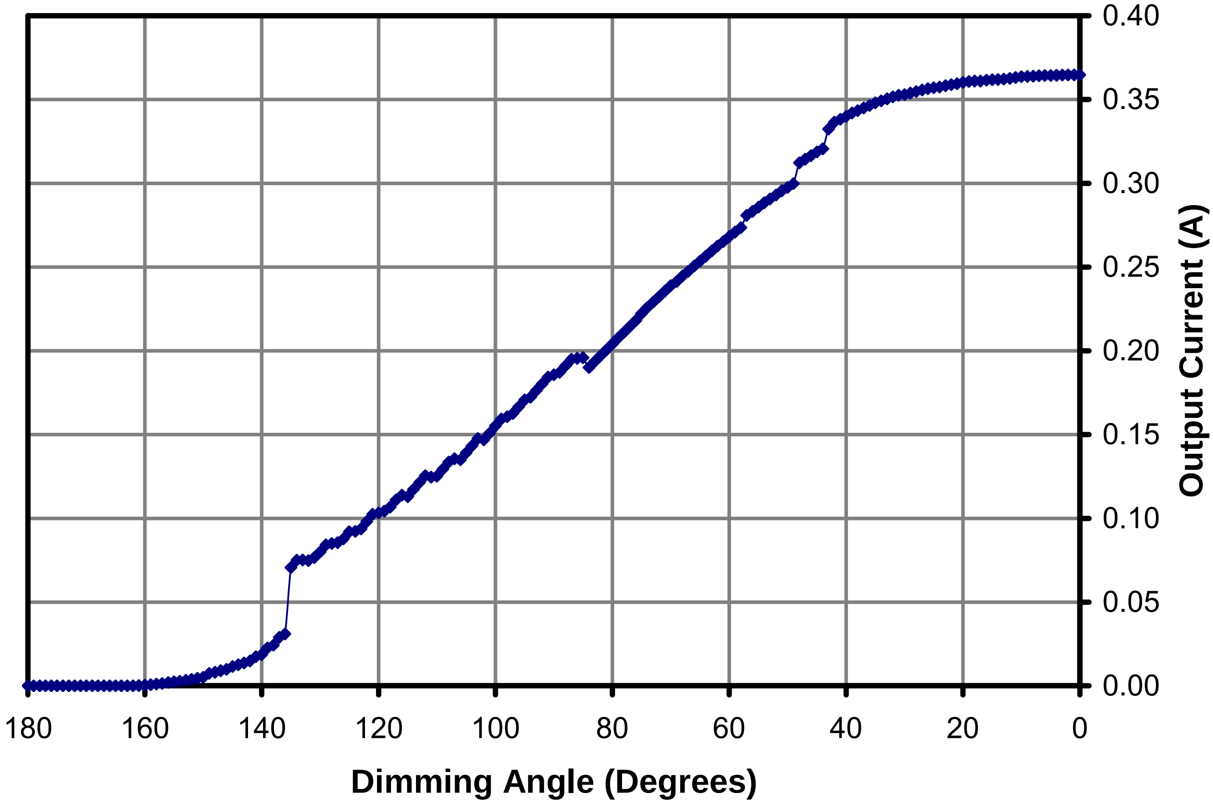

Figure 17 – 230 V Phase Angle Dimming Characteristic (Increasing Output Current).

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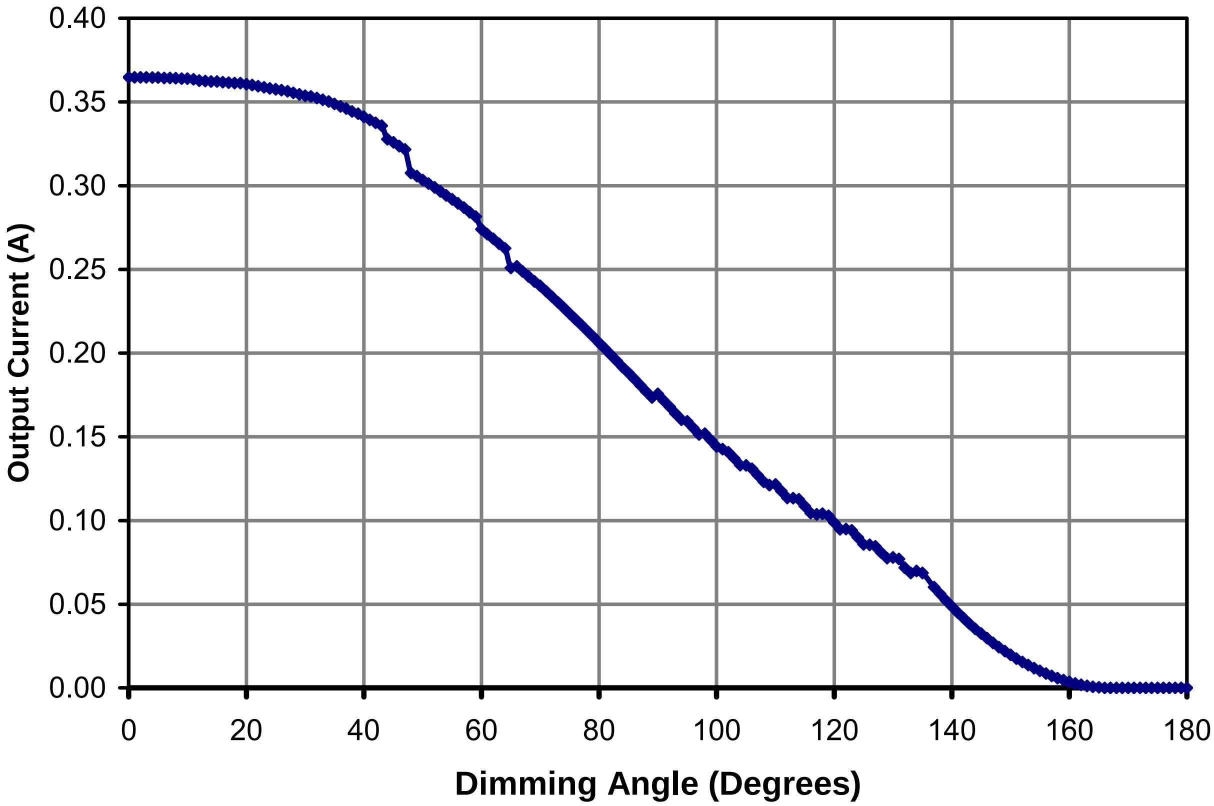

Figure 18 – 230 V Phase Angle Dimming Characteristic (Increasing Output Current).

9.7.2 Unit to Unit Tracking

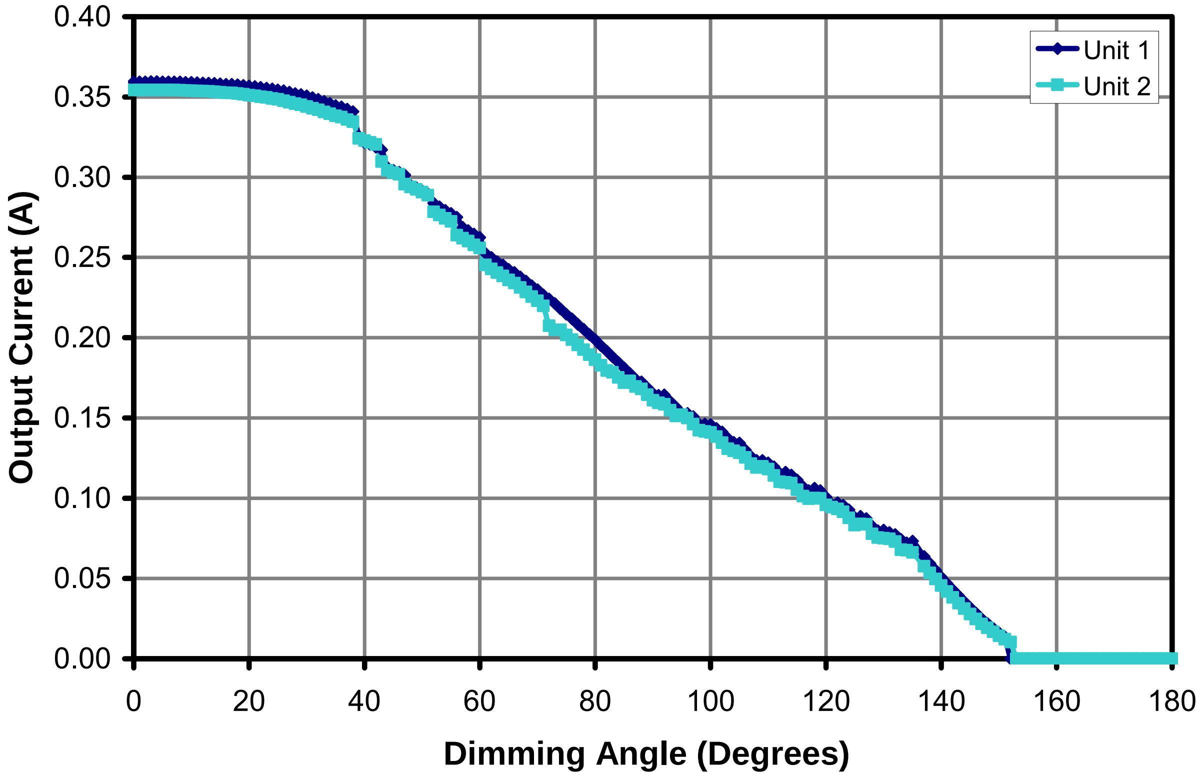

Figure 19 – Sample Curve for Unit to Unit Output Current Dimming Performance at 115 V / 60 Hz.

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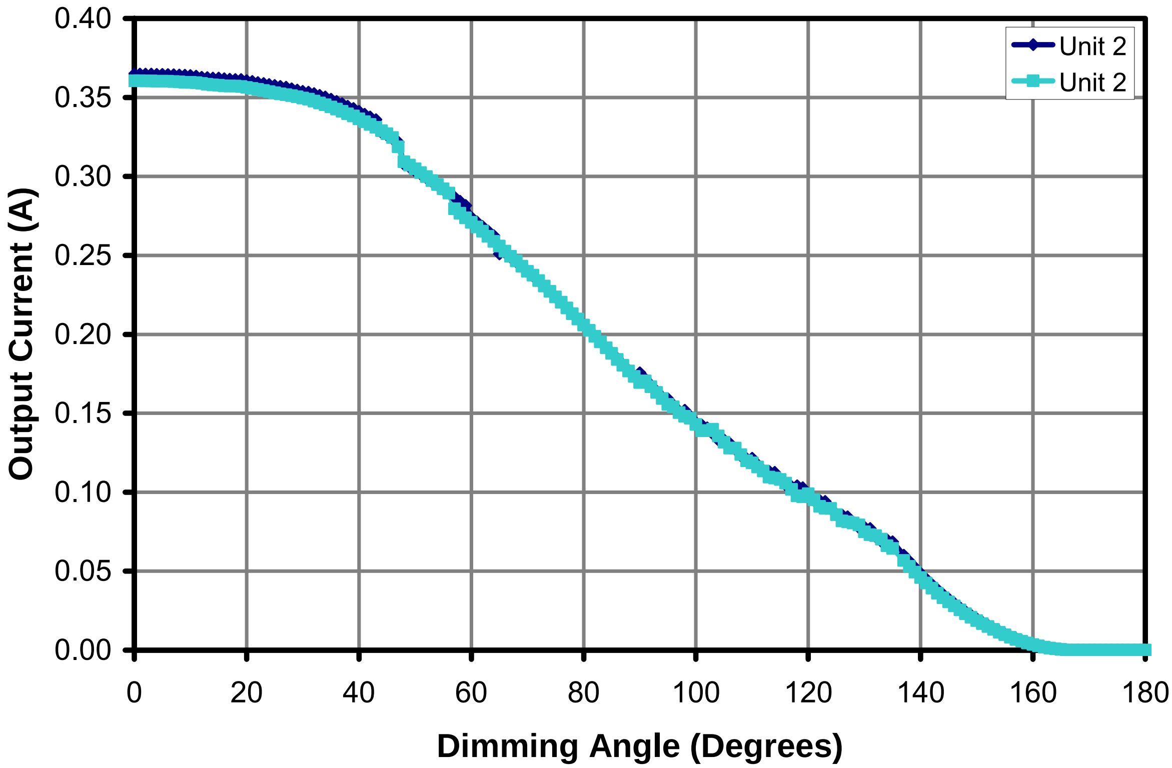

Figure 20 – Sample Curve for Unit to Unit Output Current Dimming Performance at 230 V / 50 Hz.

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10 Thermal Performance

10.1 Thermal Set-up

The unit was verified inside a cardboard box to avoid the influence of circulating air inside the thermal chamber.

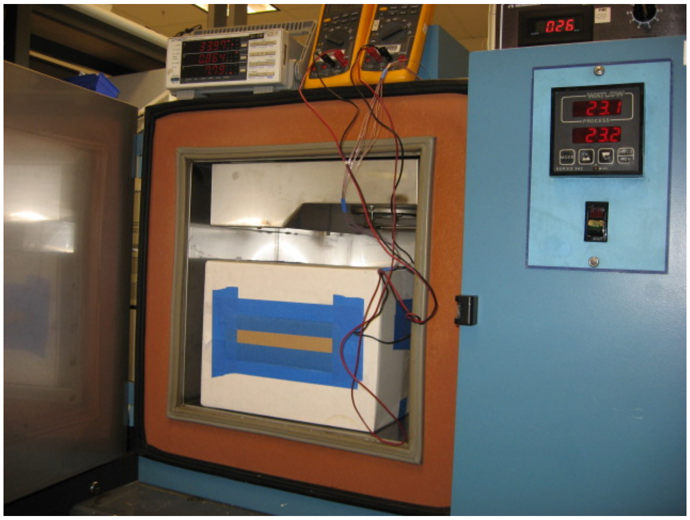

Figure 21 – Thermal Chamber Set-up Showing Box Used to Prevent Airflow Over UUT.

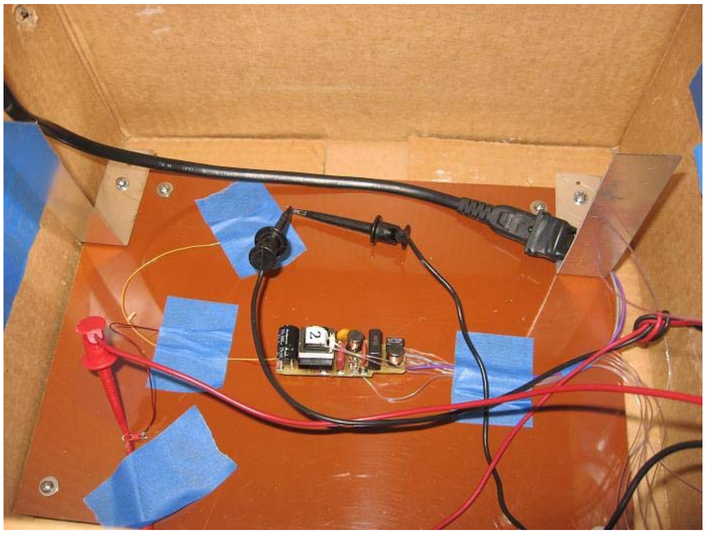

Figure 22 – UUT Within Box.

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10.2 Equipment Used

Chamber: Tenney Environmental Chamber
Model No: TJR-17 942

AC Source: Chroma Programmable AC Source
Model No: 6415

Wattmeter: Yokogawa Power Meter
Model No: WT2000

Data Logger: Monogram
SN:1290492

10.3 Thermal Result

Load: 5 LED in series (15 V / 350 mA). Ambient of 80°C simulates operation inside sealed LED replacement enclosure. Supply correctly started up and operated at -30°C

Item	Normal Operation (ºC)				Output Shorted	Cold Start-up (PASS)	
	90 V 50 Hz	115 V 60 Hz	230 V 50 Hz	265 V 60 Hz	265 V 60 Hz	90 V 50 Hz	265 V 60 Hz
Ambient (ºC)	80	80	80	80	80	-30	-30
Bridge (BR1)	101	112	104	97	92		
Fet (damper) (Q2)	99	110	104	100	93		
Input Inductor (L2)	96	105	101	99	88		
Transformer Core (T1)	101	109	107	106	88		
Transformer Winding (T1)	105	114	112	111	87		
LNK457 (U1)	113	126	122	120	95		
Output Capacitor (C11)	96	103	101	101	81		
Output Diode (D5)	110	120	118	118	89		

Table 3 – Thermal Data for Dimmable Unit.

10.4 Thermal Scan

Load: 5 LED in series (15 V / 350 mA)

Figure 23 – LNK457DG Device Temperature at 25ºC Open Air.

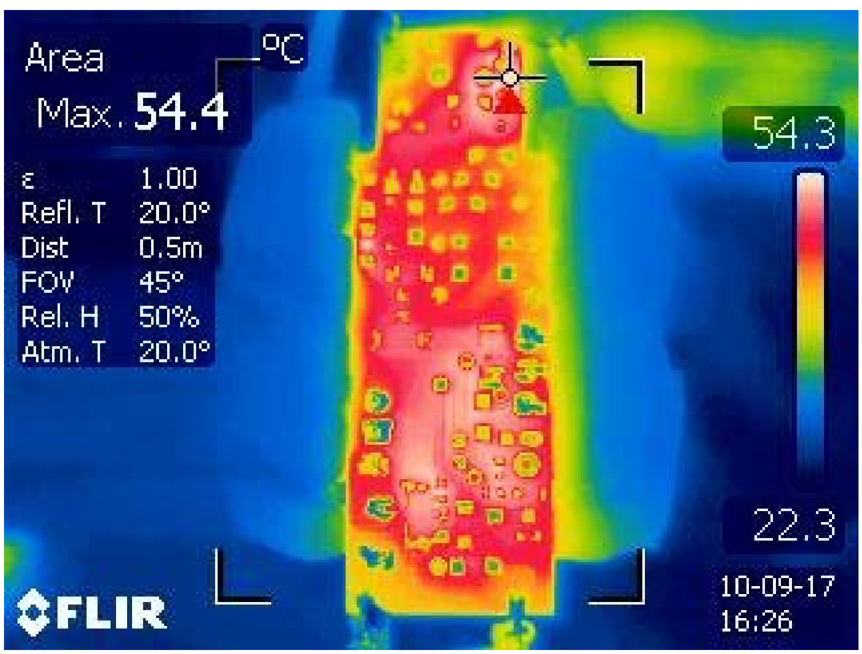

Figure 24 – Bottom Side of PCB, Trace and Device Temperature.

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11 Waveforms

11.1 Drain Voltage and Current

11.1.1 Normal Steady State Operation

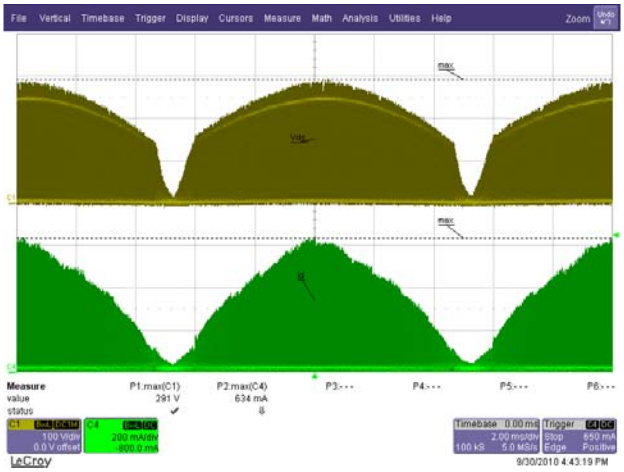

Figure 25 – 90 VAC / 50 Hz,
6 LED in Series (18.2 V / 350 mA).
Upper: V_{DRAIN}, 100 V / div., 2 ms / div.
Lower: I_{DRAIN}, 0.2 A / div.

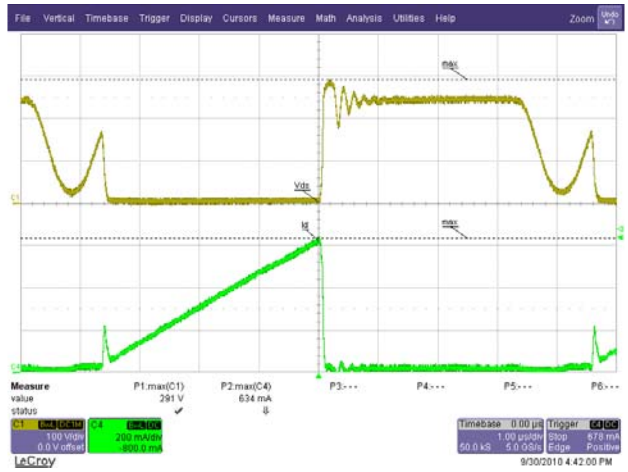

Figure 26 – 90 VAC / 50 Hz,
6 LED in Series (18.2 V / 350 mA).
Upper: V_{DRAIN}, 100 V / div., 1 µs / div.
Lower: I_{DRAIN}, 0.2 A / div.

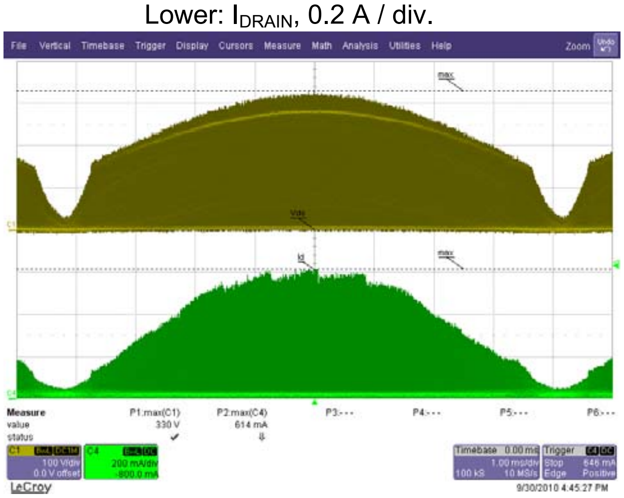

Figure 27 – 115 VAC / 60 Hz,
6 LED in Series (18.2 V / 350 mA).
Upper: V_{DRAIN}, 100 V / div., 1 ms / div.
Lower: I_{DRAIN}, 0.2 A / div.

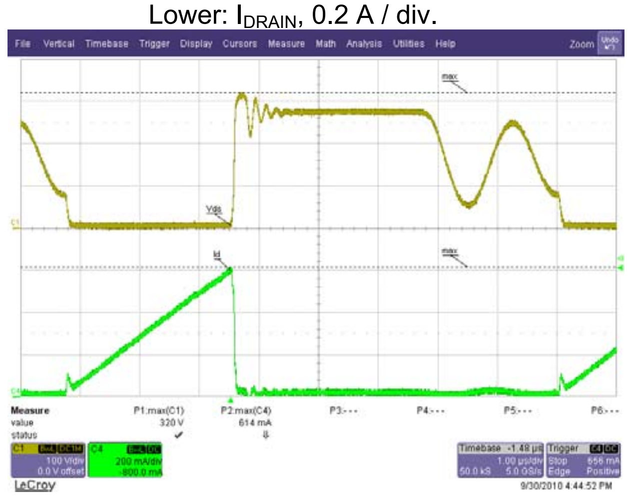

Figure 28 – 115 VAC / 60 Hz,
6 LED in Series (18.2 V / 350 mA).
Upper: V_{DRAIN}, 100 V / div., 1 µs / div.
Lower: I_{DRAIN}, 0.2 A / div.

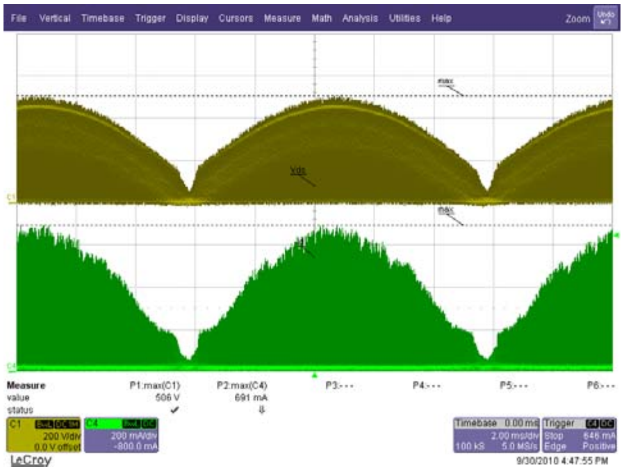

Figure 29 – 230 VAC / 50 Hz,
6 LED in Series (18.2 V / 350 mA).
Upper: V_{DRAIN}, 200 V / div., 5 ms / div.
Lower: I_{DRAIN}, 0.2 A / div.

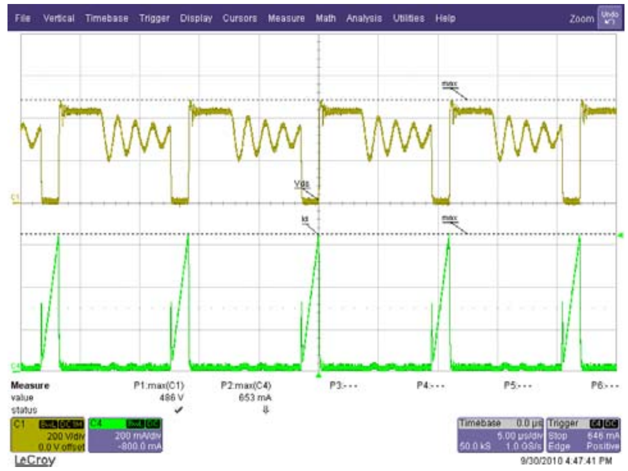

Figure 30 – 230 VAC / 50 Hz,
6 LED in Series (18.2 V / 350 mA).
Upper: V_{DRAIN}, 200 V / div., 5 µs / div.
Lower: I_{DRAIN}, 0.2 A / div.

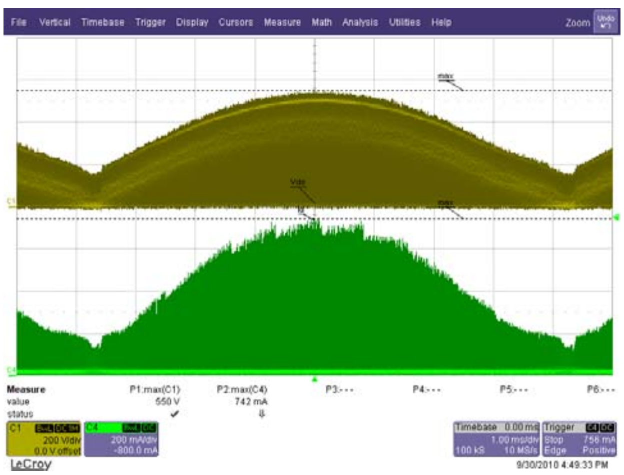

Figure 31 – 265 VAC / 63 Hz,
6 LED in Series (18.2 V / 350 mA).
Upper: V_{DRAIN}, 200 V / div., 1 ms / div.
Lower: I_{DRAIN}, 0.2 A / div.

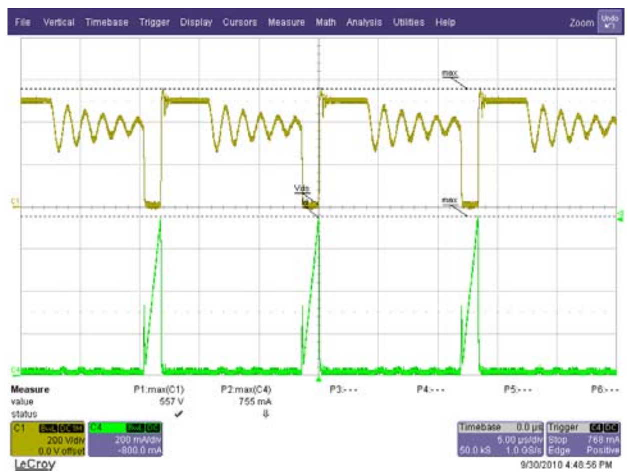

Figure 32 – 265 VAC / 63 Hz,
6 LED in Series (18.2 V / 350 mA).
Upper: V_{DRAIN}, 200 V / div., 5 µs / div.
Lower: I_{DRAIN}, 0.2 A / div.

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11.1.2 AC Start-up

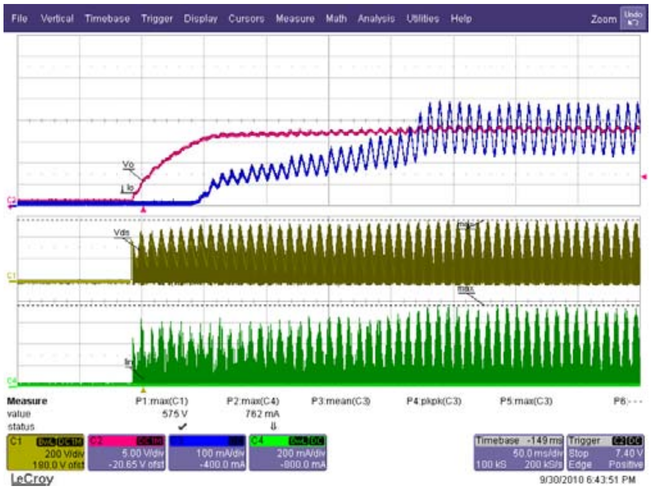

Figure 33 – 265 VAC / 63 Hz,
6 LED in Series (18.2 V / 350 mA).
Ch1(Yellow): V_{DS}, 200 V / div.
Ch2(Red): V_O, 5 V / div.
Ch3(Blue): I_O, 100 mA / div.
Ch4(Green): I_{DS}, 200 mA / div., 50 ms / div.

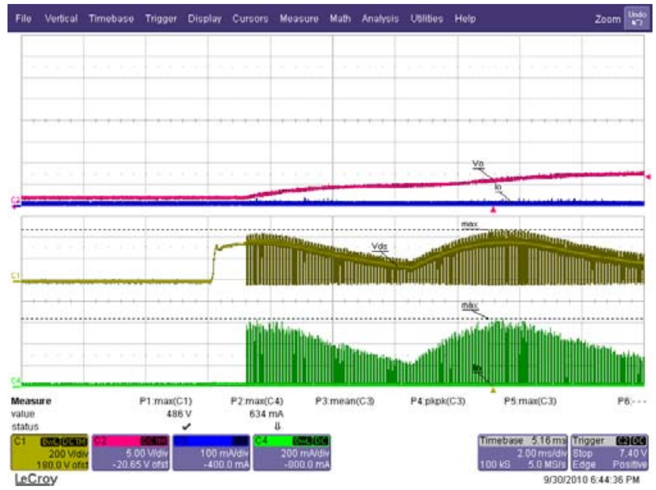

Figure 34 – 265 VAC / 63 Hz,
6 LED in Series (18.2 V / 350 mA).
Ch1(Yellow): V_{DS}, 200 V / div.
Ch2(Red): V_O, 5 V / div.
Ch3(Blue): I_O, 100 mA / div.
Ch4(Green): I_{DS}, 200 mA / div., 2 ms / div.

11.1.3 115 V TRIAC in Series with AC Input

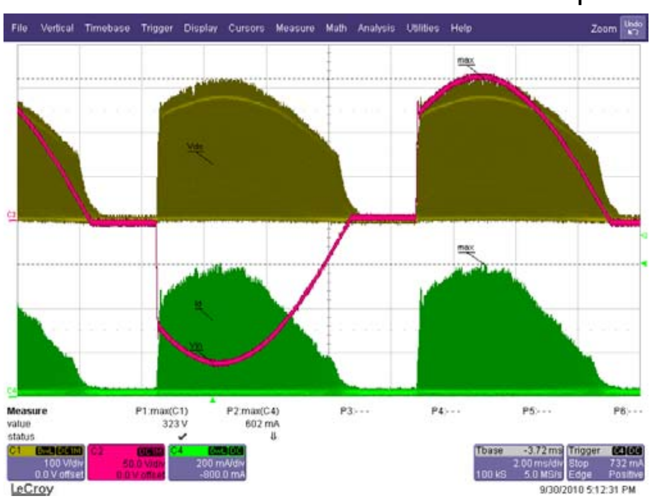

Figure 35 – 115 VAC / 60 Hz,
45º Dimming Phase Angle.
6 LED in Series (18.2 V / 350 mA).
Ch1(Yellow): V_{DS}, 100 V / div.
Ch2(Red): V_{IN}, 50 V / div.
Ch4(Green): I_{DS}, 200 mA / div., 2 ms / div.

Figure 36 – 115 VAC / 60 Hz,
45º Dimming Phase Angle.
6 LED in Series (18.2 V / 350 mA).
Ch1(Yellow): V_{DS}, 100 V / div.
Ch2(Red): V_{IN}, 50 V / div.
Ch4(Green): I_{DS}, 200 mA / div., 100 µs / div.

Figure 37 – 115 VAC / 60 Hz,
90º Dimming Phase Angle.
6 LED in Series (18.2 V / 350 mA)
Ch1(Yellow): V_{DS}, 100 V / div.
Ch2(Red): V_{IN}, 50 V / div.
Ch4(Green): I_{DS}, 200 mA / div., 2 ms / div.

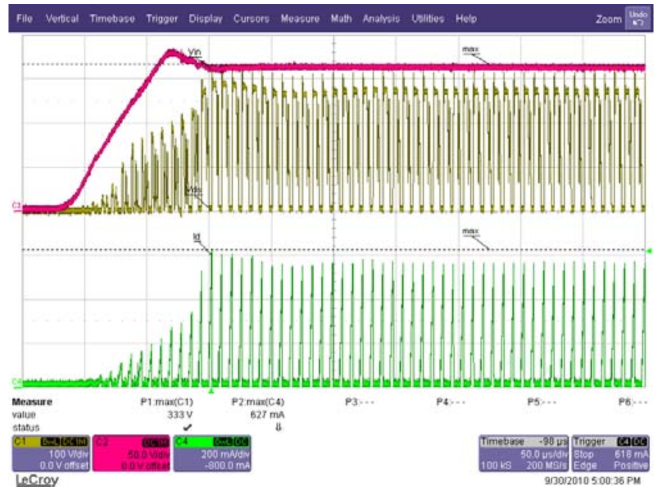

Figure 38 – 115 VAC / 60 Hz,
90º Dimming Phase Angle.
6 LED in Series (18.2 V / 350 mA)
Ch1(Yellow): V_{DS}, 100 V / div.
Ch2(Red): V_{IN}, 50 V / div.
Ch4(Green): I_{DS}, 200 mA / div., 50 µs / div.

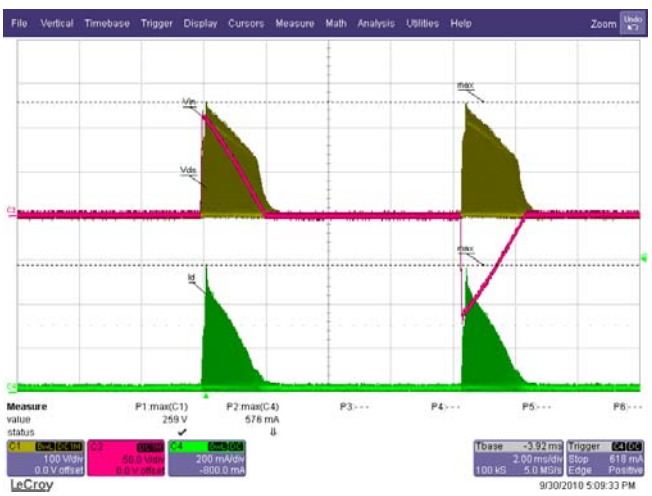

Figure 39 – 115 VAC / 60 Hz,
135º Dimming Phase Angle.
6 LED in Series (18.2 V / 350 mA)
Ch1(Yellow): V_{DS}, 100 V / div.
Ch2(Red): V_{IN}, 50 V / div.
Ch4(Green): I_{DS}, 200 mA / div., 2 ms / div.

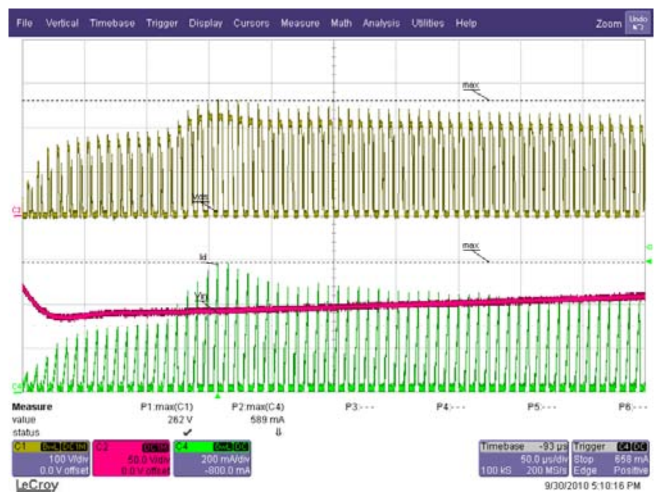

Figure 40 – 115 VAC / 60 Hz,
135º Dimming Phase Angle.
6 LED in Series (18.2 V / 350 mA)
Ch1(Yellow): V_{DS}, 100 V / div.
Ch2(Red): V_{IN}, 50 V / div.
Ch4(Green): I_{DS}, 200 mA / div., 50 µs / div.

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11.1.4 230 V TRIAC in Series with AC Input

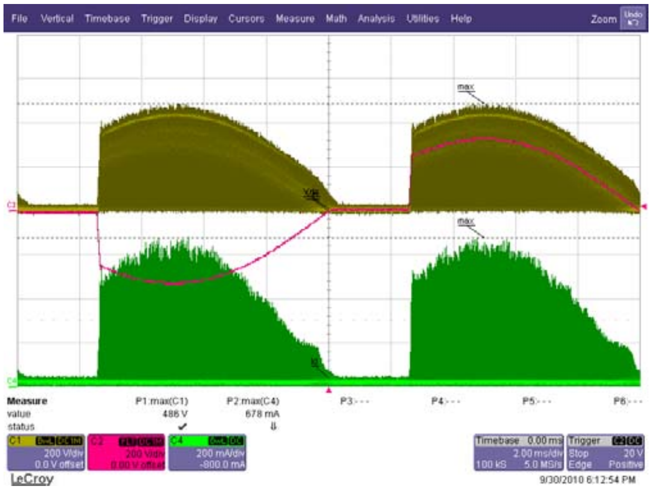

Figure 41 – 230 VAC / 50 Hz,
45º Dimming Phase Angle.
6 LED in Series (18.2 V / 350 mA)
Ch1(Yellow): V_{DS}, 200 V / div.
Ch2(Red): V_{IN}, 200 V / div.
Ch4(Green): I_{DS}, 200 mA / div., 2 ms / div.

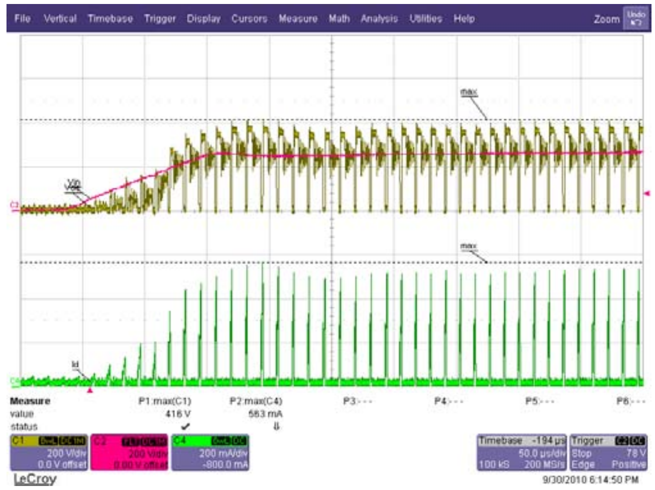

Figure 42 – 230 VAC / 50 Hz,
45º Dimming Phase Angle.
6 LED in Series (18.2 V / 350 mA)
Ch1(Yellow): V_{DS}, 200 V / div.
Ch2(Red): V_{IN}, 200 V / div.
Ch4(Green): I_{DS}, 200 mA / div., 50 µs / div.

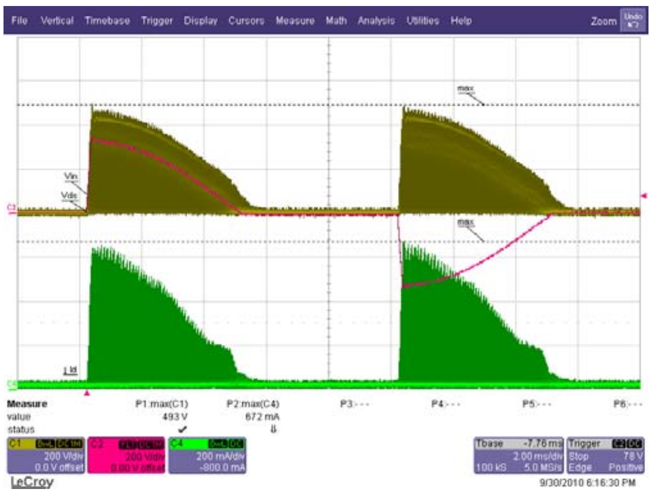

Figure 43 – 230 VAC / 50 Hz,
90º Dimming Phase Angle.
6 LED in Series (18.2 V / 350 mA)
Ch1(Yellow): V_{DS}, 200 V / div.
Ch2(Red): V_{IN}, 200 V / div.
Ch4(Green): I_{DS}, 200 mA / div., 2 ms / div.

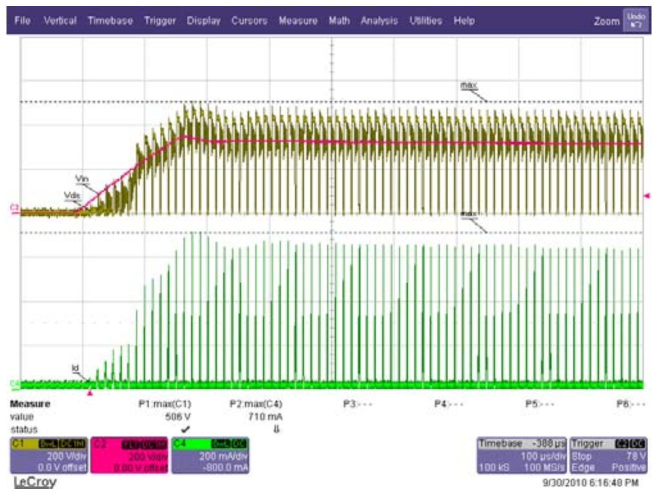

Figure 44 – 230 VAC / 50 Hz,
90º Dimming Phase Angle.
6 LED in Series (18.2 V / 350 mA)
Ch1(Yellow): V_{DS}, 200 V / div.
Ch2(Red): V_{IN}, 200 V / div.
Ch4(Green): I_{DS}, 200 mA / div., 100 µs / div.

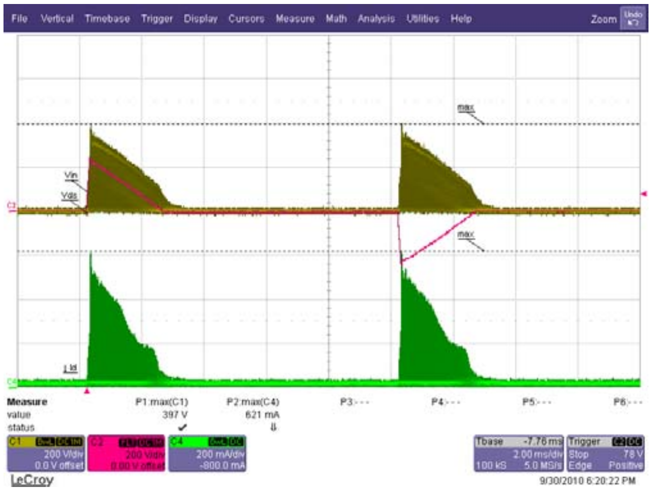

Figure 45 – 230 VAC / 50 Hz,
135º Dimming Phase Angle.
6 LED in Series (18.2 V / 350 mA)
Ch1(Yellow): V_{DS}, 200 V / div.
Ch2(Red): V_{IN}, 200 V / div.
Ch4(Green): I_{DS}, 200 mA / div., 2 ms / div.

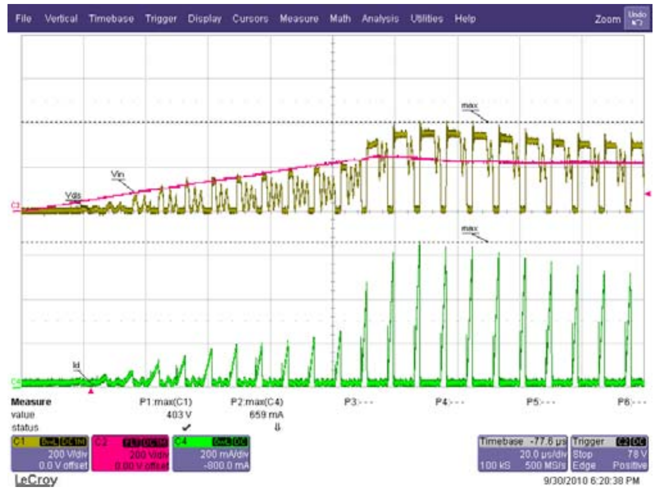

Figure 46 – 230 VAC / 50 Hz,
135º Dimming Phase Angle.
6 LED in Series (18.2 V / 350 mA)
Ch1(Yellow): V_{DS}, 200 V / div.
Ch2(Red): V_{IN}, 200 V / div.
Ch4(Green): I_{DS}, 200 mA / div., 20 µs / div.

11.1.5 Fault Conditions (Output Shorted / Open Circuit)

Figure 47 – 265 VAC.
Load Shorted.
Upper: V_{DRAIN}, 200 V / div.
Lower: I_{DRAIN}, 0.2 A / div., 2 ms / div.

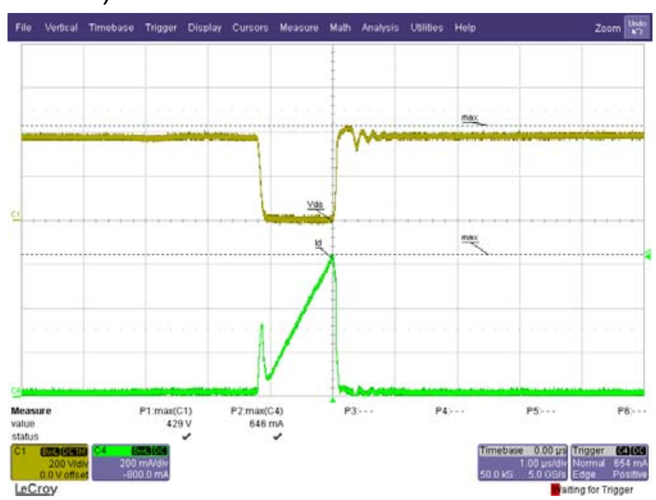

Figure 48 – 265 VAC.
Load Shorted.
Upper: V_{DRAIN}, 200 V / div.
Lower: I_{DRAIN}, 0.2 A / div., 1 µs / div.

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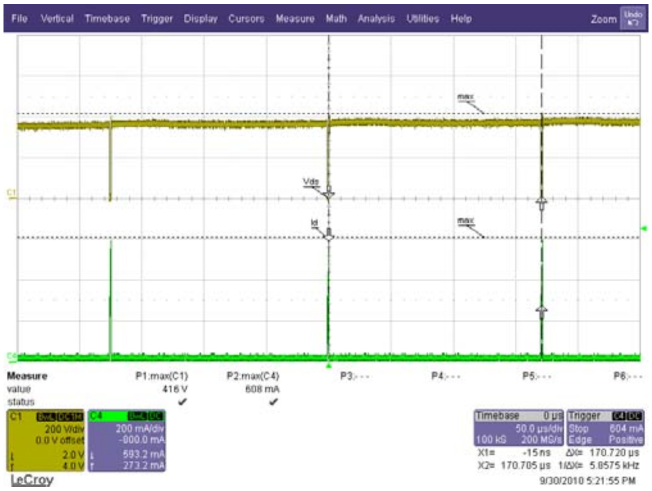

Figure 49 – 265 VAC.
Load Shorted.
Upper: V_{DRAIN}, 200 V / div.
Lower: I_{DRAIN}, 0.2 A / div., 50 µs / div.

Figure 50 – 265 VAC.
Load Open.
Ch1(Yellow): V_{DS}, 200 V / div.
Ch2(Red): V_O, 10 V / div.
Ch4(Green): I_{DS}, 200 mA / div., 20 µs / div.

11.2 Output Current Start-up Profile

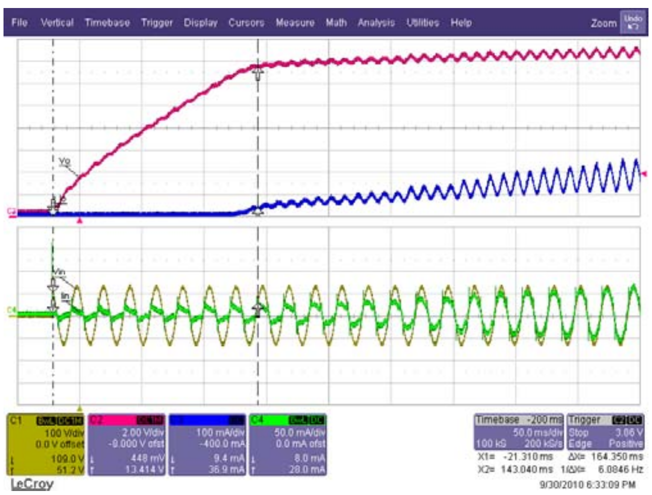

Figure 51 –90 VAC / 47 Hz.
5 LED in Series (15V).
Ch1(Yellow): V_{IN}, 100 V / div.
Ch2(Red): V_O, 2 V / div.
Ch3(Blue): I_O, 100 mA / div.
Ch4(Green): I_{IN}, 500 mA / div., 50 ms / div.

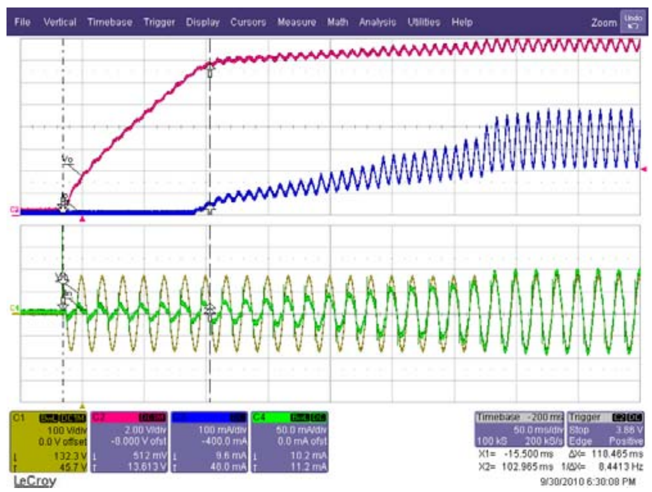

Figure 52 –115 VAC / 60 Hz.
5 LED in Series (15V).
Ch1(Yellow): V_{IN}, 100 V / div.
Ch2(Red): V_O, 2 V / div.
Ch3(Blue): I_O, 100 mA / div.
Ch4(Green): I_{IN}, 500 mA / div., 50 ms / div.

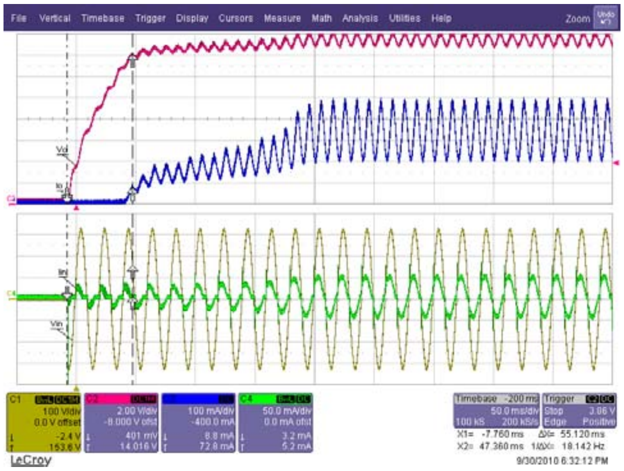

Figure 53 – 230 VAC / 50 Hz.
5 LED in Series (15 V).
Ch1(Yellow): V_{IN}, 100 V / div.
Ch2(Red): V_O, 2 V / div.
Ch3(Blue): I_O, 100 mA / div.
Ch4(Green): I_{IN}, 500 mA / div., 50 ms / div.

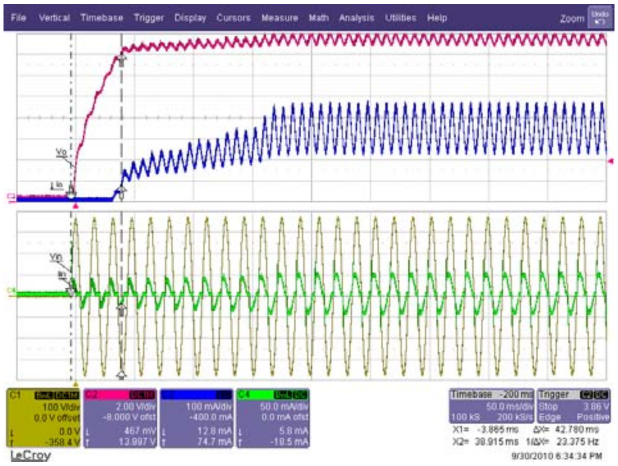

Figure 54 – 265 VAC / 63 Hz.
5 LED in Series (15 V).
Ch1(Yellow): V_{IN}, 100 V / div.
Ch2(Red): V_O, 2 V / div.
Ch3(Blue): I_O, 100 mA / div.
Ch4(Green): I_{IN}, 500 mA / div., 50 ms / div.

11.3 Input and Output Waveforms

11.3.1 Normal Operation (V_{IN}, I_{IN}, V_O and I_O)

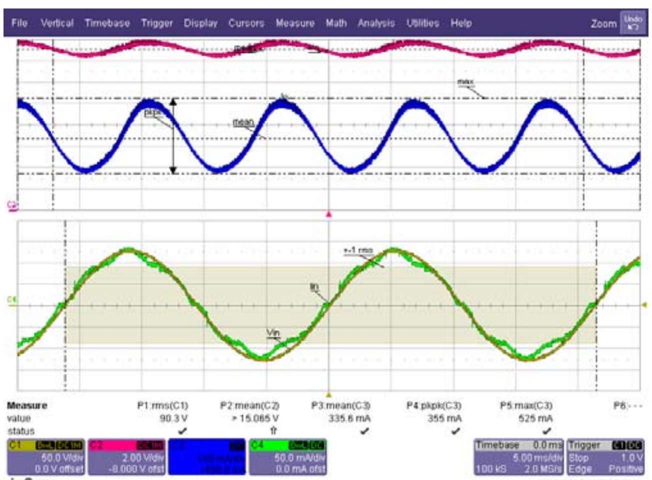

Figure 55 – 90 VAC / 47 Hz.
5 LED in Series (15 V).
Ch1(Yellow): V_{IN}, 50 V / div.
Ch2(Red): V_O, 2 V / div.
Ch3(Blue): I_O, 100 mA / div.
Ch4(Green): I_{IN}, 50 mA / div., 5 ms / div.

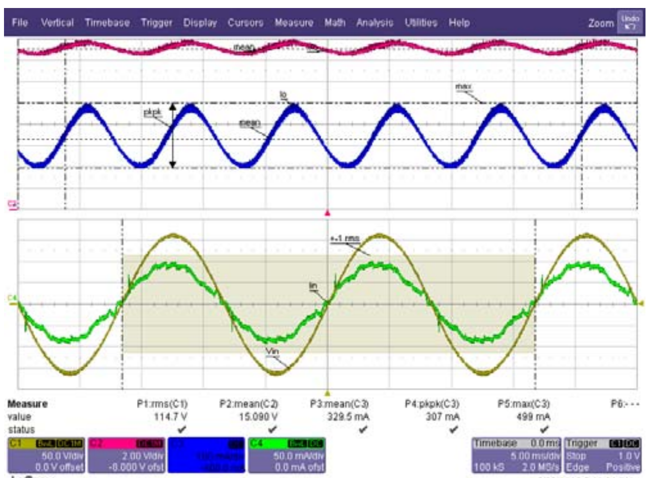

Figure 56 – 115 VAC / 60 Hz.
5 LED in Series (15 V).
Ch1(Yellow): V_{IN}, 50 V / div.
Ch2(Red): V_O, 2 V / div.
Ch3(Blue): I_O, 100 mA / div.
Ch4(Green): I_{IN}, 50 mA / div., 5 ms / div.

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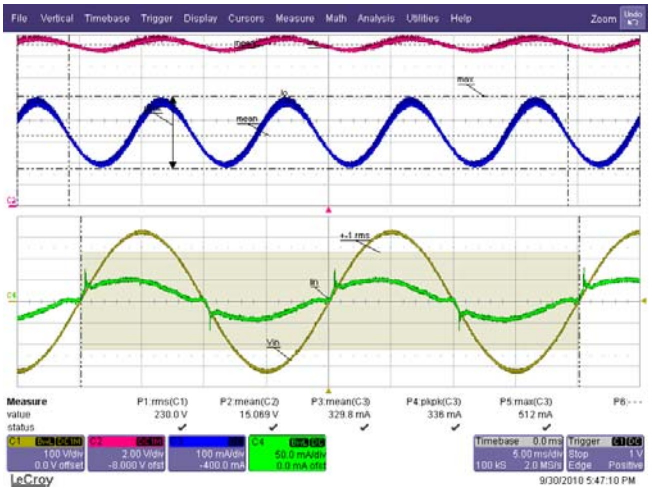

Figure 57 – 230 VAC / 50 Hz.
5 LED in Series (15 V).
Ch1(Yellow): V_{IN}, 100 V / div.
Ch2(Red): V_O, 2 V / div.
Ch3(Blue): I_O, 100 mA / div.
Ch4(Green): I_{IN}, 50 mA / div., 5 ms / div.

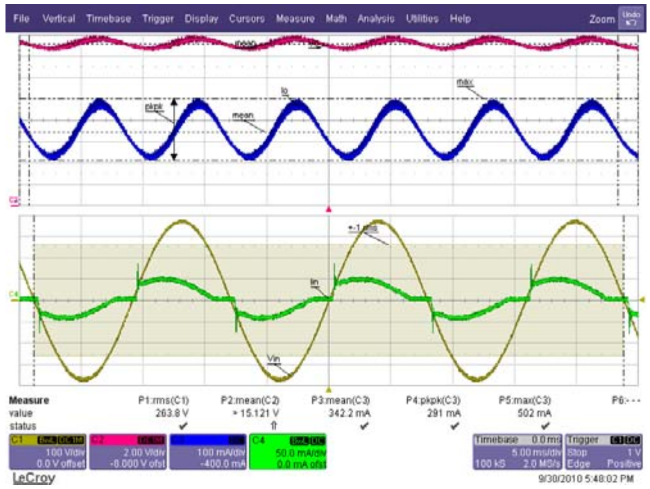

Figure 58 – 265 VAC / 63 Hz.
5 LED in Series (15 V).
Ch1(Yellow): V_{IN}, 100 V / div.
Ch2(Red): V_O, 2 V / div.
Ch3(Blue): I_O, 100 mA / div.
Ch4(Green): I_{IN}, 50 mA / div., 5 ms / div.

11.4 Dimming Operation (V_{IN}, I_{IN}, V_O and I_O)

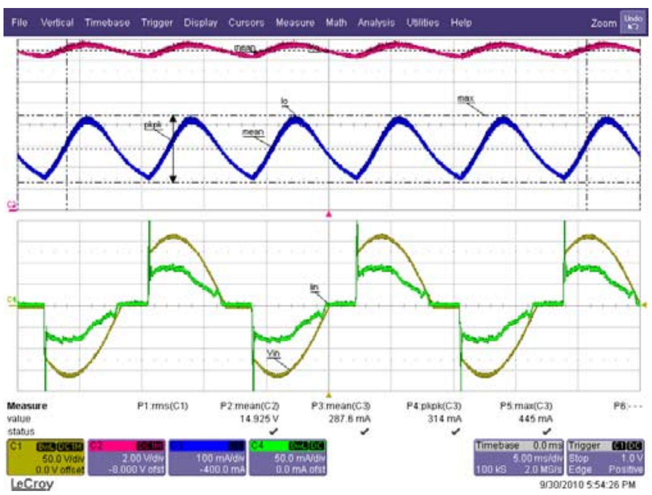

Figure 59 – 115 VAC / 60 Hz.
45º Dimming Phase Angle.
5 LED in Series (15 V).
Ch1(Yellow): V_{IN}, 50 V / div.
Ch2(Red): V_O, 2 V / div.
Ch3(Blue): I_O, 100 mA / div.
Ch4(Green): I_{IN}, 50 mA / div., 5 ms / div.

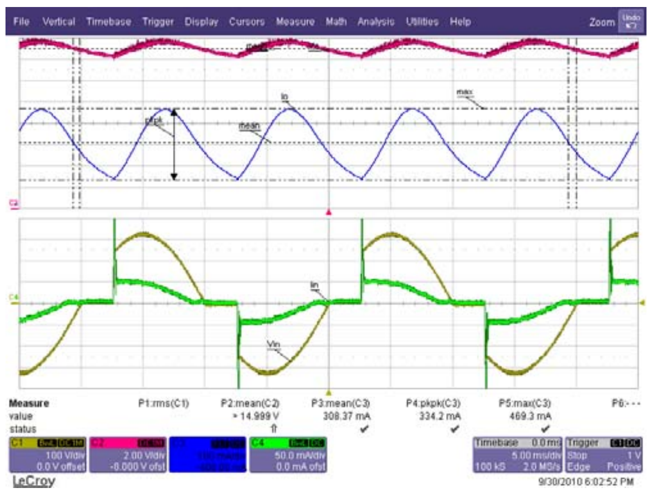

Figure 60 – 230 VAC / 50 Hz.
45º Dimming Phase Angle.
5 LED in Series (15 V).
Ch1(Yellow): V_{IN}, 100 V / div.
Ch2(Red): V_O, 2 V / div.
Ch3(Blue): I_O, 100 mA / div.
Ch4(Green): I_{IN}, 50 mA / div., 5 ms/ div.

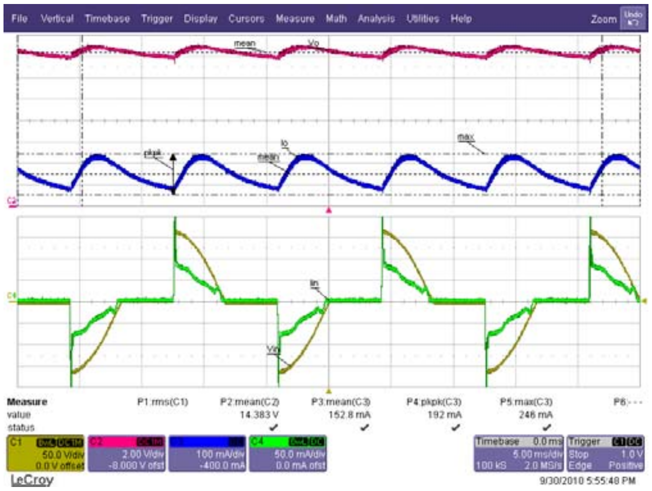

Figure 61 – 115 VAC / 60 Hz.
45º Dimming Phase Angle.
5 LED in Series (15 V)
Ch1(Yellow): V_{IN}, 50 V / div.
Ch2(Red): V_O, 2 V / div.
Ch3(Blue): I_O, 100 mA / div.
Ch4(Green): I_{IN}, 50 mA / div., 5 ms / div.

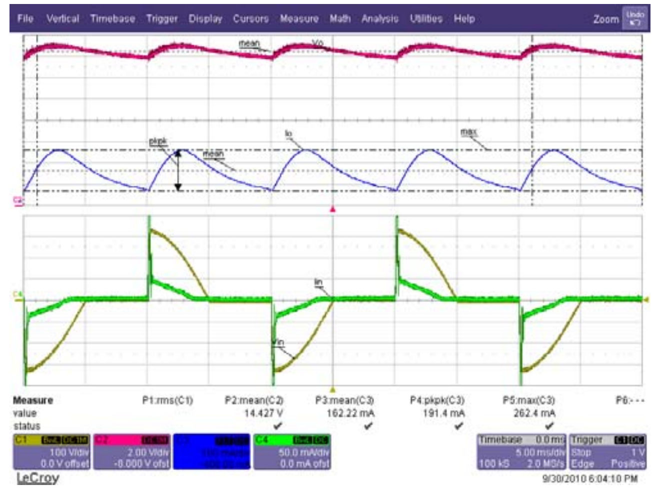

Figure 62 – 230 VAC / 50 Hz.
45º Dimming Phase Angle.
5 LED in Series (15 V)
Ch1(Yellow): V_{IN}, 100 V / div.
Ch2(Red): V_O, 2 V / div.
Ch3(Blue): I_O, 100 mA / div.
Ch4(Green): I_{IN}, 50 mA / div., 5 ms / div.

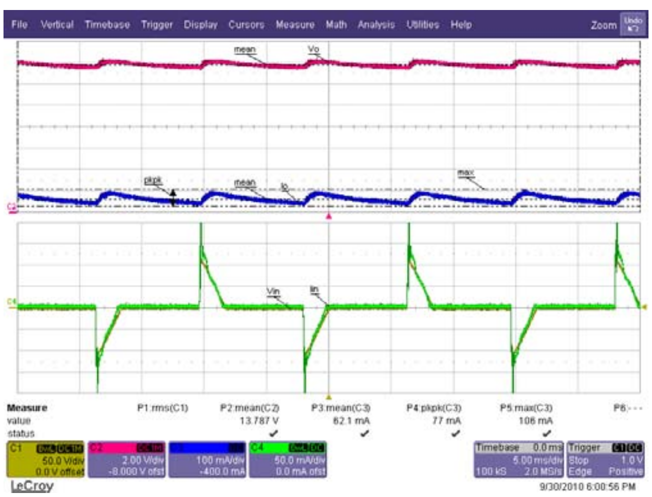

Figure 63 – 115 VAC / 60 Hz.
45º Dimming Phase Angle.
5 LED in Series (15 V)
Ch1(Yellow): V_{IN}, 50 V / div.
Ch2(Red): V_O, 2 V / div.
Ch3(Blue): I_O, 100 mA / div.
Ch4(Green): I_{IN}, 50 mA / div., 5 ms / div.

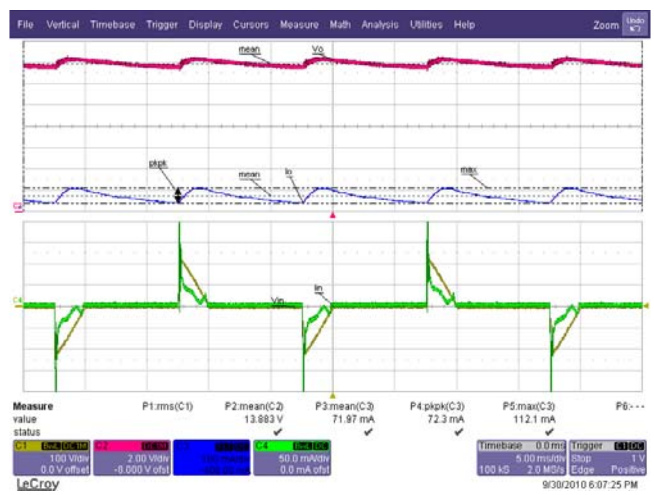

Figure 64 – 230 VAC / 50 Hz.
45º Dimming Phase Angle.
5 LED in Series (15 V)
Ch1(Yellow): V_{IN}, 100 V / div.
Ch2(Red): V_O, 2 V / div.
Ch3(Blue): I_O, 100 mA / div.
Ch4(Green): I_{IN}, 50 mA / div., 5 ms / div.

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11.5 Line Transient Response

In the figures shown below, signal averaging was used to better enable viewing the load transient response. The oscilloscope was triggered using the load current step as a trigger source. Since the output switching and line frequency occur essentially at random with respect to the load transient, contributions to the output ripple from these sources will average out, leaving the contribution only from the load step response.

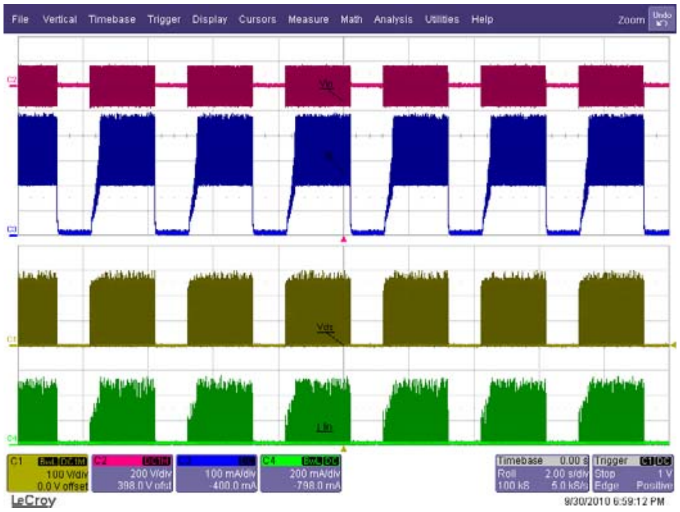

Figure 65 – 115-0-115 VAC / 60 Hz.
5 LED in Series (15 V).
Ch1(Yellow): V_{DS}, 100 V / div.
Ch2(Red): V_{IN}, 200 V / div.
Ch3(Blue): I_O, 100 mA / div.
Ch4(Green): I_{DS}, 200 mA / div., 2 s / div.

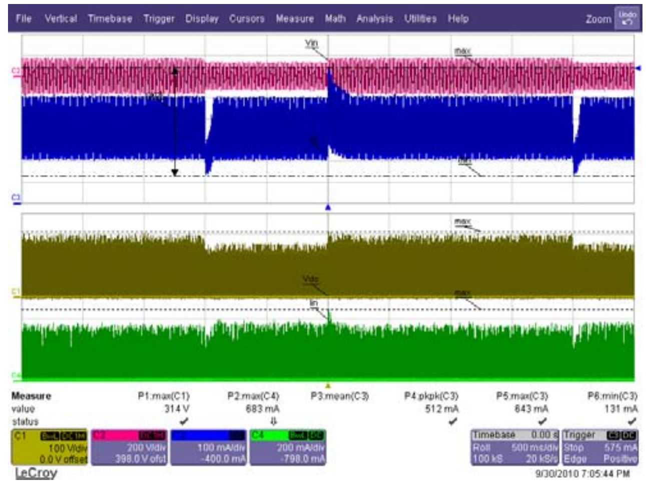

Figure 66 – 115-85-115 VAC / 60 Hz.
5 LED in Series (15 V).
Ch1(Yellow): V_{DS}, 100 V / div.
Ch2(Red): V_{IN}, 200 V / div.
Ch3(Blue): I_O, 100 mA / div.
Ch4(Green): I_{DS}, 200 mA / div., 2 s / div.

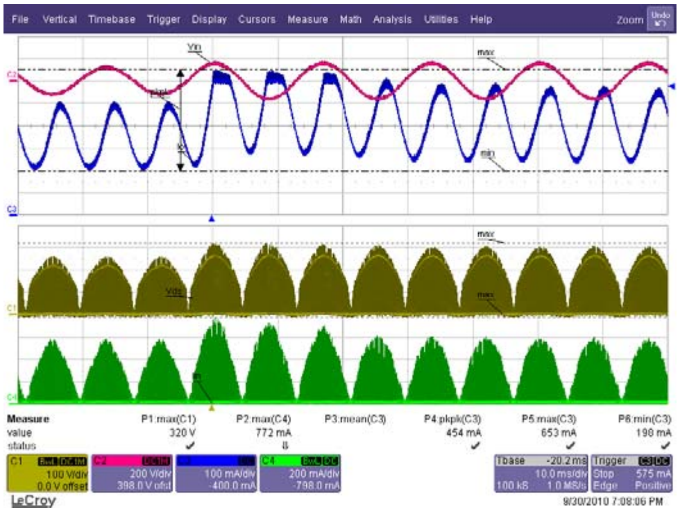

Figure 67 – 115-85-115 VAC / 60 Hz.
5 LED in Series (15 V).
Ch1(Yellow): V_{DS}, 100 V / div.
Ch2(Red): V_{IN}, 200 V / div.
Ch3(Blue): I_O, 100 mA / div.
Ch4(Green): I_{DS}, 200 mA / div., 10 ms / div.

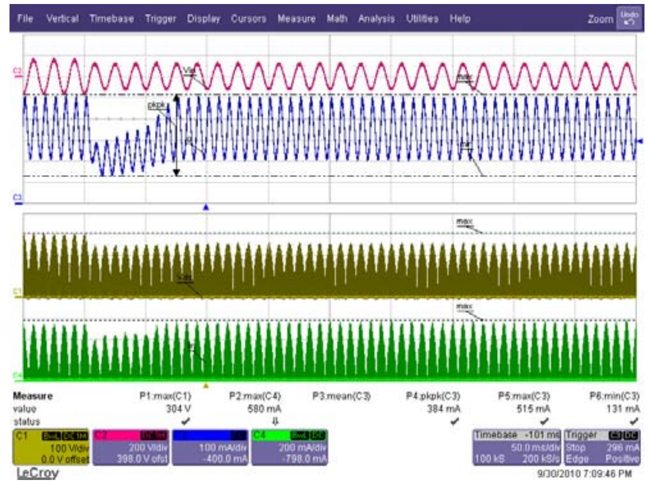

Figure 68 – 115-85-115 VAC / 60 Hz.
5 LED in Series (15 V).
Ch1(Yellow): V_{DS}, 100 V / div.
Ch2(Red): V_{IN}, 200 V / div.
Ch3(Blue): I_O, 100 mA / div.
Ch4(Green): I_{DS}, 200 mA / div., 50 ms / div

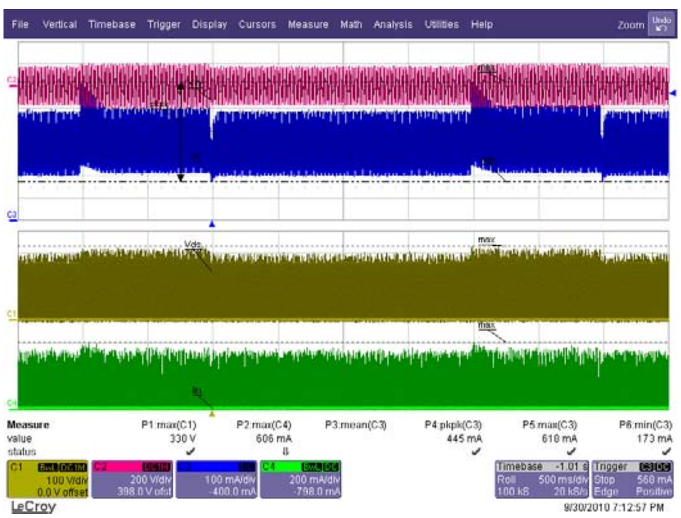

Figure 69 – 115-132-115 VAC / 60 Hz.
5 LED in Series (15 V).
Ch1(Yellow): V_{DS}, 100 V / div.
Ch2(Red): V_{IN}, 200 V / div.
Ch3(Blue): I_O, 100 mA / div.
Ch4(Green): I_{DS}, 200 mA / div., 500 ms / div.

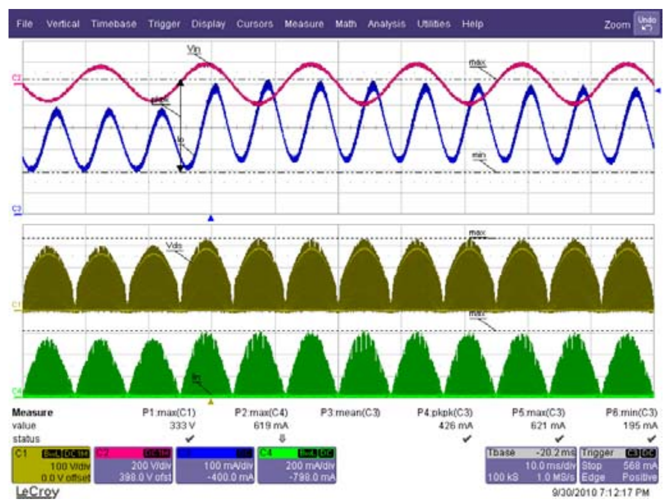

Figure 70 – 115-132-115 VAC / 60 Hz.
5 LED in Series (15 V).
Ch1(Yellow): V_{DS}, 100 V / div.
Ch2(Red): V_{IN}, 200 V / div.
Ch3(Blue): I_O, 100 mA / div.
Ch4(Green): I_{DS}, 200 mA / div., 10 ms / div.

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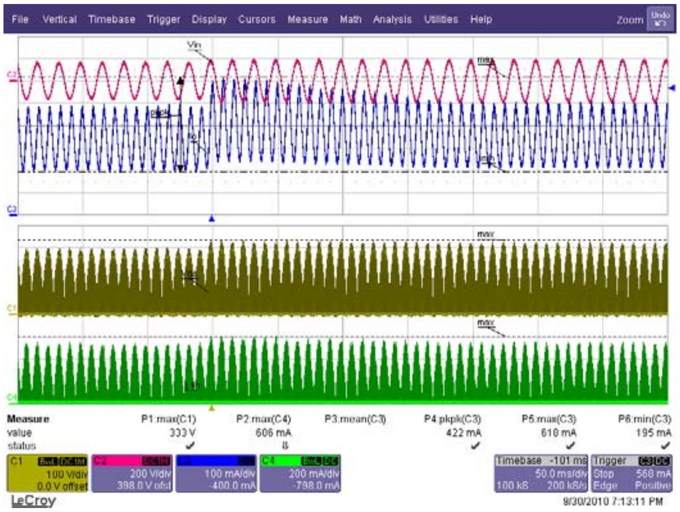

Figure 71 – 115-132-115 VAC / 60 Hz.
5 LED in Series (15 V).
Ch1(Yellow): V_{DS}, 100 V / div.
Ch2(Red): V_{IN}, 200 V / div.
Ch3(Blue): I_O, 100 mA / div.
Ch4(Green): I_{DS}, 200 mA / div., 50 ms / div.

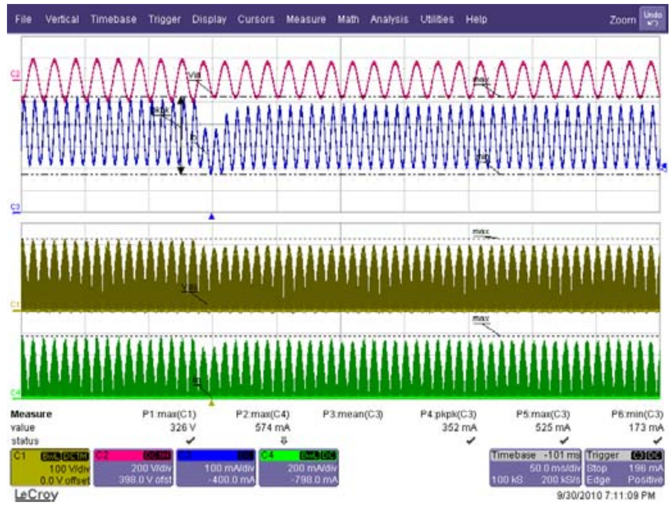

Figure 72 – 115-132-115 VAC / 60 Hz.
5 LED in Series (15 V).
Ch1(Yellow): V_{DS}, 100 V / div.
Ch2(Red): V_{IN}, 200 V / div.
Ch3(Blue): I_O, 100 mA / div.
Ch4(Green): I_{DS}, 200 mA / div., 50 ms / div.

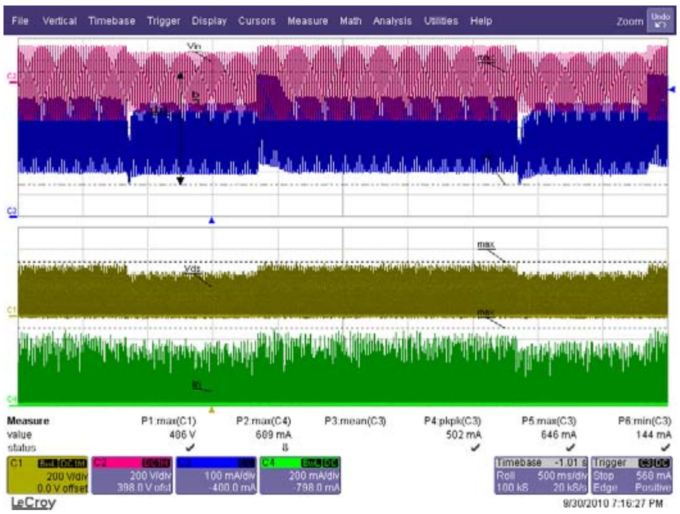

Figure 73 – 230-180-230 VAC / 50 Hz.
5 LED in Series (15 V).
Ch1(Yellow): V_{DS}, 200 V / div.
Ch2(Red): V_{IN}, 200 V / div.
Ch3(Blue): I_O, 100 mA / div.
Ch4(Green): I_{DS}, 200 mA / div., 50 ms / div.

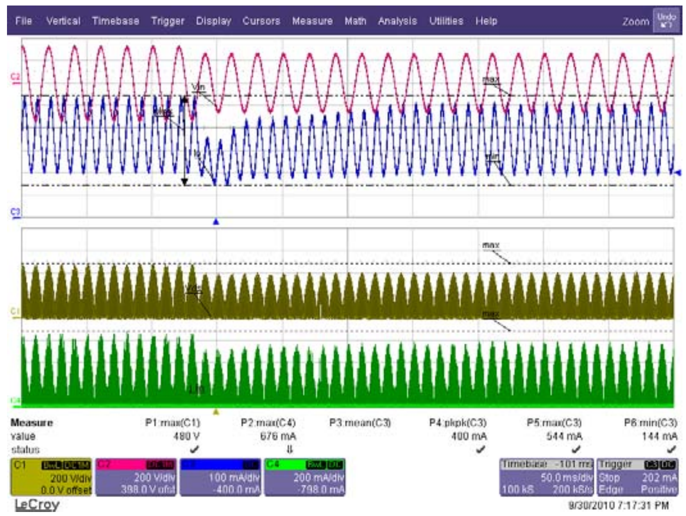

Figure 74 – 230-180-230 VAC / 50 Hz.
5 LED in Series (15 V).
Ch1(Yellow): V_{DS}, 200 V / div.
Ch2(Red): V_{IN}, 200 V / div.
Ch3(Blue): I_O, 100 mA / div.
Ch4(Green): I_{DS}, 200 mA / div., 50 ms / div.

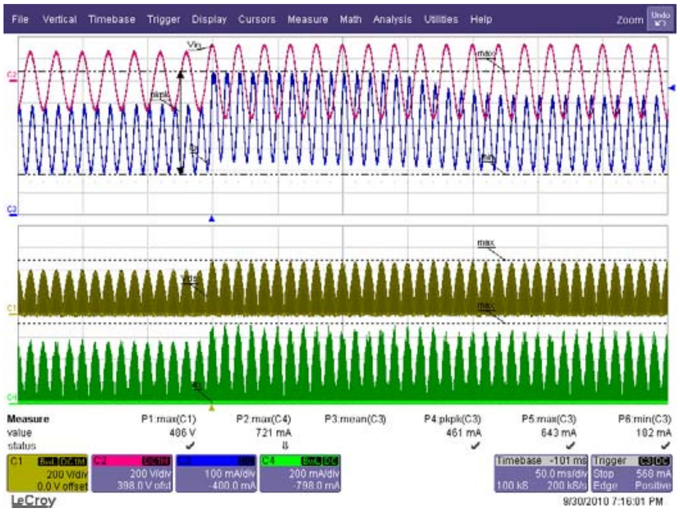

Figure 75 – 230-180-230 VAC / 50 Hz.
5 LED in Series (15 V).
Ch1(Yellow): V_{DS}, 200 V / div.
Ch2(Red): V_{IN}, 200 V / div.
Ch3(Blue): I_O, 100 mA / div.
Ch4(Green): I_{DS}, 200 mA / div., 50 ms / div.

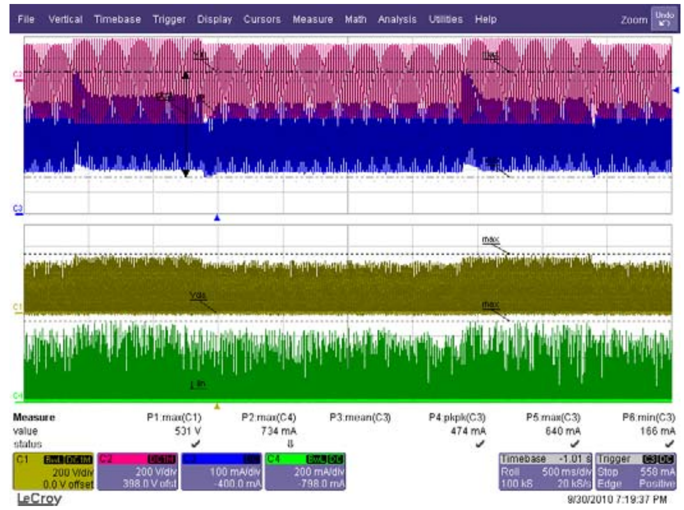

Figure 76 – 230-265-230 VAC / 50 Hz.
5 LED in Series (15 V).
Ch1(Yellow): V_{DS}, 200 V / div.
Ch2(Red): V_{IN}, 200 V / div.
Ch3(Blue): I_O, 100 mA / div.
Ch4(Green): I_{DS}, 200 mA / div., 50ms / div.

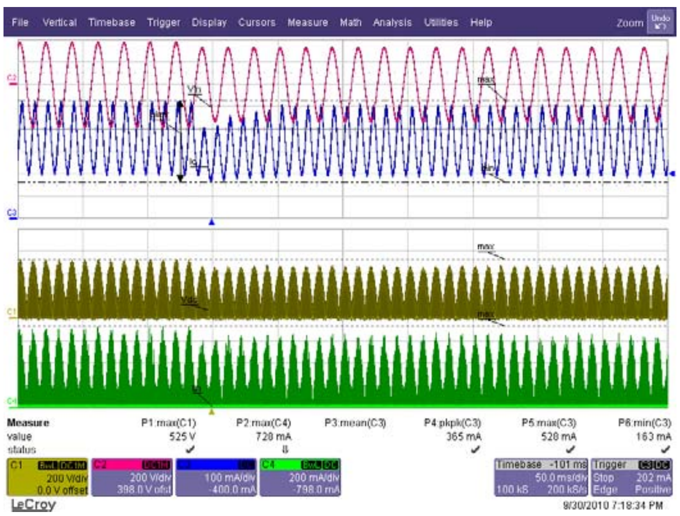

Figure 77 – 230-180-230 VAC / 50 Hz.
5 LED in Series (15 V).
Ch1(Yellow): V_{DS}, 200 V / div.
Ch2(Red): V_{IN}, 200 V / div.
Ch3(Blue): I_O, 100 mA / div.
Ch4(Green): I_{DS}, 200 mA / div., 50 ms / div.

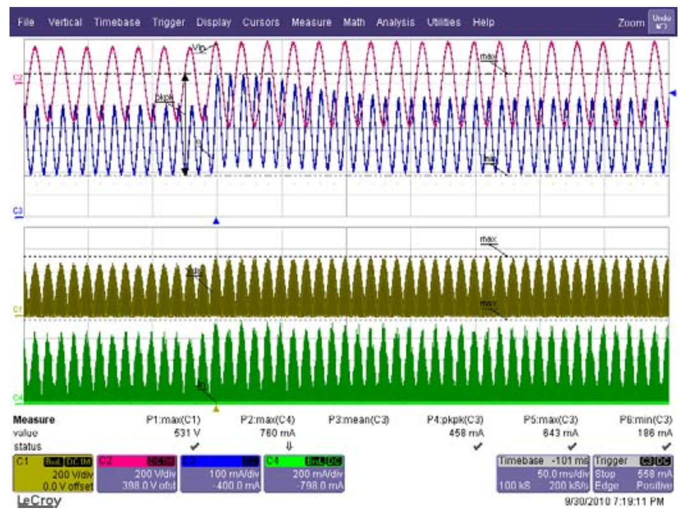

Figure 78 – 230-265-230 VAC / 50 Hz.
5 LED in Series (15 V).
Ch1(Yellow): V_{DS}, 200 V / div.
Ch2(Red): V_{IN}, 200 V / div.
Ch3(Blue): I_O, 100 mA / div.
Ch4(Green): I_{DS}, 200 mA / div., 50 ms / div.

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12 Line Surge

Differential input line 1.2/50 µs surge testing was completed on a single test unit to IEC61000-4-5. Input voltage was set at 230 VAC / 60 Hz. Output was loaded with 5 LED in series (14.5 V / 350 mA) and operation was verified following each surge event.

Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Surge Type	Test Result (Pass/Fail)
+500	230	L1 to L2	90	Line	Pass
-500	230	L1 to L2	90	Line	Pass
+2500	230	L1 to L2	90	Ring Wave (200 A)	Pass
-2500	230	L1 to L2	90	Ring Wave (200 A)	Pass

Unit passed all test conditions.

13 Conducted EMI

13.1 Equipment:

Receiver:

Rohde & Schwarz
ESPI - Test Receiver (9 kHz – 3 GHz)
Model No: ESPI3

LISN:

Rohde & Scharrz
Two-Line-V-Network
Model No: ENV216

13.2 EMI Test Set-up

LED driver is placed in a conical metal housing (for self-ballasted lamps; CISPR15 Edition 7.2).

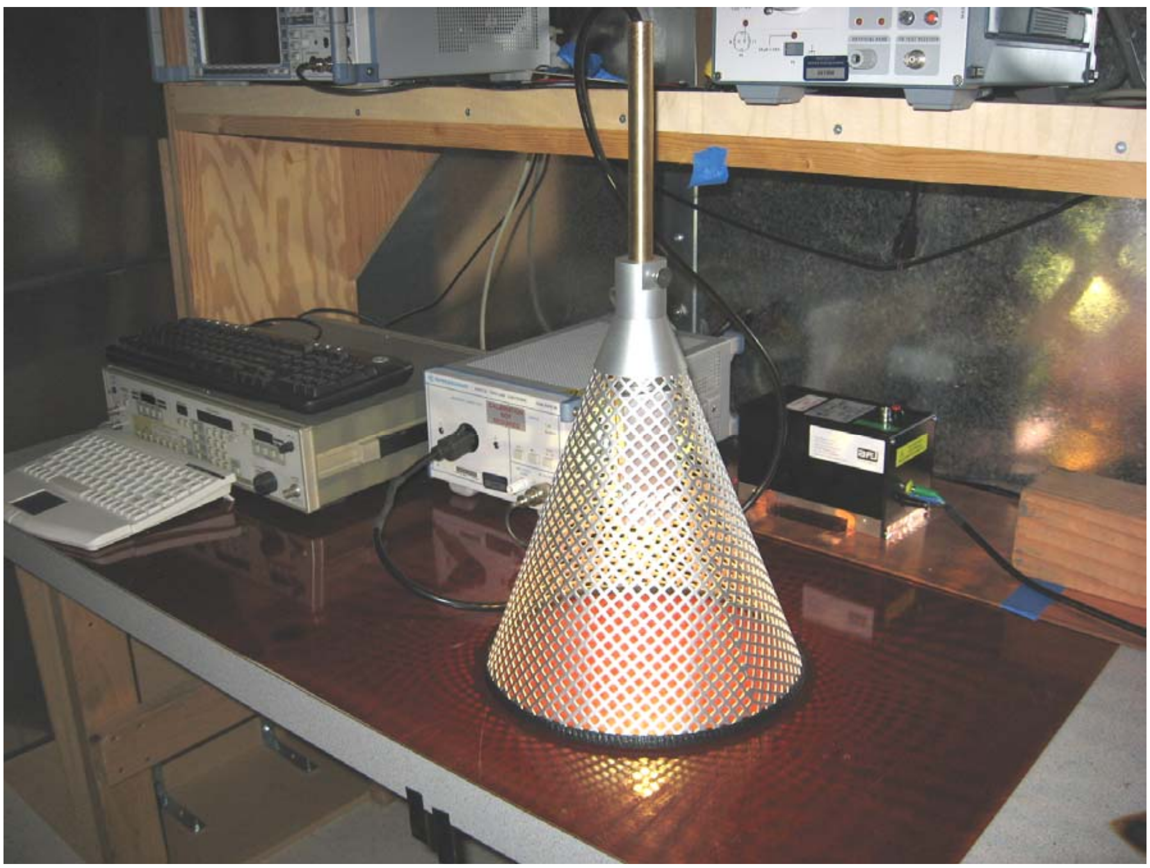

Figure 79 – Conducted Emissions Measurement Set-up
Showing Conical Ground Plane Inside which UUT was Mounted.

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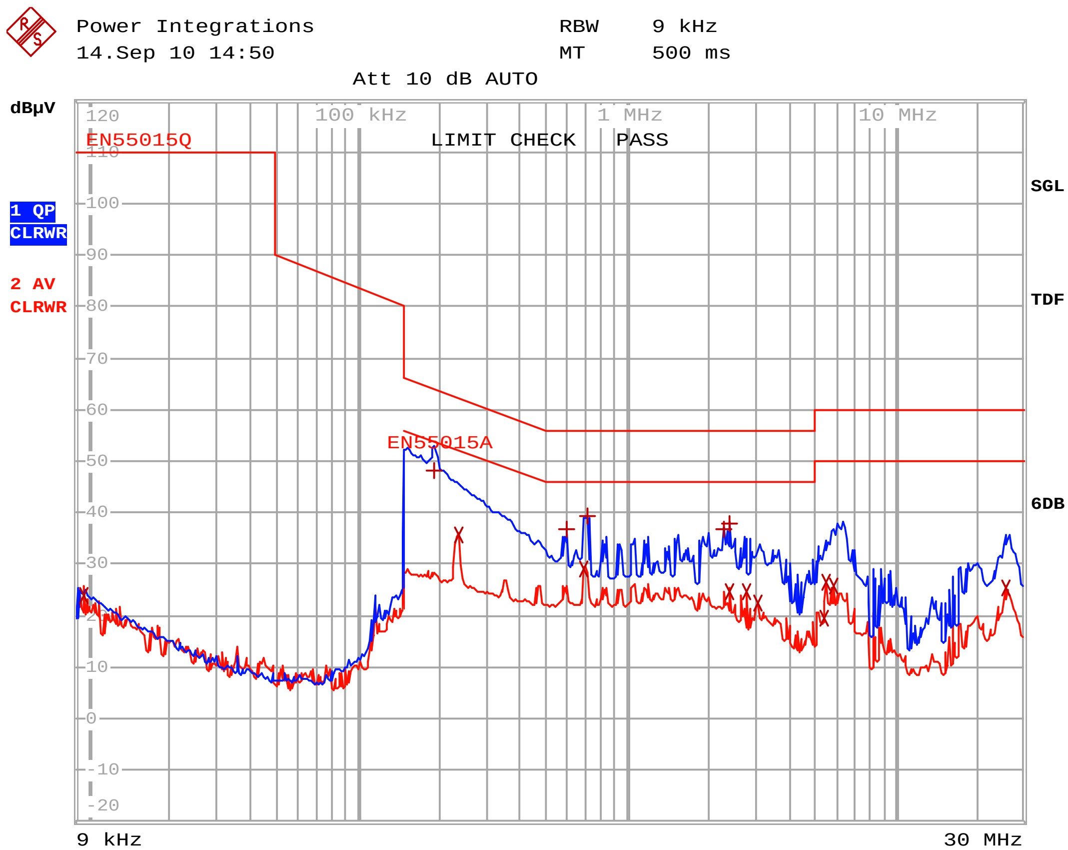

Figure 80– Pre-scan Conducted EMI, Maximum Steady State Load, 115 VAC, 60 Hz, and EN55015 Limits. Note Blue Line is Peak Result vs. QP Limit Line – Refer to Table for QP Margin.

EDIT PEAK LIST (Final Measurement Results)				
Trace1:	EN55015Q			
Trace2:	EN55015A			
Trace3:	---			
TRACE		FREQUENCY	LEVEL dBµV	DELTA LIMIT dB
2	Average	9.55368135541 kHz	23.74 N gnd	
1	Quasi Peak	192.364799253 kHz	48.15 L1 gnd	-15.78
2	Average	234.721612085 kHz	35.78 N gnd	-16.49
1	Quasi Peak	598.084042089 kHz	36.58 N gnd	-19.41
2	Average	694.357005568 kHz	29.14 N gnd	-16.85
1	Quasi Peak	708.31358138 kHz	39.40 N gnd	-16.59
1	Quasi Peak	2.29164676133 MHz	36.68 N gnd	-19.31
1	Quasi Peak	2.40854377744 MHz	37.70 N gnd	-18.29
2	Average	2.40854377744 MHz	24.64 N gnd	-21.35
2	Average	2.76855896362 MHz	24.55 N gnd	-21.44
2	Average	3.08879360159 MHz	22.42 N gnd	-23.57
2	Average	5.39244619915 MHz	19.52 N gnd	-30.48
2	Average	5.50083436776 MHz	26.60 N gnd	-23.39
2	Average	5.89763899176 MHz	25.57 N gnd	-24.42
2	Average	25.7182553901 MHz	25.22 N gnd	-24.77

Table 4 – Conducted EMI, Maximum Steady State Load, 115 VAC, 60 Hz, and EN55015 Margin.

Figure 81 – Pre-scan Conducted EMI, Maximum Steady State Load, 230 VAC, 60 Hz, and EN55015 Limits. Note Blue Line is Peak Result vs. QP Limit Line – Refer to Table for QP Margin.

EDIT PEAK LIST (Final Measurement Results)			
Trace1:	EN55015Q		
Trace2:	EN55015A		
Trace3:	---		
TRACE	FREQUENCY	LEVEL dBµV	DELTA LIMIT dB
2 Average	9.74571035065 kHz	22.61 N gnd	
2 Average	140.262531674 kHz	29.46 N gnd	
2 Average	147.417330442 kHz	29.17 L1 gnd	
2 Average	150 kHz	38.55 L1 gnd	-17.44
2 Average	214.615317539 kHz	34.76 N gnd	-18.26
1 Quasi Peak	774.672132397 kHz	37.07 N gnd	-18.92
2 Average	2.20222749414 MHz	24.22 N gnd	-21.77
2 Average	4.83337742374 MHz	24.00 N gnd	-21.99
2 Average	4.97983359306 MHz	24.81 N gnd	-21.18
2 Average	5.07992824828 MHz	25.47 N gnd	-24.53
2 Average	26.2351923234 MHz	23.25 N gnd	-26.75

Table 5 – Conducted EMI, Maximum Steady State Load, 230 VAC, 60 Hz, and EN55015 Margin.

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14 Dimming Compatibility

The operation of a single unit was tested with the dimmers listed in the table below.

Test Voltage	Test Freq	Power Rating		Manufacturer	Part Number	Dimmer Type	Application/ Remarks	Single Unit		2 Units in Parallel	
		Min	Max					Min (mA)	Max (mA)	Min (mA)	Max (mA)
115 V	60 Hz	N.S.	500 W	DIING CHUNG	WS-5005	TRIAC	Wide angle operation	0.024	360	0.083	352.2
115 V	60 Hz	N.S.	600W	Lutron	TGLV-600PR	TRIAC	Limited angle operation	7.6	286.9	16.4	296.7
115 V	60 Hz	N.S.	600 W	Lutron (Skylark)	S-600PR-WH	TRIAC	Limited angle operation	1.5	286	6.89	298
115 V	60 Hz	N.S.		Smartlabs	2476D	Electronic	Electronic dimmer	2.66	324	0.082	320.6
115 V	60 Hz	N.S.	800W	Hsien Long Co.,Ltd	Y-25082A	TRIAC	Incandescent / Halogen	0.036	357.3	0.014	352
115 V	60 Hz	N.S.	300 W	Leviton	6615-POW	Electronic Low Voltage	Trailing edge dimmer	91.8	365.8	82.9	354.1
115 V	60 Hz	N.S.	600 W	Lutron	D-600R-WH	Triac		0.008	282.6	0.008	282.2
100 V	60 Hz	40 W	400 W	Panasonic	WN575149	TRIAC		***	***	14.16	294.4
100 V	60 Hz	40 W	500 W	Panasonic	WT57615K	TRIAC		***	***	22.54	303.9
100 V	60 Hz	40 W	500 W	Toshiba	NWD9051	TRIAC		***	***	1.75	331.1
110 V	60 Hz		500 W	Songkung				***	***	2.843	346.4
230 V		40 W	500 W	Relco	RTM 34LED DAX S	Two way switch - MOS-FET; built-in soft-start	Incandescent Electronic transformer Electro-mechanical transformer	25.14	284.9	21.91	281.1
230 V	50 Hz	40 W	160 W	Relco	RM34DMA	TRIAC	Incandescent	***	***	87.5*	362 *
230 V	50 Hz	100 W	500 W	Relco	RT34DMA			***	***	78.1 **	347**
230 V	50 Hz				RH34LED	Electronic	Trailing edge dimmer	8.31	381	2.23	375.9
230 V	50 Hz	40 W	300 W	Relco	RTS 34.43 RLI	TRIAC	Incandescent	***	***	36.29 **	353.8**
230 V	50 Hz	100 W	500 W	Relco	RT34DSL	TRIAC (DIAC in gate, 2 1.2mH in series to TRIAC, 150nF across terminals of dimmer)	High power Incandescent	***	***	76.2**	363**
230 V	50 Hz			Clipmei				1	347	0.79	359.3

Note:

**** Holding current of dimmer is well above the drawn current of UUT
** 6 units in parallel
* 3 units in parallel
N.S. – Not Specified.

15 Output Current Production Distribution

Figure 82 shows the production distribution of output current for 267 RD251 boards. The data was gathered using a NH Research 5600 series power supply test system, commonly used in the power supply industry for production testing of power supplies. The data is also summarized in table 6.

Measurements were made at room temperature, V_O of 16 V and input voltages of 115 VAC and 230 VAC. This distribution includes variations not only from the LinkSwitch-PL devices but also all the components of the driver.

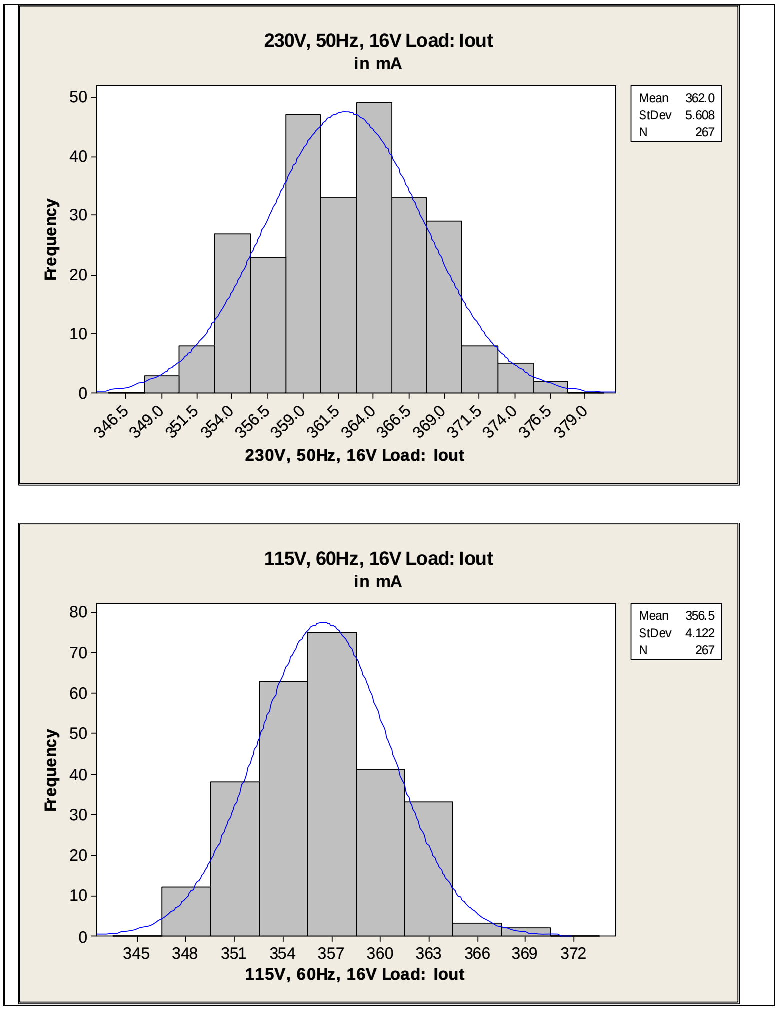

Figure 82 – Output current distribution plot for RD251

From the data it can be seen that the output current could be centered slightly (-1.9% at 115 VAC) to achieve the 350 mA nominal output current by adjusting the output current sense resistor value. Therefore to correctly demonstrate the achievable tolerance of the design, C_P values were calculated versus C_{PK}. C_P provides process capability

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when the distribution is centered (C_P=C_{PK} for a centered process) such as would be the case if the sense resistor were adjusted.

Output current tolerance values are given based on C_P of 1.33, 1.5, and 1.67. A value of 1.33 is typical for high volume production. A value of 1.5 is generally considered to indicate a 6 sigma process (allowing for a 1.5 sigma drift from the mean with a C_P of 2).

For reference Table 7 shows the expected PPM fallout rate for a given C_P/C_{PK} value.

Input Voltage (VAC)	Mean (mA)	σ (mA)	I_O Tolerance for given C_P Value		
			C_P=1.33	C_P=1.5	C_P=1.67
115	356.5	4.12	±4.7%	±5.3%	±5.9%
230	362.0	5.61	±6.4%	±7.2%	±8%

Table 6 - Output current tolerance vs C_P value

C_{PK}	Sigma	PPM
1	3	2700
1.33	4	64
1.5	4.5	7
1.67	5	1

Table 7 – PPM Fallout rate vs C_{PK} value

The data in Table 6 shows that the design meets the +/-7% target specification with a C_P of >1.33. In additional the design is capable of meeting a tolerance specification of < +/-5% at low line.

16 Revision History

Date	Author	Revision	Description & changes	Reviewed
20-Oct-10	JDC	1.8	Initial Release	Apps & Mktg
14-Dec-10	JDC	1.9	BOM Updated	Apps & Mktg
03-Feb-11	PV	1.91	Production distribution of output current added (section 15).	Apps & Mktg
15-Feb-11	PV	1.92	Edited distribution test	

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