Data Sheet | October 16, 2008 | FN2809.8

16-Bit Numerically Controlled Oscillator

The Intersil HSP45106 is a high performance 16-bit quadrature Numerically Controlled Oscillator (NCO16). The NCO16 simplifies applications requiring frequency and phase agility such as frequency-hopped modems, PSK modems, spread spectrum communications, and precision signal generators. As shown in the block diagram, the HSP45106 is divided into a Phase/Frequency Control Section (PFCS) and a Sine/Cosine Section.

The inputs to the Phase/Frequency Control Section consist of a microprocessor interface and individual control lines. The frequency resolution is 32 bits, which provides for resolution of better than 0.008Hz at 33MHz. User programmable center frequency and offset frequency registers give the user the capability to perform phase coherent switching between two sinusoids of different frequencies. Further, a programmable phase control register allows for phase control of better than 0.006°. In applications requiring up to 8-level PSK, three discrete inputs are provided to simplify implementation.

The output of the PFCS is a 28-bit phase which is input to the Sine/Cosine Section for conversion into sinusoidal amplitude. The outputs of the Sine/Cosine Section are two 16-bit quadrature signals. The spurious free dynamic range of this complex vector is greater than 90dBc.

For added flexibility when using the NCO16 in conjunction with DACs, a choice of either parallel or serial outputs with either two's complement or offset binary encoding is provided. In addition, a synchronization signal is available which indicates serial word boundaries.

Features

- 25.6MHz, 33MHz Versions
- 32-Bit Center and Offset Frequency Control
- 16-Bit Phase Control
- 8-Level PSK Supported Through Three Pin Interface
- Simultaneous 16-Bit Sine and Cosine Outputs
- Output in Two's Complement or Offset Binary
- <0.008Hz Tuning Resolution at 33MHz
- Serial or Parallel Outputs
- Spurious Frequency Components <-90dBc
- 16-Bit Microprocessor Compatible Control Interface
- Pb-Free available (RoHS compliant)

Applications

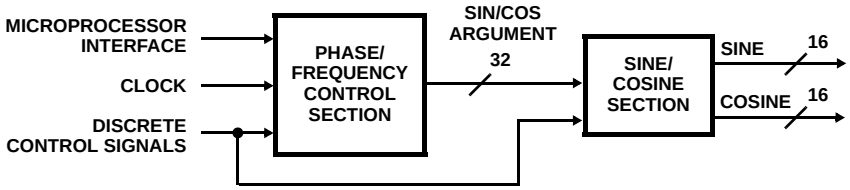
- Direct Digital Synthesis
- Quadrature Signal Generation
- Spread Spectrum Communications
- PSK Modems
- Modulation - FM, FSK, PSK (BPSK, QPSK, 8PSK)
- Frequency Hopping Communications
- Precision Signal Generation
- Related Products
  - Use with Data Acquisition Parts HI5731 or HI5741

Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
HSP45106JC-25	HSP45106JC-25	0 to +70	84 Ld PLCC	N84.1.15
HSP45106JC-25Z (Note)	HSP45106JC-25Z	0 to +70	84 Ld PLCC (Pb-free)	N84.1.15
HSP45106JC-33	HSP45106JC-33	0 to +70	84 Ld PLCC	N84.1.15
HSP45106JC-33Z (Note)	HSP45106JC-33Z	0 to +70	84 Ld PLCC (Pb-free	N84.1.15

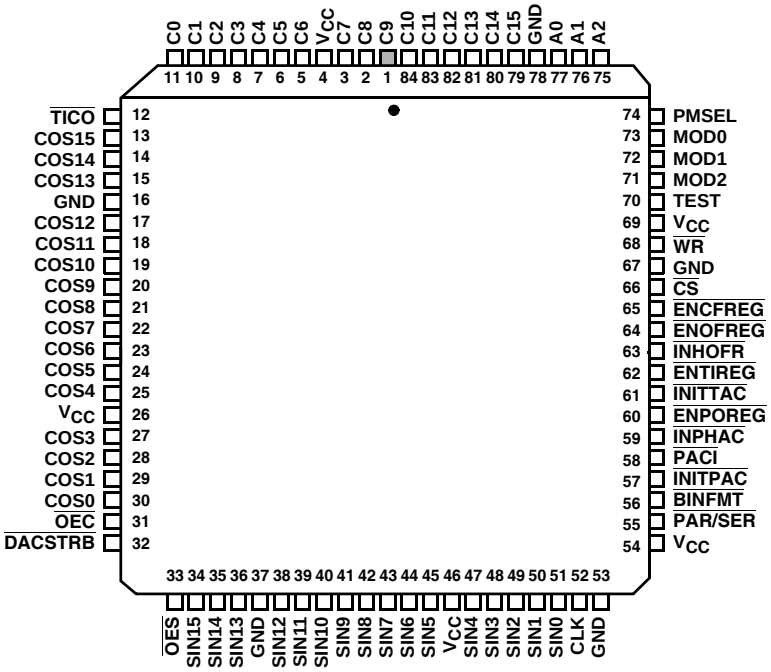
NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Block Diagram



Pinouts

HSP45106
(84 LD PLCC)
TOP VIEW



Pin Descriptions

NAME	TYPE	DESCRIPTION
V_{CC}		+5 power supply pin.
GND		Ground.
C(15:0)	I	Control input bus for loading phase, frequency, and timer data into the PFCS. C0 is LSB.
A(2:0)	I	Address pins for selecting destination of C(15:0) data (Table 2). A0 is the LSB
$\overline{CS}$	I	Chip select (active low). Enables data to be written into Control Registers by $\overline{WR}$.
$\overline{WR}$	I	Write enable (active low). Data is clocked into the register selected by A(2:0) on the rising edge of $\overline{WR}$ when $\overline{CS}$ is low.
CLK	I	Clock. All registers, except the Control Registers clocked with $\overline{WR}$, are clocked (when enabled) by the rising edge of CLK.
$\overline{ENPOREG}$	I	Phase Offset Register Enable (active low). Registered on chip by CLK. When active, after being clocked onto chip, $\overline{ENPOREG}$ enables the clocking of data into the Phase Offset Register. Allows ROM address to be updated regardless of $\overline{ENPHAC}$.
$\overline{ENOFREG}$	I	Offset Frequency Register Enable (active low). Registered on chip by CLK. When active, after being clocked onto chip, $\overline{ENOFREG}$ enables the clocking of data into the Offset Frequency Register.
$\overline{ENCFREG}$	I	Center Frequency Register Enable (active low). Registered on chip by CLK. When active, after being clocked onto chip, $\overline{ENCFREG}$ enables the clocking of data into the Center Frequency Register.

Pin Descriptions (Continued)

NAME	TYPE	DESCRIPTION
$\overline{\text{ENPHAC}}$	I	Phase Accumulator Register Enable (active low). Registered on chip by CLK. When active, after being clocked onto chip, $\overline{\text{ENPHAC}}$ enables the clocking of data into the Phase Accumulator Register.
$\overline{\text{ENTIREG}}$	I	Timer Increment Register Enable (active low). Registered on chip by CLK. When active, after being clocked onto chip, $\overline{\text{ENTIREG}}$ enables the clocking of data into the Timer Increment Register.
$\overline{\text{INHOFR}}$	I	Inhibit Offset Frequency Register Output (active low). Registered on chip by CLK. When active, after being clocked onto chip, $\overline{\text{INHOFR}}$ zeroes the data path from the Offset Frequency Register to the Frequency Adder. New data can be still clocked into the Offset Frequency Register. $\overline{\text{INHOFR}}$ does not affect the contents of the register.
$\overline{\text{INITPAC}}$	I	Initialize Phase Accumulator (active low). Registered on chip by CLK. Zeroes the feedback path in the Phase Accumulator. Does not clear the Phase Accumulator Register.
MOD(2:0)	I	Modulation Control Inputs. When selected with the PMSEL line, these bits add an offset of 0, 45, 90, 135, 180, 225, 270, or 315 degrees to the current phase (i.e., modulate the output). The lower 13 bits of the phase control are set to zero. These bits are registered when the Phase Offset Register is enabled.
PMSEL	I	Phase Modulation Select input. Registered on-chip by CLK. This input determines the source of the data clocked into the Phase Offset Register. When high, the Phase Input Register is selected. When low, the external modulation pins (MOD(2:1)) control the three most significant bits of the Phase Offset Register and the 13 least significant bits are set to zero.
$\overline{\text{PACI}}$	I	Phase Accumulator Carry Input (active low). Registered on-chip by CLK.
$\overline{\text{INITTAC}}$	I	Initialize Timer Accumulator (active low). This input is registered on chip by CLK. When active, after being clocked onto chip, $\overline{\text{INITTAC}}$ enables the clocking of data into the Timer increment Register, and also zeroes the feedback path in the Timer Accumulator.
TEST	I	Test Select Input. Registered on chip by CLK. This input is active high. When active, this input enables test busses to the outputs instead of the sine and cosine data.
$\overline{\text{PAR/SER}}$	I	Parallel/Serial Output Select. This input is registered on chip by CLK. When low, the sine and cosine outputs are in serial mode. The Output Shift Registers will load in new data after $\overline{\text{ENPHAC}}$ goes low and will start shifting the data out after $\overline{\text{ENPHAC}}$ goes high. When this input is high, the Output Registers are loaded every clock and no shifting takes place.
$\overline{\text{BINFMT}}$	I	Format. This input is registered on chip by CLK. When low, the MSB of the SIN and COS are inverted to form an offset binary (unsigned) number.
$\overline{\text{OES}}$	I	Three-state control for bits SIN(15:0). Outputs are enabled when $\overline{\text{OES}}$ is low.
$\overline{\text{OEC}}$	I	Three-state control for bits COS(15:0). Outputs are enabled when $\overline{\text{OEC}}$ is low.
$\overline{\text{TICO}}$	O	Timer Accumulator Carry Output. Active low, registered. This output goes low when a carry is generated by the Timer Accumulator.
$\overline{\text{DACSTRB}}$	O	DAC Strobe (active low). In serial mode, this output will go low when the first bit of a new output word is valid at the shift register output. This pin is active only in serial mode.
SIN(15:0)	O	Sine Output Data. When parallel mode is enabled, data is output on SIN(15:0). When serial mode is enabled, output data bits are shifted out of SIN15 and SIN0. The bit stream on SIN15 is provided MSB first while the bit stream on SIN0 is provided LSB first.
COS(15:0)	O	Cosine Output Data. When parallel mode is enabled, data is output on COS(15:0). When serial mode is enabled, output data bits are shifted out of COS15 and COS0. The bit stream on COS15 is provided MSB first while the bit stream in COS0 is provided LSB first.
Index Pin		Used to align chip in socket or on circuit board. Must be left as a no connect in circuit. (CPGA Package only).

Functional Description

The 16-bit Numerically Controlled Oscillator (NCO16) produces a digital complex sinusoid waveform whose frequency and phase are controlled through a standard microprocessor interface and discrete inputs. The NCO16 generates 16-bit sine and cosine vectors at a maximum sample rate of 33MHz. The NCO16 can be preprogrammed to produce a constant (CW) sine and cosine output for Direct Digital Synthesis (DDS) applications. Alternatively, the phase and frequency inputs can be updated in real time to produce a FM, PSK, FSK, or MSK modulated waveform. To simplify PSK generation, a 3 pin interface is provided to support modulation of up to 8 levels.

As shown in Figure 1, the HSP45106 Block Diagram, the NCO16 is comprised of a Phase and Frequency Control Section (PFCS) and Sine/ Cosine Section. The PFCS stores the phase and frequency control inputs and uses them to calculate the phase angle of a rotating complex vector. The Sine/Cosine Section performs a lookup on this phase and generates the appropriate amplitude values for the sine and cosine. These quadrature outputs may be configured as serial or parallel with either two's complement or offset binary format.

Phase/Frequency Control Section

The phase and frequency of the quadrature outputs are controlled by the PFCS (see Figure 1). The PFCS generates a 32-bit word which represents the instantaneous phase (Sin/Cos argument) of the sine and cosine waves being generated. This phase is incremented on the rising edge of each CLK by the preprogrammed amounts in the phase and Frequency Control Registers. As the instantaneous phase steps from 0 through full scale (2^{32} - 1), the phase of the quadrature outputs proceeds from 0° around the unit circle counter clockwise.

The PFCS is comprised of a Phase Accumulator Section, Phase Offset adder, Input Section, and a Timer Accumulator Section. The Phase Accumulator computes the instantaneous phase angle from user programmed values in the Center and Offset Frequency Registers. This angle is then fed into the Phase Offset adder where it is offset by the preprogrammed value in the Phase Offset Register. The Input Section routes data from a microprocessor compatible control bus and discrete input signals into the appropriate configuration registers. The Timer Accumulator supplies a pulse to mark the passage of a user programmed period of time.

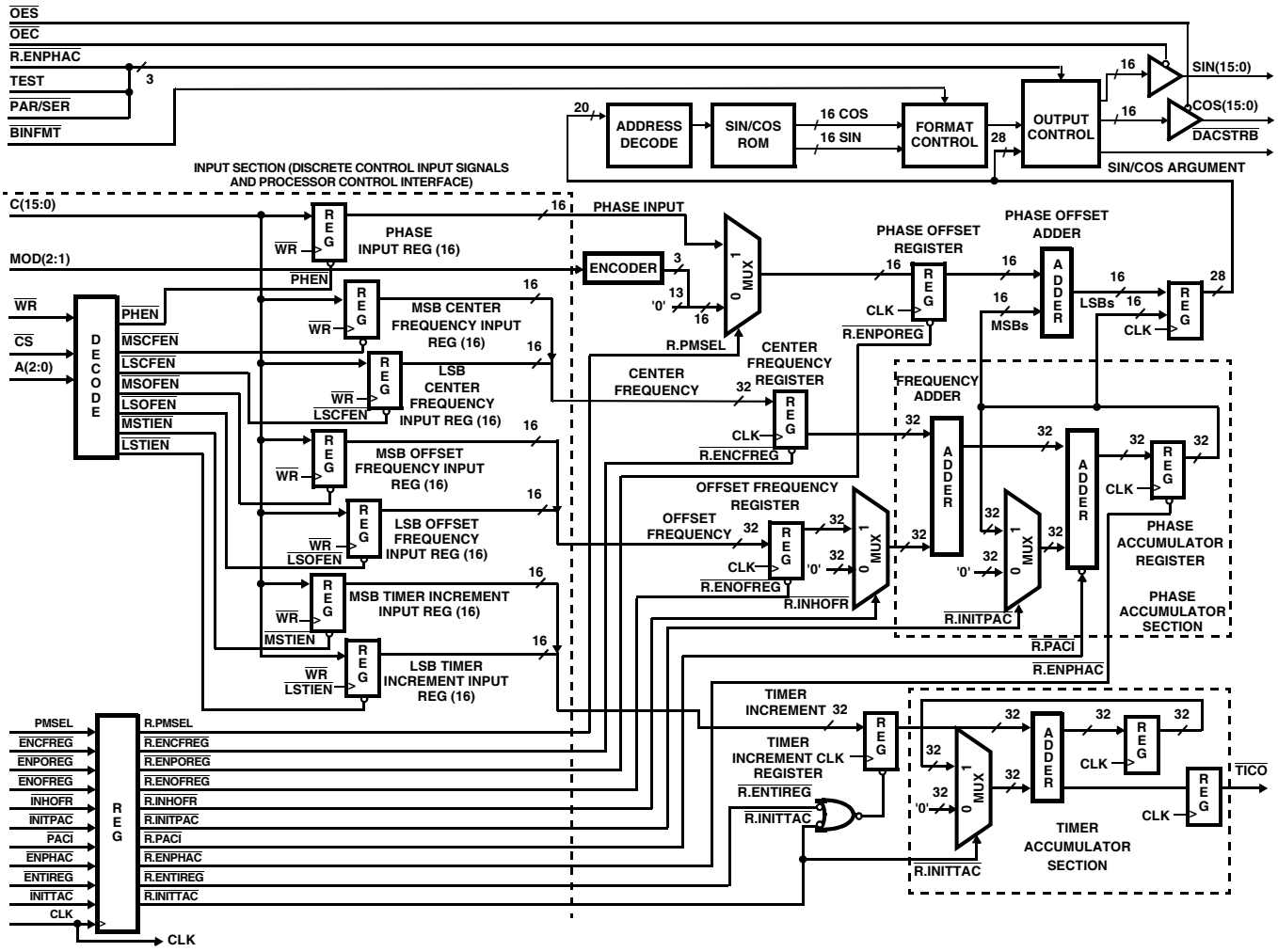


FIGURE 1. BLOCK DIAGRAM OF THE HSP45106

Input Section

The Input Section loads the data on C(15:0) into one of the seven input registers, the LSB and MSB Center Frequency Input Registers, the LSB and MSB Offset Frequency Registers, the LSB and MSB Timer Input Registers, and the Phase Input Register. The destination depends on the state of A(2:0) when $\overline{CS}$ and $\overline{WR}$ are low (Table 1).

TABLE 1. ADDRESS DECODE MAPPING

MOD(2:0) DECODING					
A2	**A1**	**A0**	**CS**	**WR**	**FUNCTION**
0	0	0	0	↑	Load least significant bits of Center Frequency input.
0	0	1	0	↑	Load most significant bits of Center Frequency input.
0	1	0	0	↑	Load least significant bits of Offset Frequency input.
0	1	1	0	↑	Load most significant bits of Offset Frequency input.
1	0	0	0	↑	Load least significant bits of Timing Interval input.
1	0	1	0	↑	Load most significant bits of Timing Interval input.
1	1	0	0	↑	Load Phase Register
1	1	1	0	↑	Reserved
X	X	X	1	X	Input Disabled

Once the Input Registers have been loaded, the control inputs $\overline{ENCFREG}$, $\overline{ENOFREG}$, $\overline{ENTIREG}$, $\overline{ENCTIREG}$, and $\overline{ENPOREG}$ will allow the Input Registers to be downloaded to the PFCS Control Registers with the input CLK. The control inputs are latched on the rising edge of CLK and the Control Registers are updated on the rising edge of the following CLK. For example, to load the Center Frequency Register, the data is loaded into the LSB and MSB Center Frequency Input Register, and $\overline{ENCFREG}$ is set to zero; the next rising edge of CLK will pass the registered version of $\overline{ENCFREG}$, R.$\overline{ENCFREG}$, to the clock enable of the Center Frequency Register; this register then gets loaded on the following rising edge of CLK. The contents of the Input Registers are downloaded to the Control Registers every clock, if the control inputs are enabled.

Phase Accumulator Section

The Phase Accumulator adds the 32-bit output of the Frequency Adder with the contents of a 32-bit Phase Accumulator Register on every clock cycle. When the sum causes the adder to overflow, the accumulation continues with the least significant 32 bits of the result.

Initializing the Phase Accumulator Register is done by putting a low on the $\overline{INITPAC}$ and $\overline{ENPHAC}$ lines. This zeroes the feedback path to the accumulator, so that the register is loaded with the current value of the Frequency Adder on the next clock.

The frequency of the quadrature outputs is based on the number of clock cycles required to step from 0 to full scale. The number of steps required for this transition depends on the phase increment calculated by the frequency adder. For example, if the Center and Offset Frequency Registers are programmed such that the output of the Frequency Adder is 4000 0000 hex, the Phase Accumulator will step the phase from 0° to 360° every 4 clock cycles. Thus, for a 30MHz CLK, the quadrature outputs will have a frequency of 30/4MHz or 7.5MHz. In general, the frequency of the quadrature output is determined by Equations 1 and 2:

$$F_{LO} = (N \times f_{CLK} / 2^{32}), \text{ or} \quad \text{(EQ. 1)}$$

$$N = INT\left[\left(\frac{f_{OUT}}{f_{CLK}}\right)2^{32}\right], \quad \text{(EQ. 2)}$$

where N is the 32 bits of frequency control word that is programmed. INT[•] is the integer of the computation. For example, if the control word is 20000000 hexadecimal and the clock frequency is 30MHz, then the output frequency would be $f_{CLK}/8$, or 3.75MHz.

The Frequency Adder sums the contents of both the Center and Offset Frequency Registers to produce a phase increment. By enabling $\overline{INHOFR}$, the output of the Offset Frequency Register is disabled so that the output frequency is determined from the Center Frequency Register alone. For BFSK modems, $\overline{INHOFR}$ can be asserted/ de-asserted to toggle the quadrature outputs between two programmed frequencies. ***NOTE: Enabling/disabling INHOFR preserves the contents of the Offset Frequency Register.***

The Block Diagram shown in Figure 2 illustrates the method of reading the phase accumulator of the NCO16 from a microprocessor. The setup shown is very similar to that used when the part is used for generating a complex sinusoid, except that the internal SIN/COS lookup is bypassed by setting the TEST pin to a logic 1(high). While the TEST pin is high, the phase accumulator continues to drive the inputs of the SIN/COS Generator while the most significant 28 bits of the phase accumulator are multiplexed out onto the output pins. Because of this, the part can be operated in two modes, one where the SIN/COS Generator is permanently bypassed, and one where the phase accumulator output is brought out to the outputs as a check.

Figure 2 illustrates a circuit for reading out the phase accumulator all the time. In this case, a microprocessor loads the frequency and phase registers of the NCO16. This is fairly straightforward, except for the Start Logic Block, which needs to be synchronous to the oscillator clock and the microprocessor interface. This has been left as an undefined function, since it is dependent on the implementation. Also note that all COS outputs (COS(15:0)) are connected, although only COS(15:4) are valid in this application. The microprocessor reads the sine and cosine data busses as if

they were RAMs, using the decoded address bus to select one or the other.

The timing for loading the Center Frequency Register (MSB and LSB) and data being output on COS(15:0) and SIN(15:0) is shown in Figure 3. This timing is independent of whether the output data represents the phase accumulator data or the SIN/COS Generator output.

When it is desired for the output of the NCO16 to be switched back and forth between sine/cosine and the phase accumulator, a circuit such as the one shown in Figure 4 could be used. In this case, the sinusoidal output cannot be interrupted, so the phase accumulator must be read out between samples. This is possible due to the fact that the TEST signal is simply the control line for a multiplexer on the output of the SIN/COS Generator, but carries with it a limitation on the maximum possible clock rate. Since TEST is a synchronous input, the output of the NCO16 must be either driven by the SIN/COS Generator or the phase accumulator for an entire clock cycle. Therefore, the part must be driven at twice the desired speed at all times so there is a clock cycle available for TEST, when necessary. Note that the processor must be driven from the same clock that generates the NCO clock in order to maintain synchronous operation.

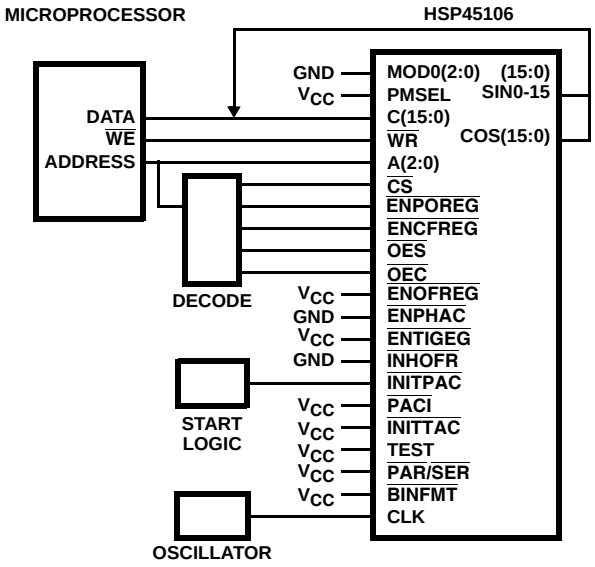


FIGURE 2. CIRCUIT FOR READING PHASE ACCUMULATOR OF NCO16

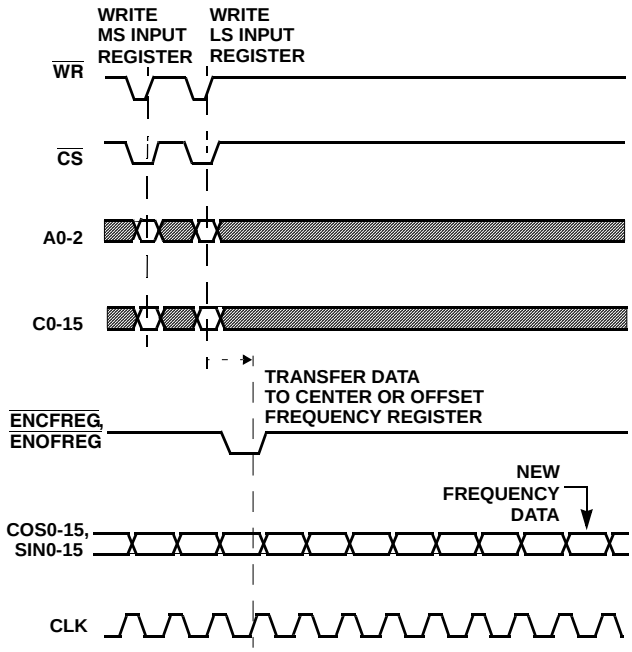


FIGURE 3. NCO16 PIPELINE DELAY

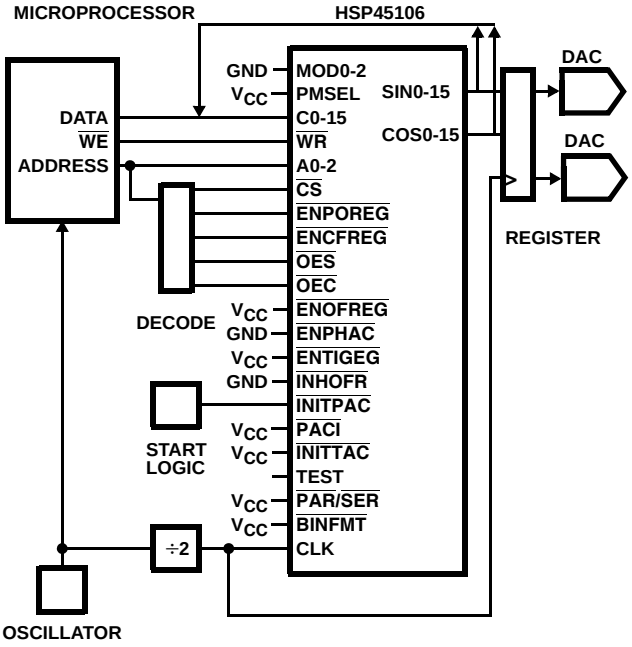


FIGURE 4. CIRCUIT FOR READING PHASE ACCUMULATOR OF NCO16 WHILE GENERATING SINUSOID

Phase Offset Adder

The output of the Phase Accumulator goes to the Phase Offset Adder, which adds the 16-bit contents of the Phase Offset Register to the 16 MSBs of the phase. Twenty-eight (28) bits of the resulting 32-bit number forms the instantaneous phase which is fed to the Sine/Cosine Section.

The user has the option of loading the Phase Offset Registers with the contents of the Phase Input Register or with the MOD(2:0) inputs depending on the state of PMSEL. When PMSEL is high, the contents of the Phase Input Register are loaded. If PMSEL is low, MOD(2:0) encode the upper 3 bits of the Phase Offset Register while the lower 13 bits are cleared. The MOD(2:0) inputs simplify PSK modulation by providing a 3 input interface to phase modulate the carrier as shown in Table 2. The control input ENPOREG acts as a clock enable and must be low to enable clocking of data into the Phase Offset Register.

TABLE 2. MODULATION CONTROL MAP

MOD(2:0) DECODING			
MOD2	**MOD1**	**MOD0**	**PHASE SHIFT (DEGREES)**
0	0	0	0
0	0	1	45
0	1	0	90
0	1	1	135
1	0	0	270
1	0	1	315
1	1	0	180
1	1	1	225

Timer Accumulator Section

The Timer Accumulator consists of a register which is incremented on every clock. The amount by which it increments is loaded into the Timer Increment Input Registers and is latched into the Timer Increment Register on rising edges of CLK while $\overline{\text{ENTIREG}}$ is low. The output of the Timer Accumulator is the accumulator carry out, $\overline{\text{TICO}}$. $\overline{\text{TICO}}$ can be used as a timer to enable the periodic sampling of the output of the NCO-16. The number programmed into this register equals:

$$N = \text{INT}\left[\left(\frac{f_{OUT}}{f_{CLK}}\right)2^{32}\right], \quad \text{(EQ. 3)}$$

where INT[x] is the integer portion of the result of the computation.

Sine/Cosine Section

The Sine/Cosine Section (Figure 5) converts the instantaneous phase from the PFCS Section into the appropriate amplitude values for the sine and cosine outputs. It takes the most significant 20 bits of the PFCS output and passes them through a Sine/Cosine look up to form the 16-bit quadrature outputs. The sine and cosine values are computed to reduce the amount of ROM needed. The magnitude of the error in the computed value of the complex vector is less than -90.2dB. The error in the sine or cosine alone is approximately 2dB better. The 20-bit phase word maps into 2p radians so that the angular resolution is $(2p)/2^{20}$. An address of zero corresponds to 0 radians and an address of hex FFFFF corresponds to $2\pi-((2\pi)/2^{20})$ radians. The outputs of the Sine/Cosine Section are two's complement sine and cosine values. The ROM contents have been scaled by $(2^{16}-1)/(2^{16}+1)$ for symmetry about zero.

To simplify interfacing with D/A converters, the format of the Sine/cosine outputs may be changed to offset binary by enabling $\overline{\text{BINFMT}}$. When $\overline{\text{BINFMT}}$ is enabled, the MSB of the Sine and Cosine outputs (SIN15 and COS15 when the outputs are in parallel mode) are inverted. Depending upon the state of $\overline{\text{BINFMT}}$, the output is centered around midscale and ranges from 8001H to 7FFFH (two's complement mode) or 0001H to FFFFH (offset binary mode).

Serial output mode is chosen by enabling $\overline{\text{PAR/SER}}$. In this mode the user loads the Output Shift Registers with Sine/Cosine ROM output by enabling $\overline{\text{ENPHAC}}$. After $\overline{\text{ENPHAC}}$ goes inactive the data is shifted out serially. For example, to clock out one 16-bit Sine/Cosine output, $\overline{\text{ENPHAC}}$ would be active for one cycle to load the output Shift Register, and would then go inactive for the following 15 cycles to clock the remaining bits out. Output bit streams are provided in formats with either MSB first or LSB first. The MSB first format is available on the SIN15 and COS15 output pins. The LSB first format is available on the SIN0 and COS0 output pins. In MSB first format, zero's follow the LSB if a new output word is not loaded into the Shift Register. In LSB first format, the sine extension bit follows the MSB if a new data word is not loaded. The output signal $\overline{\text{DACSTRB}}$ is provided to signal the first bit of a new output word is valid (Figure 6). ***NOTE: All unused pins of SIN(15:0) and COS(15:0) should be left floating.***

A test mode is supplied which enables the user to access the phase input to the Sine/Cosine ROM. If TEST and $\overline{\text{PAR/SER}}$ are both high, the 28 MSBs of the phase input to the Sine/Cosine Section are made available on SIN(15:0) and COS(15:4). The SIN(15:0) outputs represent the MSW of the address.

The Timing Diagrams in Figures 7, 8 and 9 show the pipeline delays through the HSP45106 NCO16 from the time that data is applied to the inputs until the outputs are affected by the change. The delay is shown as a number of clock cycles, with no attempt made to accurately represent the setup and hold times or the clock to output delays.

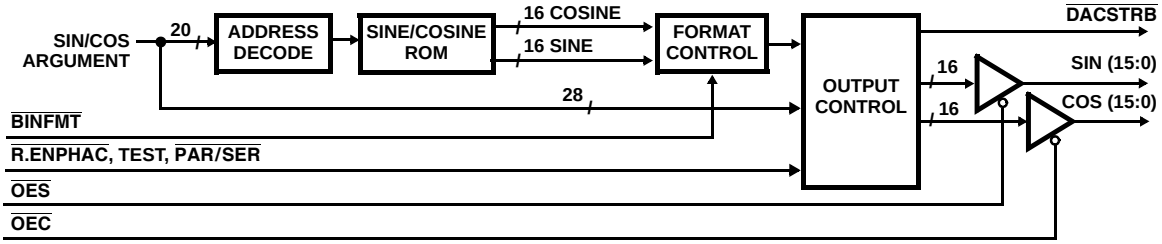


FIGURE 5. SINE/COSINE SECTION BLOCK DIAGRAM

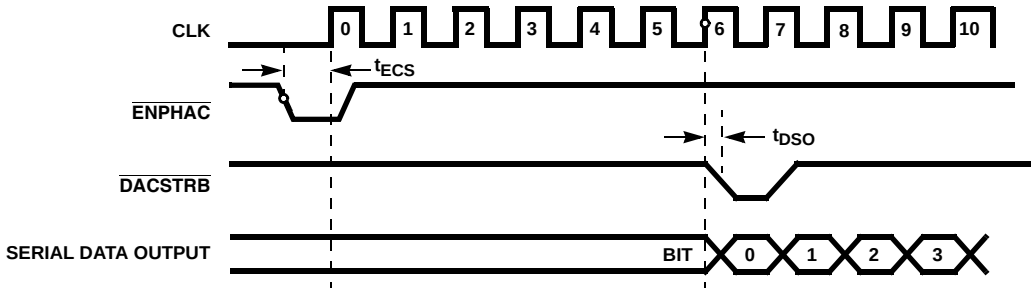


FIGURE 6. SERIAL OUTPUT I/O TIMING DIAGRAM

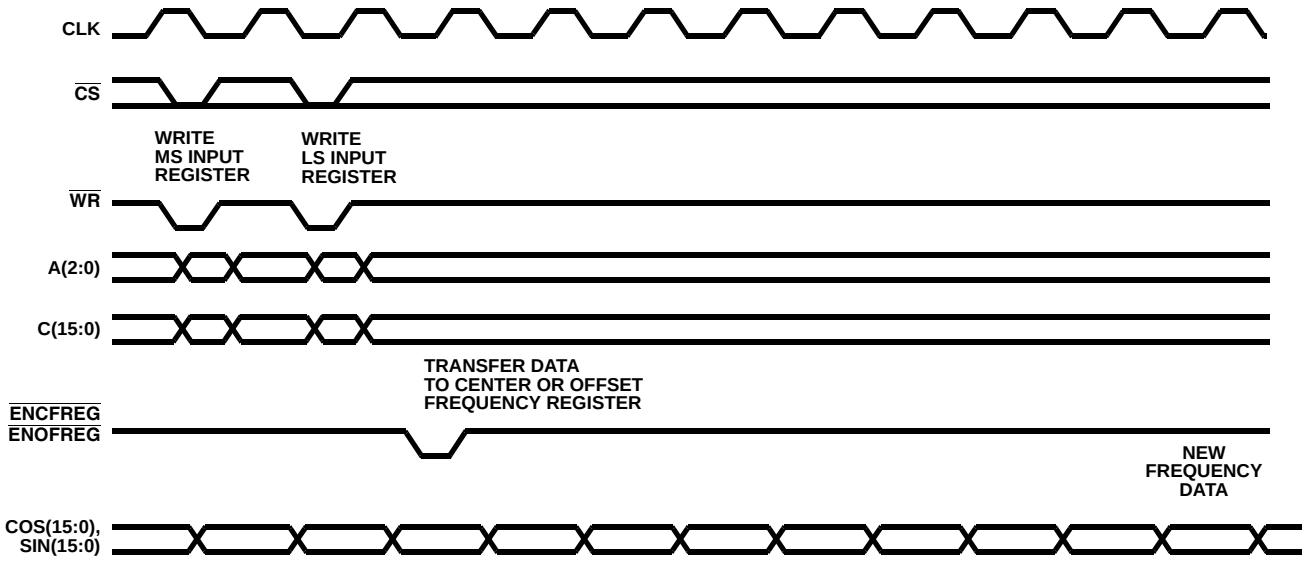


FIGURE 7. FREQUENCY TO OUTPUT DELAY

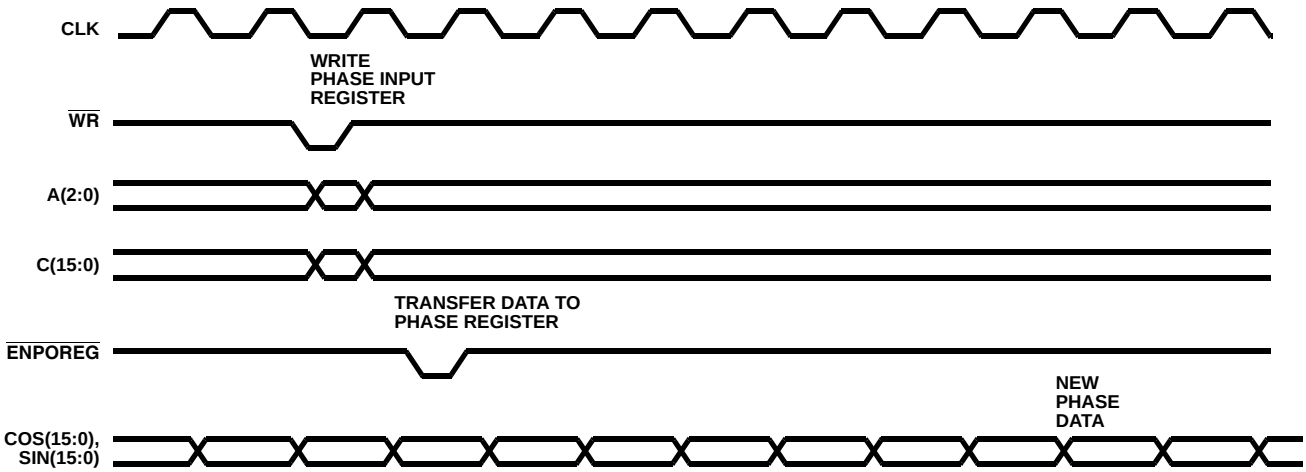


FIGURE 8. PHASE TO OUTPUT DELAY

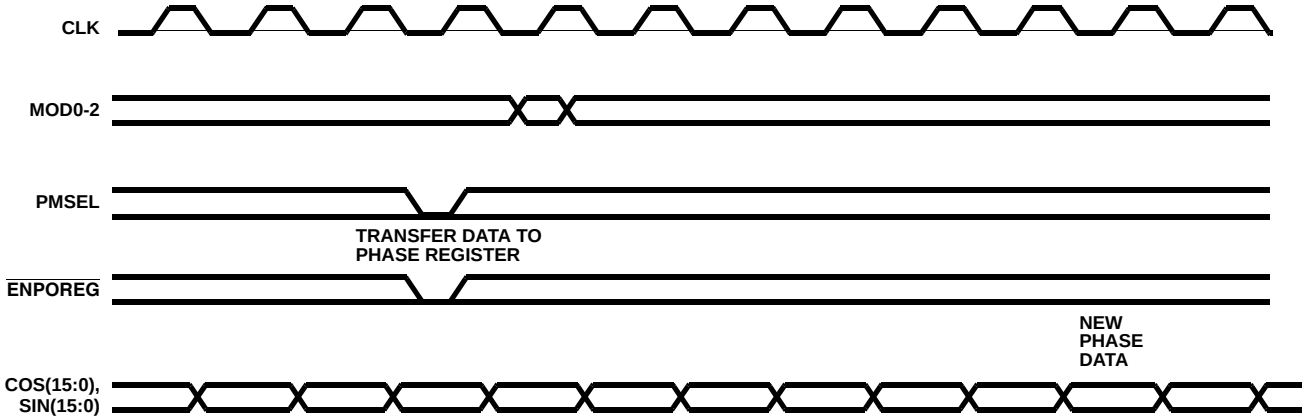


FIGURE 9. PHASE MODULATION TO OUTPUT DELAY

Absolute Maximum Ratings T_A = +25°C

Supply Voltage . . . . . +6.0V
Input, Output or I/O Voltage Applied . . . . . GND -0.5V to V_{CC} +0.5V
ESD Classification . . . . . Class 1

Operating Conditions

Voltage Range . . . . . +4.75V to +5.25V
Temperature Range . . . . . 0°C to +70°C

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} (°C/W)
PLCC Package. 36
Maximum Junction Temperature
PLCC Package. . . . . +150°C
Maximum Storage Temperature Range. . . . . -65°C to +150°C
Pb-Free Reflow Profile. . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Die Characteristics

Backside Potential . . . . . V_{CC}

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.

DC Electrical Specifications

Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
Logical One Input Voltage	V_{IH}	V_{CC} = 5.25V	2.0	-	V
Logical Zero Input Voltage	V_{IL}	V_{CC} = 4.75V	-	0.8	V
High Level Clock Input	V_{IHC}	V_{CC} = 5.25V	3.0	-	V
Low Level Clock Input	V_{ILC}	V_{CC} = 4.75V	-	0.8	V
Output HIGH Voltage	V_{OH}	I_{OH} = -400µA, V_{CC} = 4.75V	2.6	-	V
Output LOW Voltage	V_{OL}	I_{OL} = +2.0mA, V_{CC} = 4.75V	-	0.4	V
Input Leakage Current	I_I	V_{IN} = V_{CC} or GND, V_{CC} = 5.25V	-10	10	µA
I/O Leakage Current	I_O	V_{OUT} = V_{CC} or GND, V_{CC} = 5.25V	-10	10	µA
Standby Power Supply Current	I_{CCSB}	V_{IN} = V_{CC} or GND, V_{CC} = 5.25V, (Note 4)	-	500	µA
Operating Power Supply Current	I_{CCOP}	f = 25.6MHz, V_{IN} = V_{CC} or GND V_{CC} = 5.25V, (Notes 2 and 4)	-	180	mA

Capacitance T_A = +25°C, (Note 3)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
Input Capacitance	C_{IN}	FREQ = 1MHz, V_{CC} = Open. All measurements are referenced to device ground	-	10	pF
Output Capacitance	C_O		-	10	pF

NOTES:

2. Power supply current is proportional to operating frequency. Typical rating for I_{CCOP} is 7mA/MHz.
3. Not tested, but characterized at initial design and at major process/design changes.
4. Output load per test load circuit with switch open and C_L = 40pF.

AC Electrical Specifications

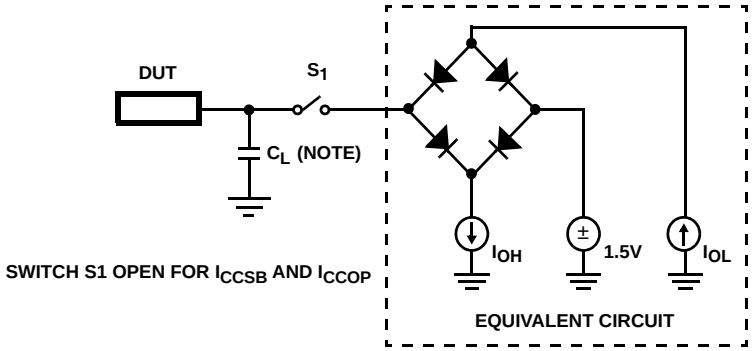
V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C (Note 5). Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

PARAMETER	SYMBOL	NOTES	25.6MHz		33MHz		UNITS
			MIN	MAX	MIN	MAX	
CLK Period	t_{CP}		39	-	30	-	ns
CLK High	t_{CH}		15	-	12	-	ns
CLK Low	t_{CL}		15	-	12	-	ns
$\overline{WR}$ Period	t_{WP}		39	-	30	-	ns
$\overline{WR}$ High	t_{WH}		15	-	12	-	ns
$\overline{WR}$ Low	t_{WL}		15	-	12	-	ns
Setup Time A(2:0), $\overline{CS}$ to $\overline{WR}$ Going High	t_{AWS}		13	-	13	-	ns
Hold Time A(2:0), $\overline{CS}$ from $\overline{WR}$ Going High	t_{AWH}		1	-	1	-	ns
Setup Time C(15:0) to $\overline{WR}$ Going High	t_{CWS}		15	-	15	-	ns
Hold Time C(15:0) from $\overline{WR}$ Going High	t_{CWH}		0	-	0	-	ns
Setup Time $\overline{WR}$ High to CLK High	t_{WC}	(Note 6)	16	-	12	-	ns
Setup Time MOD(2:0) to CLK Going High	t_{MCS}		15	-	15	-	ns
Hold Time MOD(2:0) from CLK Going High	t_{MCH}		0	-	0	-	ns
Setup Time $\overline{ENPOREG}$, $\overline{ENOFREG}$, $\overline{ENCFREG}$, $\overline{ENPHAC}$, $\overline{ENTIREG}$, $\overline{INHOFR}$, PMSEL, $\overline{INITPAC}$, $\overline{BINFMT}$, TEST, PAR/$\overline{SER}$, $\overline{PACI}$, $\overline{INITTAC}$ to CLK Going High	t_{ECS}		12	-	12	-	ns
Hold Time $\overline{ENPOREG}$, $\overline{ENOFREG}$, $\overline{ENCFREG}$, $\overline{ENPHAC}$, $\overline{ENTIREG}$, $\overline{INHOFR}$, PMSEL, $\overline{INITPAC}$, $\overline{BINFMT}$, TEST, PAR/$\overline{SER}$, $\overline{PACI}$, $\overline{INITTAC}$ from CLK Going High	t_{ECH}		0	-	0	-	ns
CLK to Output Delay SIN(15:0), COS(15:0), $\overline{TICO}$	t_{DO}		-	18	-	15	ns
CLK to Output Delay $\overline{DACSTRB}$	t_{DSO}		2	18	2	15	ns
Output Enable Time	t_{OE}		-	12	-	12	ns
Output Disable Time	t_{OD}	(Note 7)	-	15	-	15	ns
Output Rise, Fall Time	t_{RF}	(Note 7)	-	8	-	8	ns

NOTES:

5. AC testing is performed as follows: Input levels (CLK Input) 4.0V and 0V; input levels (all other inputs) 0V and 3.0V; timing reference levels (CLK) 2.0V; all others 1.5V. Output load per test load circuit with switch closed and C_L = 40pF. Output transition is measured at V_{OH} > 1.5V and V_{OL} < 1.5V.
6. If $\overline{ENOFREG}$, $\overline{ENCFREG}$, $\overline{ENTIREG}$, or $\overline{ENPOREG}$ are active, care must be taken to not violate setup and hold times to these registers when writing data into the chip via the C(15:0) port.
7. Controlled via design or process parameters and not directly tested. Characterized upon initial design and after major process and/or changes.

AC Test Load Circuit



NOTE: Test head capacitance.

Waveforms

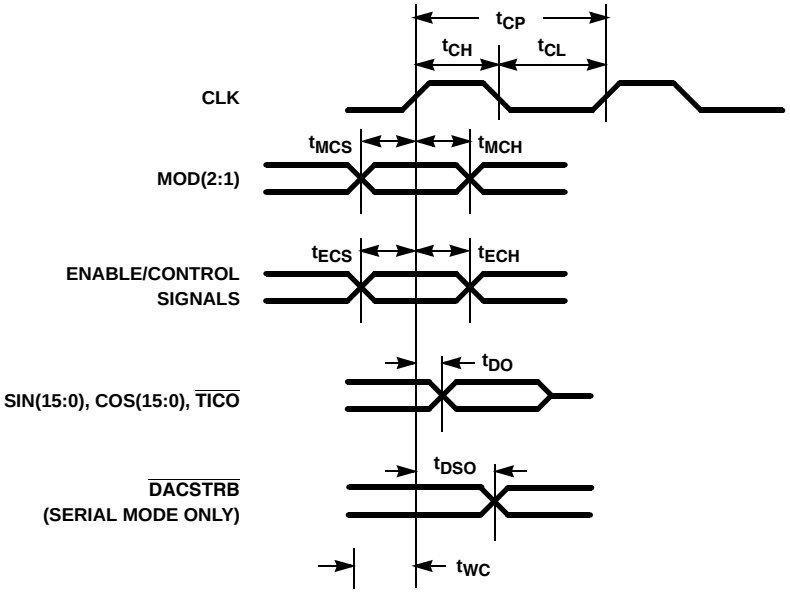


FIGURE 10. SYNCHRONOUS TIMING

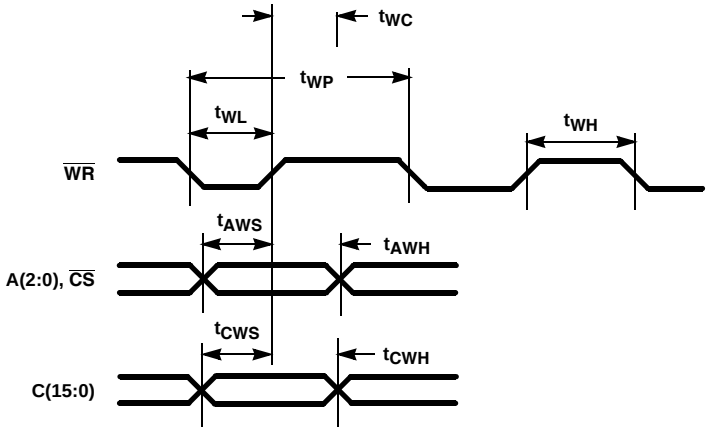


FIGURE 11. ASYNCHRONOUS TIMING

Waveforms (Continued)

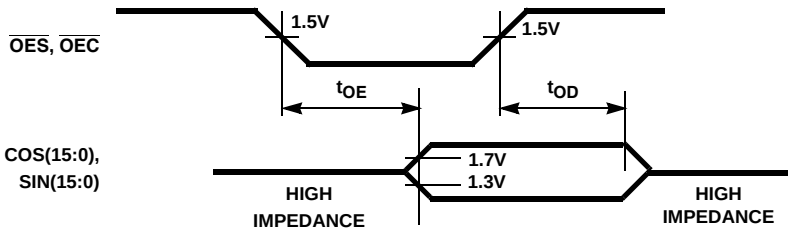


FIGURE 12. OUTPUT ENABLE, DISABLE TIMING

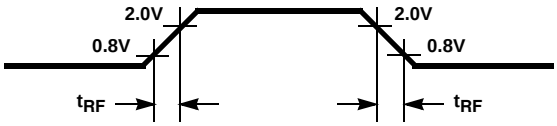
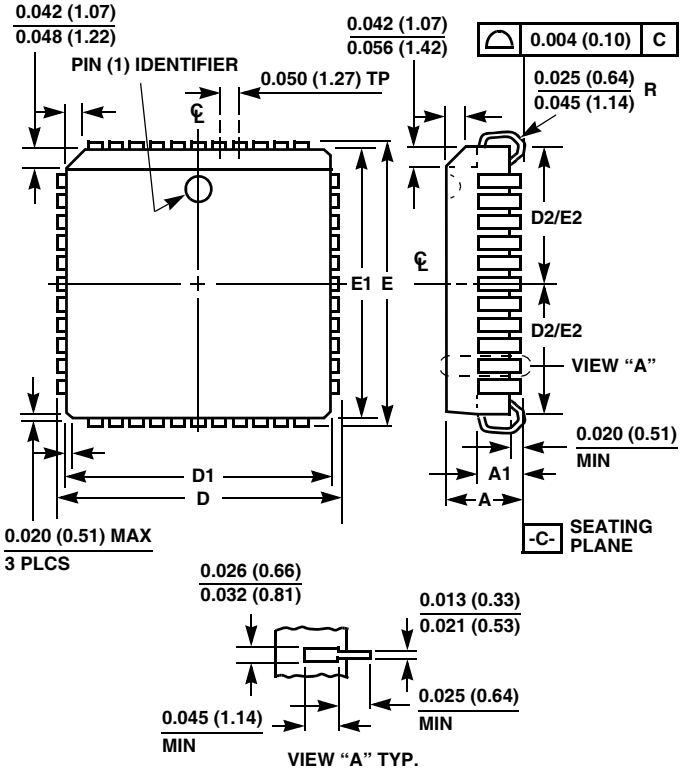


FIGURE 13. OUTPUT RISE AND FALL TIMES

Plastic Leaded Chip Carrier Packages (PLCC)



N84.1.15 (JEDEC MS-018AF ISSUE A)
84 LEAD PLASTIC LEADED CHIP CARRIER PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.180	4.20	4.57	-
A1	0.090	0.120	2.29	3.04	-
D	1.185	1.195	30.10	30.35	-
D1	1.150	1.158	29.21	29.41	3
D2	0.541	0.569	13.75	14.45	4, 5
E	1.185	1.195	30.10	30.35	-
E1	1.150	1.158	29.21	29.41	3
E2	0.541	0.569	13.75	14.45	4, 5
N	84		84		6

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NOTES:

1. Controlling dimension: INCH. Converted millimeter dimensions are not necessarily exact.
2. Dimensions and tolerancing per ANSI Y14.5M-1982.
3. Dimensions D1 and E1 do not include mold protrusions. Allowable mold protrusion is 0.010 inch (0.25mm) per side. Dimensions D1 and E1 include mold mismatch and are measured at the extreme material condition at the body parting line.
4. To be measured at seating plane -C- contact point.
5. Centerline to be determined where center leads exit plastic body.
6. "N" is the number of terminal positions.