TimerBlox: Resettable, Low Frequency Oscillator

FEATURES

- **Period Range: 1ms to 9.5 Hours**
- Configured with 1 to 3 Resistors
- <1.5% Maximum Frequency Error
- Output Reset Function
- 2.25V to 5.5V Single Supply Operation
- 55µA to 80µA Supply Current (2ms to 9.5hr Clock Period)
- 500µs Start-Up Time
- CMOS Output Driver Sources/Sinks 20mA
- –40°C to 125°C Operating Temperature Range
- Available in Low Profile (1mm) SOT-23 (ThinSOT™) and 2mm × 3mm DFN Packages

APPLICATIONS

- "Heartbeat" Timers
- Watchdog Timers
- Intervalometers
- Periodic "Wake-Up" Call
- High Vibration, High Acceleration Environments
- Portable and Battery-Powered Equipment

DESCRIPTION

The LTC®6991 is a silicon oscillator with a programmable period range of 1.024ms to 9.54 hours (29.1µHz to 977Hz), specifically intended for long duration timing events. The LTC6991 is part of the TimerBlox™ family of versatile silicon timing devices.

A single resistor, R_{SET}, programs the LTC6991's internal master oscillator frequency. The output clock period is determined by this master oscillator and an internal frequency divider, N_{DIV}, programmable to eight settings from 1 to 2^{21}.

$$t_{OUT} = \frac{N_{DIV} \bullet R_{SET}}{50k\Omega} \bullet 1.024ms,\ N_{DIV} = 1,8,64,...,2^{21}$$

In normal operation, the LTC6991 oscillates with a 50% duty cycle. A reset function is provided to truncate the pulse (reducing the duty cycle). The reset pin can also be used to prevent the output from oscillating.

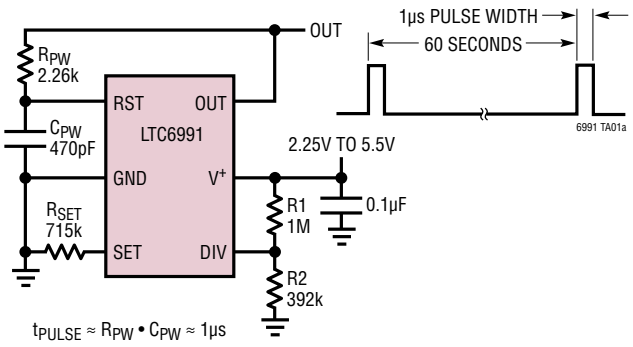
The RST and OUT pins can be configured for active-low or active-high operation using a polarity function.

POL BIT	RST PIN	OUTPUT STATE
0	0	Oscillating
0	1	0 (reset)
1	0	1 (reset)
1	1	Oscillating

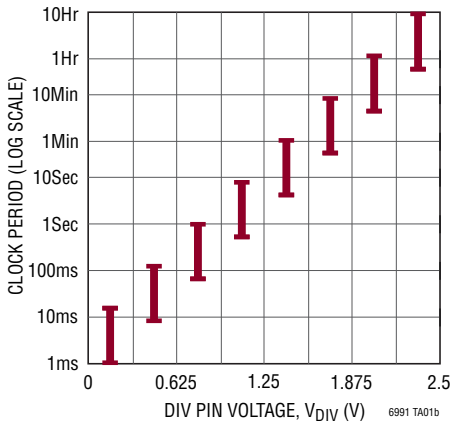
The LTC6991 is available in the 6-lead SOT-23 (ThinSOT) package or a 6-lead 2mm × 3mm DFN.

TYPICAL APPLICATION

Low Frequency Pulse Generator



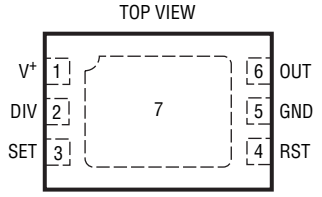
Clock Period Range over Eight Divider Settings



ABSOLUTE MAXIMUM RATINGS (Note 1)

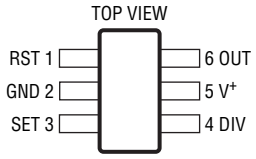
Supply Voltage (V^+) to GND 6V
Maximum Voltage
on Any Pin ..... $(GND - 0.3V) \le V_{PIN} \le (V^+ + 0.3V)$
Operating Temperature Range (Note 2)
LTC6991C ..... –40°C to 85°C
LTC6991I ..... –40°C to 85°C
LTC6991H ..... –40°C to 125°C
Specified Temperature Range (Note 3)
LTC6991C ..... 0°C to 70°C
LTC6991I ..... –40°C to 85°C
LTC6991H ..... –40°C to 125°C
Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
S6 Package ..... 300°C

PIN CONFIGURATION



DCB PACKAGE
6-LEAD (2mm × 3mm) PLASTIC DFN

T_{JMAX} = 150°C, θ_{JA} = 64°C/W, θ_{JC} = 10.6°C/W
EXPOSED PAD (PIN 7) CONNECTED TO GND,
PCB CONNECTION OPTIONAL



S6 PACKAGE
6-LEAD PLASTIC TSOT-23

T_{JMAX} = 150°C, θ_{JA} = 192°C/W, θ_{JC} = 51°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LTC6991CDCB#PBF	LTC6991CDCB#TRPBF	LDWZ	6-Lead (2mm × 3mm) Plastic DFN	0°C to 70°C
LTC6991IDCB#PBF	LTC6991IDCB#TRPBF	LDWZ	6-Lead (2mm × 3mm) Plastic DFN	–40°C to 85°C
LTC6991HDCB#PBF	LTC6991HDCB#TRPBF	LDWZ	6-Lead (2mm × 3mm) Plastic DFN	–40°C to 125°C
LTC6991CS6#PBF	LTC6991CS6#TRPBF	LTDWY	6-Lead Plastic TSOT-23	0°C to 70°C
LTC6991IS6#PBF	LTC6991IS6#TRPBF	LTDWY	6-Lead Plastic TSOT-23	–40°C to 85°C
LTC6991HS6#PBF	LTC6991HS6#TRPBF	LTDWY	6-Lead Plastic TSOT-23	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Test conditions are V^+ = 2.25V to 5.5V, RST = 0V, DIVCODE = 0 to 15 (N_{DIV} = 1 to 2^{21}), R_{SET} = 50k to 800k, R_{LOAD} = 5k, C_{LOAD} = 5pF unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{OUT}	Output Clock Period			1.024m		34,360	Seconds
f_{OUT}	Output Frequency			29.1µ		977	Hz
Δf_{OUT}	Frequency Accuracy (Note 4)	29.1µHz ≤ f_{OUT} ≤ 977Hz	 ●		±0.8	±1.5 ±2.2	% %
$\Delta f_{OUT}/\Delta T$	Frequency Drift Over Temperature		●		±0.005		%/°C
	Frequency Drift Over Supply	V^+ = 4.5V to 5.5V V^+ = 2.25V to 4.5V	● ●		0.23 0.06	0.55 0.16	%/V %/V
	Period Jitter (Note 10)	N_{DIV} = 1 N_{DIV} = 8			15 7		ppm_{RMS} ppm_{RMS}
BW	Frequency Modulation Bandwidth				0.4 • f_{OUT}		Hz
t_S	Frequency Change Settling Time (Note 9)				1		Cycle
Analog Inputs							
V_{SET}	Voltage at SET Pin		●	0.97	1.00	1.03	V
$\Delta V_{SET}/\Delta T$	V_{SET} Drift Over Temperature		●		±75		µV/°C
R_{SET}	Frequency-Setting Resistor		●	50		800	kΩ
V_{DIV}	DIV Pin Voltage		●	0		V^+	V
$\Delta V_{DIV}/\Delta V^+$	DIV Pin Valid Code Range (Note 5)	Deviation from Ideal V_{DIV}/V^+ = (DIVCODE + 0.5)/16	●			±1.5	%
	DIV Pin Input Current		●			±10	nA
Power Supply							
V^+	Operating Supply Voltage Range		●	2.25		5.5	V
	Power-On Reset Voltage		●			1.95	V
I_S	Supply Current	R_L = ∞, R_{SET} = 50k, V^+ = 5.5V R_L = ∞, R_{SET} = 50k, V^+ = 2.25V	● ●		135 105	170 135	µA µA
		R_L = ∞, R_{SET} = 100k, V^+ = 5.5V R_L = ∞, R_{SET} = 100k, V^+ = 2.25V	● ●		100 80	130 105	µA µA
		R_L = ∞, R_{SET} = 800k, V^+ = 5.5V R_L = ∞, R_{SET} = 800k, V^+ = 2.25V	● ●		65 55	100 85	µA µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Test conditions are V^+ = 2.25V to 5.5V, RST = 0V, DIVCODE = 0 to 15 (N_{DIV} = 1 to 2^{21}), R_{SET} = 50k to 800k, R_{LOAD} = ∞, C_{LOAD} = 5pF unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Digital I/O								
	RST Pin Input Capacitance					2.5		pF
	RST Pin Input Current	RST = 0V to V^+					±10	nA
V_{IH}	High Level RST Pin Input Voltage	(Note 6)		●	0.7 • V^+			V
V_{IL}	Low Level RST Pin Input Voltage	(Note 6)		●			0.3 • V^+	V
$I_{OUT(MAX)}$	Output Output Current	V^+ = 2.7V to 5.5V				±20		mA
V_{OH}	High Level Output Voltage (Note 7)	V^+ = 5.5V	I_{OUT} = –1mA	●	5.45	5.48		V
			I_{OUT} = –16mA	●	4.84	5.15		V
		V^+ = 3.3V	I_{OUT} = –1mA	●	3.24	3.27		V
			I_{OUT} = –10mA	●	2.75	2.99		V
		V^+ = 2.25V	I_{OUT} = –1mA	●	2.17	2.21		V
			I_{OUT} = –8mA	●	1.58	1.88		V
V_{OL}	Low Level Output Voltage (Note 7)	V^+ = 5.5V	I_{OUT} = 1mA	●		0.02	0.04	V
			I_{OUT} = 16mA	●		0.26	0.54	V
		V^+ = 3.3V	I_{OUT} = 1mA	●		0.03	0.05	V
			I_{OUT} = 10mA	●		0.22	0.46	V
		V^+ = 2.25V	I_{OUT} = 1mA	●		0.03	0.07	V
			I_{OUT} = 8mA	●		0.26	0.54	V
t_{RST}	Reset Propagation Delay	V^+ = 5.5V				16		ns
		V^+ = 3.3V				24		ns
		V^+ = 2.25V				40		ns
t_{WIDTH}	Minimum Input Pulse Width	V^+ = 3.3V				5		ns
t_r	Output Rise Time (Note 8)	V^+ = 5.5V				1.1		ns
		V^+ = 3.3V				1.7		ns
		V^+ = 2.25V				2.7		ns
t_f	Output Fall Time (Note 8)	V^+ = 5.5V				1.0		ns
		V^+ = 3.3V				1.6		ns
		V^+ = 2.25V				2.4		ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC6991C is guaranteed functional over the operating temperature range of –40°C to 85°C.

Note 3: The LTC6991C is guaranteed to meet specified performance from 0°C to 70°C. The LTC6991C is designed, characterized and expected to meet specified performance from –40°C to 85°C but it is not tested or QA sampled at these temperatures. The LTC6991I is guaranteed to meet specified performance from –40°C to 85°C. The LTC6991H is guaranteed to meet specified performance from –40°C to 125°C.

Note 4: Frequency accuracy is defined as the deviation from the f_{OUT} equation, assuming R_{SET} is used to program the frequency.

Note 5: See Operation section, Table 1 and Figure 2 for a full explanation of how the DIV pin voltage selects the value of DIVCODE.

Note 6: The RST pin has hysteresis to accommodate slow rising or falling signals. The threshold voltages are proportional to V^+. Typical values can be estimated at any supply voltage using $V_{RST(RISING)} \approx 0.55 \bullet V^+ + 185mV$ and $V_{RST(FALLING)} \approx 0.48 \bullet V^+ – 155mV$.

Note 7: To conform to the Logic IC Standard, current out of a pin is arbitrarily given a negative value.

Note 8: Output rise and fall times are measured between the 10% and the 90% power supply levels with 5pF output load. These specifications are based on characterization.

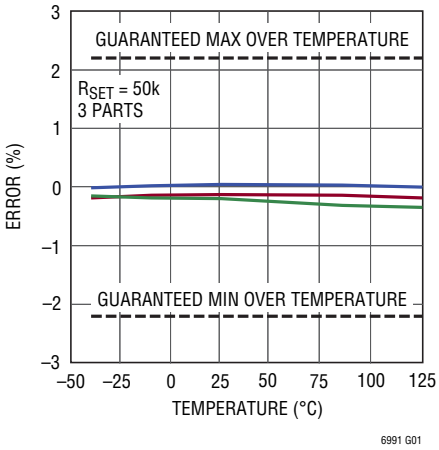
Note 9: Settling time is the amount of time required for the output to settle within ±1% of the final frequency after a 0.5× or 2× change in I_{SET}.

Note 10: Jitter is the ratio of the deviation of the period to the mean of the period. This specification is based on characterization and is not 100% tested.

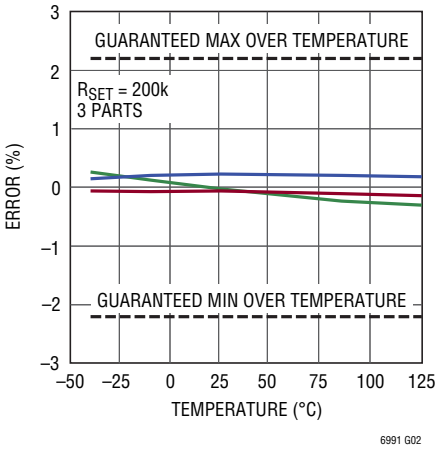
TYPICAL PERFORMANCE CHARACTERISTICS

V^+ = 3.3V, R_{SET} = 200k, T_A = 25°C unless otherwise noted.

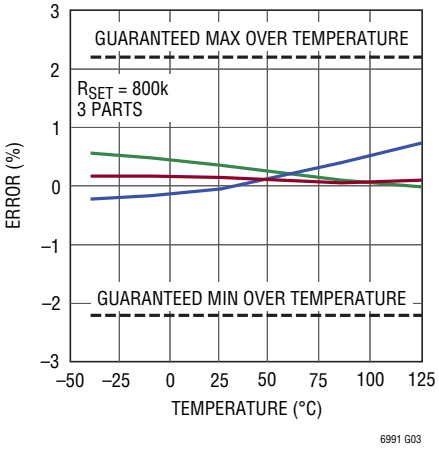
Frequency Error vs Temperature



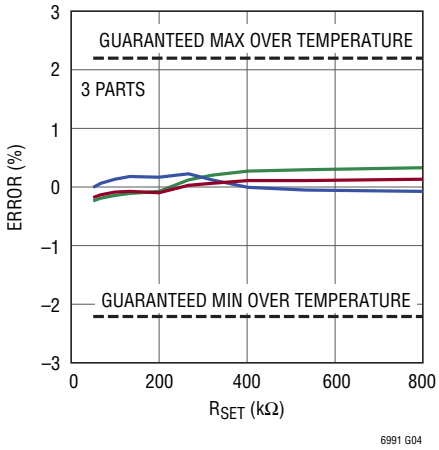
Frequency Error vs Temperature



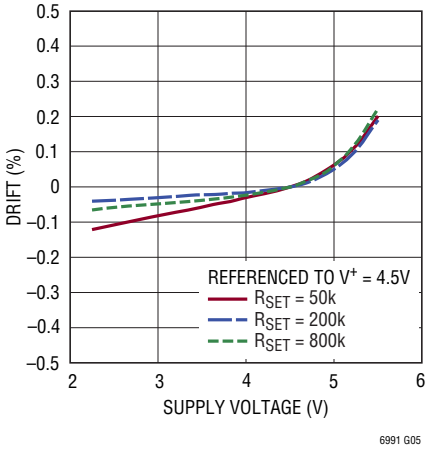
Frequency Error vs Temperature



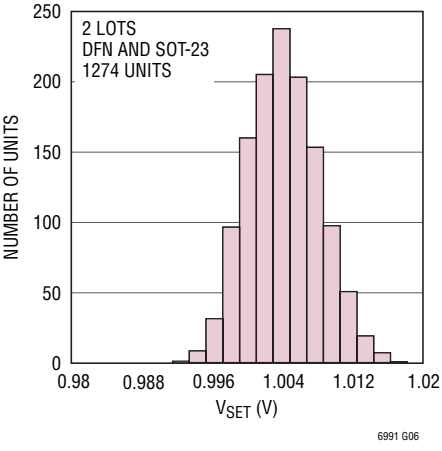
Frequency Error vs R_{SET}



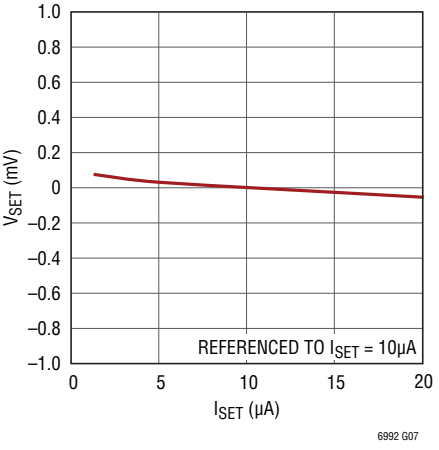
Frequency Drift vs Supply Voltage



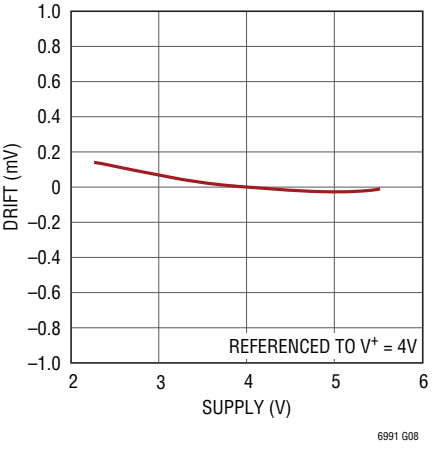
Typical V_{SET} Distribution



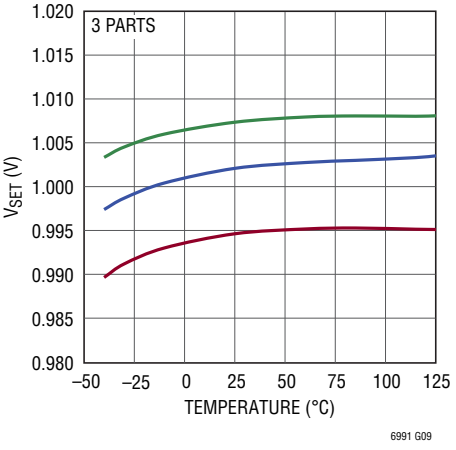
V_{SET} Drift vs I_{SET}



V_{SET} Drift vs Supply



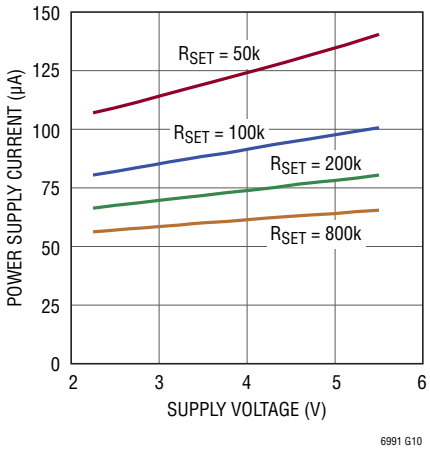
V_{SET} vs Temperature



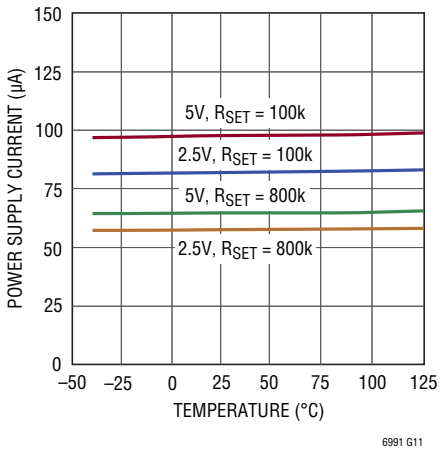
TYPICAL PERFORMANCE CHARACTERISTICS

V^+ = 3.3V, R_{SET} = 200k, T_A = 25°C unless otherwise noted.

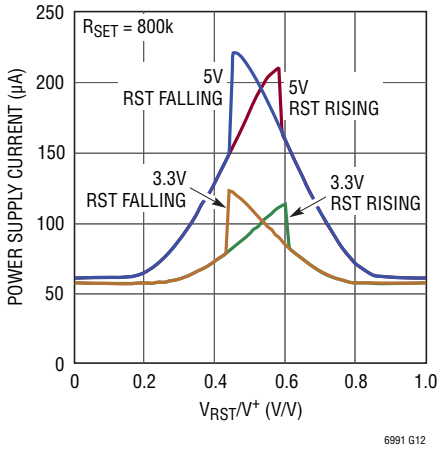
Supply Current vs Supply Voltage



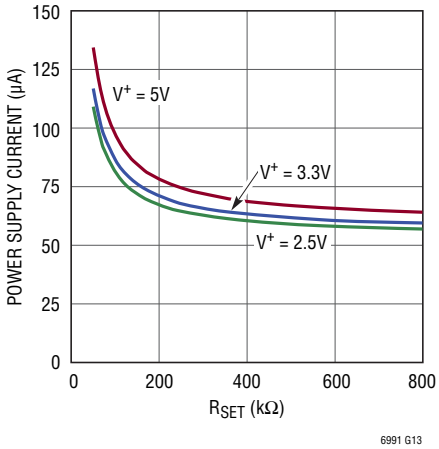
Supply Current vs Temperature



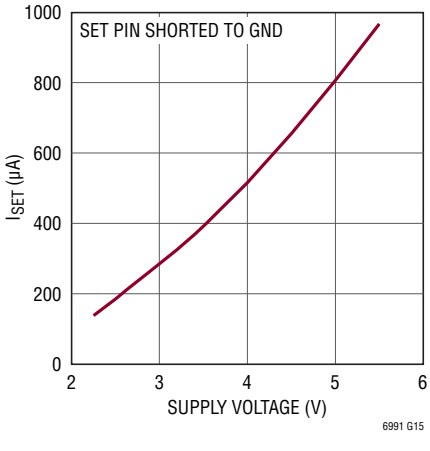
Supply Current vs RST Pin Voltage



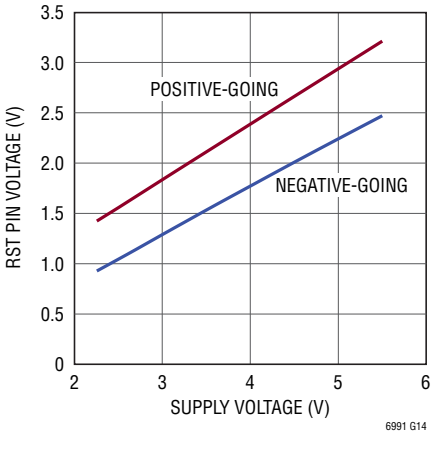
Supply Current vs R_{SET}



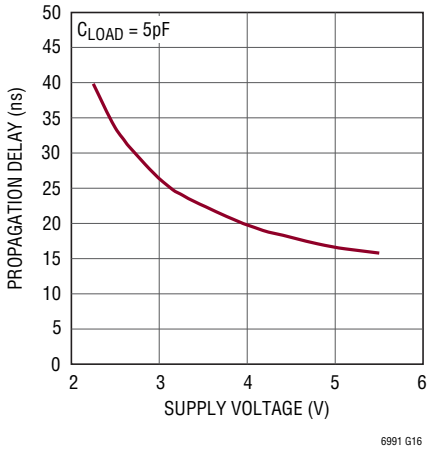
Typical I_{SET} Current Limit vs V^+



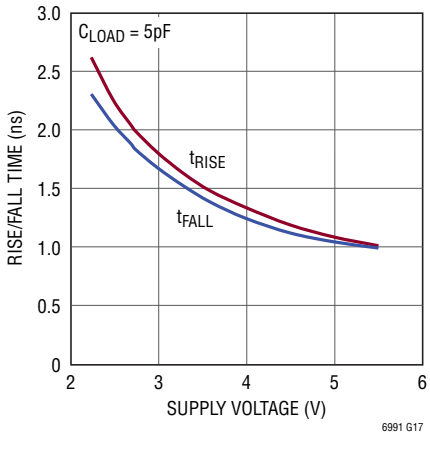
RST Threshold Voltage vs Supply Voltage



Reset Propagation Delay (t_{RST}) vs Supply Voltage



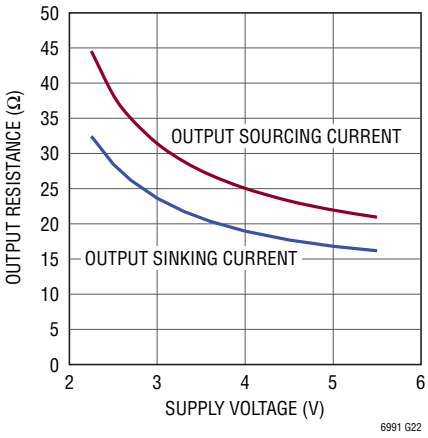
Rise and Fall Time vs Supply Voltage



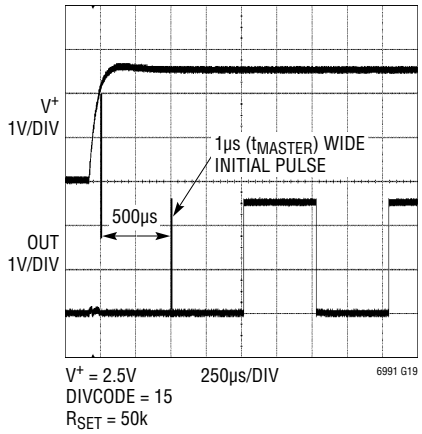
TYPICAL PERFORMANCE CHARACTERISTICS

V^+ = 3.3V, R_{SET} = 200k, T_A = 25°C unless otherwise noted.

Output Resistance vs Supply Current



Typical Start-Up with POL = 1



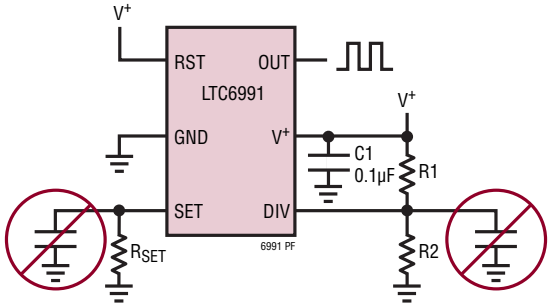
PIN FUNCTIONS (DCB/S6)

V^+ (Pin 1/Pin 5): Supply Voltage (2.25V to 5.5V). This supply should be kept free from noise and ripple. It should be bypassed directly to the GND pin with a 0.1µF capacitor.

DIV (Pin 2/Pin 4): Programmable Divider and Polarity Input. A V^+ referenced A/D converter monitors the DIV pin voltage (V_{DIV}) to determine a 4-bit result (DIVCODE). V_{DIV} may be generated by a resistor divider between V^+ and GND. Use 1% resistors to ensure an accurate result. The DIV pin and resistors should be shielded from the OUT pin or any other traces that have fast edges. Limit the capacitance on the DIV pin to less than 100pF so that V_{DIV} settles quickly. The MSB of DIVCODE (POL) determines the polarity of the RST and OUT pins. If POL = 0, RST is active-high, and forces OUT low. If POL = 1, RST is active-low and forces OUT high.

SET (Pin 3/Pin 3): Frequency-Setting Input. The voltage on the SET pin (V_{SET}) is regulated to 1V above GND. The amount of current sourced from the SET pin (I_{SET}) programs the master oscillator frequency. The I_{SET} current range is 1.25µA to 20µA. The output oscillation will stop if I_{SET} drops below approximately 500nA. A resistor connected between SET and GND is the most accurate way to set the frequency. For best performance, use a precision metal or thin film resistor of 0.5% or better tolerance and 50ppm/°C or better temperature coefficient. For lower accuracy applications an inexpensive 1% thick film resistor may be used.

Limit the capacitance on the SET pin to less than 10pF to minimize jitter and ensure stability. Capacitance less than 100pF maintains the stability of the feedback circuit regulating the V_{SET} voltage.



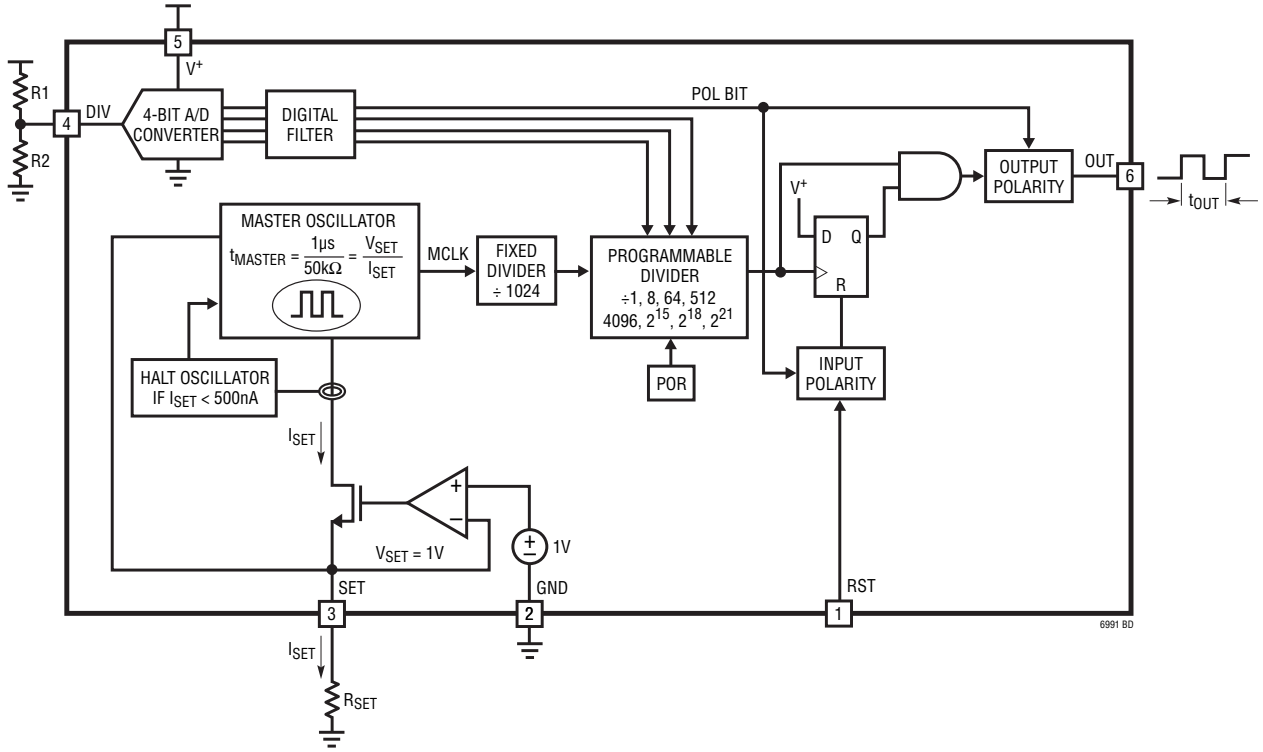
RST (Pin 4/Pin 1): Output Reset. The behavior of the RST pin is dependent on the polarity bit (POL). The POL bit is configured via the DIVCODE setting. When POL = 0, setting RST high forces OUT low and setting RST low allows the output to oscillate. When POL = 1, RST is active low. In that case, setting RST low forces OUT high and setting RST high allows the output to oscillate.

PIN FUNCTIONS (DCB/S6)

GND (Pin 5/Pin 2): Ground. Tie to a low inductance ground plane for best performance.

OUT (Pin 6/Pin 6): Oscillator Output. The OUT pin swings from GND to V^+ with an output resistance of approximately 30Ω. When driving an LED or other low impedance load a series output resistor should be used to limit source/sink current to 20mA.

BLOCK DIAGRAM (S6 package pin numbers shown)



OPERATION

The LTC6991 is built around a master oscillator with a 1MHz maximum frequency. The oscillator is controlled by the SET pin current (I_{SET}) and voltage (V_{SET}), with a 1MHz • 50k conversion factor that is accurate to ±0.8% under typical conditions.

$$f_{MASTER} = \frac{1}{t_{MASTER}} = 1MHz \bullet 50k\Omega \bullet \frac{I_{SET}}{V_{SET}}$$

A feedback loop maintains V_{SET} at 1V ±30mV, leaving I_{SET} as the primary means of controlling the output frequency. The simplest way to generate I_{SET} is to connect a resistor (R_{SET}) between SET and GND, such that $I_{SET} = V_{SET}/R_{SET}$. The master oscillator equation reduces to:

$$f_{MASTER} = \frac{1}{t_{MASTER}} = \frac{1MHz \bullet 50k\Omega}{R_{SET}}$$

From this equation, it is clear that V_{SET} drift will not affect the output frequency when using a single program resistor (R_{SET}). Error sources are limited to R_{SET} tolerance and the inherent frequency accuracy Δf_{OUT} of the LTC6991.

R_{SET} may range from 50k to 800k (equivalent to I_{SET} between 1.25µA and 20µA).

Before reaching the OUT pin, the oscillator frequency passes through a fixed ÷1024 divider. The LTC6991 also includes a programmable frequency divider which can further divide the frequency by 1, 8, 64, 512, 4096, 2^{15}, 2^{18} or 2^{21}. The divider ratio N_{DIV} is set by a resistor divider attached to the DIV pin.

$$f_{OUT} = \frac{1MHz \bullet 50k\Omega}{1024 \bullet N_{DIV}} \bullet \frac{I_{SET}}{V_{SET}}, \text{ or}$$

$$t_{OUT} = \frac{1}{f_{OUT}} = \frac{N_{DIV}}{50k\Omega} \bullet \frac{V_{SET}}{I_{SET}} \bullet 1.024ms$$

with R_{SET} in place of V_{SET}/I_{SET} the equation reduces to:

$$t_{OUT} = \frac{N_{DIV} \bullet R_{SET}}{50k\Omega} \bullet 1.024ms$$

DIVCODE

The DIV pin connects to an internal, V^+ referenced 4-bit A/D converter that determines the DIVCODE value. DIVCODE programs two settings on the LTC6991:

1. DIVCODE determines the output frequency divider setting, N_{DIV}.
2. DIVCODE determines the polarity of the RST and OUT pins, via the POL bit.

V_{DIV} may be generated by a resistor divider between V^+ and GND as shown in Figure 1.

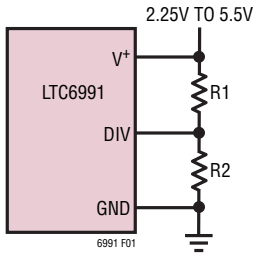


Figure 1. Simple Technique for Setting DIVCODE

Table 1 offers recommended 1% resistor values that accurately produce the correct voltage division as well as the corresponding N_{DIV} and POL values for the recommended resistor pairs. Other values may be used as long as:

1. The V_{DIV}/V^+ ratio is accurate to ±1.5% (including resistor tolerances and temperature effects)
2. The driving impedance (R1||R2) does not exceed 500kΩ.

If the voltage is generated by other means (i.e., the output of a DAC) it must track the V^+ supply voltage. The last column in Table 1 shows the ideal ratio of V_{DIV} to the supply voltage, which can also be calculated as:

$$\frac{V_{DIV}}{V^+} = \frac{DIVCODE + 0.5}{16} \pm 1.5\%$$

For example, if the supply is 3.3V and the desired DIVCODE is 4, V_{DIV} = 0.281 • 3.3V = 928mV ± 50mV.

Figure 2 illustrates the information in Table 1, showing that N_{DIV} is symmetric around the DIVCODE midpoint.

OPERATION

Table 1. DIVCODE Programming

DIVCODE	POL	N_{DIV}	RECOMMENDED t_{OUT}	R1 (kΩ)	R2 (kΩ)	V_{DIV}/V^+
0	0	1	1.024ms to 16.384ms	Open	Short	≤0.03125 ±0.015
1	0	8	8.192ms to 131ms	976	102	0.09375 ±0.015
2	0	64	65.5ms to 1.05sec	976	182	0.15625 ±0.015
3	0	512	524ms to 8.39sec	1000	280	0.21875 ±0.015
4	0	4,096	4.19sec to 67.1sec	1000	392	0.28125 ±0.015
5	0	32,768	33.6sec to 537sec	1000	523	0.34375 ±0.015
6	0	262,144	268sec to 4,295sec	1000	681	0.40625 ±0.015
7	0	2,097,152	2,147sec to 34,360sec	1000	887	0.46875 ±0.015
8	1	2,097,152	2,147sec to 34,360sec	887	1000	0.53125 ±0.015
9	1	262,144	268sec to 4,295sec	681	1000	0.59375 ±0.015
10	1	32,768	33.6sec to 537sec	523	1000	0.65625 ±0.015
11	1	4,096	4.19sec to 67.1sec	392	1000	0.71875 ±0.015
12	1	512	524ms to 8.39sec	280	1000	0.78125 ±0.015
13	1	64	65.5ms to 1.05sec	182	976	0.84375 ±0.015
14	1	8	8.192ms to 131ms	102	976	0.90625 ±0.015
15	1	1	1.024ms to 16.384ms	Short	Open	≥0.96875 ±0.015

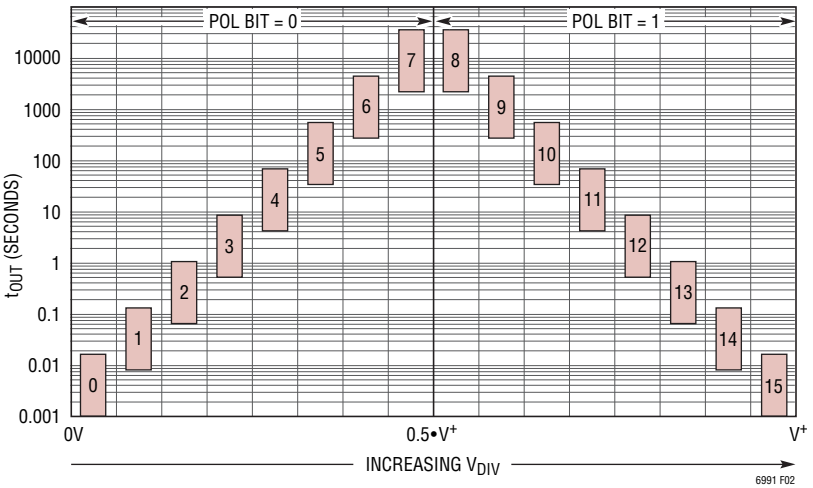


Figure 2. Frequency Range and POL Bit vs DIVCODE

OPERATION

RST Pin and Polarity (POL) Bit

The RST pin controls the state of the LTC6991's output as seen on the OUT pin. The active/inactive voltage levels depend on the POL bit setting.

Table 2. Output States

POL BIT	RST PIN	OUTPUT STATE
0	0	Oscillating
0	1	0 (reset)
1	0	1 (reset)
1	1	Oscillating

Each period of the LTC6991's internal oscillator clocks the output state latch (see Block Diagram). The reset pin (RST) can reset or hold off the output latch. The active state of the reset pin is determined by the polarity function (POL). Similarly, the output latch is followed by a buffer that can invert the output. The output polarity is also controlled by the POL bit.

If POL = 0, the reset pin is active high and the output latch is not inverted. Therefore, pulling the RST pin high will reset the output latch and force the OUT pin low. Pulling RST low will allow the output to oscillate, with the next rising edge dependent on the internal oscillator.

If POL = 1, the reset pin is active low and the output latch is inverted. Therefore, pulling the RST pin low will reset the output latch and force the OUT pin high. Pulling RST high will allow the output to oscillate, with the next falling edge dependent on the internal oscillator.

Note that the master oscillator frequency and phase are not affected by the RST pin; The LTC6991 continues to oscillate, internally, even when RST is active. While the reset function can block an output pulse, its exact placement in time can only be changed by power cycling the LTC6991.

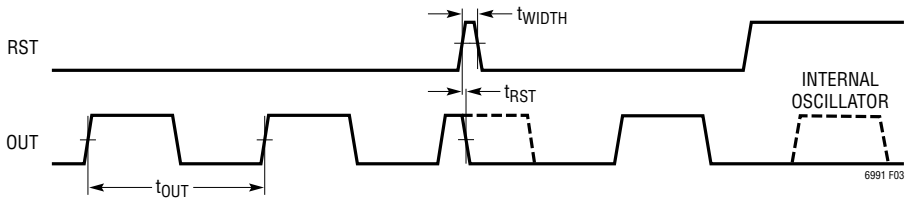


Figure 3. RST Timing Diagram (POL = 0)

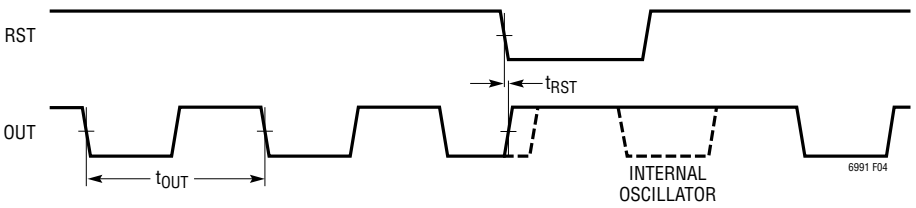


Figure 4. RST Timing Diagram (POL = 1)

OPERATION

Changing DIVCODE After Start-Up

Following start-up, the A/D converter will continue monitoring V_{DIV} for changes. The LTC6991 will respond to DIVCODE changes in less than one cycle.

$$t_{DIVCODE} < 500 \bullet t_{MASTER} < t_{OUT}$$

The output may have an inaccurate pulse width during the frequency transition. But the transition will be glitch-free and no high or low pulse can be shorter than the master clock period. A digital filter is used to guarantee the DIVCODE has settled to a new value before making changes to the output.

Start-Up Time

When power is first applied, the power-on reset (POR) circuit will initiate the start-up time, t_{START}. The OUT pin is held low during this time. The typical value for t_{START} ranges from 0.5ms to 8ms depending on the master oscillator frequency (independent of N_{DIV}):

$$t_{START(TYP)} = 500 \bullet t_{MASTER}$$

During start-up, the DIV pin A/D converter must determine the correct DIVCODE before the output is enabled. The start-up time may increase if the supply or DIV pin voltages are not stable. For this reason, it is recommended to minimize the capacitance on the DIV pin so it will properly track V^+. Less than 100pF will not affect performance.

Start-Up Behavior

When first powered up, the output is held low. If the polarity is set for non-inversion (POL = 0) and the output is enabled (RST = 0) at the end of the start-up time, OUT will begin oscillating. If the output is being reset (RST = 1) at the end of the start-up time, the first pulse will be skipped. Subsequent pulses will also be skipped until RST = 0.

In inverted operation (POL = 1), the start-up sequence is similar. However, the LTC6991 does not know the correct DIVCODE setting when first powered up, so the output defaults low. At the end of t_{START}, the value of DIVCODE is recognized and OUT goes high (inactive) because POL = 1. If RST = 1 (inactive) then OUT will quickly fall after a single t_{MASTER} cycle. If RST = 0 at the end of the start-up time, the output is held in reset and remains high.

Figures 7 to 10 detail the four possible start-up sequences.

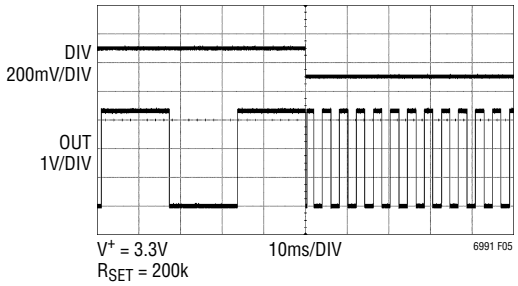


Figure 5. DIVCODE Change from 1 to 0

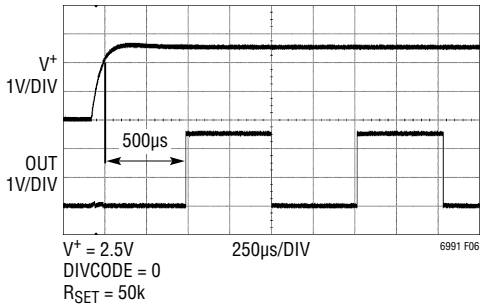


Figure 6. Typical Start-Up

OPERATION

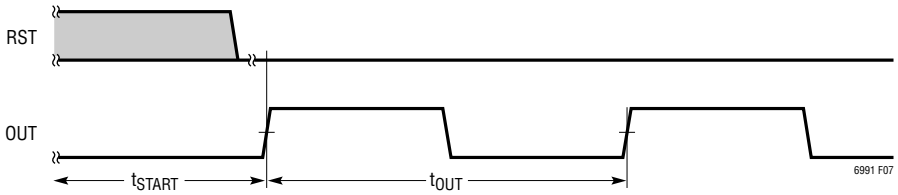


Figure 7. Start-Up Timing Diagram (RST = 0, POL = 0)

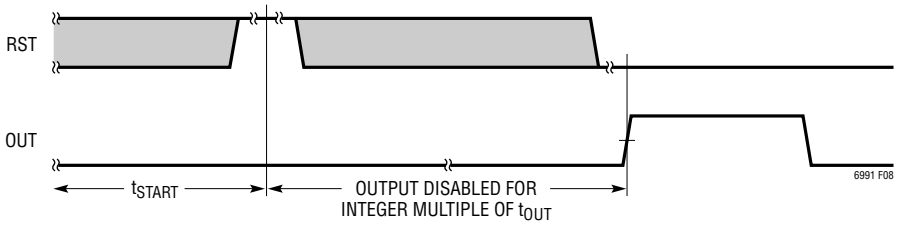


Figure 8. Start-Up Timing Diagram (RST = 1, POL = 0)

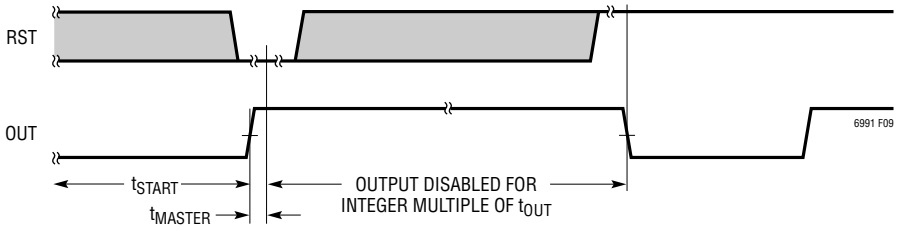


Figure 9. Start-Up Timing Diagram (RST = 0, POL = 1)

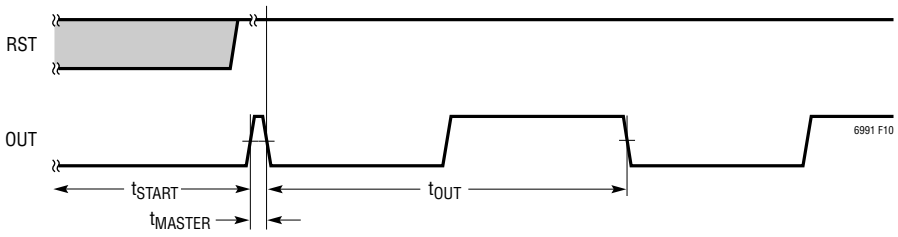


Figure 10. Start-Up Timing Diagram (RST = 1, POL = 1)

APPLICATIONS INFORMATION

Basic Operation

The simplest and most accurate method to program the LTC6991 is to use a single resistor, R_{SET}, between the SET and GND pins. The design procedure is a 3-step process. First select the POL bit setting and N_{DIV} value, then calculate the value for the R_{SET} resistor.

Step 1: Select the POL Bit Setting

The LTC6991 can operate in normal (active-high) or inverted (active-low) modes, depending on the setting of the POL bit. The best choice depends on the the application.

Step 2: Select the N_{DIV} Frequency Divider Value

As explained earlier, the voltage on the DIV pin sets the DIVCODE which determines both the POL bit and the N_{DIV} value. For a given output clock period, N_{DIV} should be selected to be within the following range.

$$\frac{t_{OUT}}{16.384ms} \leq N_{DIV} \leq \frac{t_{OUT}}{1.024ms} \quad (1)$$

To minimize supply current, choose the lowest N_{DIV} value (generally recommended). Alternatively, use Table 1 as a guide to select the best N_{DIV} value for the given application.

With POL already chosen, this completes the selection of DIVCODE. Use Table 1 to select the proper resistor divider or V_{DIV}/V^+ ratio to apply to the DIV pin.

Step 3: Calculate and Select R_{SET}

The final step is to calculate the correct value for R_{SET} using the following equation.

$$R_{SET} = \frac{50k}{1.024ms} \bullet \frac{t_{OUT}}{N_{DIV}} \quad (2)$$

Select the standard resistor value closest to the calculated value.

Example: Design a 1Hz oscillator with minimum power consumption and active-high reset input.

Step 1: Select the POL Bit Setting

For noninverted (active-high) functionality, choose POL = 0.

Step 2: Select the N_{DIV} Frequency Divider Value

Choose an N_{DIV} value that meets the requirements of Equation (1), using t_{OUT} = 1000ms:

$61.04 \leq N_{DIV} \leq 976.6$

Potential settings for N_{DIV} include 64 and 512. N_{DIV} = 64 is the best choice, as it minimizes supply current by using a large R_{SET} resistor. POL = 0 and N_{DIV} = 64 requires DIVCODE = 2. Using Table 1, choose R1 = 976k and R2 = 182k values to program DIVCODE = 2.

Step 3: Select R_{SET}

Calculate the correct value for R_{SET} using Equation (2).

$$R_{SET} = \frac{50k}{1.024ms} \bullet \frac{1000ms}{64} = 763k$$

Since 763k is not available as a standard 1% resistor, substitute 768k if a –0.7% frequency shift is acceptable. Otherwise, select a parallel or series pair of resistors such as 576k + 187k to attain a more precise resistance.

The completed design is shown in Figure 11.

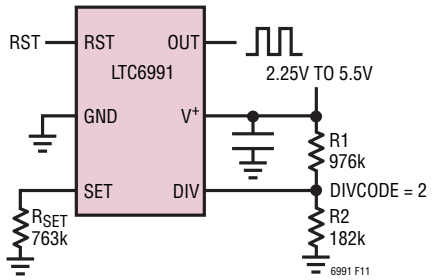


Figure 11. 1Hz Oscillator

APPLICATIONS INFORMATION

LTC6991 as "Wake-Up Timer"

The output latch reset function provided by the RST pin allows the LTC6991 to enable a larger system at regular intervals. The on-time can be controlled by the system. This allows the system to shut itself down immediately after performing its tasks, reducing power consumption.

Figure 12 shows an example using "black boxes" for a switching regulator and the system being duty-cycled. In some cases, an RC filter may be necessary at the RST input to filter start-up glitches from the system as it is powered on.

If the LTC6991 is enabling a switching regulator that can operate on supplies greater than 5.5V, it will be necessary to limit the supply voltage provided to the LTC6991. If the LTC6991 output is not heavily loaded, and if a large R_{SET} resistor is used, the supply current will not be much larger than 100µA, so a simple regulator circuit can be constructed using a Zener diode.

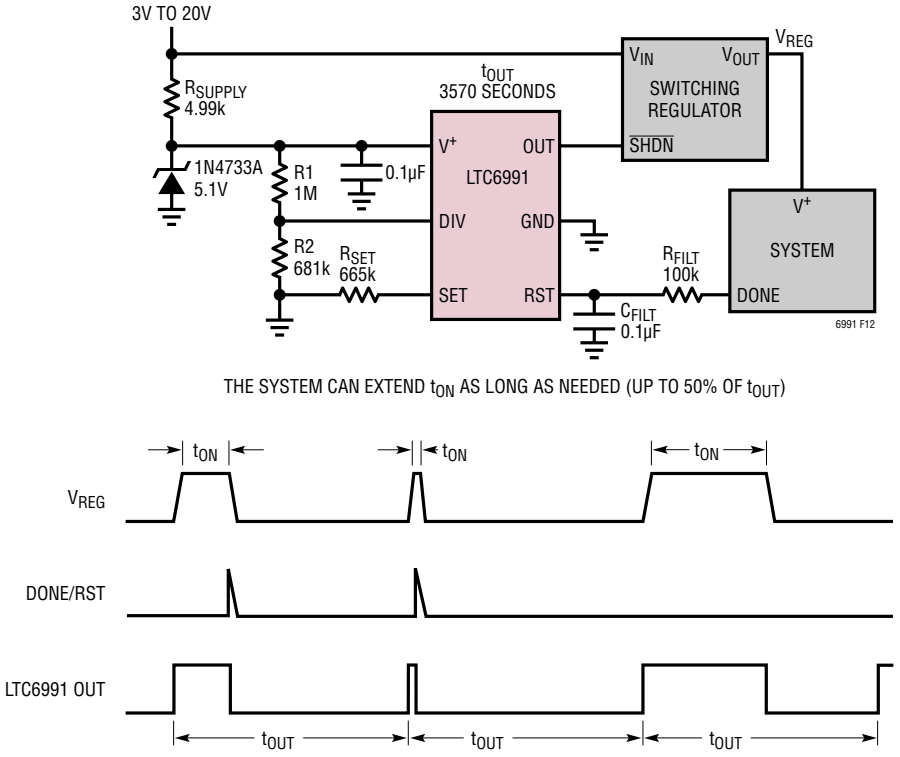


Figure 12. Powering Up a System Once an Hour

APPLICATIONS INFORMATION

Self-Resetting Circuits

The RST pin has hysteresis to accommodate slow-changing input voltages. Furthermore, the trip points are proportional to the supply voltage (see Note 6 and the RST Threshold Voltage vs Supply Voltage curve in Typical Performance Characteristics). This allows an RC time constant at the RST input to generate a delay that is nearly independent of the supply voltage.

A simple application of this technique allows the LTC6991 output to reset itself, producing a well-controlled pulse once each cycle. Figures 13a and 13b show circuits that produce approximately 1µs pulses once a minute. The only difference is in the POL bit setting, which controls whether the pulse is positive or negative.

Voltage Controlled Frequency

With one additional resistor, the LTC6991 output frequency can be manipulated by an external voltage. As shown in Figure 14, voltage V_{CTRL} sources/sinks a current through R_{VCO} to vary the I_{SET} current, which in turn modulates the output frequency as described in Equation (3).

$$f_{OUT} = \frac{1MHz \bullet 50k\Omega}{1024 \bullet N_{DIV} \bullet R_{VCO}} \bullet \left(1 + \frac{R_{VCO}}{R_{SET}} - \frac{V_{CTRL}}{V_{SET}}\right) \quad (3)$$

Digital Frequency Control

The control voltage can be generated by a DAC (digital-to-analog converter), resulting in a digitally-controlled frequency. Many DACs allow for the use of an external reference. If such a DAC is used to provide the V_{CTRL} voltage, the V_{SET} dependency can be eliminated by buffering V_{SET} and using it as the DAC's reference voltage, as shown in Figure 15. The DAC's output voltage now tracks any V_{SET} variation and eliminates it as an error source. The SET pin cannot be tied directly to the reference input of the DAC because the current drawn by the DAC's REF input would affect the frequency.

I_{SET} Extremes (Master Oscillator Frequency Extremes)

When operating with I_{SET} outside of the recommended 1.25µA to 20µA range, the master oscillator operates outside of the 62.5kHz to 1MHz range in which it is most accurate.

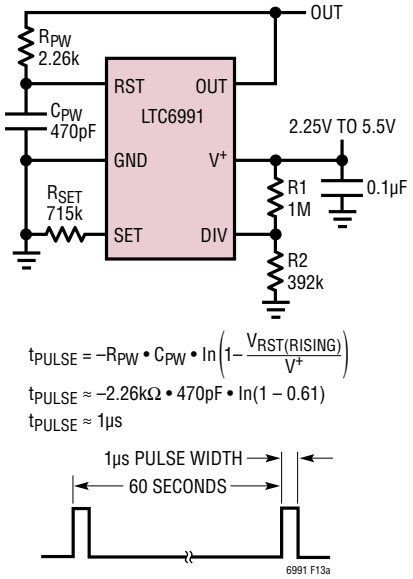


Figure 13a. Self-Resetting Circuit (DIVCODE = 4)

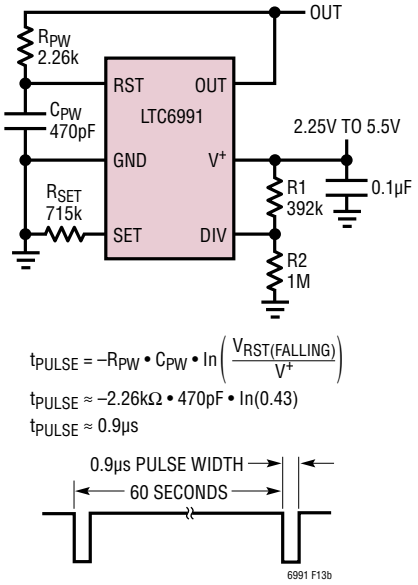


Figure 13b. Self-Resetting Circuit (DIVCODE = 11)

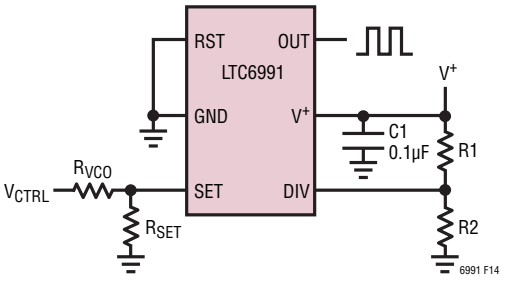


Figure 14. Voltage-Controlled Oscillator

APPLICATIONS INFORMATION

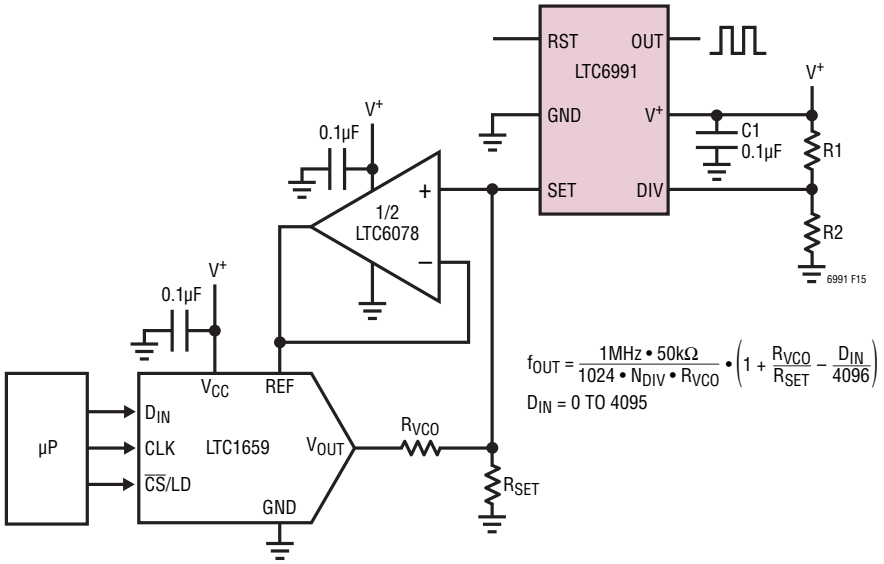


Figure 15. Digitally-Controlled Oscillator

The oscillator can still function with reduced accuracy for I_{SET} < 1.25µA. At approximately 500nA, the oscillator output will be frozen in its current state. The output could halt in a high or low state. This avoids introducing short pulses when frequency modulating a very low frequency output.

At the other extreme, it is not recommended to operate the master oscillator beyond 2MHz because the accuracy of the DIV pin ADC will suffer.

Frequency Modulation and Settling Time

The LTC6991 will respond to changes in I_{SET} up to a –3dB bandwidth of 0.4 • f_{OUT}.

Following a 2× or 0.5× step change in I_{SET}, the output frequency takes less than one cycle to settle to within 1% of the final value.

Power Supply Current

The power supply current varies with frequency, supply voltage and output loading. It can be estimated under any condition using the following equation. This equation ignores C_{LOAD} (valid for C_{LOAD} < 1nF) and assumes the output has 50% duty cycle.

$$I_{S(TYP)} \approx V^+ \bullet f_{MASTER} \bullet 7.8pF + \frac{V^+}{420k\Omega} + \frac{V^+}{2 \bullet R_{LOAD}} + 1.8 \bullet I_{SET} + 50\mu A$$

Supply Bypassing and PCB Layout Guidelines

The LTC6991 is a 2.2% accurate silicon oscillator when used in the appropriate manner. The part is simple to use and by following a few rules, the expected performance is easily achieved. Adequate supply bypassing and proper PCB layout are important to ensure this.

Figure 18 shows example PCB layouts for both the TSOT-23 and DFN packages using 0603 sized passive components. The layouts assume a two layer board with a ground plane layer beneath and around the LTC6991. These layouts are a guide and need not be followed exactly.

APPLICATIONS INFORMATION

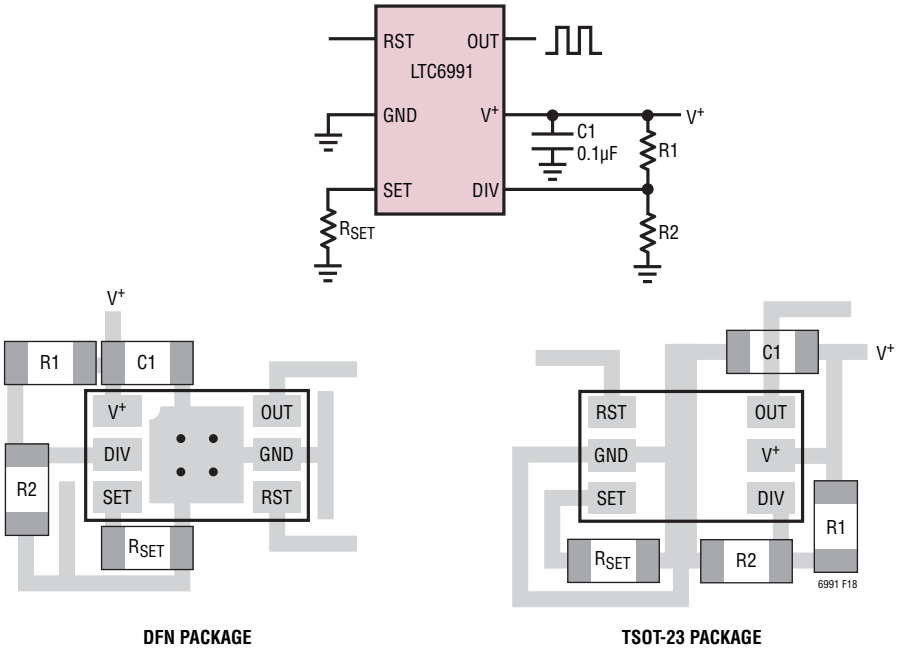
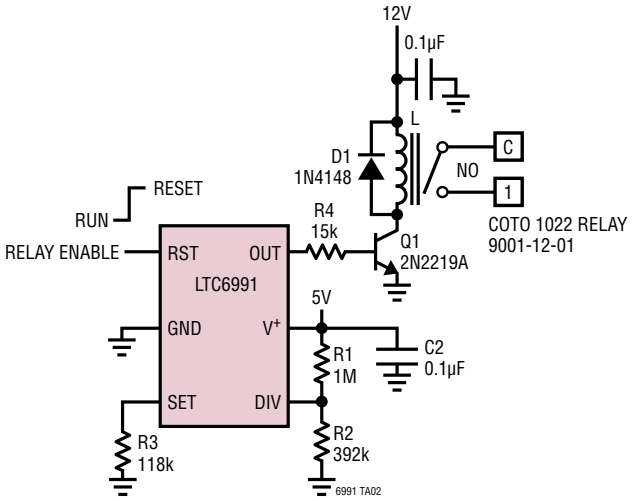


Figure 18. Supply Bypassing and PCB Layout

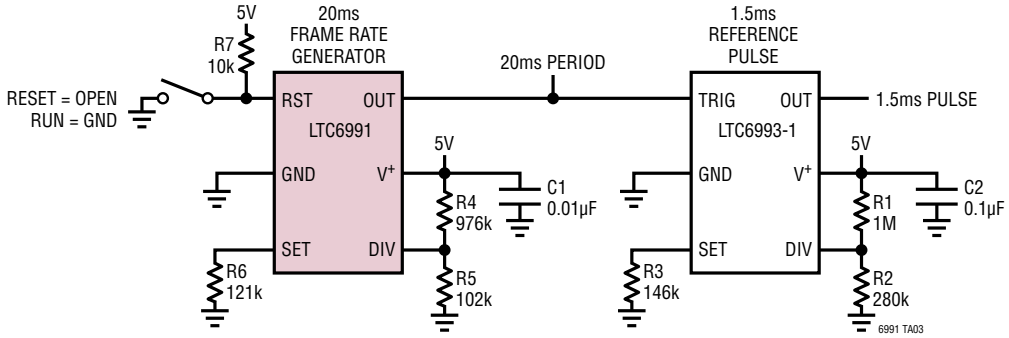
1. Connect the bypass capacitor, C1, directly to the V^+ and GND pins using a low inductance path. The connection from C1 to the V^+ pin is easily done directly on the top layer. For the DFN package, C1's connection to GND is also simply done on the top layer. For the TSOT-23, OUT can be routed through the C1 pads to allow a good C1 GND connection. If the PCB design rules do not allow that, C1's GND connection can be accomplished through multiple vias to the ground plane. Multiple vias for both the GND pin connection to the ground plane and the C1 connection to the ground plane are recommended to minimize the inductance. Capacitor C1 should be a 0.1µF ceramic capacitor.
2. Place all passive components on the top side of the board. This minimizes trace inductance.
3. Place R_{SET} as close as possible to the SET pin and make a direct, short connection. The SET pin is a current summing node and currents injected into this pin directly modulate the operating frequency. Having a short connection minimizes the exposure to signal pickup.
4. Connect R_{SET} directly to the GND pin. Using a long path or vias to the ground plane will not have a significant affect on accuracy, but a direct, short connection is recommended and easy to apply.
5. Use a ground trace to shield the SET pin. This provides another layer of protection from radiated signals.
6. Place R1 and R2 close to the DIV pin. A direct, short connection to the DIV pin minimizes the external signal coupling.

TYPICAL APPLICATIONS

5 Second On/Off Timed Relay Driver

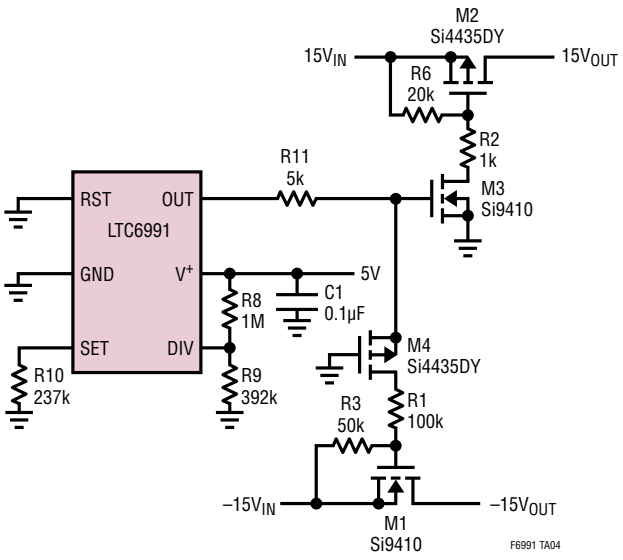


1.5ms Radio Control Servo Reference Pulse Generator

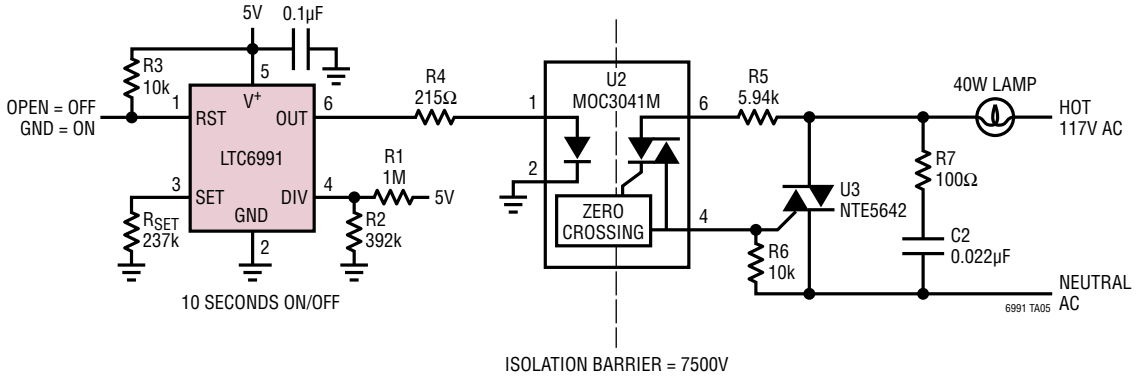


TYPICAL APPLICATIONS

Cycling (10 Seconds On/Off) Symmetrical Power Supplies

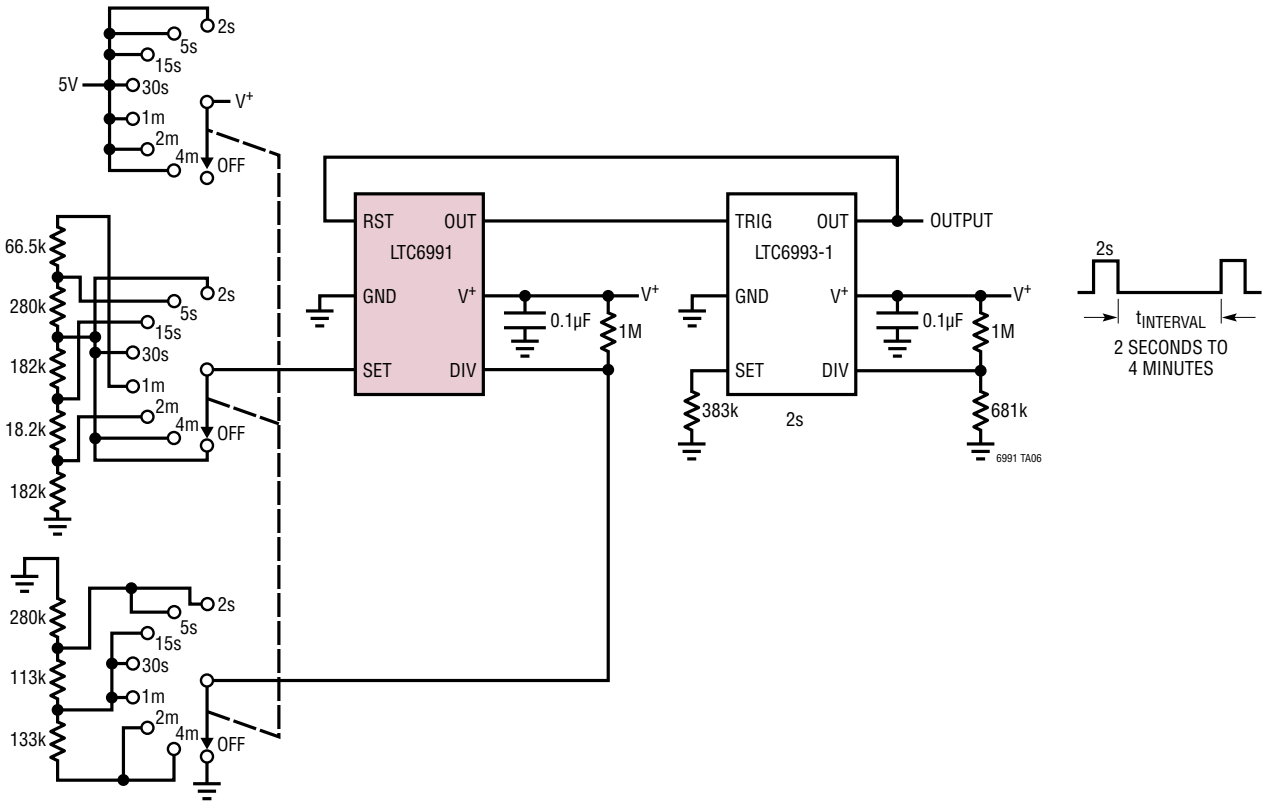


Isolated AC Load Flasher



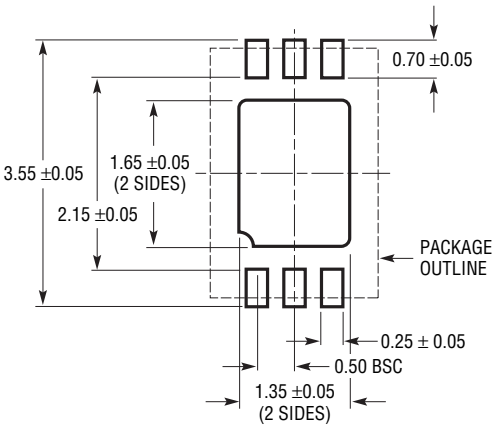
TYPICAL APPLICATIONS

Interval (Wiper) Timer

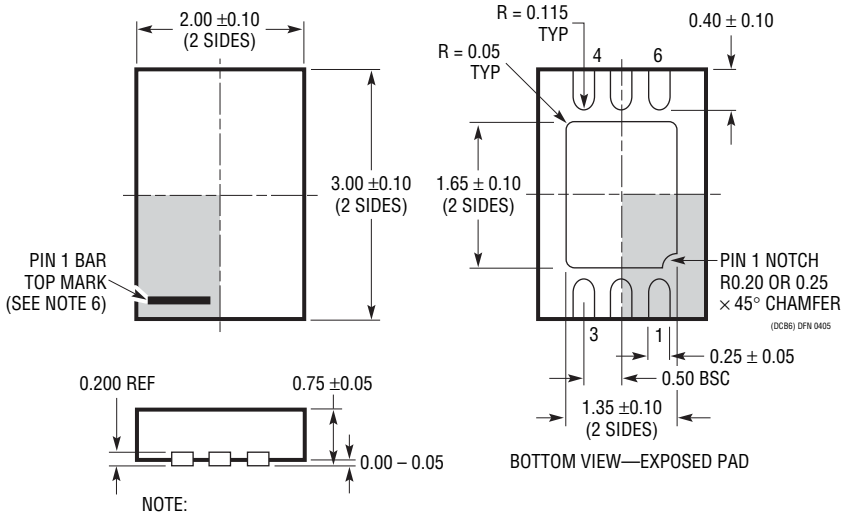


PACKAGE DESCRIPTION

DCB Package
6-Lead Plastic DFN (2mm × 3mm)
(Reference LTC DWG # 05-08-1715 Rev A)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

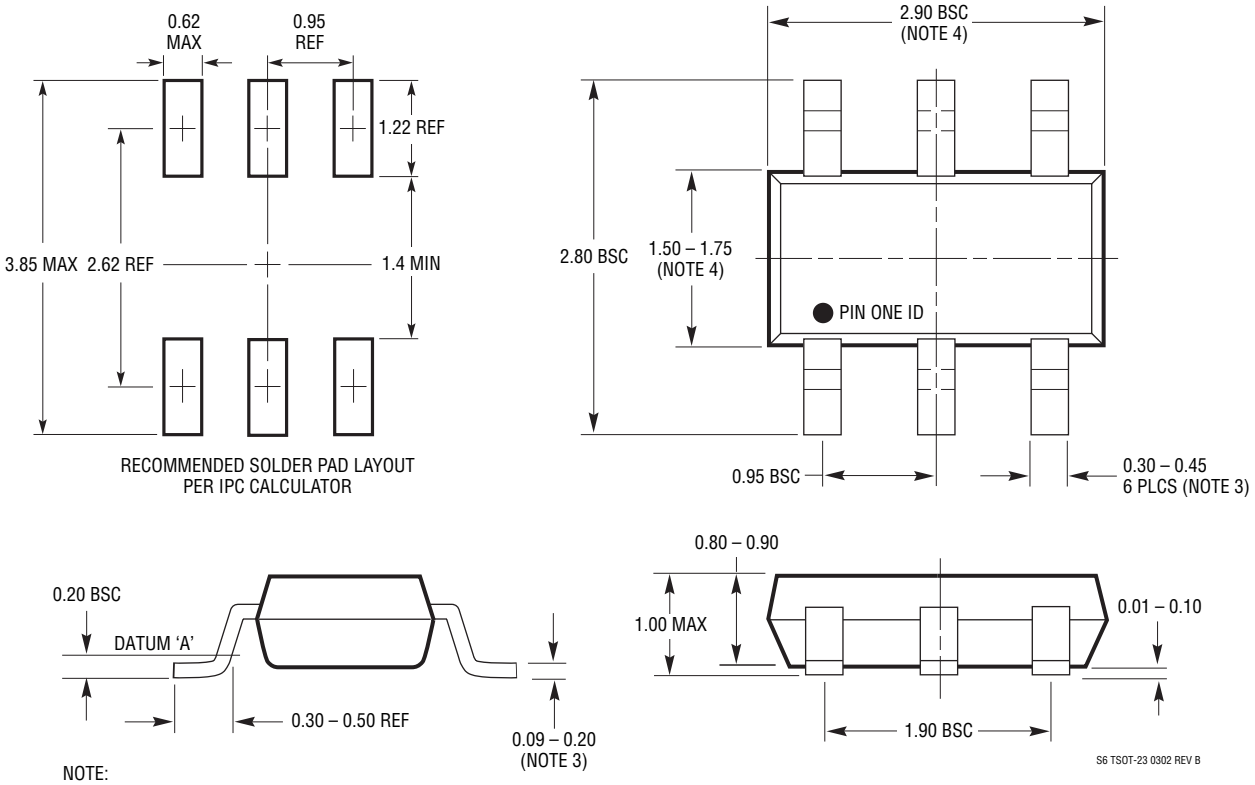


BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (TBD)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

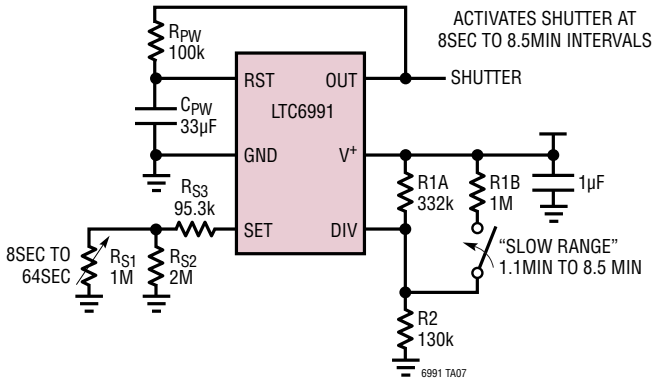
S6 Package
6-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1636)



NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

TYPICAL APPLICATION

Intervalometer for Time-Lapse Photography



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1799	1MHz to 33MHz ThinSOT Silicon Oscillator	Wide Frequency Range
LTC6900	1MHz to 20MHz ThinSOT Silicon Oscillator	Low Power, Wide Frequency Range
LTC6906/LTC6907	10kHz to 1MHz or 40kHz ThinSOT Silicon Oscillators	Micropower, I_{SUPPLY} = 35µA at 400kHz
LTC6930	Fixed Frequency Oscillator, 32.768kHz to 8.192MHz	0.09% Accuracy, 110µs Start-Up Time, 105µA at 32kHz
LTC6990	TimerBlox: Voltage-Controlled Silicon Oscillator	Fixed-Frequency or Voltage-Controlled Operation
LTC6992	TimerBlox: Voltage-Controlled Pulse Width Modulator (PWM)	Simple PWM with Wide Frequency Range
LTC6993	TimerBlox: Monostable Pulse Generator (One Shot)	Resistor Programmable Pulse Width of 1µs to 34sec
LTC6994	TimerBlox: Delay Block/Debouncer	Delays Rising, Falling or Both Edges 1µs to 34sec

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