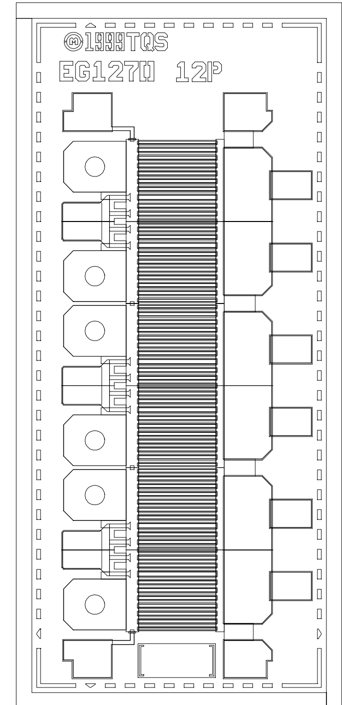
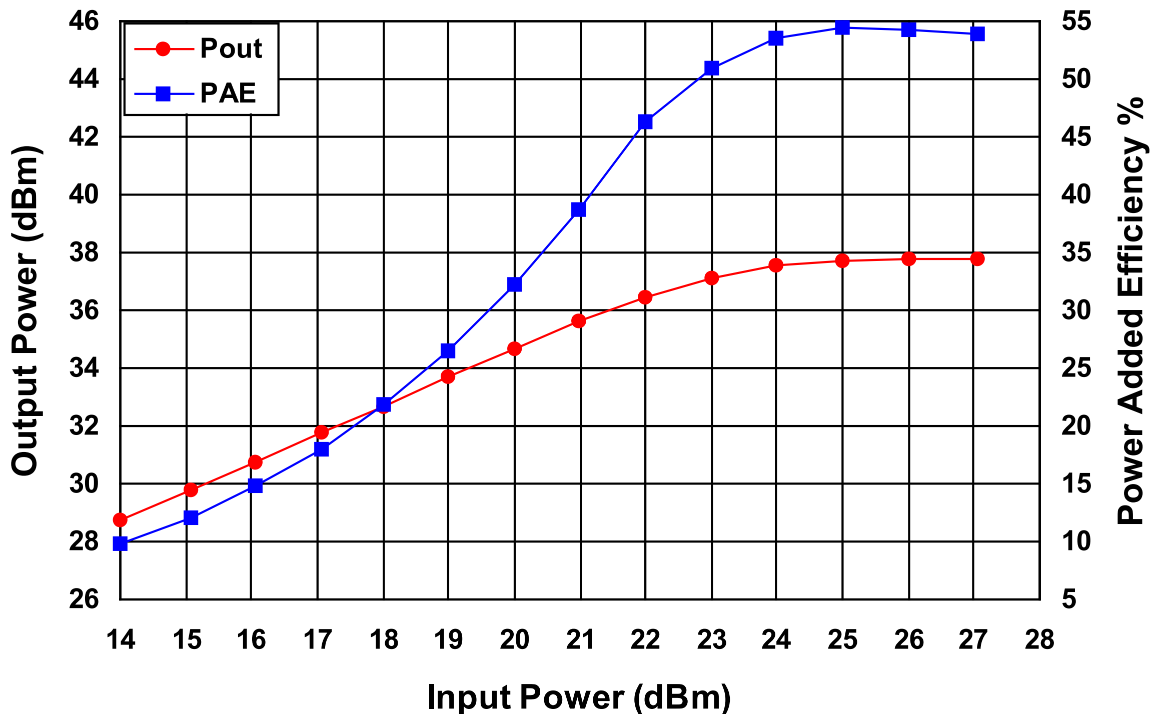
4112

February 22, 2001



- **0.5 um gate finger length**
- **Nominal Pout of 6.0 Watts at 2.3 GHz**
- **Nominal PAE of 54.5% at 2.3 GHz**
- **Nominal Gain of 12.7 dB at 2.3 GHz**
- **Die size 33.0 x 71.0 x 4.0 mils (0.8330 x 1.804 x 0.1016 mm)**

TGF4112-EPU RF Performance at F = 2.3 GHz
Vd = 8.0 V, Vg = -1.3 V, Iq = 0.75 A and T_A = 25°C



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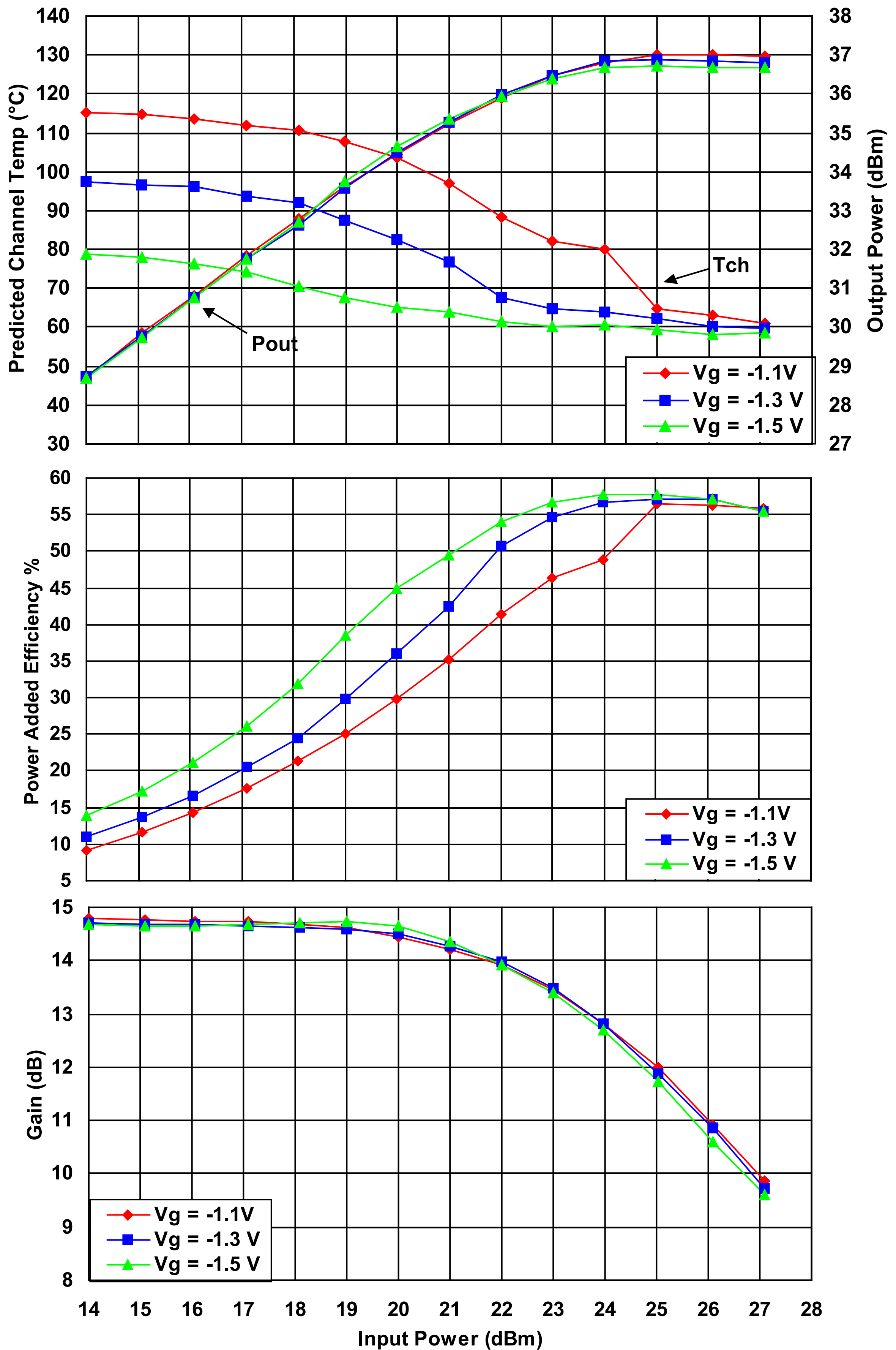

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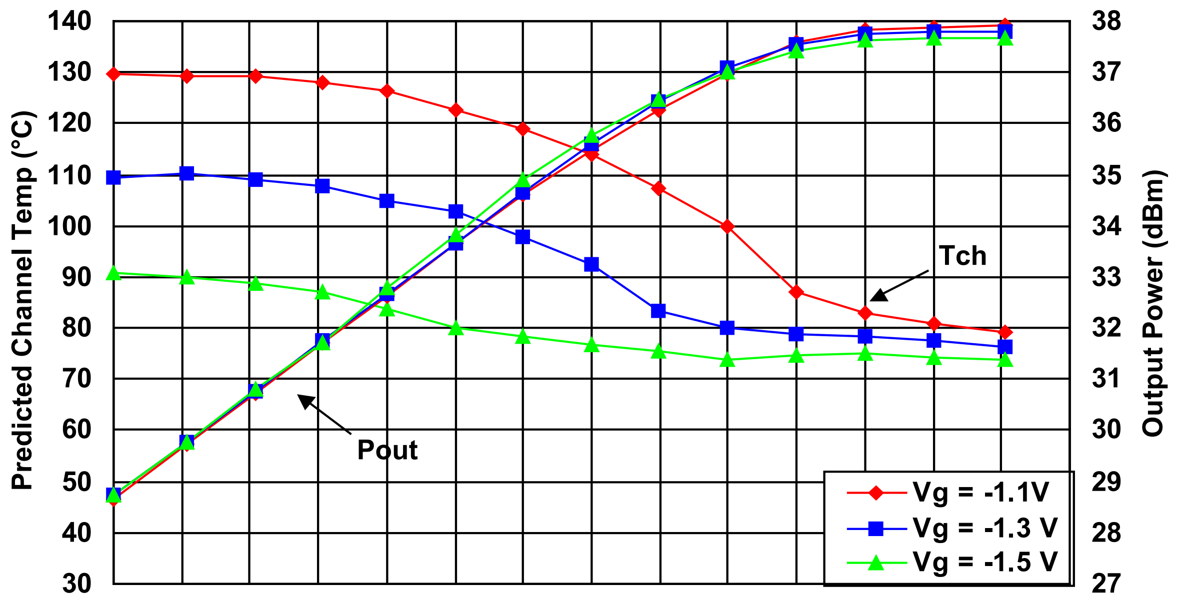
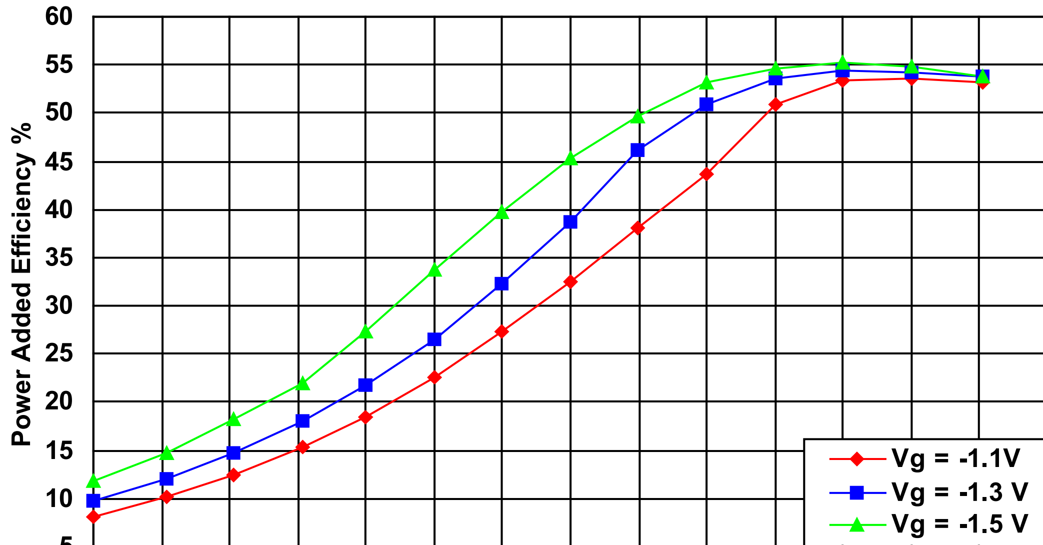
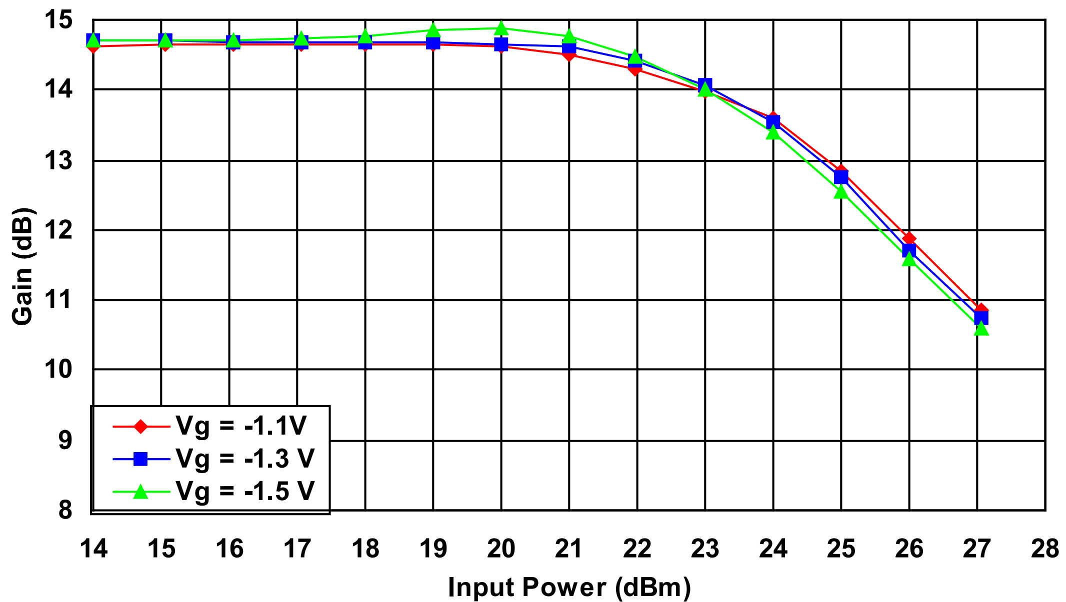
TGF4112-EPU RF Performance for Vd = 8.0 V, F = 2.3 GHz, and T_A = 25°C
Quiescent Id is 0.92 A (Vg = -1.1 V), 0.75 A (Vg = -1.3 V), and 0.65 A (Vg = -1.5 V)







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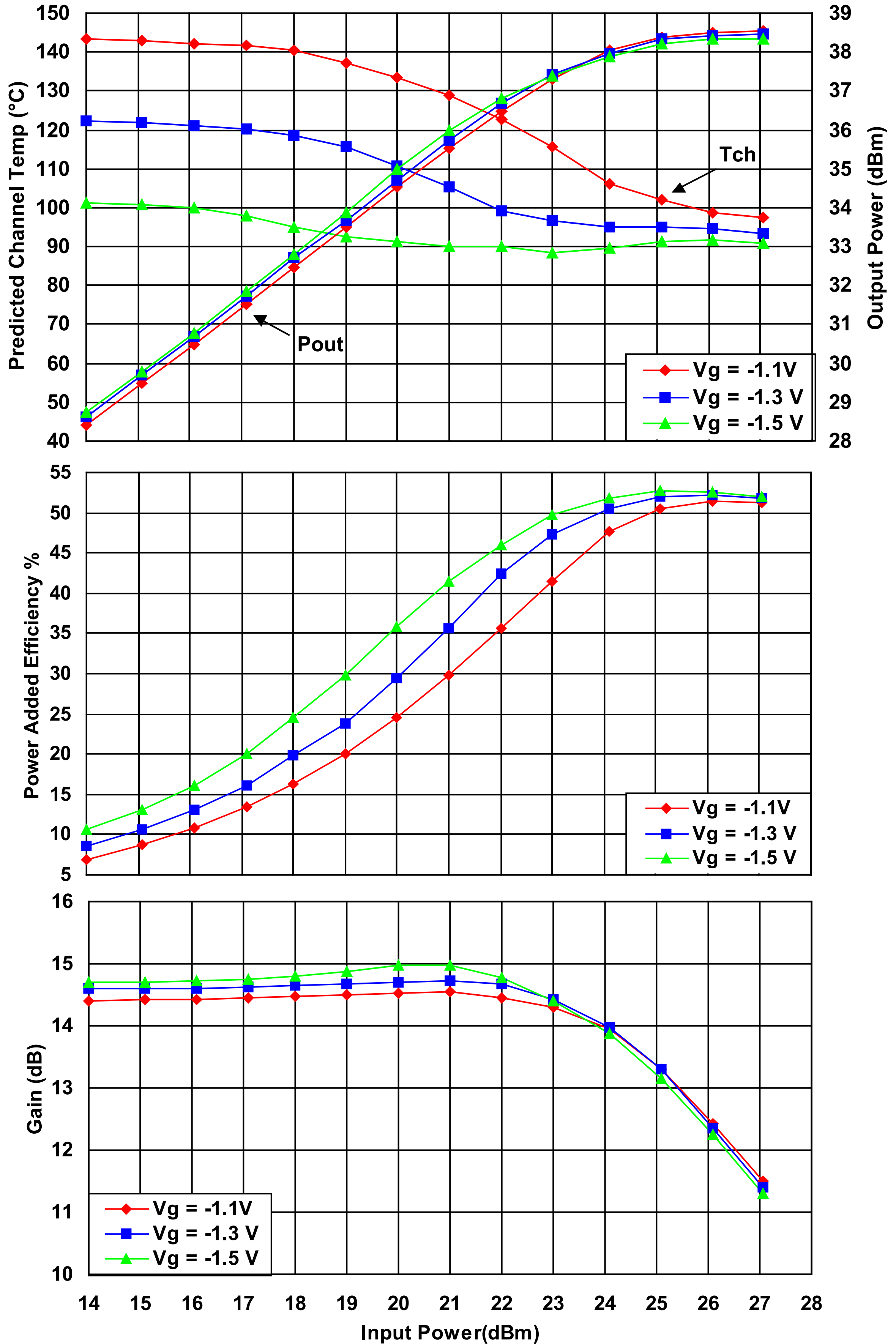

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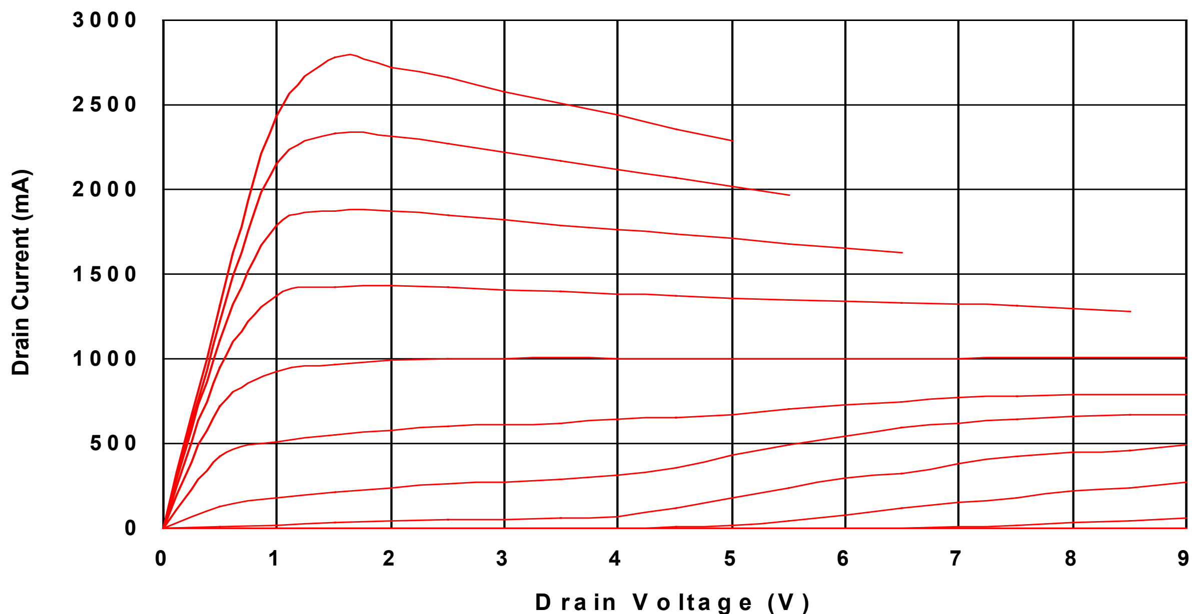
DC Characteristics for the TGF4112-EPU

	DC probe Parameters	Nominal	Unit
IDSS	Drain Saturation Current	2940	mA
GM	Transconductance	1980	mS
VP	Pinch Off Voltage	-1.85	V
BVGS	Breakdown Voltage Gate-Source	-22	V
BVGD	Breakdown Voltage Gate-Drain	-22	V

Example of DC I-V Curves
Vg = 0.0 V to -2.75 V in 0.25 steps T_A = 25°C



Absolute Maximum Ratings

Drain-to-source Voltage, Vds..12 V
Gate-to-source Voltage, Vgs..-5 V to 0 V
Mounting Temperature..320°C
Storage Temperature.. -65°C to 200°C
Power Dissipation..refer to Thermal Model
Operating Channel Temperature..refer to Thermal Model

Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in this document is not implied. Exposure to absolute maximum rated conditions for extended periods of time may affect device reliability.

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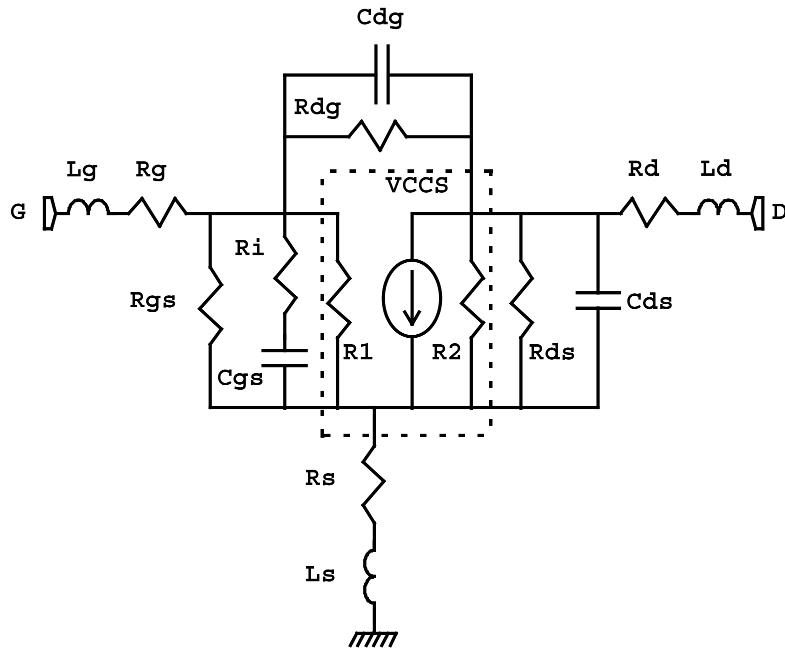
TGF4112-EPU Linear Model
Vds = 8 V and Ids = 975 mA at T = 25°C

FET Elements
Lg = .00067 nH
Rg = 0.41613 Ω
Rgs = 8170 Ω
Ri = 0.0790 Ω
Cgs = 13.5015 pF
Cdg = 0.48075 pF
Rdg = 20400 Ω
Rs = 0.08699 Ω
Ls = 0.01055 nH
Rds = 12.324 Ω
Cds = 2.2848 pF
Rd = 0.1968 Ω
Ld = 0.0067 nH
VCCS Parameters
M = 1.275 S
A = 0
R1 = 1E19
R2 = 1E19
F = 0
T = 4.51 pS



Freq-GHz	MAG-S11	ANG-S11	MAG-S21	ANG-S21	MAG-S12	ANG-S12	MAG-S22	ANG-S22
0.5	0.95286	-144.028	7.3922	104.264	0.01151	19.6716	0.70565	-175.503
1	0.9552	-161.568	3.82496	91.4018	0.01191	14.6956	0.71781	-176.052
1.5	0.95597	-167.666	2.55225	84.3852	0.01192	15.1613	0.72441	-175.654
2	0.95657	-170.752	1.9021	78.9656	0.01187	17.2723	0.73143	-175.05
2.5	0.9572	-172.62	1.50652	74.2525	0.01181	20.2495	0.73948	-174.426
3	0.95789	-173.879	1.23965	69.954	0.01177	23.8306	0.74848	-173.853
3.5	0.95862	-174.793	1.04694	65.9513	0.01179	27.8756	0.75824	-173.359
4	0.9594	-175.491	0.901	62.1894	0.01189	32.2635	0.76851	-172.956
4.5	0.9602	-176.049	0.78651	58.6402	0.01208	36.8625	0.77908	-172.647
5	0.96102	-176.51	0.69426	55.2884	0.01238	41.529	0.78973	-172.427

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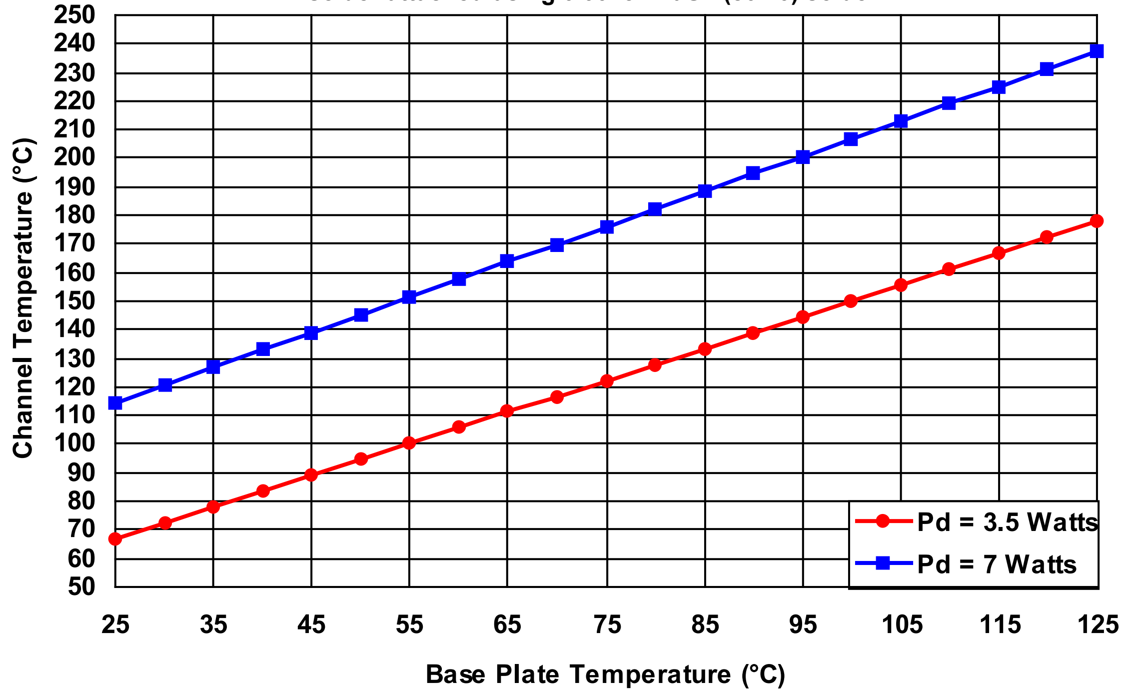
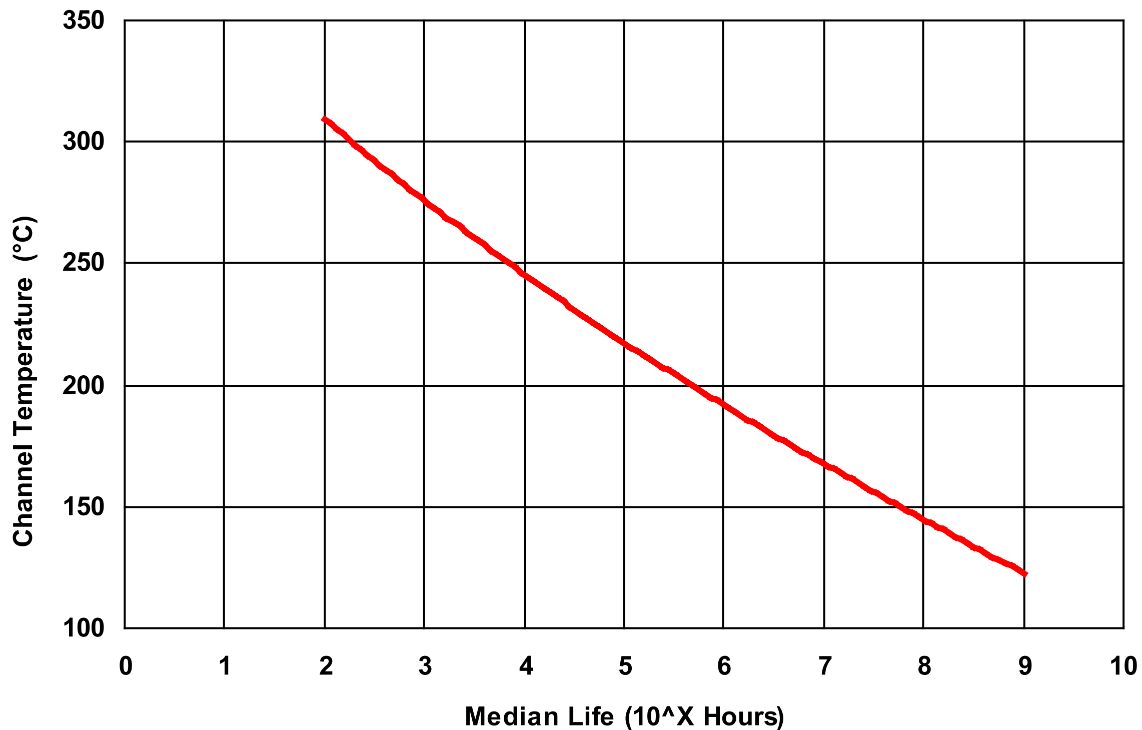
Thermal Model of TGF4112-EPU



$T_{ch} = 1.67 + 9.72 \times Pd + 0.288 \times Pd^2 + (1.00 + 0.0289 \times Pd + 0.000544 \times Pd^2) \times T_{base}$
(Predicted Channel Temperature equation for the given assembly stack up)
This model assumes a perfect solder connection (no voids) between the FET and the carrier plate.



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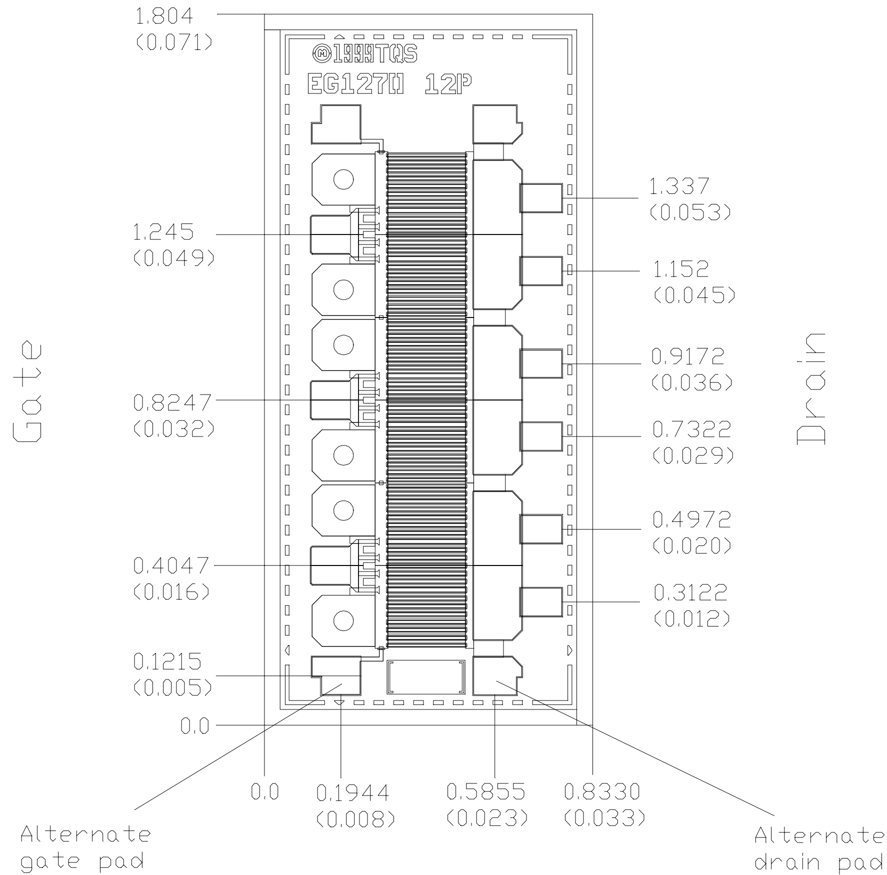
Mechanical Drawing of TGF4112-EPU



Units: millimeters (inches)
Thickness: 0.1016 (0.004) (reference only)
Chip edge to bond pad dimensions are shown to center of bond pad
Chip size tolerance: +/- 0.051 (0.002)

Gate pad size are 0.100 x 0.100 (0.004 x 0.004)
Drain pad size are 0.120 x 0.370 (0.005 x 0.015)
A minimum of three gate bonds and six drain bonds is recommended for operation. Sources are connected to backside metalization. Alternate gate and drain pads are located on either end of the FET for paralleling TGF4112-EPUs.

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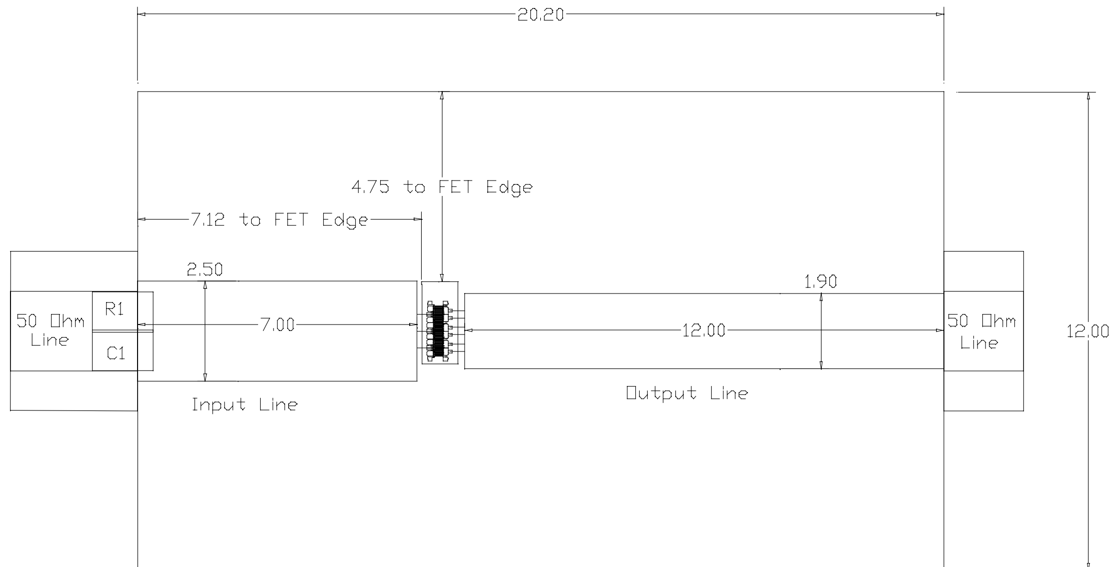
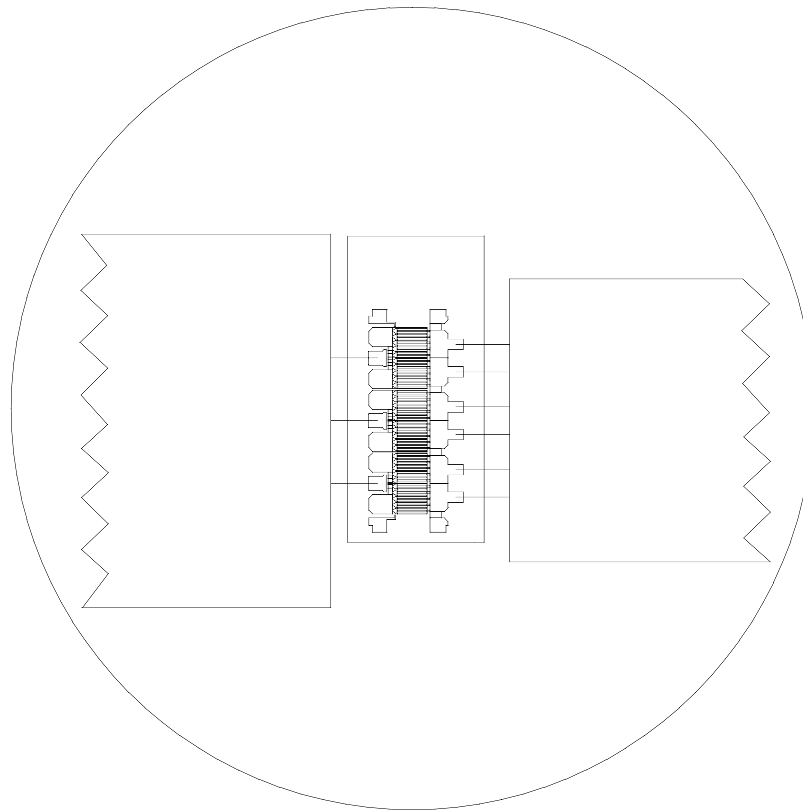
Application circuit for the TGF4112-EPU at 2.3 GHz





The FET is soldered using AuSn solder at 300°C for 30 secs. Input matching network is 0.381 mm ZrSn Tioxide substrates (Er = 38). Output matching network is 0.381mm Alumina (Er = 9.6). The design load impedance is between 6 Ω and 7 Ω with the 4 pF output capacitance of the FET included in the output network. For further explanation refer to the application note “Designing High Efficiency Amplifiers using HFETs”. The carrier plate is 0.51 mm gold plated copper molybdenum. Gold wire 0.018 mm diameter is used for the bonds. Three gate bonds are required with a length of 0.42 mm. Six drain bonds are required with a length of 0.45 mm. Bondwire end points on the FET are in the middle of the bond pad. Refer to the figures above for bondwire locations. Connection between the 50 ohm line input to the input match is made through a parallel RC network. R1 in this network is 10 ohms, and C1 is 5.6 pF. R1 and C1 are surface mount 0603 piece parts.

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