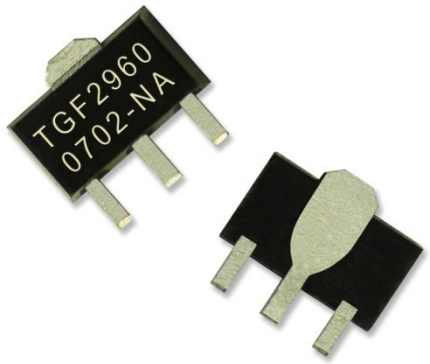
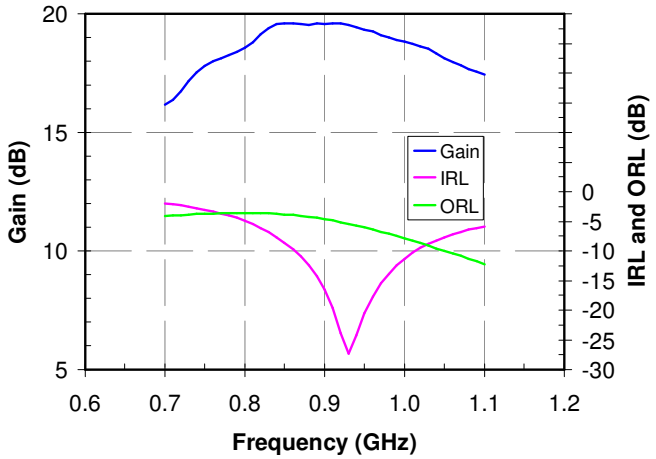
TGF2960-SD

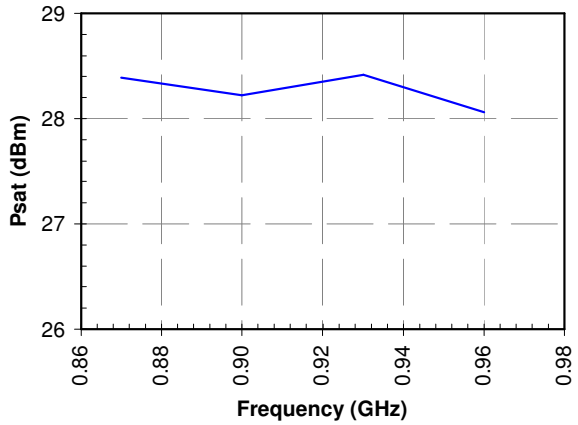
0.5 Watt DC-5 GHz Packaged HFET



900 MHz Application Board Performance

Bias conditions: Vd = 8 V, Idq = 100 mA, Vg = -1.0 V Typical





Key Features

- Frequency Range: DC-5 GHz

Nominal 900 MHz Application Board Performance:

- TOI: 40 dBm
- 28 dBm Psat, 27 dBm P1dB
- Gain: 19 dB
- Input Return Loss: -10 dB
- Output Return Loss: -5 dB
- Bias: Vd = 8 V, Idq = 100 mA, Vg = -1.0 V (Typical)
- Package Dimensions: 4.5 x 4 x 1.5 mm

Primary Applications

- Cellular Base Stations
- WiMAX
- Wireless Infrastructure
- IF & LO Buffer Applications
- RFID

Product Description

The TGF2960-SD is a high performance 1/2-watt Heterojunction GaAs Field Effect Transistor (HFET) housed in a low cost SOT89 surface mount package.

The device's ideal operating point is at a drain bias of 8 V and 100 mA. At this bias at 900 MHz when matched into 50 ohms using external components, this device is capable of 19 dB of gain, 28 dBm of saturated output power, and 40 dBm of output IP3.

Evaluation boards at 900 MHz, 1900 MHz and 2100 MHz available on request.

RoHS and Lead-Free compliant.

Datasheet subject to change without notice.

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Table I
Absolute Maximum Ratings 1/

Symbol	Parameter	Value	Notes
Vd-Vg	Drain to Gate Voltage	17 V	
Vd	Drain Voltage	9 V	2/
Vg	Gate Voltage Range	-5 to 0 V	
Id	Drain Current	390 mA	2/
Ig	Gate Current Range	-2.4 to 17.8 mA	
Pin	Input Continuous Wave Power	26 dBm	2/

1/ These ratings represent the maximum operable values for this device. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device and / or affect device lifetime. These are stress ratings only, and functional operation of the device at these conditions is not implied.

2/ Combinations of supply voltage, supply current, input power, and output power shall not exceed the maximum power dissipation listed in Table IV.

Table II
Recommended Operating Conditions

Symbol	Parameter 1/	Typical Value
Vd	Drain Voltage	8 V
Idq	Drain Current	100 mA
Id	Drain Current at Psat	130 mA
Vg	Gate Voltage	-1.0 V

1/ See assembly diagram for bias instructions.

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Table III
Electrical Performance

Test conditions unless otherwise specified: f_{in} = 900 MHz, 25°C; Vd = 8V, Idq = 100 mA, Vg = -1.0 Typical; See test circuit for 900 MHz operation

SYMBOL	PARAMETER	Min	Nom	UNIT
Gain	Small Signal Gain	18	19	dB
P1dB	Output Power @ 1dB Compression	25.5	27	dBm
OTOI	3rd Order Output Intercept Point 1/	37	40	dBm

1/ 900 and 910 MHz, 16 dBm output power per tone

Table IIIa
RF Characterization Table

Bias: Vd = 8 V, Idq = 100 mA, Vg = -1.0 V, typical

SYMBOL	PARAMETER	TEST CONDITIONS	NOMINAL	UNITS	NOTES
Gain	Small Signal Gain	900 MHz 1900 MHz 2100 MHz	19 16 15	dB	1/ 2/ 3/
IRL	Input Return Loss	900 MHz 1900 MHz 2100 MHz	-10 -10 -10	dB	1/ 2/ 3/
ORL	Output Return Loss	900 MHz 1900 MHz 2100 MHz	-5 -6 -6	dB	1/ 2/ 3/
Psat	Saturated Output Power	900 MHz 1900 MHz 2100 MHz	28 28 28	dBm	1/ 2/ 3/
P1dB	Output Power @ 1dB Compression	900 MHz 1900 MHz 2100 MHz	27 27 27	dBm	1/ 2/ 3/
TOI	Output TOI	900 MHz 1900 MHz 2100 MHz	40 39 39	dBm	1/ 4/ 5/
NF	Noise Figure	900 MHz 1900 MHz 2100 MHz	3.7 4.3 4.3	dB	1/ 2/ 3/

1/ Using 900 MHz Application Board

2/ Using 1900 MHz Application Board tuned for maximum output power

3/ Using 2100 MHz Application Board tuned for maximum output power

4/ Using 1900 MHz Application Board tuned for maximum TOI (reduces output power reduced by 1 dB)

5/ Using 2100 MHz Application Board tuned for maximum TOI (reduces output power reduced by 1 dB)

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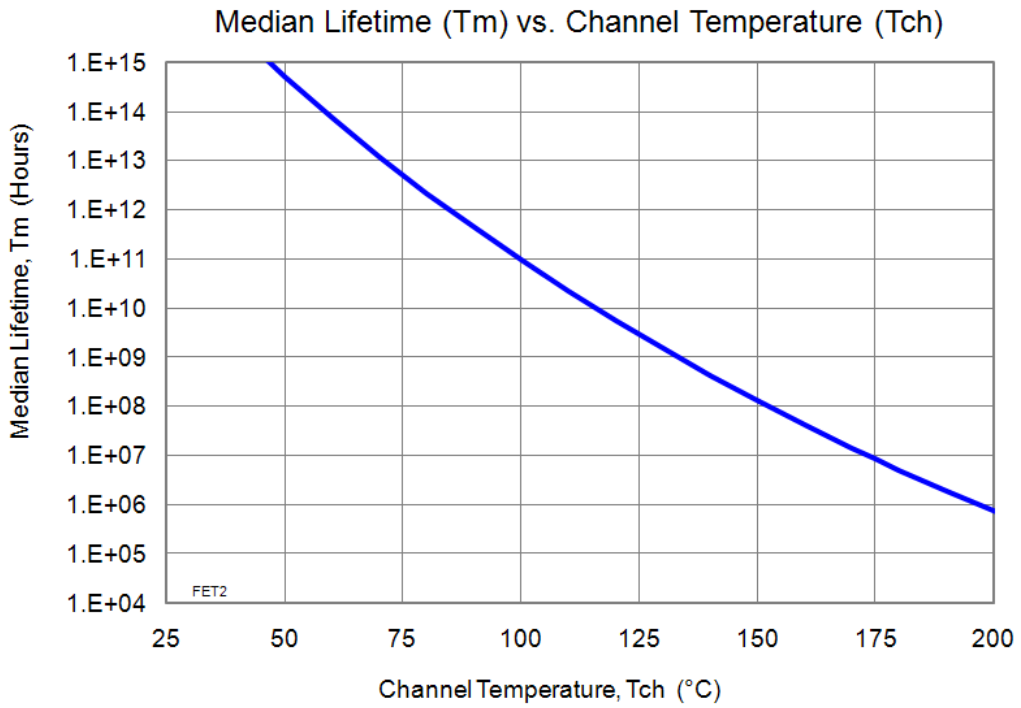
Table IV
Power Dissipation and Thermal Properties

Parameter	Test Conditions	Value
Maximum Power Dissipation	Tbaseplate = 70°C	Pd = 1.37 W Tchannel = 175°C Tm = 8.77E+06 Hrs
Thermal Resistance, θjc	Vd = 8 V Id = 100 mA Pd = 0.8 W Tbaseplate = 85°C	θjc = 77 (°C/W) Tchannel = 146.5°C Tm = 2.06E+08 Hrs
Thermal Resistance, θjc at Psat	Vd = 8 V Id =130 mA Pout = 27 dBm Pd = 0.54 W Tbaseplate = 85°C	θjc = 77 (°C/W) Tchannel = 126°C Tm = 2.48E+09 Hrs
Mounting Temperature	See 'Typical Solder Reflow Profiles' Table	
Storage Temperature		-65 to 150°C



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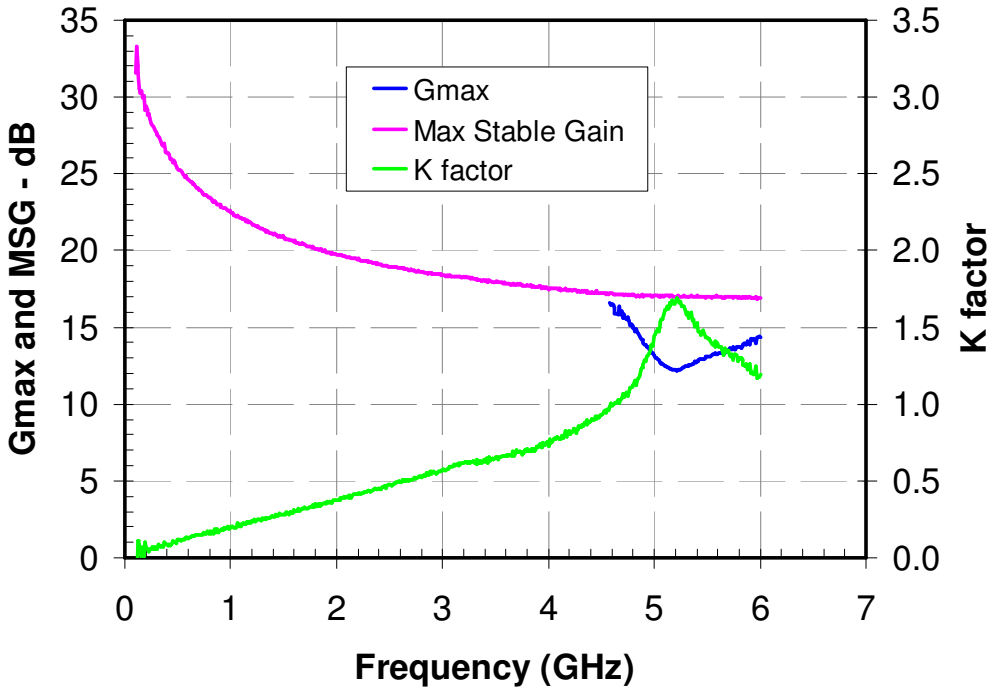
Gmax, Max Stable Gain, K factor

Bias conditions: Vd = 8 V, Idq = 100 mA, Vg = -1.0 V Typical



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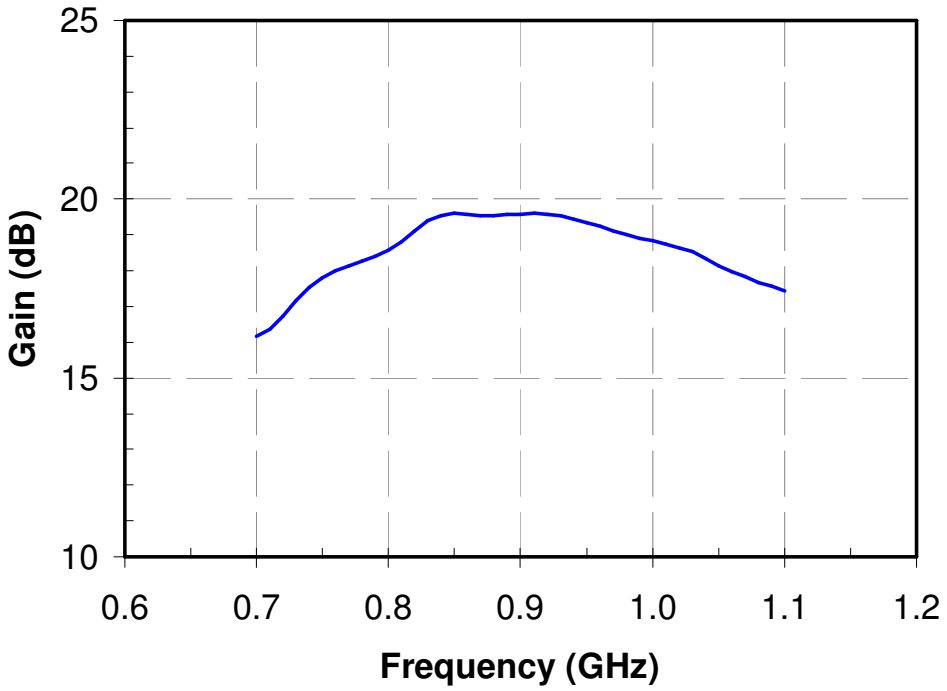
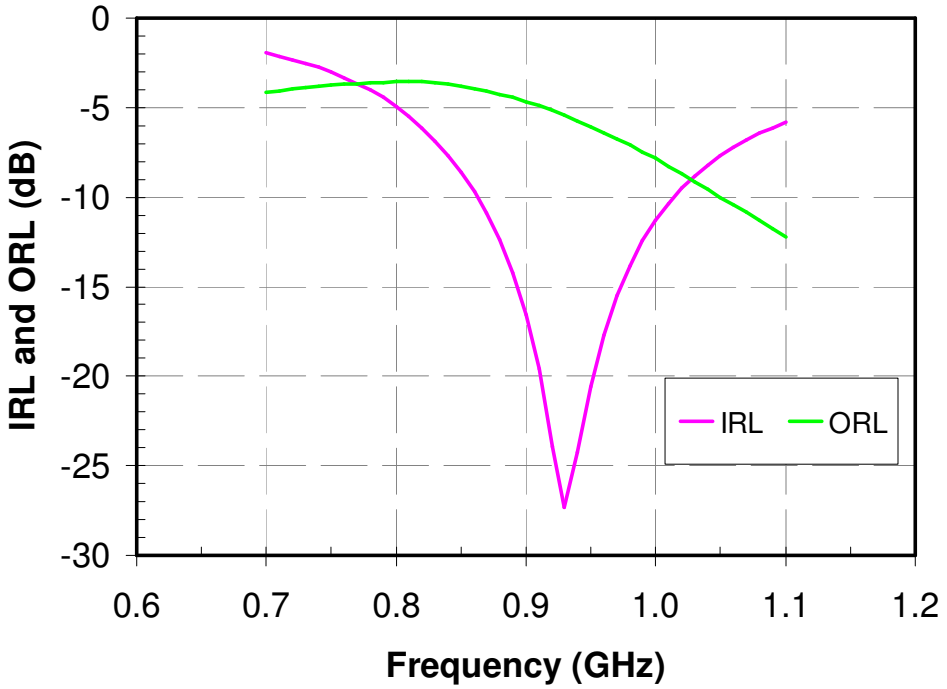
Measured Data 900 MHz Application Board

Bias conditions: Vd = 8 V, Idq = 100 mA, Vg = -1.0 V Typical





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Measured Data 900 MHz Application Board

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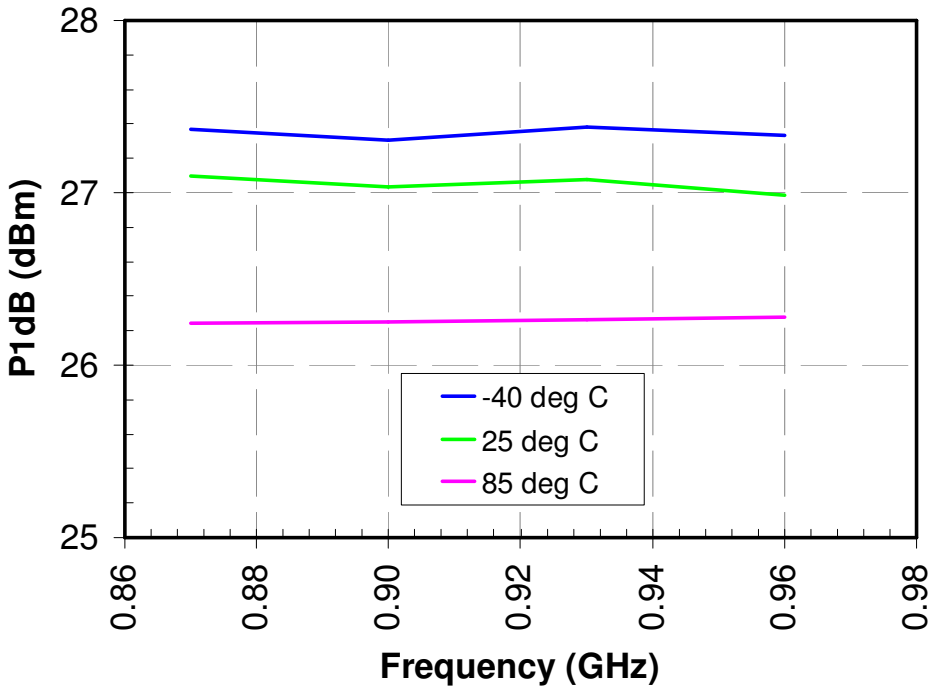

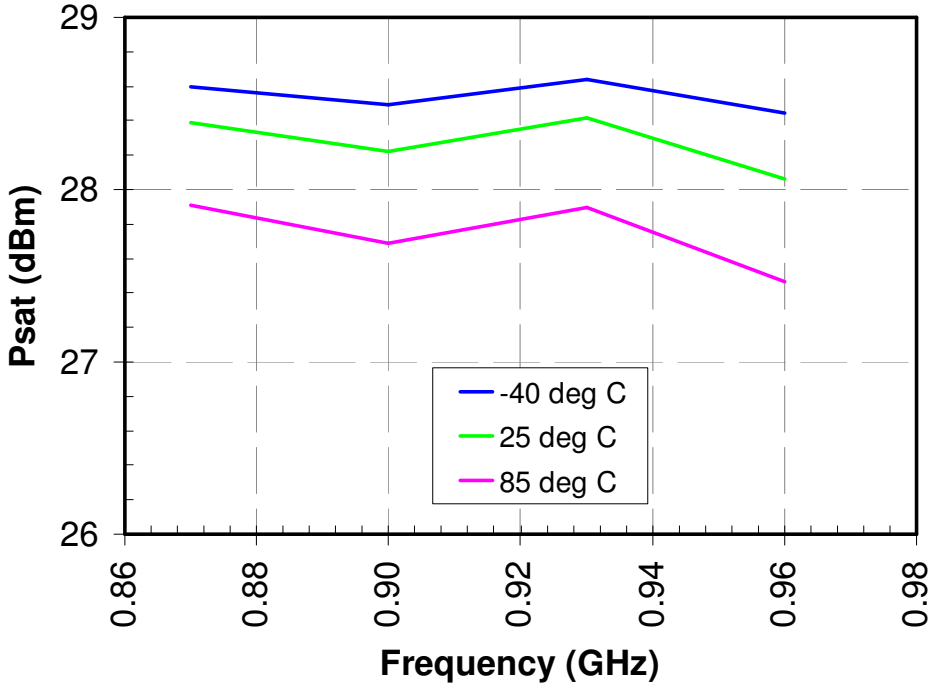

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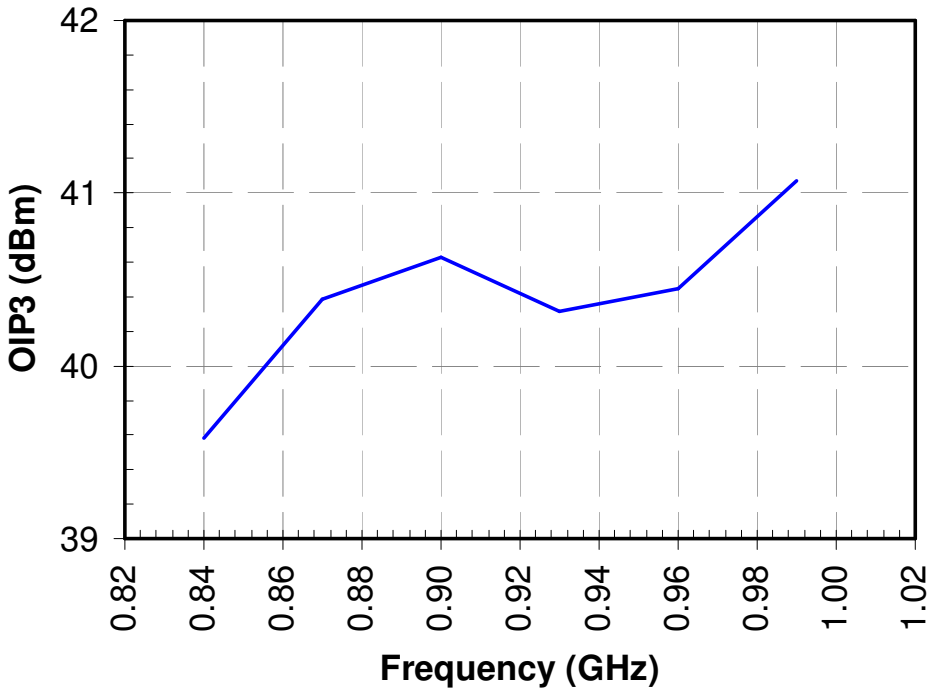

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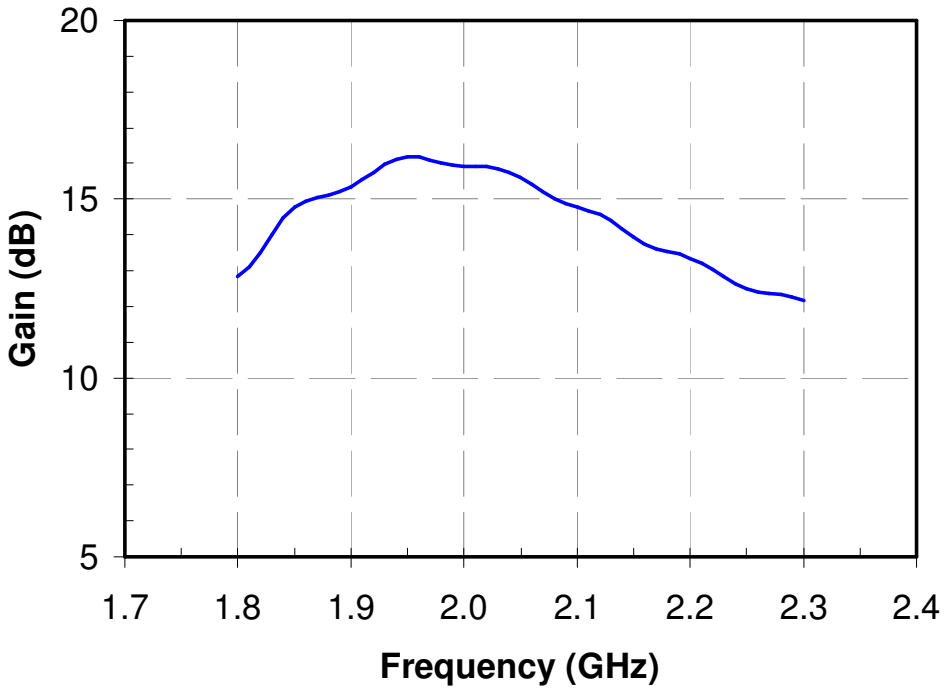
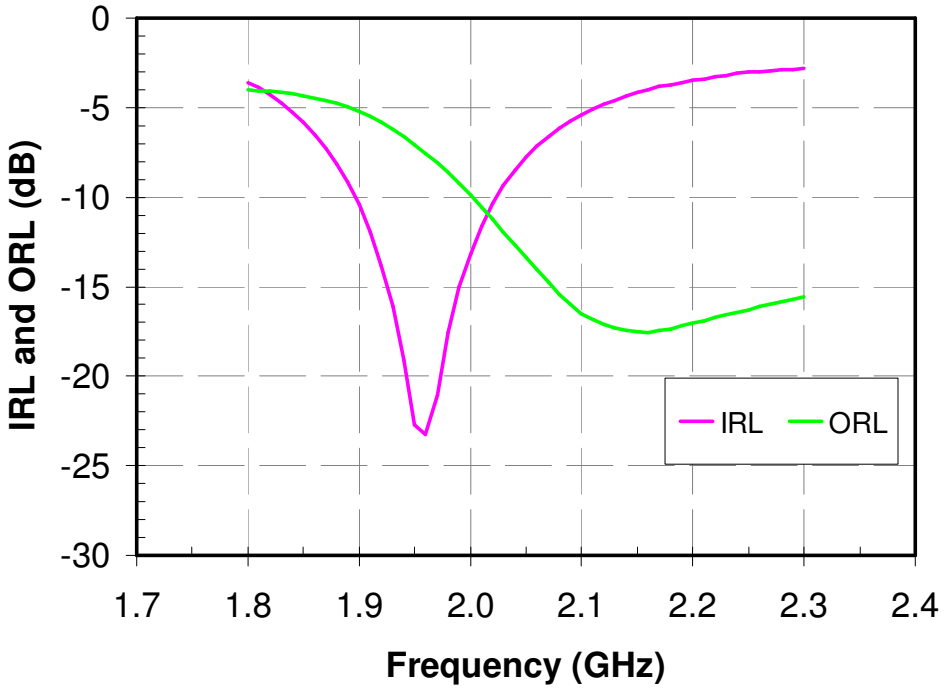
Measured Data 1900 MHz Application Board

Bias conditions: Vd = 8 V, Idq = 100 mA, Vg = -1.0 V Typical





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Measured Data 1900 MHz Application Board

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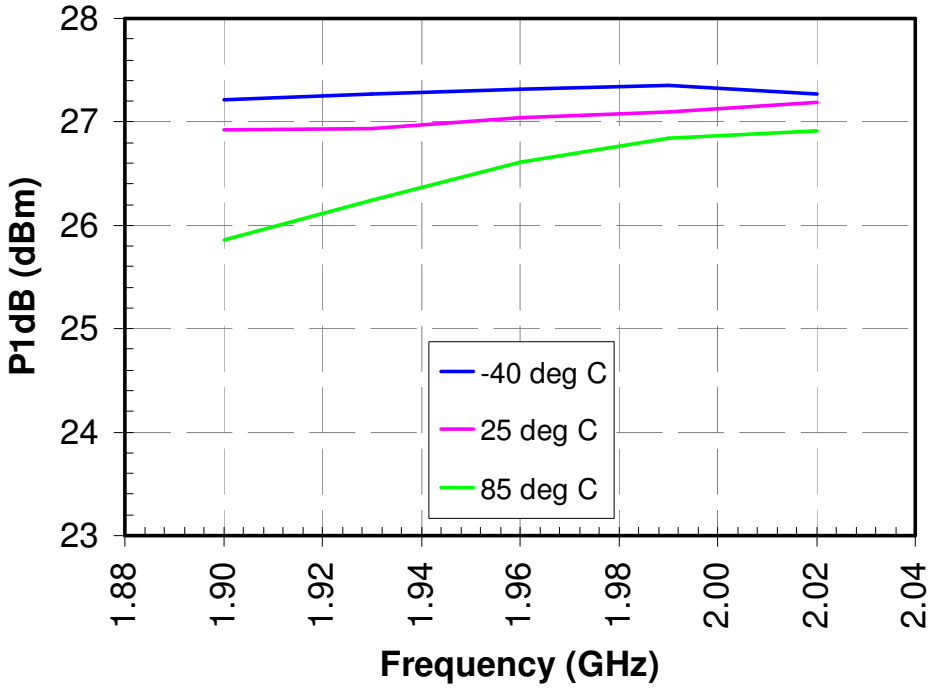

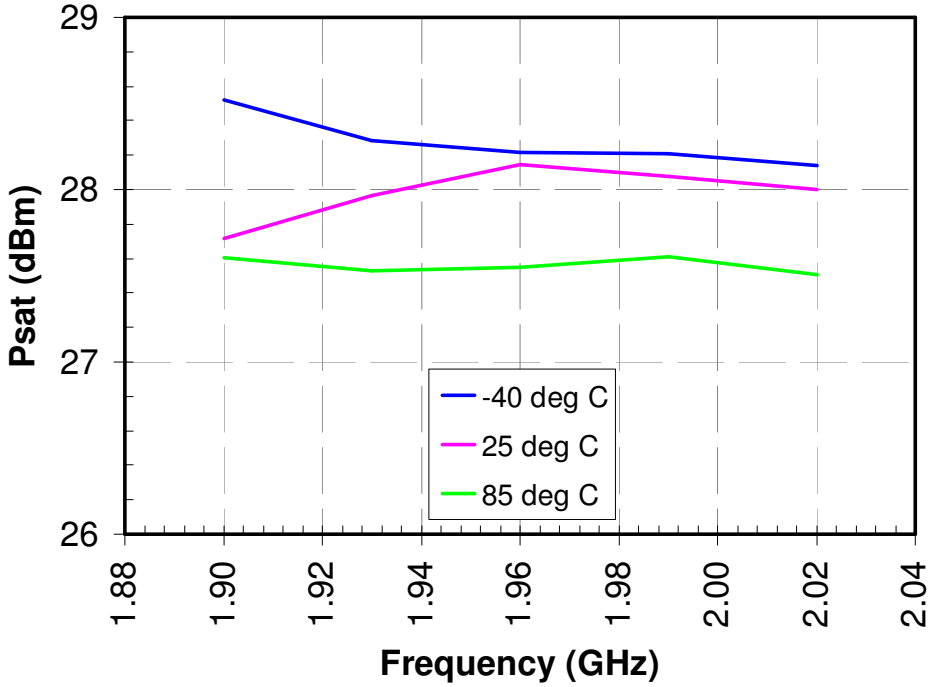

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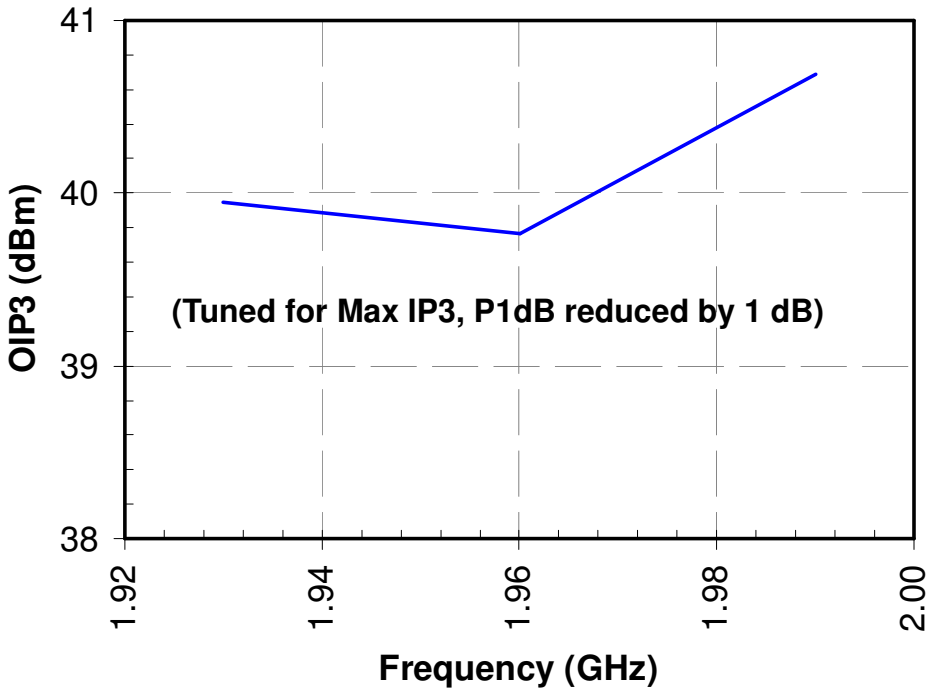
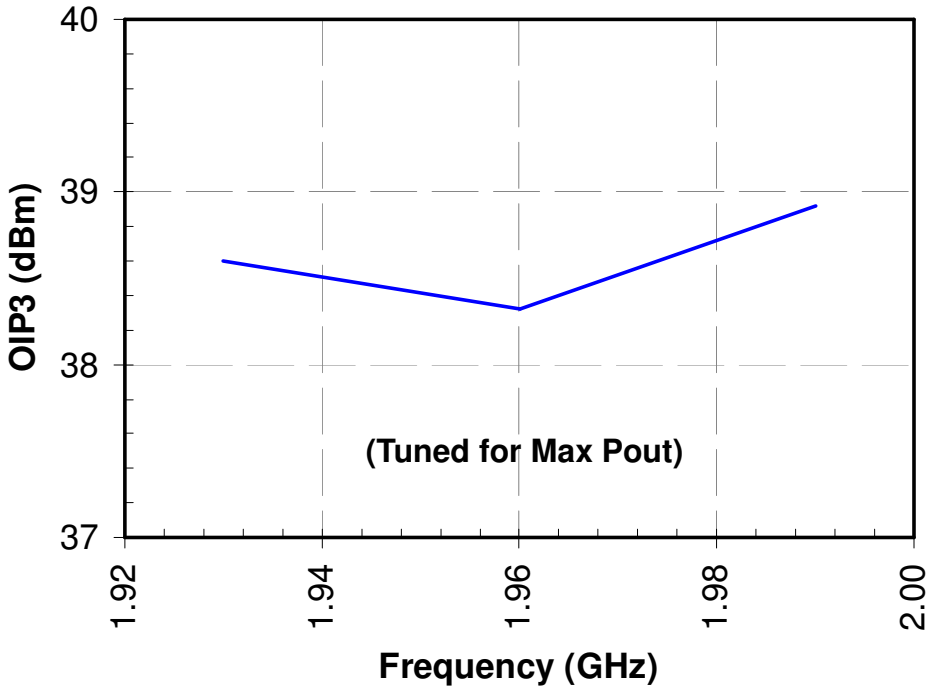
Measured Data 1900 MHz Application Board

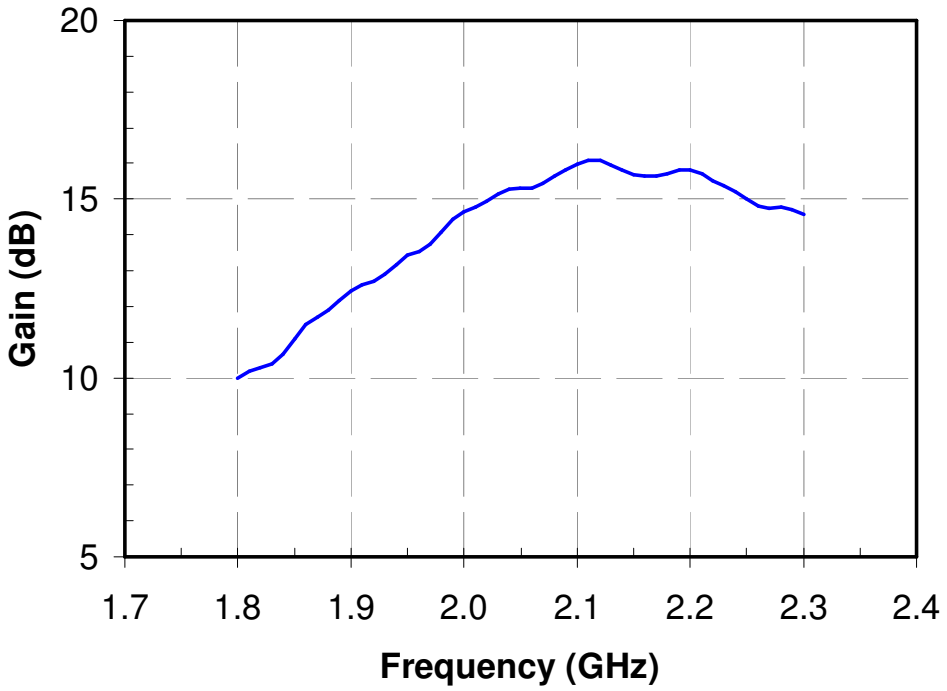
Bias conditions: Vd = 8 V, Idq = 100 mA, Vg = -1.0 V Typical

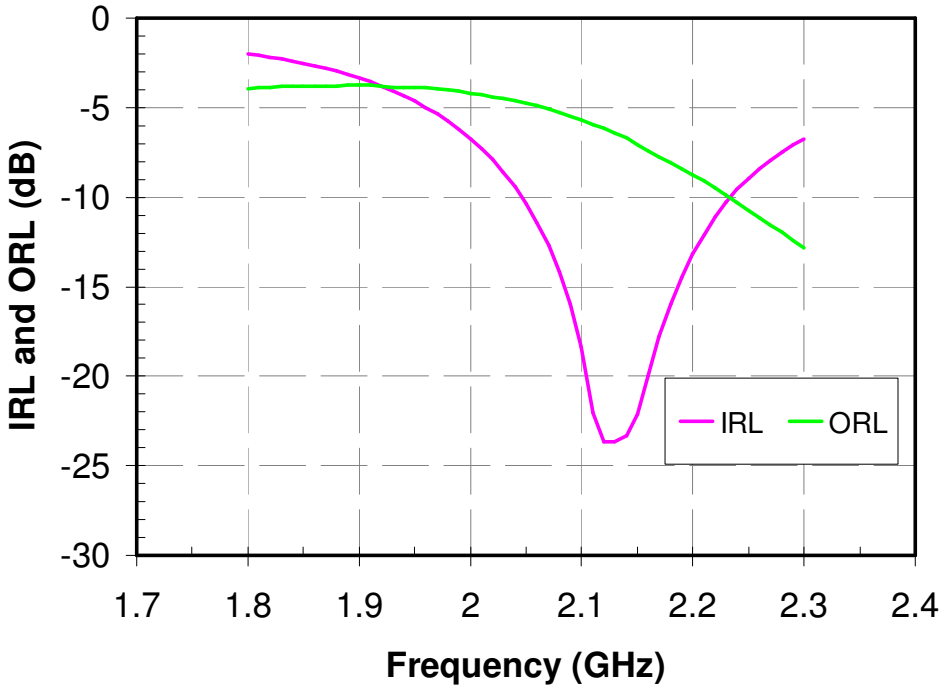




Measured Data 2100 MHz Application Board

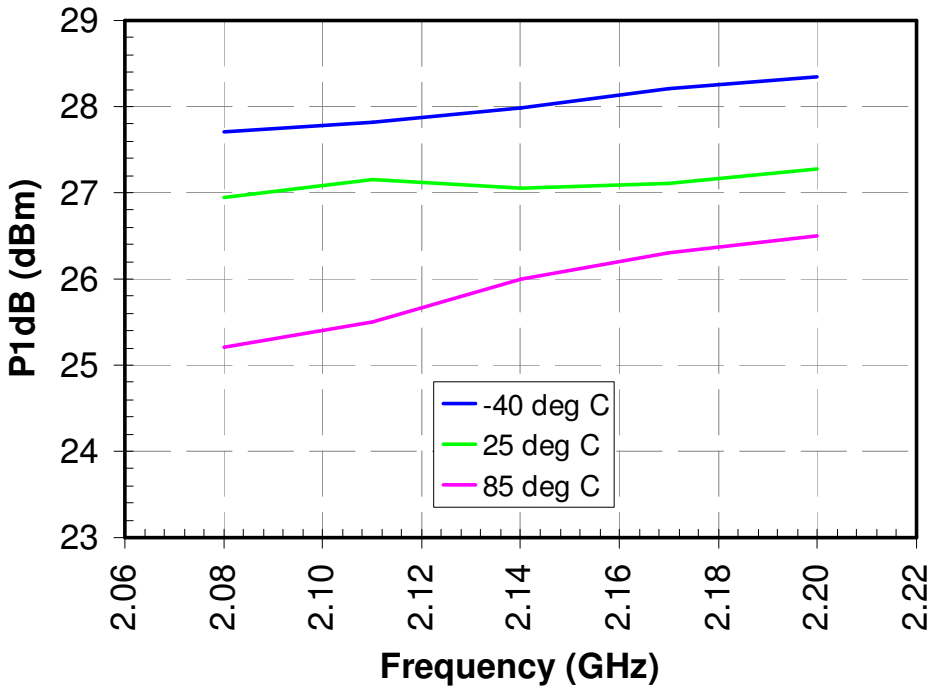
Bias conditions: Vd = 8 V, Idq = 100 mA, Vg = -1.0 V Typical

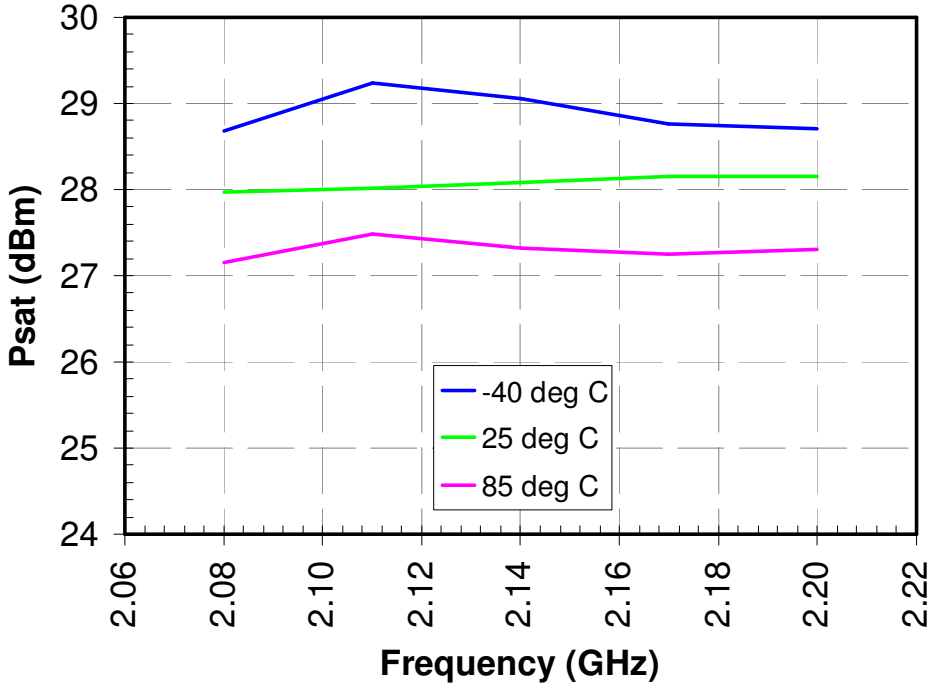




Measured Data 2100 MHz Application Board

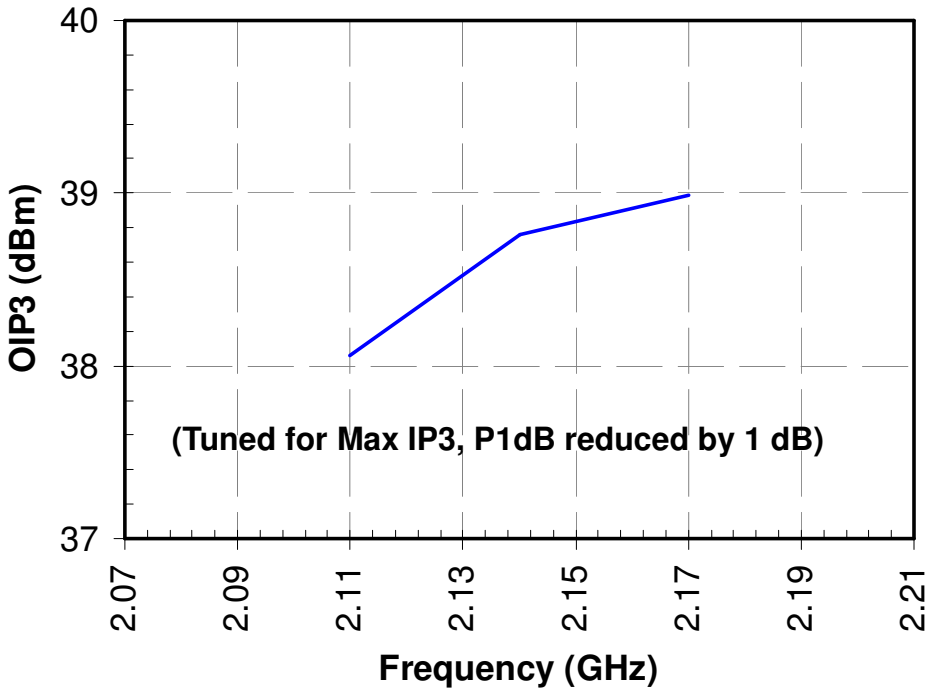
Bias conditions: Vd = 8 V, Idq = 100 mA, Vg = -1.0 V Typical

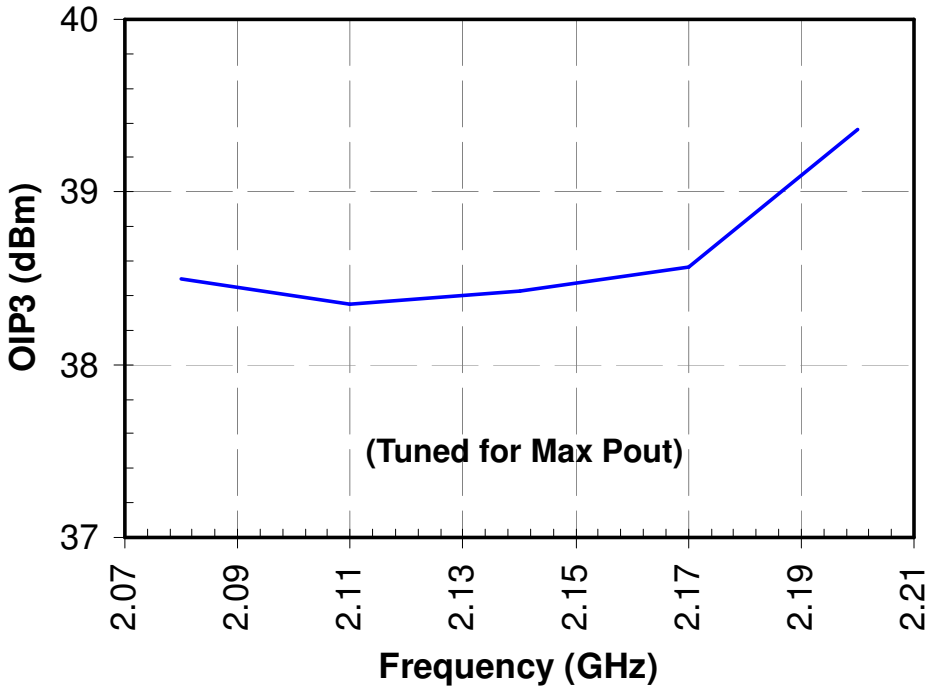




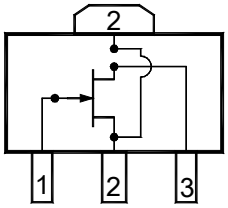
Measured Data 2100 MHz Application Board

Bias conditions: Vd = 8 V, Idq = 100 mA, Vg = -1.0 V Typical





Electrical Schematic



Pin	Signal
1	RF In (Gate)
2	Gnd (Source)
3	RF Out (Drain)

Bias Procedures

Bias-up Procedure

- Vg set to -2.5 V
- Vd set to +8 V
- Adjust Vg more positive until Idq is 100 mA. This will be ~ Vg = -1.0 V
- Apply RF signal to input

Bias-down Procedure

- Turn off RF signal at input
- Reduce Vg to -2.5V. Ensure Id ~ 0 mA
- Turn Vd to 0 V
- Turn Vg to 0 V

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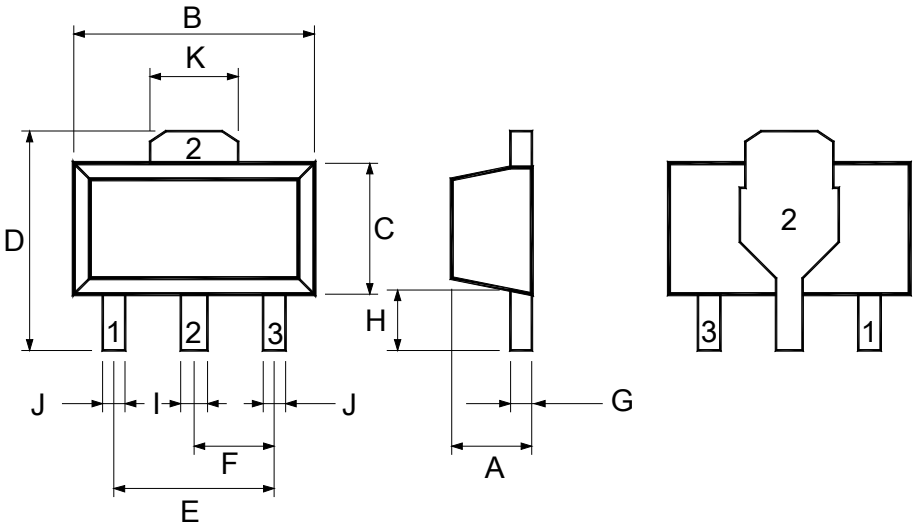
Mechanical Drawing



Dim	Millimeters	
	Min	Max
A	1.40	1.60
B	4.40	4.60
C	2.29	2.60
D	3.94	4.25
E	3.00 Center-Center	
F	1.50 Center-Center	
G	0.35	0.44
H	0.89	1.20
I	0.44	0.56
J	0.36	0.48
K	1.50	1.83

GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.

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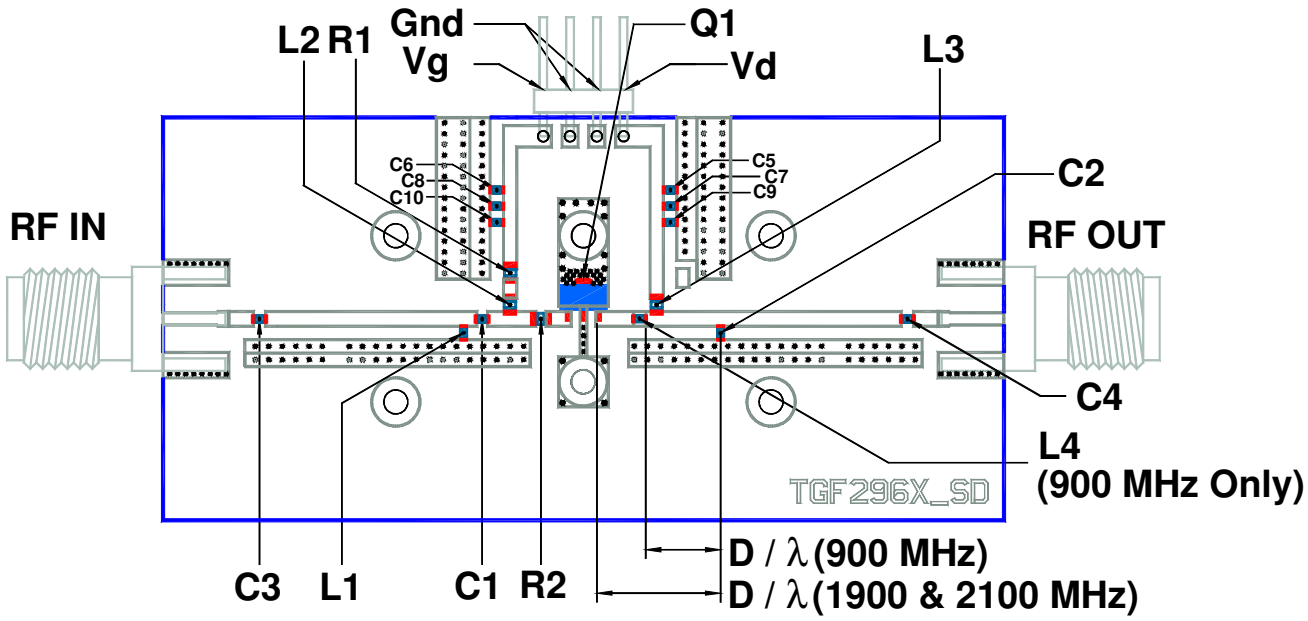
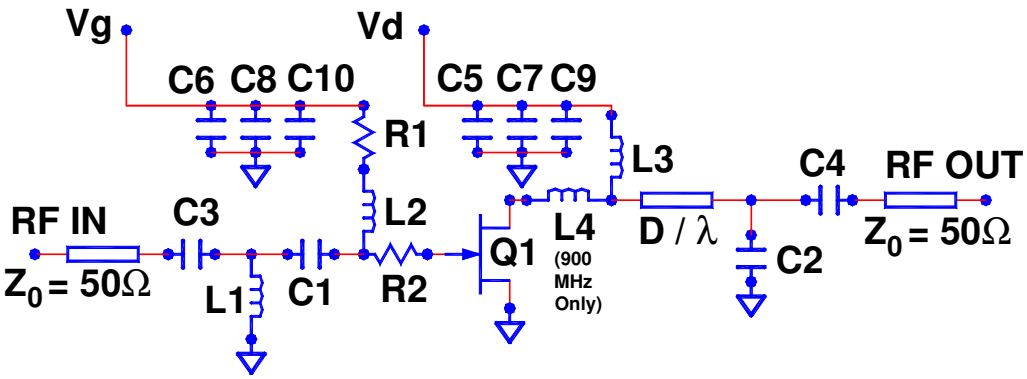
Evaluation Board



Evaluation Board Schematic



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Evaluation Board Bill of Materials

Ref Des	Value for Freq (MHz)			Description
	900	1900	2100	
L1	4.7 nH	1.2 nH	1.5 nH	0603 ACCU-L AVX Inductor
C1	22 pF	1.2 pF	1.2 pF	0603 ACCU-P AVX Capacitor
C2	0.7 pF	0.6 pF	0.6 pF	0603 ACCU-P AVX Capacitor
D	18.8 mm	14.2 mm	5.8 mm	Physical Location for C2
D	18.8 mm	14.2 mm	5.8 mm	Physical Location for C2 for maximum power
λ	36°@0.9 GHz	58°@1.9 GHz	26°@2.1 GHz	50 Ohm Transmission Line Length D for maximum power
D	18.8 mm	17.2 mm	9.6 mm	Physical Location for C2 for maximum TOI
λ	36°@0.9 GHz	70°@1.9 GHz	39°@2.1 GHz	50 Ohm Transmission Line Length D for maximum TOI
L2, L3	50 nH			0805 Inductor
L4	1.2 nH	--	--	0603 ACCU-L AVX Inductor
C3,C4	150 pF			0603 Capacitor
C5, C6	0.1 µF			0603 Capacitor
C7, C8	0.01 µF			0603 Capacitor
C9, C10	1000 pF			0603 Capacitor
R1	50 Ohms			0805 1/8 Watt Resistor
R2	11 Ohms	3 Ohms	5.1 Ohms	0805 1/8 Watt Resistor
Q1	--			TriQuint TGF2960-SD Packaged FET
(PCB)	--			28 mil thick GETEK

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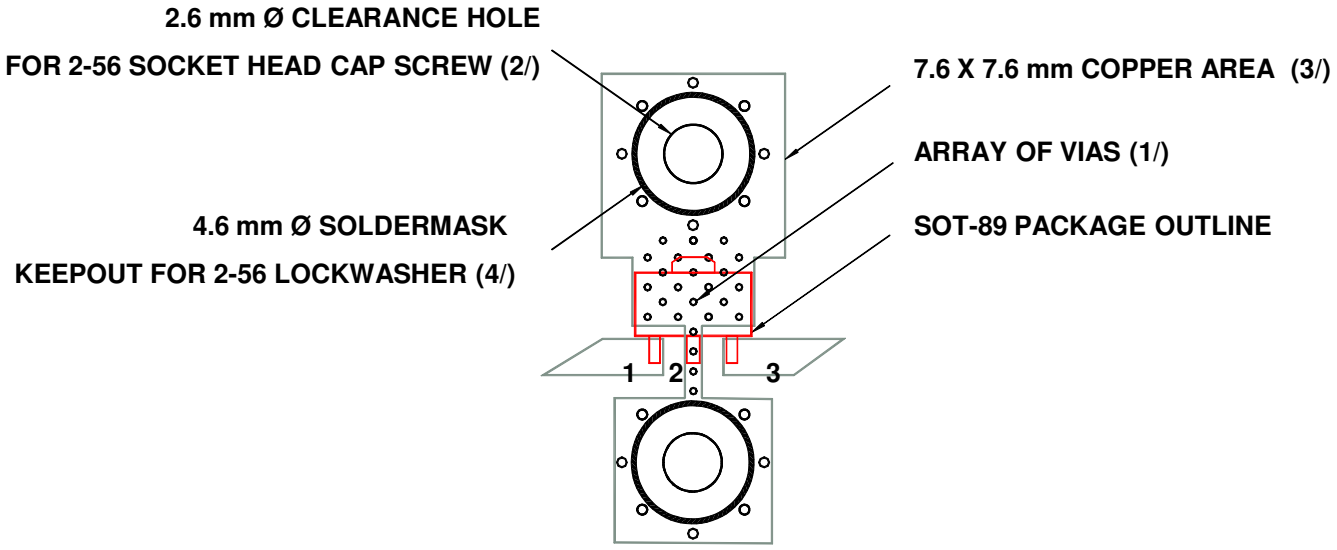
Recommended Assembly Diagram



Assembly Notes

1/ The lowest possible thermal and electrical resistance for Pin 2 is critical for optimal performance. The array of vias under Pin 2 should be as small and as dense as the PC board fabrication permits. 0.30 mm diameter vias on 0.60 mm center to center spacing is recommended.

2/ Mounting screws in the vicinity of the package improve heat transfer to the chassis or to a heat spreader located on the backside of the PC board. Shown are clearance holes and solder mask keepout zone for a 2-56 socket head cap screw. Use of a split lockwasher and proper torque on the screw will prevent compression damage to the PC board.

3/ Use of 1 oz copper (min) in the PC board construction is recommended.

4/ For lowest thermal resistance, solder mask must be removed where the copper traces on the PC board contact the heat spreader. In this example, this would be a) front and backsides of the PC board around the 2-56 screw and b) front of the PC board around package pin 2.

GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.

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Recommended Surface Mount Package Assembly

Proper ESD precautions must be followed while handling packages.

Clean the board with acetone. Rinse with alcohol. Allow the circuit to fully dry.

TriQuint recommends using a conductive solder paste for attachment. Follow solder paste and reflow oven vendors' recommendations when developing a solder reflow profile. Typical solder reflow profiles are listed in the table below.

Hand soldering is not recommended. Solder paste can be applied using a stencil printer or dot placement. The volume of solder paste depends on PCB and component layout and should be well controlled to ensure consistent mechanical and electrical performance.

Clean the assembly with alcohol.

Typical Solder Reflow Profiles

Reflow Profile	SnPb	Pb Free
Ramp-up Rate	3 °C/sec	3 °C/sec
Activation Time and Temperature	60 – 120 sec @ 140 – 160 °C	60 – 180 sec @ 150 – 200 °C
Time above Melting Point	60 – 150 sec	60 – 150 sec
Max Peak Temperature	240 °C	260 °C
Time within 5 °C of Peak Temperature	10 – 20 sec	10 – 20 sec
Ramp-down Rate	4 – 6 °C/sec	4 – 6 °C/sec

Ordering Information

Part	Package Style
TGF2960-SD, TAPE AND REEL	SOT-89, TAPE AND REEL

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