Freescale Semiconductor
Technical Data

Document Number: MRF8S9102N
Rev. 0, 2/2011

RoHS

RF Power Field Effect Transistor

N-Channel Enhancement-Mode Lateral MOSFET

Designed for CDMA base station applications with frequencies from 865 to 960 MHz. Can be used in Class AB and Class C for all typical cellular base station modulation formats.

- Typical Single-Carrier W-CDMA Performance: V_{DD} = 28 Volts, I_{DQ} = 750 mA, P_{out} = 28 Watts Avg., IQ Magnitude Clipping, Channel Bandwidth = 3.84 MHz, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF.

Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)
920 MHz	23.1	36.4	6.3	-35.5
940 MHz	23.1	36.4	6.2	-36.1
960 MHz	22.8	36.6	6.1	-35.8

- Capable of Handling 10:1 VSWR, @ 32 Vdc, 940 MHz, 144 Watts CW Output Power (3 dB Input Overdrive from Rated P_{out}), Designed for Enhanced Ruggedness
- Typical P_{out} @ 1 dB Compression Point ≃ 100 Watts CW

880 MHz

- Typical Single-Carrier W-CDMA Performance: V_{DD} = 28 Volts, I_{DQ} = 750 mA, P_{out} = 28 Watts Avg., IQ Magnitude Clipping, Channel Bandwidth = 3.84 MHz, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF.

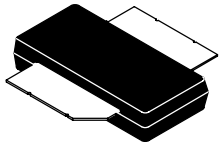
Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)
865 MHz	22.9	35.4	6.4	-34.7
880 MHz	23.0	35.5	6.2	-35.1
895 MHz	22.8	35.6	6.0	-35.7

Features

- 100% PAR Tested for Guaranteed Output Power Capability
- Characterized with Series Equivalent Large-Signal Impedance Parameters and Common Source S-Parameters
- Internally Matched for Ease of Use
- Integrated ESD Protection
- Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- Designed for Digital Predistortion Error Correction Systems
- Optimized for Doherty Applications
- 225°C Capable Plastic Package
- RoHS Compliant
- In Tape and Reel. R3 Suffix = 250 Units, 32 mm Tape Width, 13 inch Reel.

MRF8S9102NR3

**865-960 MHz, 28 W AVG., 28 V
SINGLE W-CDMA
LATERAL N-CHANNEL
RF POWER MOSFET**



**CASE 2021-03, STYLE 1
OM-780-2
PLASTIC**

freescale semiconductor

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +70	Vdc
Gate-Source Voltage	V_{GS}	-6.0, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_C	150	°C
Operating Junction Temperature (1,2)	T_J	225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 81°C, 28 W CW, 28 Vdc, I_{DQ} = 750 mA, 880 MHz Case Temperature 80°C, 100 W CW, 28 Vdc, I_{DQ} = 750 mA, 880 MHz	$R_{\theta JC}$	 0.63 0.58	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	2 (Minimum)
Machine Model (per EIA/JESD22-A115)	A (Minimum)
Charge Device Model (per JESD22-C101)	IV (Minimum)

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 70 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
On Characteristics					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 400 μAdc)	$V_{GS(th)}$	1.5	2.3	3.0	Vdc
Gate Quiescent Voltage (V_{DS} = 28 Vdc, I_D = 750 mAdc)	$V_{GS(Q)}$	—	3.1	—	Vdc
Fixture Gate Quiescent Voltage (4) (V_{DD} = 28 Vdc, I_D = 750 mAdc, Measured in Functional Test)	$V_{GG(Q)}$	4.6	6.2	7.6	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 1.7 Adc)	$V_{DS(on)}$	0.1	0.2	0.3	Vdc

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1955.
4. V_{GG} = 2 x $V_{GS(Q)}$. Parameter measured on Freescale Test Fixture, due to resistive divider network on the board. Refer to Test Circuit schematic.

(continued)

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests (1) (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 750 mA, P_{out} = 28 W Avg., f = 920 MHz, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.					
Power Gain	G_{ps}	21.5	23.1	24.0	dB
Drain Efficiency	η_D	34.0	36.4	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	6.0	6.3	—	dB
Adjacent Channel Power Ratio	ACPR	—	-35.5	-32.5	dBc
Input Return Loss	IRL	—	-14	-9	dB

Typical Broadband Performance (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 750 mA, P_{out} = 28 W Avg., Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.

Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)	IRL (dB)
920 MHz	23.1	36.4	6.3	-35.5	-14
940 MHz	23.1	36.4	6.2	-36.1	-22
960 MHz	22.8	36.6	6.1	-35.8	-17

Typical Performances (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 750 mA, 920-960 MHz Bandwidth

P_{out} @ 1 dB Compression Point, CW	P1dB	—	100	—	W
IMD Symmetry @ 82 W PEP, P_{out} where IMD Third Order Intermodulation ≅ 30 dBc (Delta IMD Third Order Intermodulation between Upper and Lower Sidebands > 2 dB)	IMD_{sym}	—	20	—	MHz
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	80	—	MHz
Gain Flatness in 40 MHz Bandwidth @ P_{out} = 28 W Avg.	G_F	—	0.3	—	dB
Gain Variation over Temperature (-30°C to +85°C)	ΔG	—	0.02	—	dB/°C
Output Power Variation over Temperature (-30°C to +85°C)	ΔP1dB	—	0.004	—	dB/°C

Typical Broadband Performance — 880 MHz (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 750 mA, P_{out} = 28 W Avg., Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.

Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)	IRL (dB)
865 MHz	22.9	35.4	6.4	-34.7	-15
880 MHz	23.0	35.5	6.2	-35.1	-23
895 MHz	22.8	35.6	6.0	-35.7	-19

1. Part internally matched both on input and output.

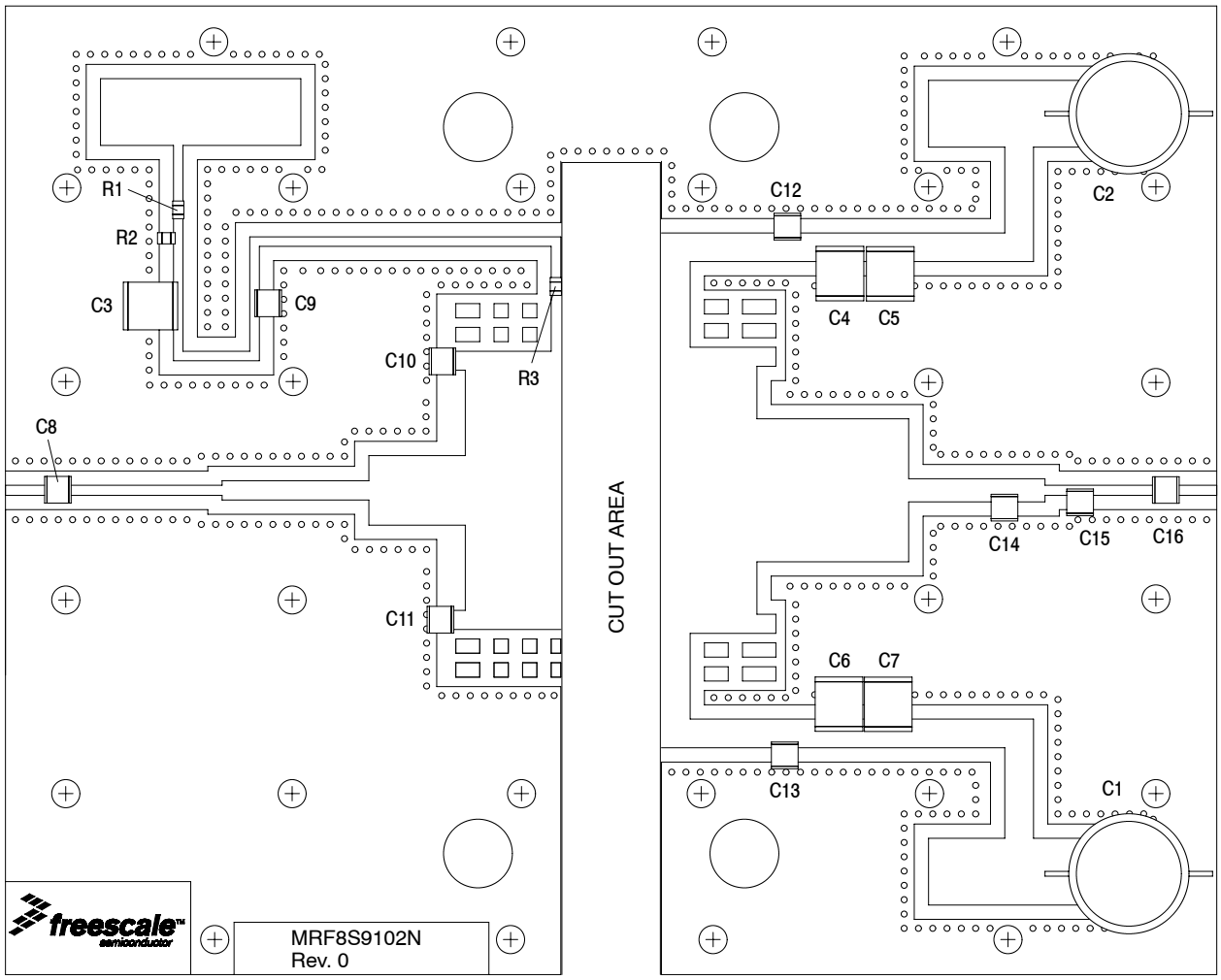


Figure 1. MRF8S9102NR3 Test Circuit Component Layout

Table 6. MRF8S9102NR3 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C2	220 μF, 63 V Electrolytic Capacitors	222212018221	Vishay
C3, C4, C5, C6, C7	10 μF, 50 V Chip Capacitors	C5750X5R1H106M	TDK
C8, C14, C15	3.0 pF Chip Capacitors	ATC100B3R0BT500XT	ATC
C9, C12, C13, C16	47 pF Chip Capacitors	ATC100B470JT500XT	ATC
C10	4.3 pF Chip Capacitor	ATC100B4R3BT500XT	ATC
C11	4.7 pF Chip Capacitor	ATC100B4R7BT500XT	ATC
R1, R2	1 KΩ, 1/8 W Chip Resistors	WCR08051KFI	Welwyn
R3	10 Ω, 1/4 W Chip Resistor	9C12063A10R0FKHFT	Yageo
PCB	0.020″, ε_r = 3.5	RO4350	Rogers

TYPICAL CHARACTERISTICS

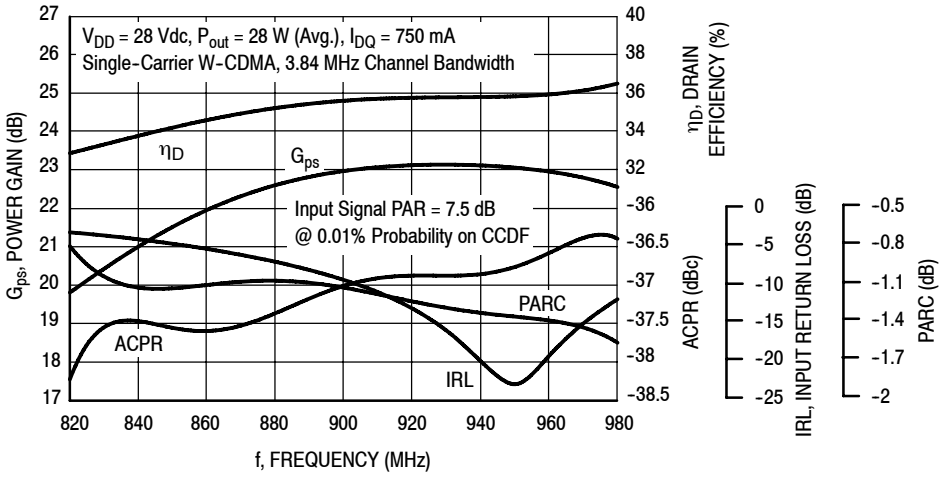


Figure 2. Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 28 Watts Avg.

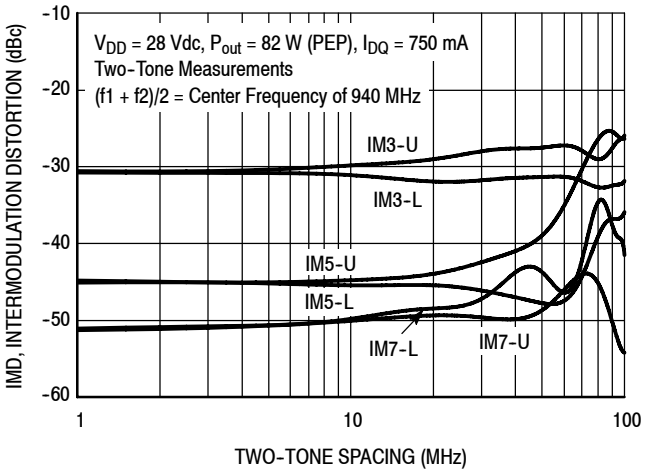


Figure 3. Intermodulation Distortion Products versus Two-Tone Spacing

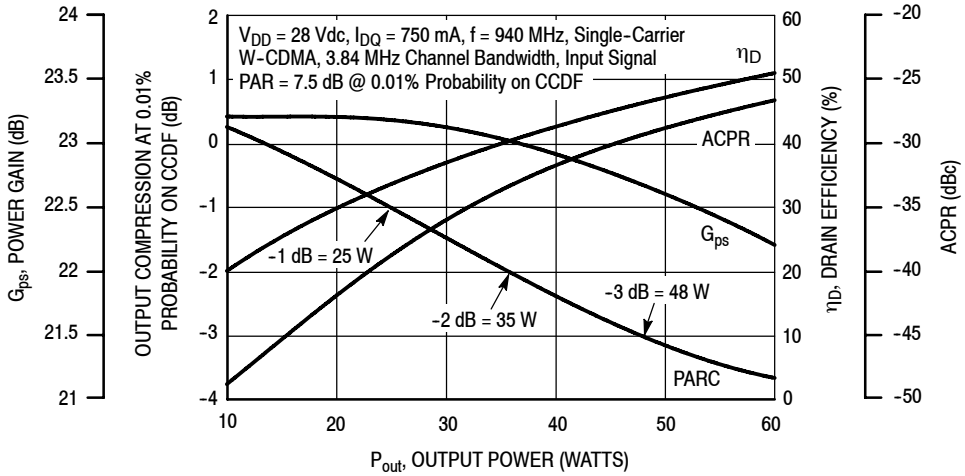


Figure 4. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

TYPICAL CHARACTERISTICS

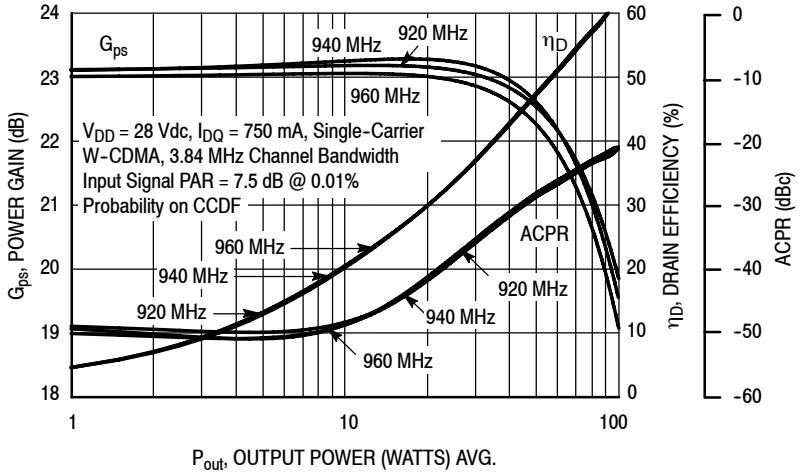


Figure 5. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

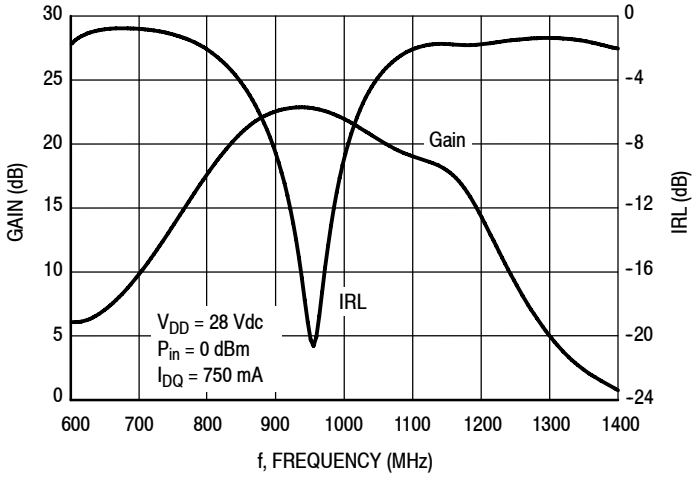


Figure 6. Broadband Frequency Response

W-CDMA TEST SIGNAL

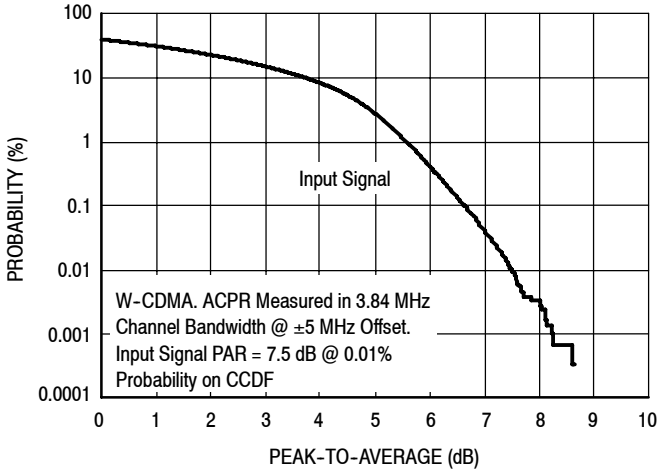


Figure 7. CCDF W-CDMA IQ Magnitude Clipping, Single-Carrier Test Signal

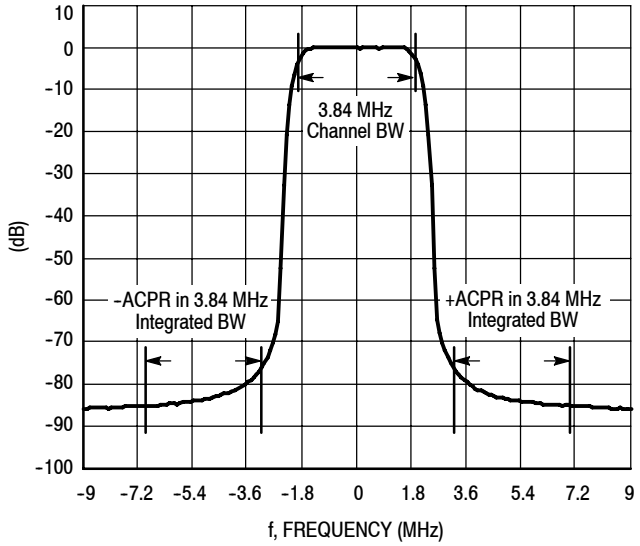


Figure 8. Single-Carrier W-CDMA Spectrum

V_{DD} = 28 Vdc, I_{DQ} = 750 mA, P_{out} = 28 W Avg.

f MHz	Z_{source} Ω	Z_{load} Ω
820	1.93 – j3.20	3.46 – j1.73
840	2.05 – j3.14	3.48 – j1.48
860	2.13 – j3.13	3.52 – j1.26
880	2.17 – j3.14	3.58 – j1.06
900	2.21 – j3.14	3.70 – j0.87
920	2.23 – j3.19	3.86 – j0.73
940	2.20 – j3.24	4.04 – j0.63
960	2.14 – j3.27	4.26 – j0.56
980	2.04 – j3.29	4.50 – j0.56

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

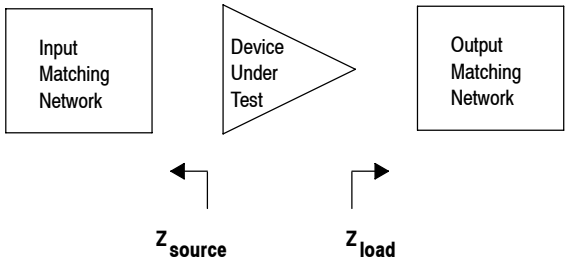
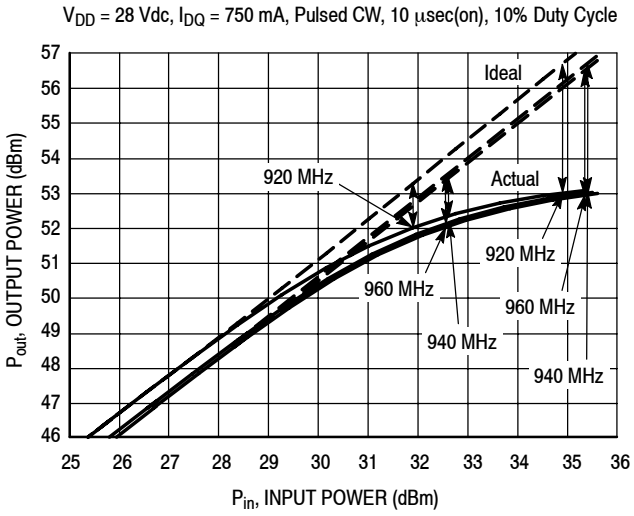


Figure 9. Series Equivalent Source and Load Impedance

ALTERNATIVE PEAK TUNE LOAD PULL CHARACTERISTICS



NOTE: Load Pull Test Fixture Tuned for Peak P1dB Output Power @ 28 V

f (MHz)	P1dB		P3dB	
	Watts	dBm	Watts	dBm
920	158	52.0	195	52.9
940	162	52.1	195	52.9
960	158	52.0	195	52.9

Test Impedances per Compression Level

f (MHz)		Z_{source} Ω	Z_{load} Ω
920	P1dB	1.60 – j2.77	8.80 – j0.18
940	P1dB	2.03 – j3.36	9.34 + j1.58
960	P1dB	2.33 – j3.55	8.42 + j3.05

Figure 10. Pulsed CW Output Power versus Input Power @ 28 V

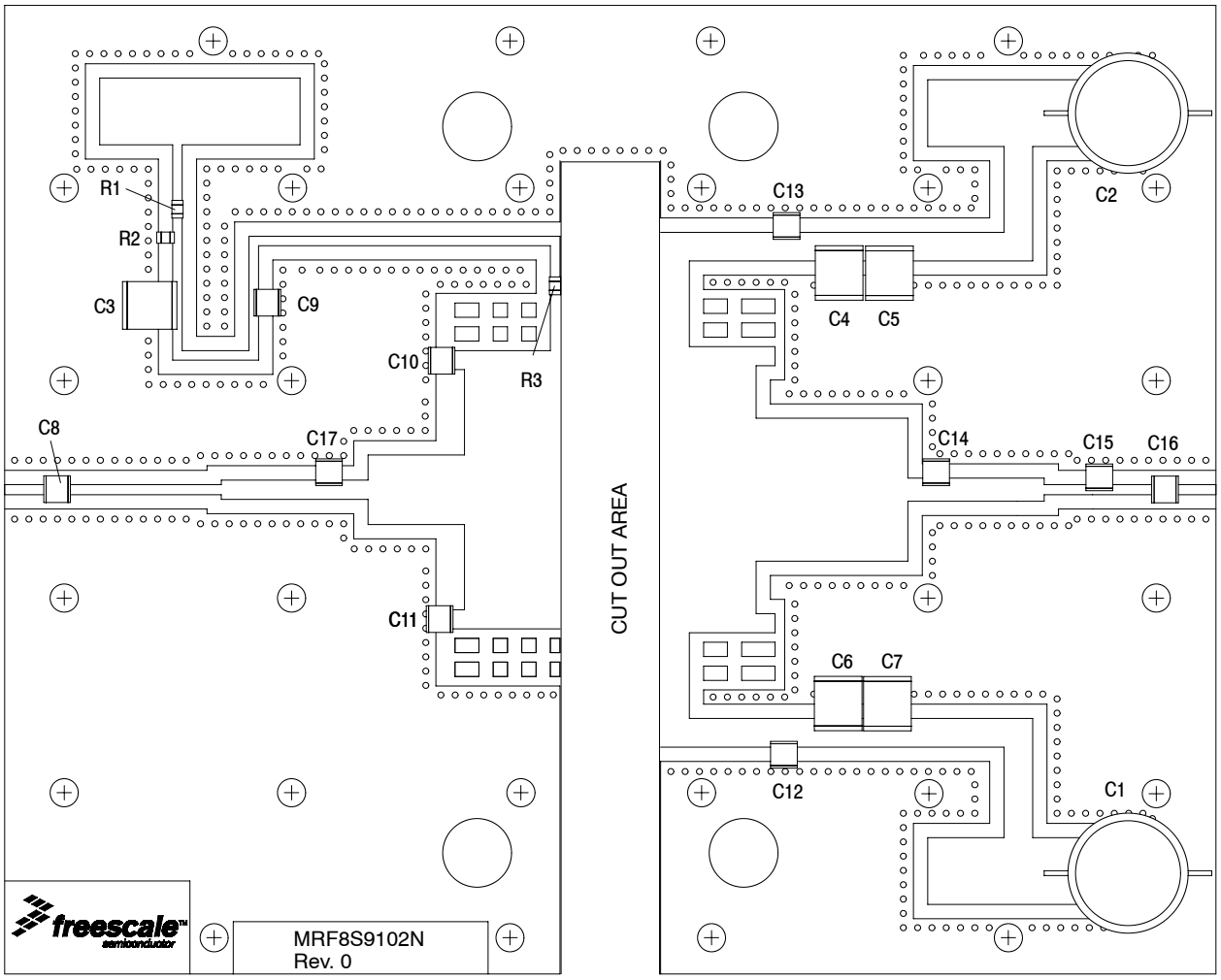


Figure 11. MRF8S9102NR3 Test Circuit Component Layout — 865-895 MHz

Table 7. MRF8S9102NR3 Test Circuit Component Designations and Values — 865-895 MHz

Part	Description	Part Number	Manufacturer
C1, C2	220 μF, 63 V Electrolytic Capacitors	222212018221	Vishay
C3, C4, C5, C6, C7	10 μF, 50 V Chip Capacitors	C5750X5R1H106M	TDK
C8	2.7 pF Chip Capacitor	ATC100B2R7BT500XT	ATC
C9, C12, C13, C16	47 pF Chip Capacitors	ATC100B470JT500XT	ATC
C10, C11	6.8 pF Chip Capacitors	ATC100B6R8BT500XT	ATC
C14, C15	3.9 pF Chip Capacitors	ATC100B3R9BT500XT	ATC
C17	1.2 pF Chip Capacitor	ATC100B1R2BT500XT	ATC
R1, R2	1 KΩ, 1/8 W Chip Resistors	WCR08051KFI	Welwyn
R3	10 Ω, 1/4 W Chip Resistor	9C12063A10R0FKHFT	Yageo
PCB	0.020″, ε_r = 3.5	RO4350	Rogers

TYPICAL CHARACTERISTICS — 865–895 MHz

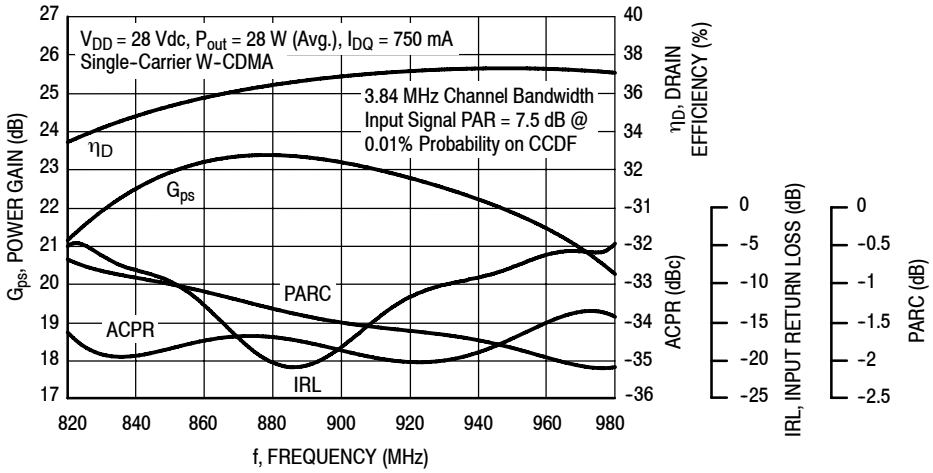


Figure 12. Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 28 Watts Avg.

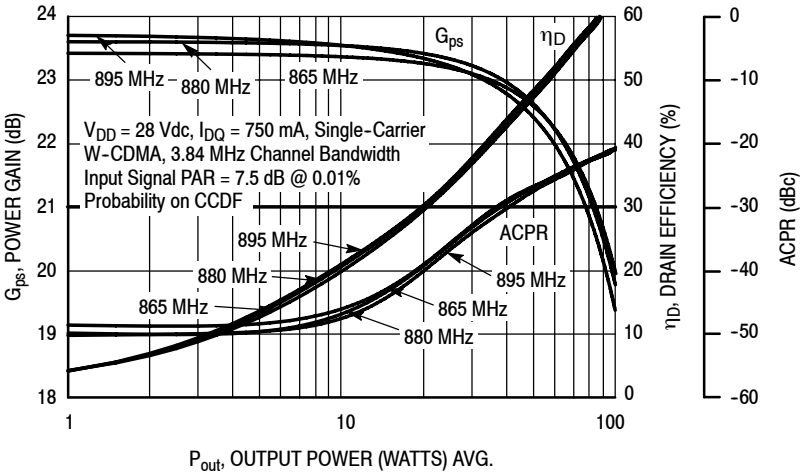


Figure 13. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

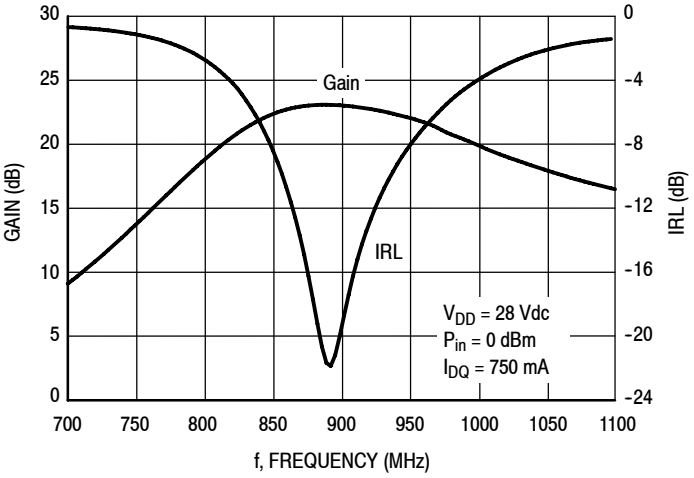


Figure 14. Broadband Frequency Response

V_{DD} = 28 Vdc, I_{DQ} = 750 mA, P_{out} = 28 W Avg.

f MHz	Z_{source} Ω	Z_{load} Ω
820	0.95 – j1.97	3.44 – j2.01
840	1.02 – j1.88	3.44 – j1.87
860	1.09 – j1.83	3.48 – j1.73
880	1.10 – j1.74	3.53 – j1.60
900	1.13 – j1.74	3.63 – j1.65
920	1.18 – j1.71	3.73 – j1.51
940	1.12 – j1.75	3.81 – j1.55
960	1.06 – j1.72	3.88 – j1.60
980	1.02 – j1.71	3.98 – j1.71

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

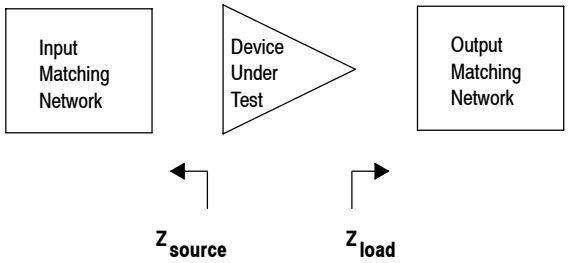
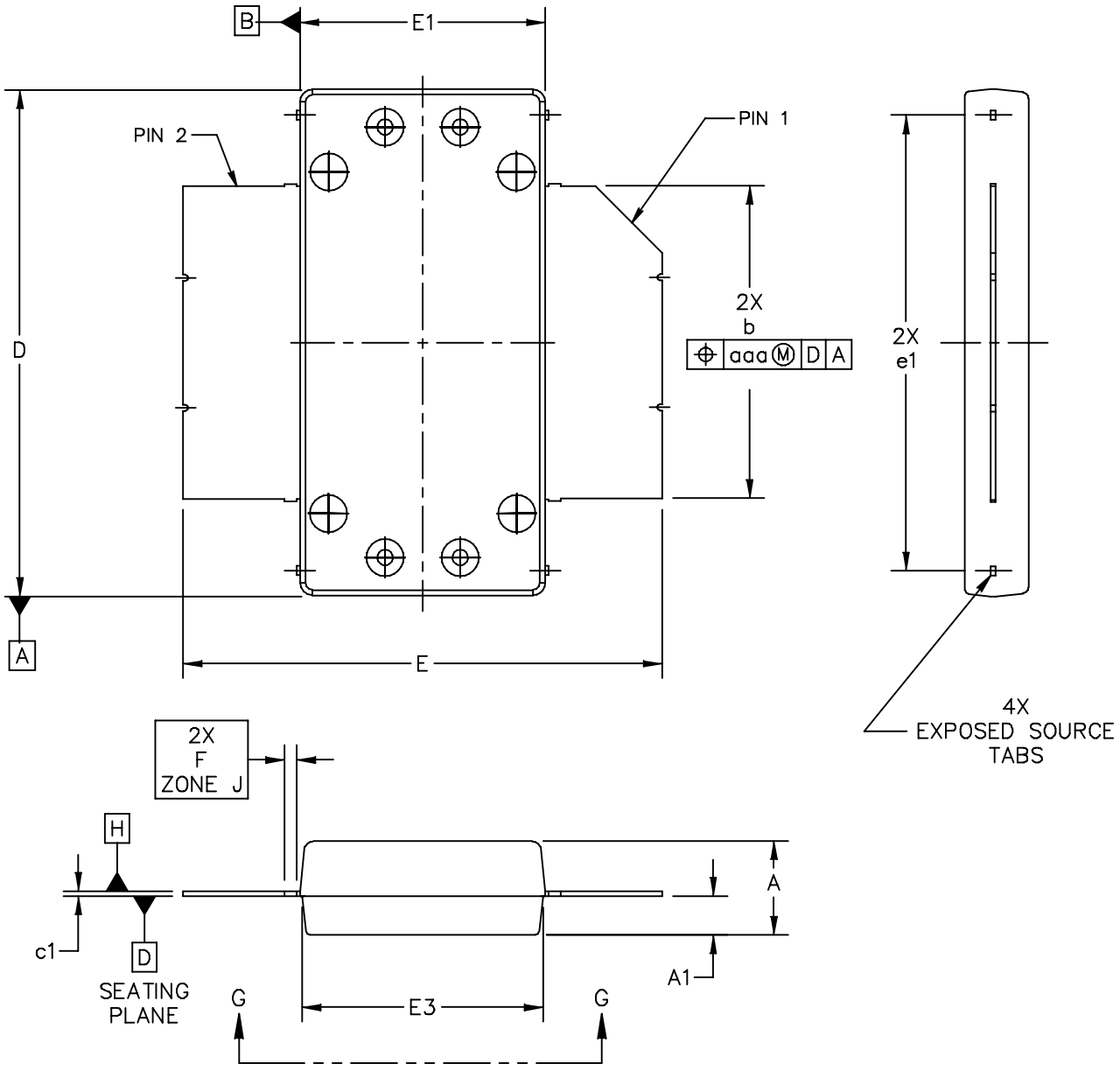


Figure 15. Series Equivalent Source and Load Impedance — 865–895 MHz

PACKAGE DIMENSIONS



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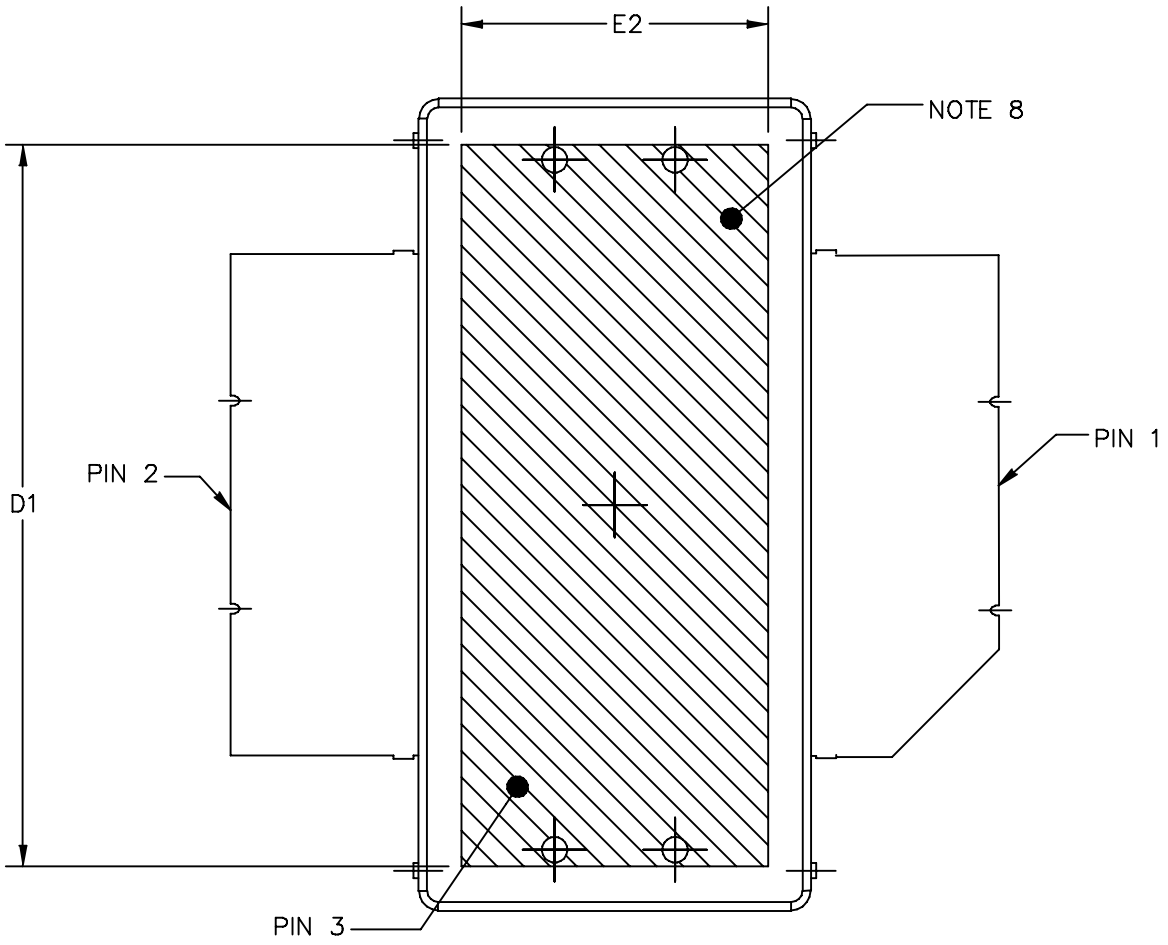
TITLE: OM780-2 STRAIGHT LEAD	DOCUMENT NO: 98ASA10831D	REV: B
	CASE NUMBER: 2021-03	22 OCT 2009
	STANDARD: NON-JEDEC	



BOTTOM VIEW
VIEW G–G

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	CASE NUMBER: 2021–03	22 OCT 2009
	STANDARD: NON–JEDEC	

NOTES:
1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.

3. DATUM PLANE -H- IS LOCATED AT TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.

5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.

6. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-.

7. DIMENSION A1 APPLIES WITHIN ZONE "J" ONLY

8. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG. THE DIMENSIONS D1 AND E2 REPRESENT THE VALUES BETWEEN THE TWO OPPOSITE POINTS ALONG THE EDGES OF EXPOSED AREA OF HEAT SLUG.

STYLE 1:
PIN 1 - DRAIN
PIN 2 - GATE
PIN 3 - SOURCE

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
A	0.148	.152	3.76	3.86	b	.497	.503	12.62	12.78
A1	.059	.065	1.50	1.65	c1	.007	.011	0.18	0.28
D	.808	.812	20.52	20.62	e1	.721	.729	18.31	18.52
D1	.720	----	18.29	----					
E	.762	.770	19.36	19.56	aaa	.004		0.10	
E1	.390	.394	9.91	10.01					
E2	.306	----	7.77	----					
E3	.383	.387	9.73	9.83					
F	.025 BSC		0.635 BSC						

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TITLE:	DOCUMENT NO: 98ASA10831D	REV: B
OM780-2 STRAIGHT LEAD	CASE NUMBER: 2021-03	22 OCT 2009
	STANDARD: NON-JEDEC	

PRODUCT DOCUMENTATION AND SOFTWARE

Refer to the following documents and software to aid your design process.

Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers
- AN3789: Clamping of High Power RF Transistors and RFICs in Over−Molded Plastic Packages

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- RF High Power Model
- .s2p File

For Software, do a Part Number search at http://www.freescale.com, and select the “Part Number” link. Go to the Software & Tools tab on the part’s Product Summary page to download the respective tool.

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Feb. 2011	• Initial Release of Data Sheet

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