



T4 Series

SNUBBERLESS™ & LOGIC LEVEL

4A TRIACs

Table 1: Main Features

Symbol	Value	Unit
$I_{T(RMS)}$	4	A
V_{DRM}/V_{RRM}	600 to 800	V
$I_{GT} (Q_1)$	5 to 35	mA

DESCRIPTION

Based on ST's Snubberless / Logic level technology providing high commutation performances, the **T4** series is suitable for use on AC inductive loads.

They are recommended for applications using universal motors, electrovalves.... such as kitchen aid equipments, power tools, dishwashers,... Available in a fully insulated package, the T4...-...W version complies with UL standards (ref. E81734).

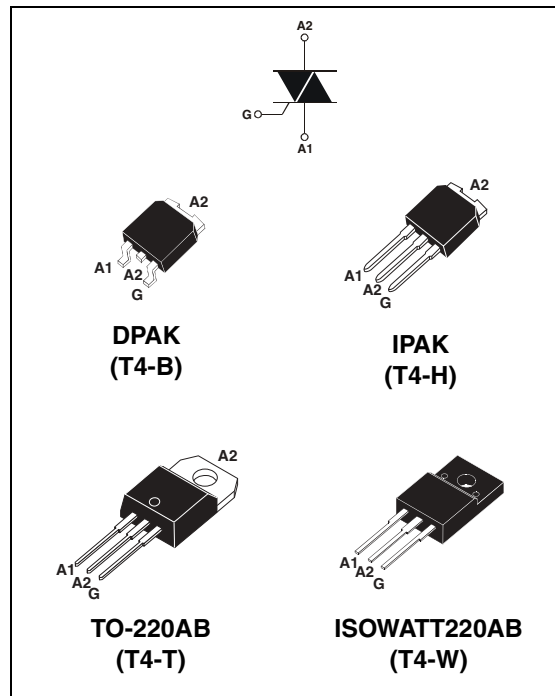


Table 2: Order Codes

Part Number	Marking
T405-xxxB	See page table 8 on page 9
T405-xxxB-TR	
T405-xxxH	
T405-xxxT	
T405-xxxW	
T410-xxxB	
T410-xxxB-TR	
T410-xxxH	
T4105-xxxT	
T410-xxxW	
T435-xxxB	
T435-xxxB-TR	
T435-xxxH	
T435-xxxT	
T435-xxxW	

T4 Series

Table 3: Absolute Maximum Ratings

Symbol	Parameter			Value	Unit
$I_{T(RMS)}$	RMS on-state current (full sine wave)	IPAK/DPAK/ TO-220AB	$T_c = 110^\circ\text{C}$	4	A
		ISOWATT220AB	$T_c = 105^\circ\text{C}$		
I_{TSM}	Non repetitive surge peak on-state current (full cycle, T_j initial = 25°C)	F = 50 Hz	t = 20 ms	30	A
		F = 60 Hz	t = 16.7 ms	31	
I^2t	I^2t Value for fusing	$t_p = 10$ ms		5.1	A^2s
di/dt	Critical rate of rise of on-state current $I_G = 2 \times I_{GT}$, $t_r \leq 100$ ns	F = 120 Hz	$T_j = 125^\circ\text{C}$	50	$\text{A}/\mu\text{s}$
I_{GM}	Peak gate current	$t_p = 20$ μs	$T_j = 125^\circ\text{C}$	4	A
$P_{G(AV)}$	Average gate power dissipation		$T_j = 125^\circ\text{C}$	1	W
T_{stg} T_j	Storage junction temperature range Operating junction temperature range			- 40 to + 150 - 40 to + 125	$^\circ\text{C}$

Tables 4: Electrical Characteristics ($T_j = 25^\circ\text{C}$, unless otherwise specified)

Symbol	Test Conditions	Quadrant		T4			Unit
				T405	T410	T435	
I_{GT} (1)	$V_D = 12$ V $R_L = 30$ Ω	I - II - III	MAX.	5	10	35	mA
V_{GT}		I - II - III	MAX.	1.3			V
V_{GD}	$V_D = V_{DRM}$ $R_L = 3.3$ k Ω $T_j = 125^\circ\text{C}$	I - II - III	MIN.	0.2			V
I_H (2)	$I_T = 100$ mA		MAX.	10	15	35	mA
I_L	$I_G = 1.2$ I_{GT}	I - III	MAX.	10	25	50	mA
		II		15	30	60	
dV/dt (2)	$V_D = 67\%$ V_{DRM} gate open $T_j = 125^\circ\text{C}$		MIN.	20	40	400	$\text{V}/\mu\text{s}$
(di/dt)c (2)	$(dV/dt)c = 0.1$ $\text{V}/\mu\text{s}$ $T_j = 125^\circ\text{C}$		MIN.	1.8	2.7	-	A/ms
	$(dV/dt)c = 10$ $\text{V}/\mu\text{s}$ $T_j = 125^\circ\text{C}$			0.9	2.0	-	
	Without snubber $T_j = 125^\circ\text{C}$			-	-	2.5	

Note 1: minimum I_{GT} is guaranteed at 5% of I_{GT} max.

Note 2: for both polarities of A2 referenced to A1.

Table 5: Static Characteristics

Symbol	Test Conditions			Value	Unit	
V_T (2)	$I_{TM} = 5.5 \text{ A}$	$t_p = 380 \mu\text{s}$	$T_j = 25^\circ\text{C}$	MAX.	1.56	V
V_{to} (2)	Threshold voltage		$T_j = 125^\circ\text{C}$	MAX.	0.89	V
R_d (2)	Dynamic resistance		$T_j = 125^\circ\text{C}$	MAX.	120	m Ω
I_{DRM} I_{RRM}	$V_{DRM} = V_{RRM}$		$T_j = 25^\circ\text{C}$	MAX.	5	μA
			$T_j = 125^\circ\text{C}$		1	mA

Note 1: minimum I_{GT} is guaranteed at 5% of I_{GT} max.

Note 2: for both polarities of A2 referenced to A1.

Table 6: Thermal resistance

Symbol	Parameter		Value	Unit	
$R_{th(j-c)}$	Junction to case (AC)		IPAK / DPAK / TO-220AB	2.6	$^\circ\text{C/W}$
			ISOWATT220AB	4.0	
$R_{th(j-a)}$	Junction to ambient	$S = 0.5 \text{ cm}^2$	DPAK	70	$^\circ\text{C/W}$
			TO-220AB / ISOWATT220AB	60	
			IPAK	100	

S = Copper surface under tab.

T4 Series

Figure 1: Maximum power dissipation versus RMS on-state current (full cycle)

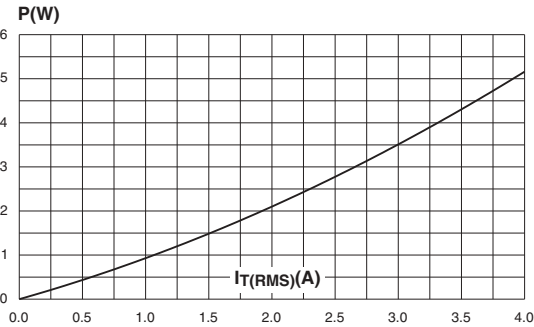


Figure 2: RMS on-state current versus case temperature (full cycle)

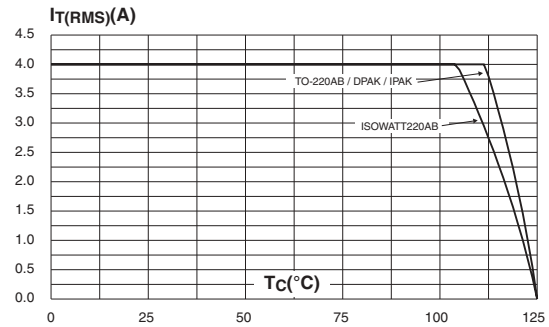


Figure 3: RMS on-state current versus ambient temperature (printed circuit board FR4, copper thickness: 35µm) (full cycle)

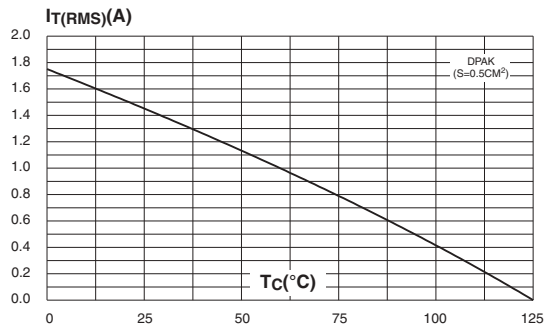


Figure 4: Relative variation of thermal impedance versus pulse duration

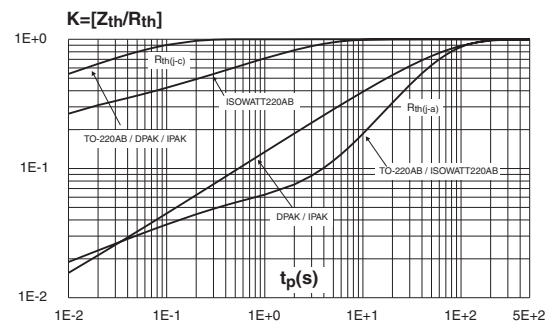


Figure 5: On-state characteristics (maximum values)

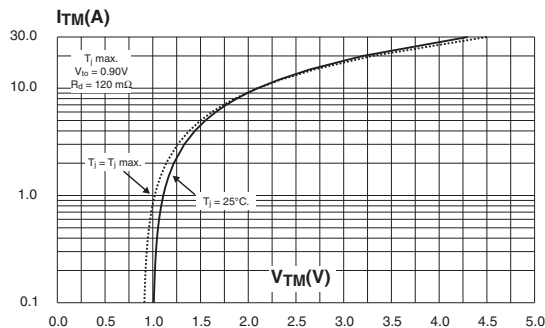


Figure 6: Surge peak on-state current versus number of cycles

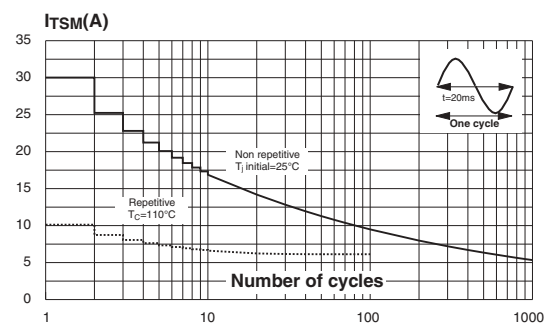


Figure 7: Non-repetitive surge peak on-state current for a sinusoidal pulse with width $t_p < 10$ ms and corresponding value of I^2t

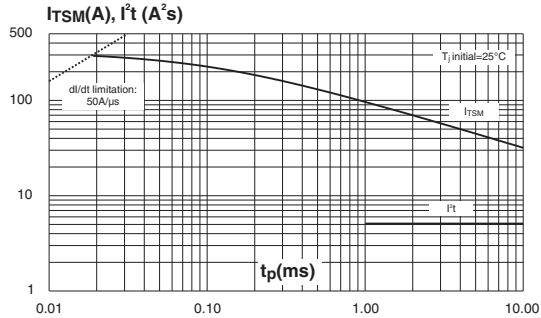


Figure 8: Relative variation of gate trigger current, holding current and latching current versus junction temperature (typical values)

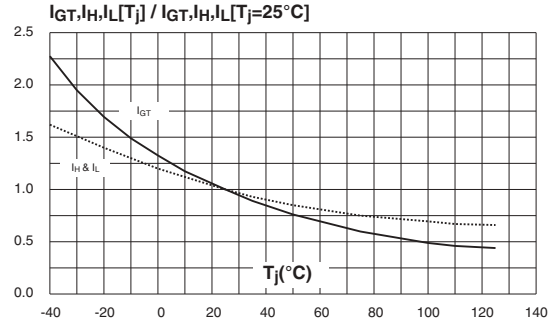


Figure 9: Relative variation of critical rate of decrease of main current versus $(dV/dt)_c$ (typical values)

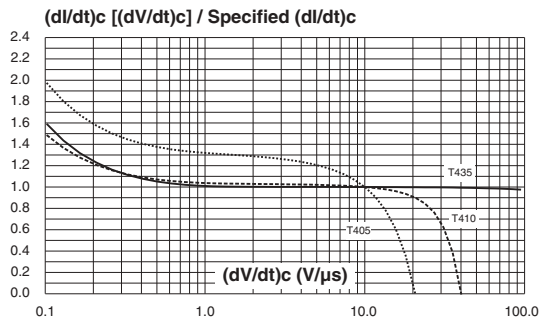


Figure 10: Relative variation of critical rate of decrease of main current versus junction temperature

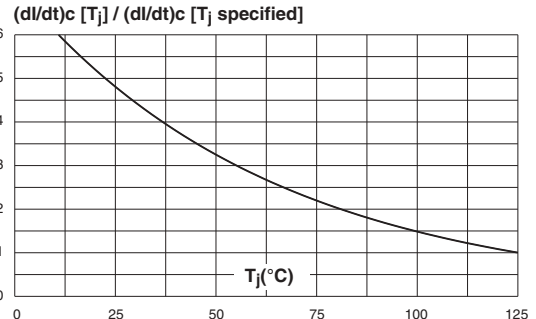
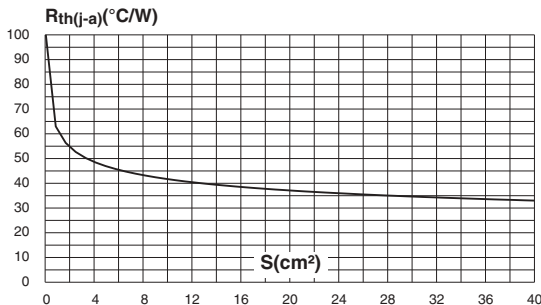


Figure 11: DPAK thermal resistance junction to ambient versus copper surface under tab (printed circuit board FR4, copper thickness: 35 μm)



T4 Series

Figure 12: Ordering Information Scheme

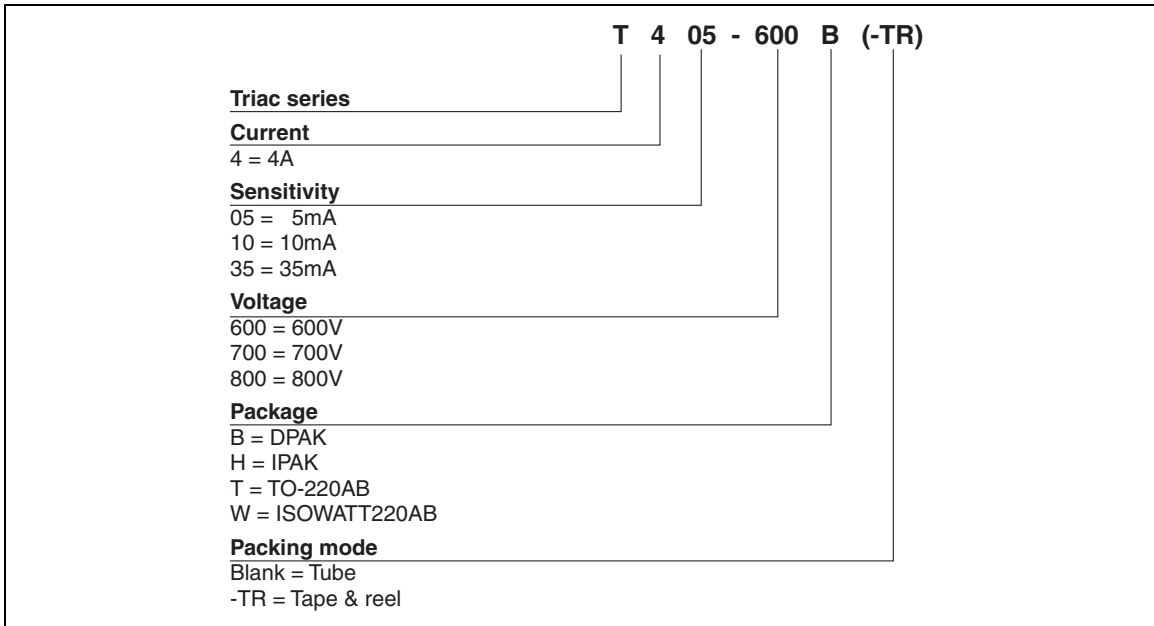


Table 7: Product Selector

Part Number	Voltage (xxx)			Sensitivity	Type	Package
	600 V	700 V	800 V			
T405-xxxB	X	X	X	5 mA	Logic level	DPAK
T405-xxxH	X	X	X	5 mA	Logic level	IPAK
T405-xxxT	X	X	X	5 mA	Logic level	TO-220AB
T405-xxxW	X	X	X	5 mA	Logic level	ISOWATT220AB
T410-xxxB	X	X	X	10 mA	Logic level	DPAK
T410-xxxH	X	X	X	10 mA	Logic Level	IPAK
T410-xxxT	X	X	X	10 mA	Logic Level	TO-220AB
T410-xxxW	X	X	X	10 mA	Logic Level	ISOWATT220AB
T435-xxxB	X	X	X	35 mA	Snubberless	DPAK
T435-xxxH	X	X	X	35 mA	Snubberless	IPAK
T435-xxxT	X	X	X	35 mA	Snubberless	TO-220AB
T435-xxxW	X	X	X	35 mA	Snubberless	ISOWATT220AB

Figure 13: DPAK Package Mechanical Data

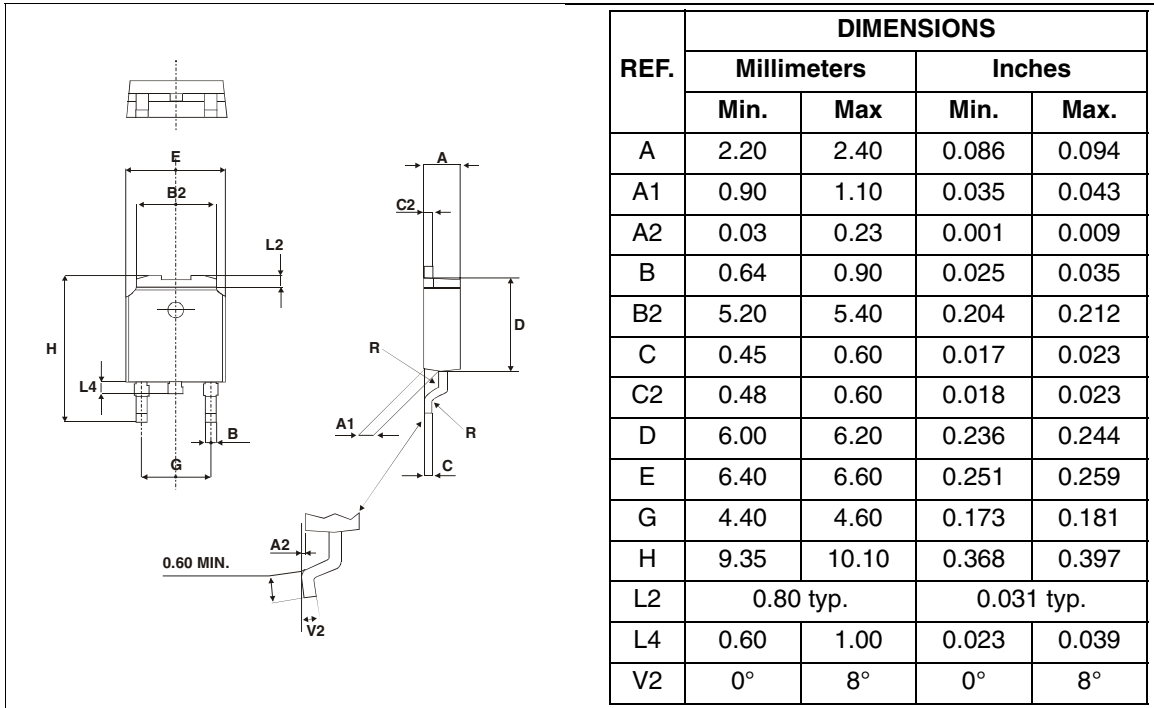
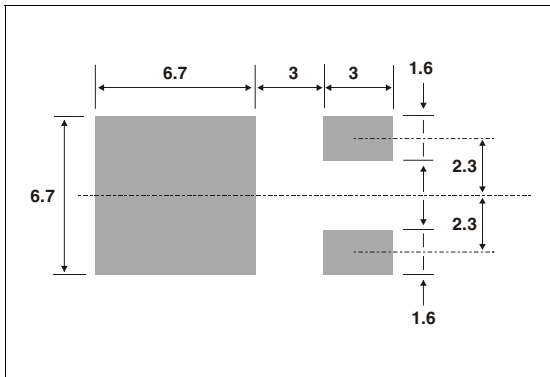


Figure 14: DPAK Foot Print Dimensions (in millimeters)



T4 Series

Figure 15: ISOWATT220AB Package Mechanical Data

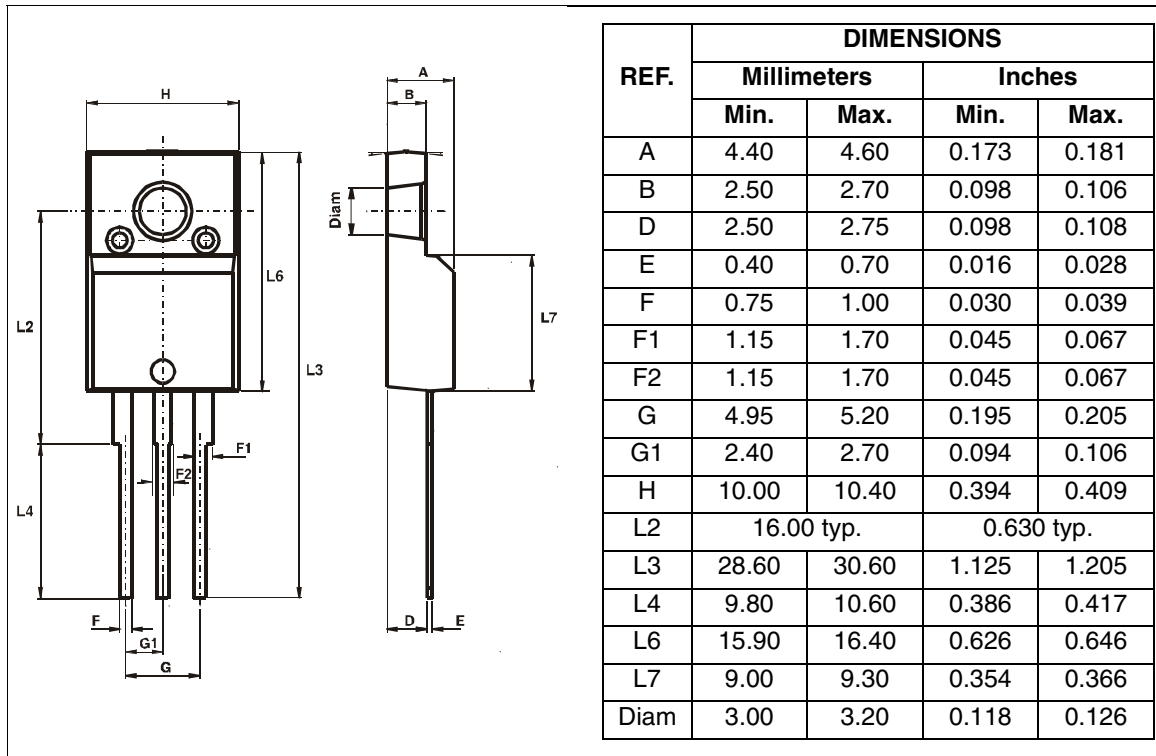


Figure 16: IPAK Package Mechanical Data

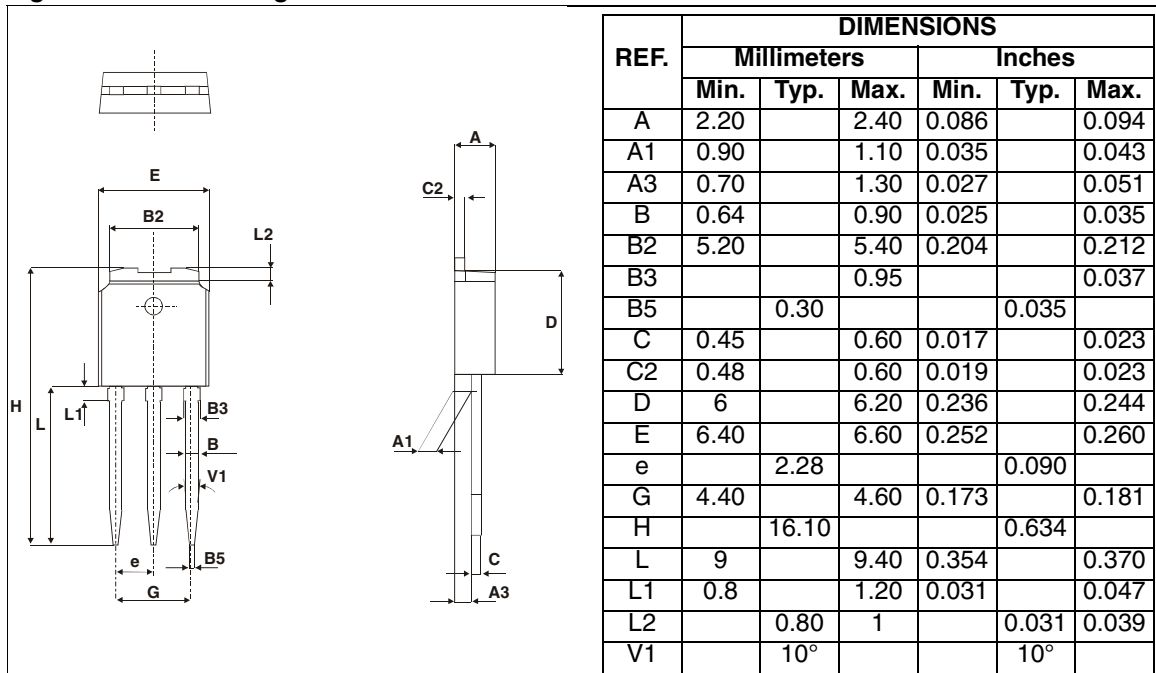


Figure 17: TO-220AB Package Mechanical Data

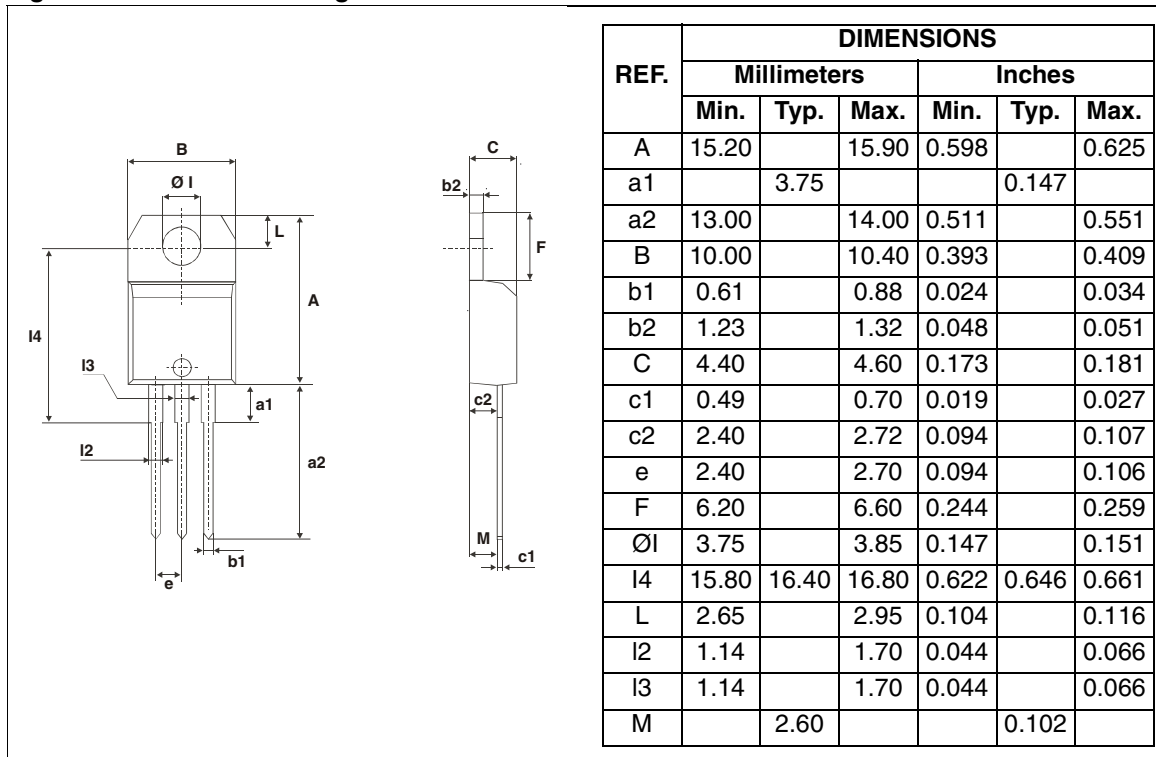


Table 8: Ordering Information

Ordering type	Marking	Package	Weight	Base qty	Delivery mode
T4xx-yyyB	T4 xxyy	DPAK	0.3 g	75	Tube
T4xx-yyyB-TR	T4 xxyy	DPAK	0.3 g	2500	Tape & reel
T4xx-yyyH	T4 xxyy	IPAK	0.4 g	75	Tube
T4xx-yyyT	T4xx yyyT	TO-220AB	2.3 g	50	Tube
T4xx-yyyB	T4xxyyyW	ISOWATT220AB	2.1 g	50	Tube

Note: xxx = voltage, yy = sensitivity

Table 9: Revision History

Date	Revision	Description of Changes
Jun-2003	5	Last update.
25-Mar-2005	6	Layout update. No content change.
25-Jan-2005	7	Markings changed in Table 8

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a registered trademark of STMicroelectronics.
All other names are the property of their respective owners

© 2005 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan -
Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America
www.st.com