

AS1121

16-Channel LED Driver with Dot Correction and Greyscale PWM

1 General Description

The AS1121 is a 16-channel, constant current-sink LED driver. Each of the 16 channels can be individually adjusted by 4096-step greyscale PWM brightness control and 64-step constant-current sink (dot correction).

The dot correction circuitry adjusts the brightness variations between the AS1121 channels and other LED drivers. Greyscale control and dot correction circuitry are accessible via the SPI-compatible serial interface. A single external resistor sets the maximum current value of all 16 channels.

The open LED detection function indicates a broken or disconnected LED at one or more of the outputs. The overtemperature protection flag indicates that the device is in an overtemperature condition.

An additional power-down pin puts the AS1121 into a 40nA standby-mode.

The AS1121 is available in a 32-pin TQFN 5x5 mm package.

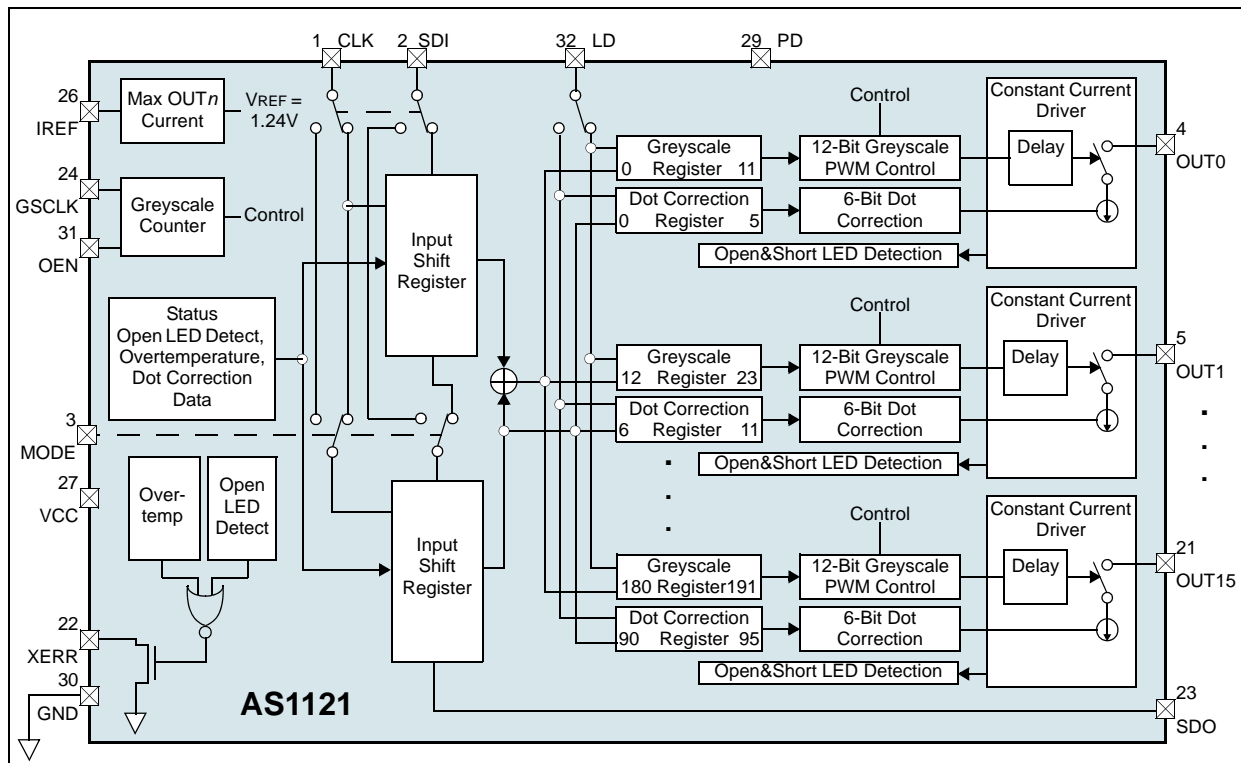
2 Key Features

- Greyscale PWM Control: 12-Bit (4096 Steps)
- Dot Correction: 6-Bit (64 Steps)
- Drive Capability (Constant-Current Sink): 0 to 40mA
- LED Power Supply Voltage: up to 30V
- Supply Voltage Range: 3.1V to 3.6V
- SPI-Compatible Serial Interface
- Output Delay for controlled Inrush Current (factory set, can be turned off)
- Factory set rise- and fall-time for EMI improvement
- PWM Clock Rate: up to 10 MHz
- Data Transfer Clock Rate: up to 30 MHz
- CMOS Level I/O
- Diagnostic Features
- 32-pin TQFN 5x5 mm Package

3 Applications

The device is ideal for mono-, multi-, and full-color LED displays, LED signboards, and display backlights.

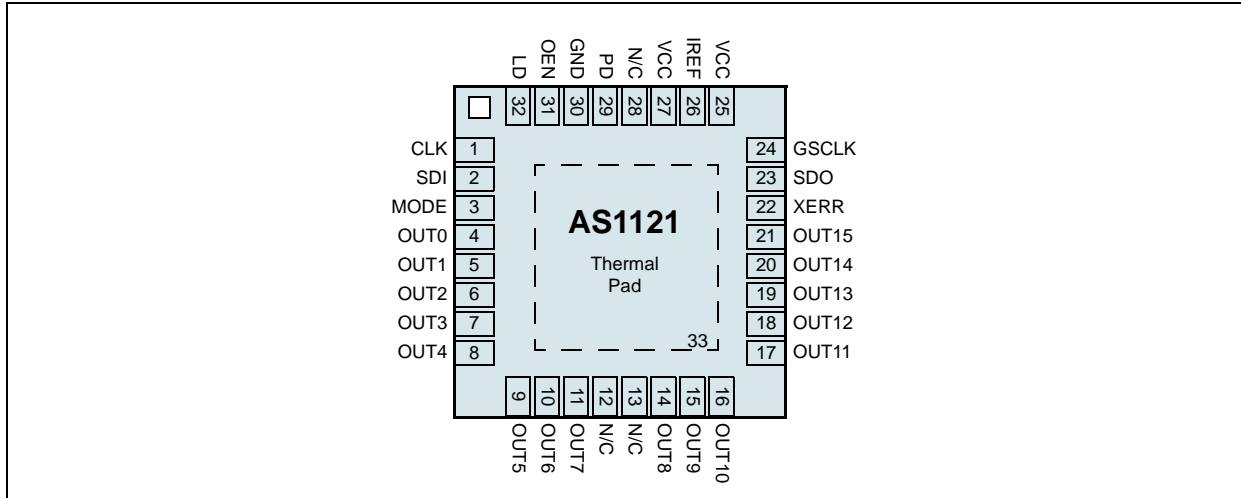
Figure 1. AS1121 - Block Diagram



4 Pinout

Pin Assignments

Figure 2. Pin Assignments (Top View)



Pin Descriptions

Table 1. Pin Descriptions

| Pin Number | Pin Name | Description |
|------------|-------------|---|
| 1 | CLK | Serial Data Shift Clock |
| 2 | SDI | Serial Data Input |
| 3 | MODE | Mode Select input with internal pulldown MODE = GND: Selects greyscale mode (see Setting Greyscale Brightness on page 11) MODE = Vcc: Selects dor correction mode (see Setting Dot Correction on page 10) |
| 4:11 | OUT0:OUT7 | Constant-Current Outputs 0:7 |
| 14:21 | OUT8:OUT15 | Constant-Current Outputs 8:15 |
| 22 | XERR | Error Output 0 = LED open detection or overtemperature condition is detected. 1 = Normal operation. |
| 23 | SDO | Serial Data Output |
| 24 | GSCLK | Greyscale Clock. Reference clock for greyscale PWM control |
| 26 | IREF | Reference Current Terminal |
| 25, 27 | VCC | Power Supply Voltage |
| 12,13,28 | N/C | This pins must not be connected |
| 29 | PD | Power Down 0 = normal operation mode 1 = power down mode |
| 30 | GND | Ground |
| 31 | OEN | Blank Outputs 0 = OUT n outputs are controlled by the greyscale PWM control. 1 = OUT n outputs are forced off; the greyscale counter is reset. |
| 32 | LD | Data Latch. The internal connections are switched by pin MODE. For LD (MODE = GND), the greyscale register receives new data. For LD (MODE = Vcc), the dot correction register receives new data. |
| 33 | Thermal Pad | Thermal Pad. This pin must be connected to GND to ensure normal operation. |

5 Absolute Maximum Ratings

Stresses beyond those listed in [Table 2](#) may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in [Electrical Characteristics on page 4](#) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

| Parameter | Min | Max | Units | Comments |
|--|------|-----------|-------|---|
| Electrical Parameters | | | | |
| VCC to GND | -0.3 | 5 | V | |
| All other pins to GND | -0.3 | VCC + 0.3 | V | |
| VSDO, VXERR to GND | -0.3 | VCC + 0.3 | V | |
| VOUT0 : VOUT15 to GND | -0.3 | 30 | V | |
| Output Current | | 50 | mA | |
| Input Current (latch-up immunity) | -100 | 100 | mA | Norm: JEDEC 78 |
| Electrostatic Discharge | | | | |
| Electrostatic Discharge HBM | | +/- 2 | kV | Norm: MIL 883 E method 3015 |
| Thermal Information | | | | |
| Junction to ambient thermal resistance | | 37 | °C/W | For more information about thermal metrics, see application note <i>AN01 Thermal Characteristics</i> . |
| Temperature Ranges and Storage Conditions | | | | |
| Junction Temperature | | +125 | °C | |
| Storage Temperature Range | -55 | +150 | °C | |
| Package Body Temperature | | +260 | °C | The reflow peak soldering temperature (body temperature) specified is in accordance with <i>IPC/JEDEC J-STD-020 Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices</i> . The lead finish for Pb-free leaded packages is matte tin (100% Sn). |
| Humidity non-condensing | 5 | 85 | % | |
| Moisture Sensitive Level | | 3 | | Represents a max. floor life time of 168h |

6 Electrical Characteristics

VCC = +3.1V to +3.6V, Typical values are at TAMB = +25°C, VCC = 3.3V (unless otherwise specified). All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods..

Table 3. Electrical Characteristics

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---------------------|--|--|--------------|-------|--------------|------|
| TAMB | Operating Temperature Range | | -40 | | +85 | °C |
| TJ | Operating Junction Temperature | | -40 | | +125 | °C |
| Input Supply | | | | | | |
| VCC | Supply Voltage | | 3.1 | | 3.6 | V |
| Icc | Supply Current | All outputs off, R _{REF} = 1kΩ | | 8.5 | 15 | mA |
| | | All outputs on, R _{REF} = 1kΩ | | 15 | 20 | |
| | | All outputs off, R _{REF} = 10kΩ | | 2 | 4 | |
| | | All outputs on, R _{REF} = 10kΩ | | 3 | 5 | |
| I | Input Current | V _{IN} = VCC or GND; Pins OEN, GSCLK, CLK, SDI, LD, PD | -1 | | 1 | μA |
| | | V _{IN} = VCC; pin MODE | | | 50 | |
| | | V _{IN} = GND; pin MODE | -1 | | 1 | |
| IPD | Power Down Current | | | 40 | | nA |
| Output | | | | | | |
| VOUT | Voltage Applied to Output (OUT0:OUT15) | | 1.5 | | 30 | V |
| ICOC | Constant Output Current | All outputs on, V _{OUT} = 1.5V, R _{REF} = 1kΩ | 36 | 40 | 44 | mA |
| ΔICOC | Constant Output Current Error | V _{OUT} = 1.5V, R _{REF} = 1kΩ, OUT0:OUT15 | | ±1 | | % |
| | | V _{OUT} = 1.5V, R _{REF} = 10kΩ, OUT0:OUT15 | | ±1.5 | | |
| | | Device to device, average current from OUT0:OUT15, R _{REF} = 1kΩ | | ±1 | | |
| | | Device to device, average current from OUT0:OUT15, R _{REF} = 10kΩ | | ±1 | | |
| I _{LEAK} | Leakage Output Current | All outputs off, V _{OUT} = 30V, R _{REF} = 1kΩ, OUT0:OUT15 | | 20 | | nA |
| ΔILNR | Line Regulation | V _{OUT} = 1V, R _{REF} = 1kΩ OUT0:OUT15 | | ±1 | ±2.5 | %V |
| | | V _{OUT} = 1V, R _{REF} = 10kΩ OUT0:OUT15 | | ±0.2 | ±2.5 | |
| ΔILD _R | Load Regulation | V _{OUT} = 1.5V to 4V, R _{REF} = 1kΩ, OUT0:OUT15 | | ±0.1 | ±0.4 | %V |
| | | V _{OUT} = 1.5V to 4V, R _{REF} = 10kΩ, OUT0:OUT15 | | ±0.01 | ±0.4 | |
| Logic Levels | | | | | | |
| V _{IH} | High-Level Input Voltage | | 0.8 x VCC | | VCC | V |
| V _{IL} | Low-Level Input Voltage | | GND | | 0.2 x VCC | V |
| V _{OH} | High-Level Output Voltage | I _{OH} = -1mA, SDO | VCC-0.5 | | | V |
| V _{OL} | Low-Level Output Voltage | I _{OL} = 1mA, SDO, XERR | | | 0.5 | V |
| I _{OH} | High-Level Output Current | VCC = 5 V at SDO | -1.0 | | | mA |

Table 3. Electrical Characteristics (Continued)

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|--------|------------------------------|------------------------|------|------|------|------|
| IOL | Low-Level Output Current | VCC = 5 V at SDO, XERR | 1.0 | | | mA |
| VLOD | LED Open Detection Threshold | | | 0.3 | 0.4 | V |
| VIREF | Reference Voltage Output | RREF = 1kΩ | 1.23 | 1.27 | 1.32 | V |

Timing Characteristics

VCC = +3.1V to +3.6V, TAMB = -40°C to +85°C. Typical values are at TAMB = +25°C, VCC = 3.3V (unless otherwise specified).

Table 4. Output Timing Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------|---|--|-----|-----|-----|------|
| tR0 | Rise Time | SDO | | 8 | | ns |
| tR1 ¹ | | OUTn, DC = 3F _{HEX} , RREF = 1kΩ | | 25 | | |
| tF0 | Fall Time | SDO | | 8 | | ns |
| tF1 ¹ | | OUTn, DC = 3F _{HEX} , RREF = 1kΩ | | 25 | | |
| tpD0 | Propagation Delay Time | CLK, SDO ² | | 15 | | ns |
| tpD1 | | OUT0, OUT1, OUT2, OUT3 ² , RREF = 1kΩ, turn ON delay | | | | |
| tpD2 | | OUT0, OUT1, OUT2, OUT3 ² , RREF = 1kΩ, turn OFF delay | | | | |
| tD | Average Output Delay Time (can be tured off on request) | OUT4, OUT5, OUT6, OUT7 ² | | 25 | | ns |
| | | OUT8, OUT9, OUT10, OUT11 ² | | | | |
| | | OUT12, OUT13, OUT14, OUT15 ² | | | | |

- Value can be factory trimmed for EMI improvement
- See Figure 10 on page 13.

Interface Characteristics

VCC = +3.1V to +3.6V, TAMB = -40°C to +85°C. Typical values are at TAMB = +25°C, VCC = 3.3V (unless otherwise specified).

Table 5. Serial Interface Timing Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------|----------------------------|------------------------------|-----|------|-----|------|
| fCLK | Data Shift Clock Frequency | CLK | | | 30 | MHz |
| fGCLK | Greyscale Clock Frequency | GCLK | | | 5 | MHz |
| tWH0/tWLO | CLK Pulse Duration | CLK = 1/0 ¹ | 16 | | | ns |
| tWH1/tWL1 | GCLK Pulse Duration | GCLK = 1/0 ² | tbd | | | ns |
| tWH2 | LD Pulse Duration | LD = 1 ¹ | 20 | | | ns |
| tWH3 | OEN Pulse Duration | OEN = 1 ² | 20 | | | ns |
| tERR | Error Detection Duration | LD = 1, OEN = 0 ³ | | 1000 | | ns |

Table 5. Serial Interface Timing Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------|------------|-------------------------|-----|-----|-----|------|
| t _{SU0} | Setup Time | SDI, CLK ⁴ | 12 | | | ns |
| t _{SU1} | | CLK, LD ³ | 12 | | | |
| t _{SU2} | | MODE, CLK ⁵ | 12 | | | |
| t _{SU3} | | MODE, LD ⁴ | 12 | | | |
| t _{SU4} | | OEN, GSCLK ² | 12 | | | |
| t _{H0} | Hold Time | CLK, SDI ³ | 12 | | | ns |
| t _{H1} | | LD, CLK ¹ | 12 | | | |
| t _{H2} | | CLK, MODE ⁴ | 12 | | | |
| t _{H3} | | LD, MODE ⁴ | 12 | | | |
| t _{H4} | | OEN, GSCLK ² | 12 | | | |

1. See [Figure 6](#) on page 10.
2. See [Figure 10](#) on page 13.
3. See [Figure 4](#) on page 8
4. See [Figure 8](#) on page 11.
5. See [Figure 3](#) on page 7.

7 Detailed Description

Serial Interface

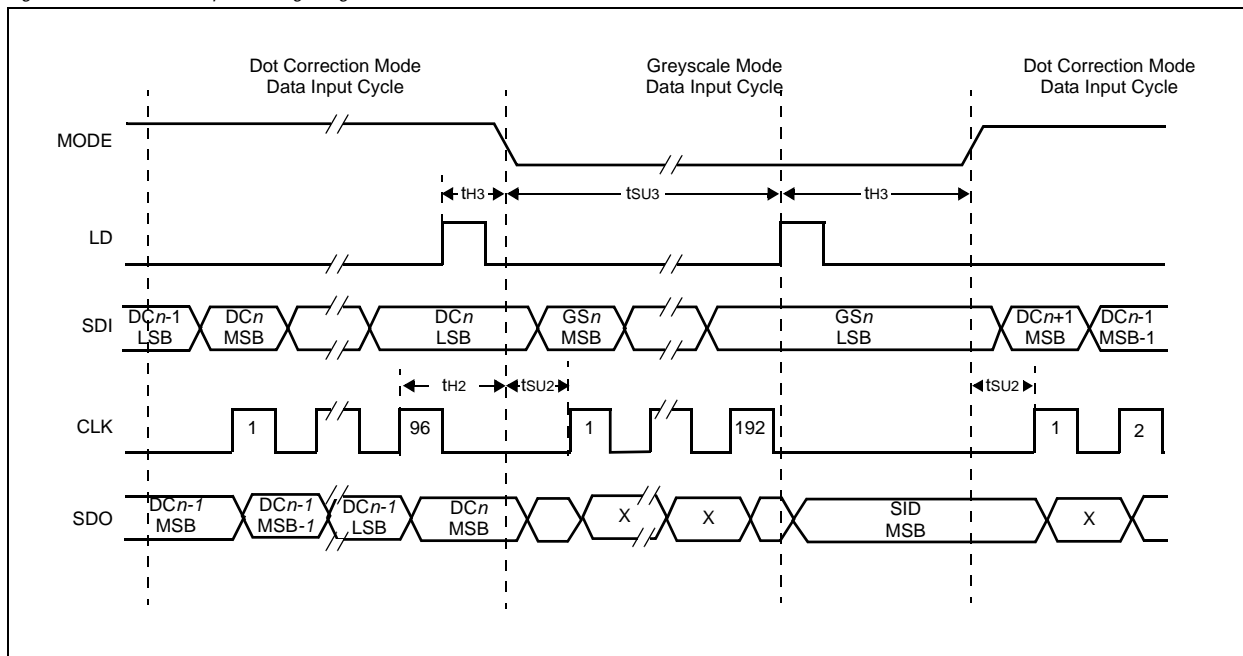
The AS1121 features a versatile 3-pin (CLK, SDI, and SDO) serial interface, which can be connected to microcontrollers or digital signal processors in various configurations.

The rising edge of the CLK signal shifts data from pin SDI to the internal register. After all data is clocked in, the serial data is latched into the internal registers at the rising edge of the LD signal.

Note: All data is clocked in with the MSB first.

Multiple AS1121 devices can be cascaded by connecting the SDO pin of one device with pin SDI of the next device (see Figure 11 on page 14). The SDO pin can also be connected to the microcontroller to receive status information from the AS1121. The serial data format is 96-bit or 192-bit wide, depending on mode of the device (see LD on page 2).

Figure 3. Serial Data Input Timing Diagram



Error Information Output

The open-drain output pin XERR indicates if the device is in error condition (open LED detect or overtemperature). During normal operation, the internal transistor connected to pin XERR is turned off and the voltage on XERR is pulled up to VCC through an external pullup resistor.

If an open LED or an overtemperature condition is detected, the internal transistor is switched on, and XERR is pulled to GND. Because XERR is an open-drain output, multiple AS1121 devices can be ORed together and pulled up to VCC with a single pullup resistor (see Figure 11 on page 14). This reduces the number of signals needed to report a system error.

To differentiate the the open LED from the overtemperature condition the status information data (SID) of the AS1121 needs to be read out.

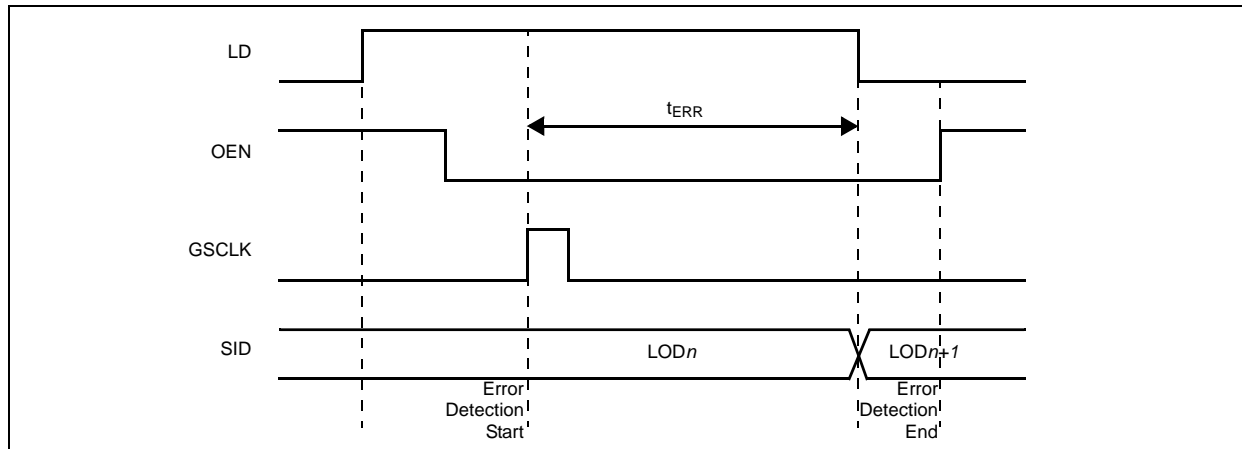
Open LED Detection

The AS1121 integrated open LED detection circuit reports an error if any of the 16 LEDs is open or disconnected from the circuit. The open LED detection circuit trips when the error detection is activated and the voltage at OUT_n is less than V_{LOD} .

Note: The voltage at each OUT_n is sampled 1 μ s after being switched on. Please refer to Figure 4 on page 8.

The open LED detection circuit also pulls XERR to GND when tripped. The open LED status of each channel can also be read out from the AS1121 status information data (SID) during a greyscale data input cycle.

Figure 4. Error Detection Timing ($GS=FFFF_{HEX}$, $DC=3F_{HEX}$)



Note: The rising edge of LD latches new data into the internal registers depending on the logic level of the pin MODE. If the pin MODE is tied GND, the greyscale registers are updated. If the pin MODE is tied to VCC, the dot correction registers are updated.

OUT_n Enable

All OUT_n channels can be collectively switched off with one signal. When OEN is set to 1, all OUT_n channels are disabled, regardless of the device logic operations. The greyscale counter is also reset when OEN is set to 1.

When OEN is set to 0, all OUT_n channels are in normal operation.

Table 6. Pin OEN Truth Table

| OEN | OUT0:OUT15 |
|-----|------------------|
| 0 | Normal Operation |
| 1 | Disabled |

Setting Maximum Channel Current

The maximum output current per channel is programmed by a single resistor, R_{IREF}, which is placed between pin IREF and GND. The voltage on pin IREF is set by an internal band gap V_{IREF} (1.27V typ). The maximum channel current is equivalent to the current flowing through R_{IREF} multiplied by a factor of 31.5. The maximum output current is calculated as:

$$I_{MAX} = \frac{V_{IREF}}{R_{IREF}} \times 31.5 \quad (EQ 1)$$

Where:

V_{IREF} = 1.27V;

R_{IREF} = User-selected external resistor.

Power Dissipation

To ensure proper operation of the device, the total power dissipation of the AS1121 must be below the power dissipation rating of the device package. Total power dissipation is calculated as:

$$PD = (V_{CC} \times I_{CC}) + (V_{OUT} \times I_{MAX} \times n \times \frac{DCn}{63} \text{ dPWM}) \quad (EQ 2)$$

Where:

V_{CC} is the device supply voltage;

I_{CC} is the device supply current;

V_{OUT} is the device OUT_n voltage when driving LED current;

I_{MAX} is the LED current adjusted by R_{IREF};

DC_n is the maximum dot correction value for OUT_n;

n is the number of OUT_n driving LED at the same time;

dPWM is the duty cycle defined by pin OEN or the greyscale PWM value.

Operating Modes

The AS1121 operates in two modes (see Table 7). Greyscale operating mode (see Figure 8 on page 11) and the shift registers are in reset state at power-up.

Table 7. Operating Modes

| Mode | Input Shift Register | Operating Mode |
|------|----------------------|--------------------------------|
| 0 | 192-bit | Greyscale PWM Mode |
| 1 | 96-bit | Dot Correction Data Input Mode |

Setting Dot Correction

The AS1121 can perform independent fine-adjustments to the output current of each channel, i.e., dot correction. Dot correction is used to adjust brightness deviations of LEDs connected to the output channels (OUT0:OUT15).

The device powers up with the following default settings: DC = 63 and GS = 4095.

The 16 channels can be individually programmed with a 6-bit word. The channel output can be adjusted in 64 steps from 0 to 100% of the maximum output current (IMAX). The output current for each OUTn channel can be calculated as:

$$I_{OUTn} = I_{MAX} \times \frac{DCn}{63} \quad (EQ 3)$$

Where:

IMAX is the maximum programmable output current for each output;

DCn is the programmed dot correction value for output (DCn = 0 to 63);

n = 0 to 15

Dot correction data are simultaneously entered for all channels. The complete dot correction data format consists of 16 x 6-bit words, which forms a 96-bit serial data packet (see Figure 5). Channel data is put on one by one, and the data is clocked in with the MSB first.

Figure 5. Dot Correction Data Packet Format

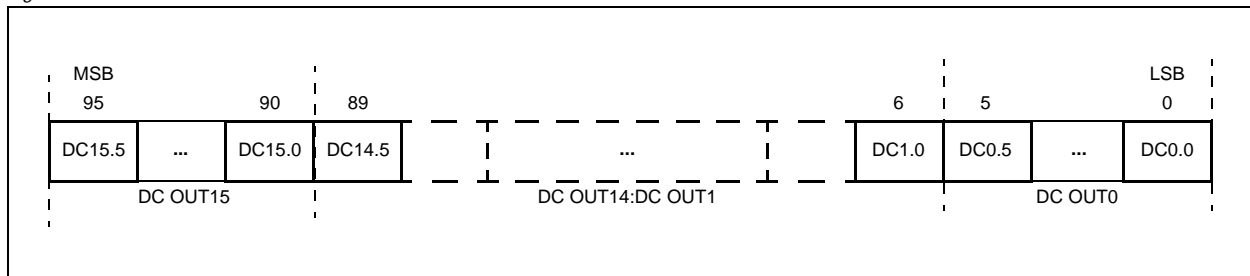
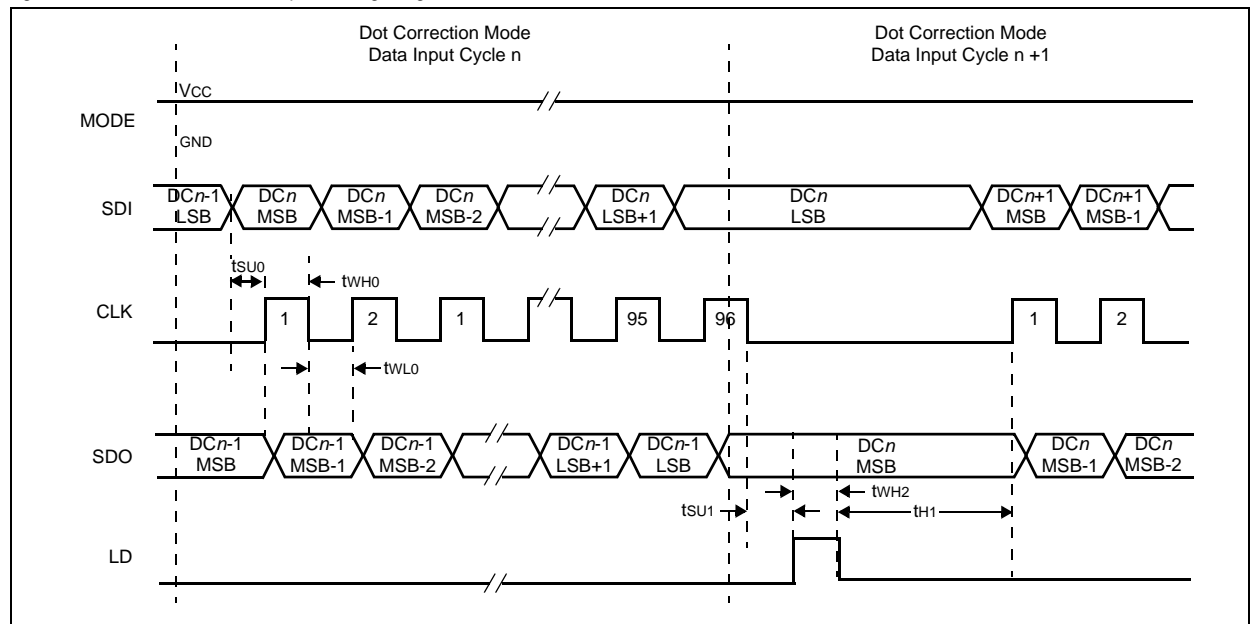


Figure 6. Dot Correction Data Input Timing Diagram



Setting Greyscale Brightness

The brightness of each channel output can be adjusted using a 12 bits-per-channel PWM control scheme which results in 4096 brightness steps, from 0% to 100% brightness. The brightness level for each output is calculated as:

$$\% \text{Brightness} = \frac{GS_n}{4095} \times 100 \quad (\text{EQ 4})$$

Where:

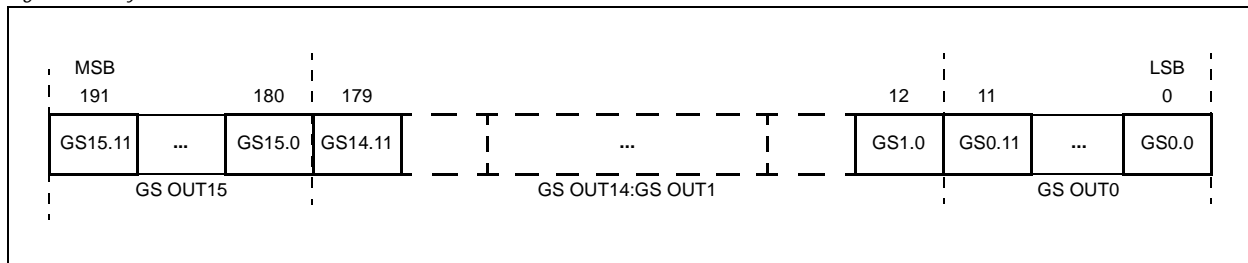
GS_n is the programmed greyscale value for OUT_n ($GS_n = 0$ to 4095);
 $n = 0$ to 15 greyscale data for all outputs.

The device powers up with the following default settings: $GS = 4095$ and $DC = 63$.

The input shift register shifts greyscale data into the greyscale register for all channels simultaneously. The complete greyscale data format consists of 16 x 12 bit words, which forms a 192-bit wide data packet (see Figure 7).

Note: The data packet must be clocked in with the MSB first.

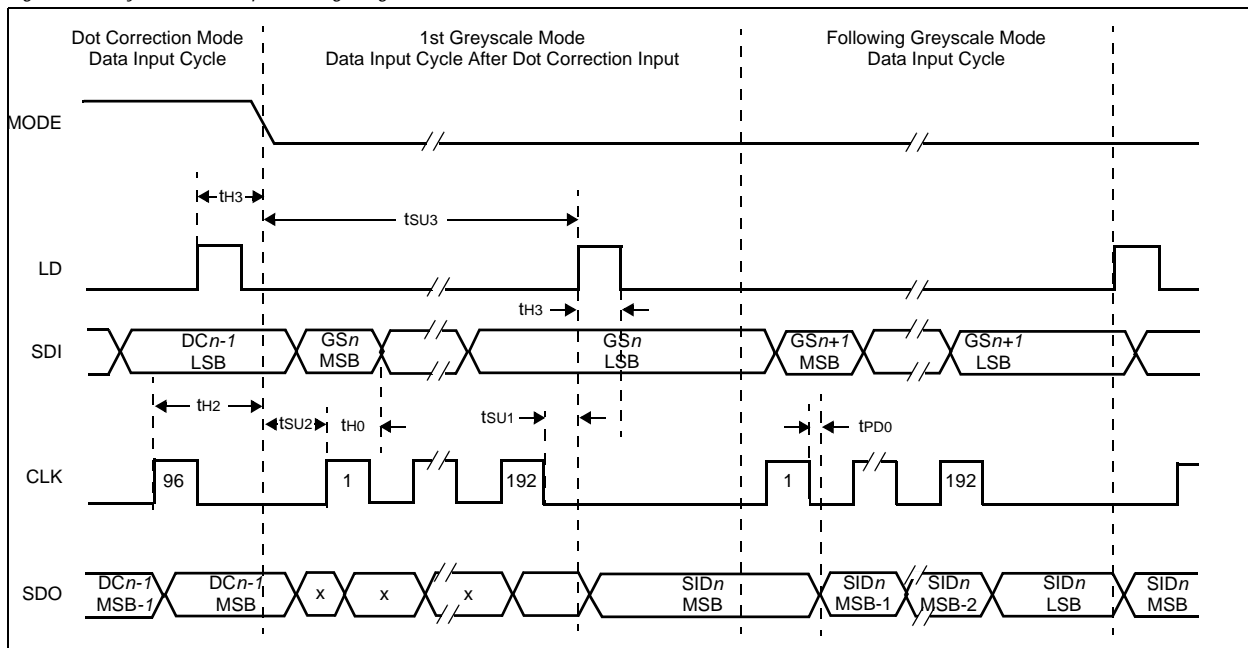
Figure 7. Greyscale Data Packet Format



When pin MODE is tied to GND, the AS1121 enters greyscale data input mode. The device switches the input shift register to 192-bit width. After all data is clocked in, the rising edge of the LD signal latches the data into the greyscale register (see Figure 8).

All greyscale data in the input shift register is replaced with status information data (SID) after latching into the greyscale register.

Figure 8. Greyscale Data Input Timing Diagram

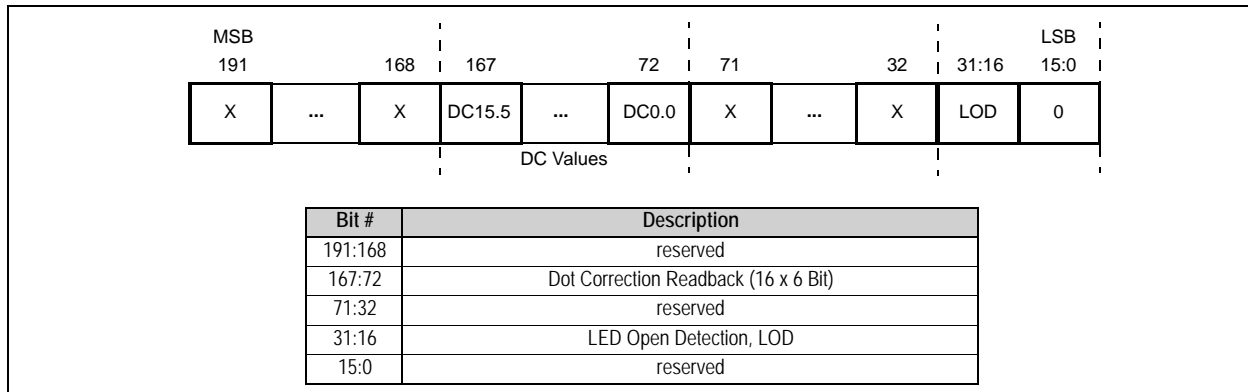


Status Information Data (SID)

The AS1121 contains an integrated status information register, which can be accessed in greyscale mode (MODE = GND). Once the LD signal latches the data into the greyscale register, the input shift register data is replaced with status information data (see Figure 9).

The Open LED information as well as the dot-correction registers can be read out at pin SDO. The status information data packet is 192 bits wide. Bits 31:16 contain the open LED detection status of each channel. Bits 167:72 contain the data of the dot-correction register. The remaining bits are reserved. The complete status information data packet is shown in Figure 9.

Figure 9. Status Information Data Packet Format

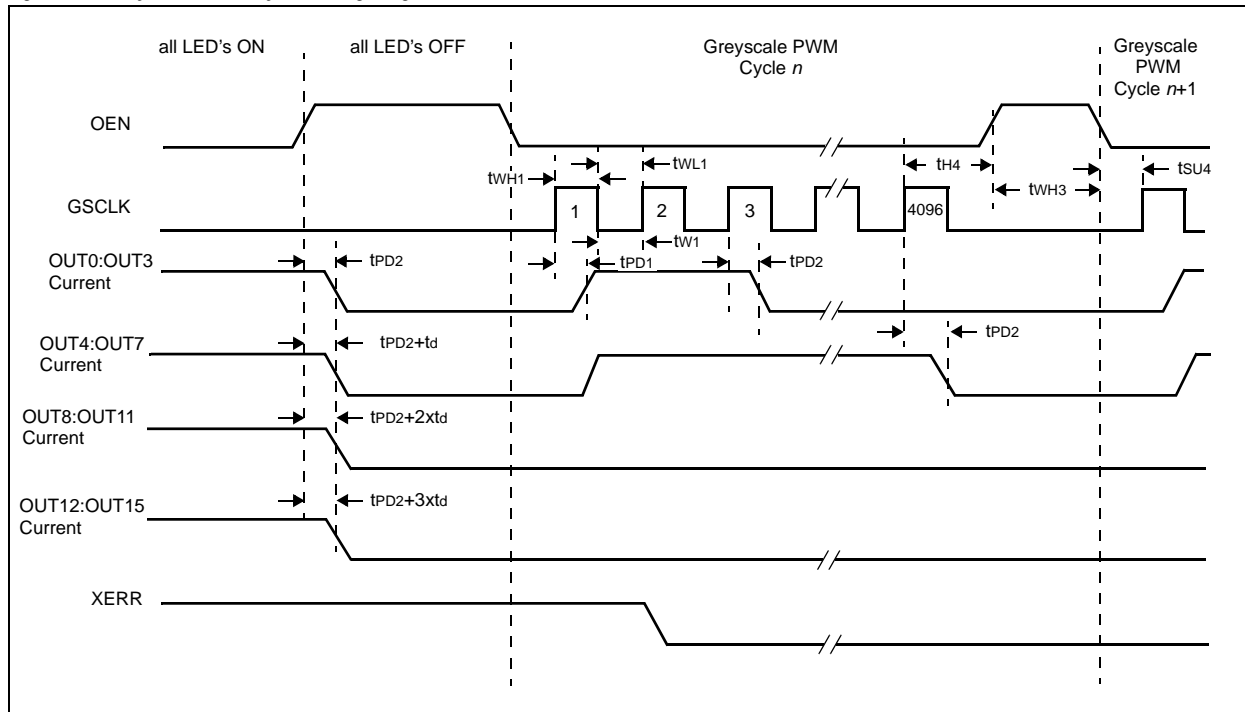


Greyscale PWM Operation

The falling edge of the OEN signal initiates a greyscale PWM cycle. The first GSCLK pulse after the falling edge of OEN increments the greyscale counter by one and switches on any OUT_n whose greyscale value does not equal zero. Each subsequent rising edge of GSCLK increments the greyscale counter by one.

The AS1121 compares the greyscale value of each OUT_n channel with the greyscale counter value. All OUT_n whose greyscale values equal the counter values are switched off. A $OEN = 1$ signal after 4096 GSCLK pulses resets the greyscale counter to zero and completes a greyscale PWM cycle (see Figure 10).

Figure 10. Greyscale PWM Cycle Timing Diagram



Output Delay

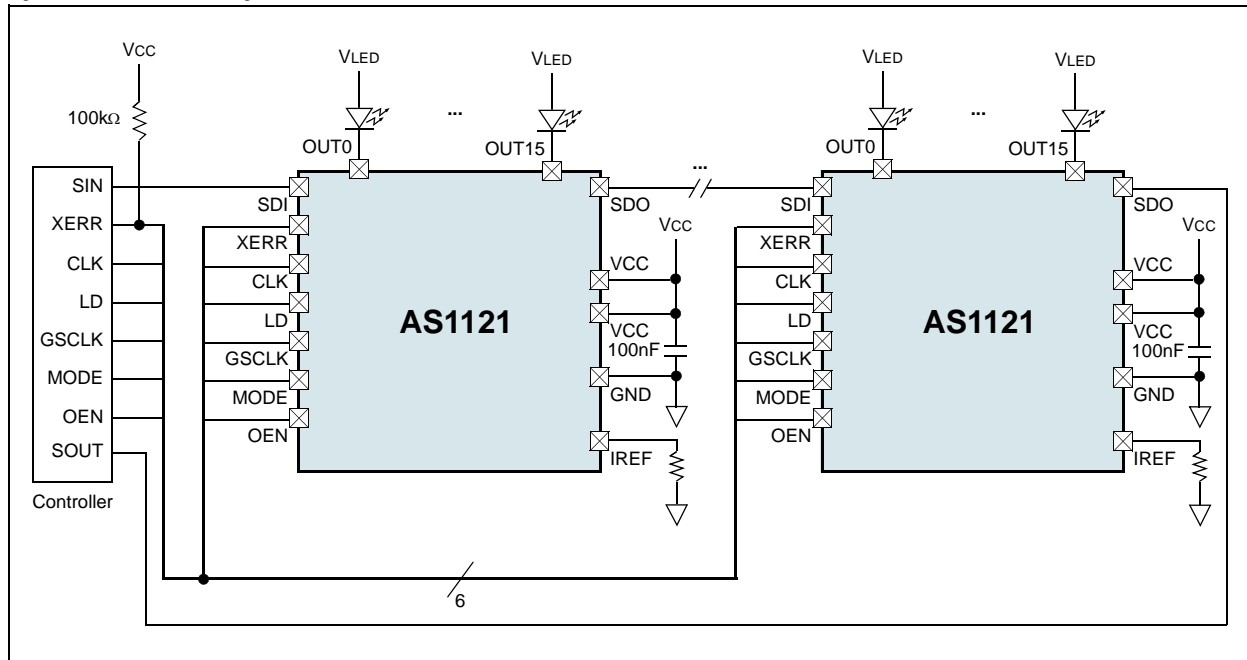
To minimize the ripple on the inrush current, the outputs are delayed and are not switching at the same time. The 16 channels of the AS1121 are combined in groups of 4. The channels within the groups OUT0:OUT3, OUT4:OUT7, OUT8:OUT11, OUT12:OUT15 are switching at the same time. Between the 4 groups a delay of $t_d = 25\text{ns}$ (typ.) is implemented. On request this delay can be turned off (see Ordering Information on page 17).

To increase the EMI performance the rising and falling edges of the OUT_n signals are symmetrical ($t_R = t_F = 25\text{ns}$). The rise- and fall-times are factory set and can be changed on request. For further information and requests, please contact us <mailto:sales@austriamicrosystems.com>.

Serial Data Transfer Rate

Figure 11 shows a cascaded arrangement AS1121 devices connected to a controller, building a basic module of an LED display system.

Figure 11. Cascaded Configuration



The maximum number of cascading AS1121 devices depends on the application system and is in the range of 40 devices. The minimum frequency needed can be calculated by the following equations:

$$f_{GSCLK} = 4096 \times f_{UPDATE} \quad (EQ 5)$$

Where:

f_{GSCLK} is the minimum frequency needed for GSCLK;
 f_{UPDATE} is the update rate of whole cascaded system.

$$f_{CLK} = 193 \times f_{UPDATE} \times n \quad (EQ 6)$$

Where:

f_{CLK} is the minimum frequency needed for CLK and SIN;
 f_{UPDATE} is the update rate of whole cascaded system;
 n is the number of cascaded of AS1121 devices.

8 Package Drawings and Markings

Figure 12. 32-pin TQFN 5x5 mm Marking

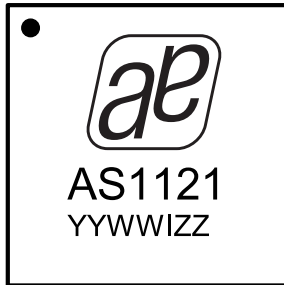
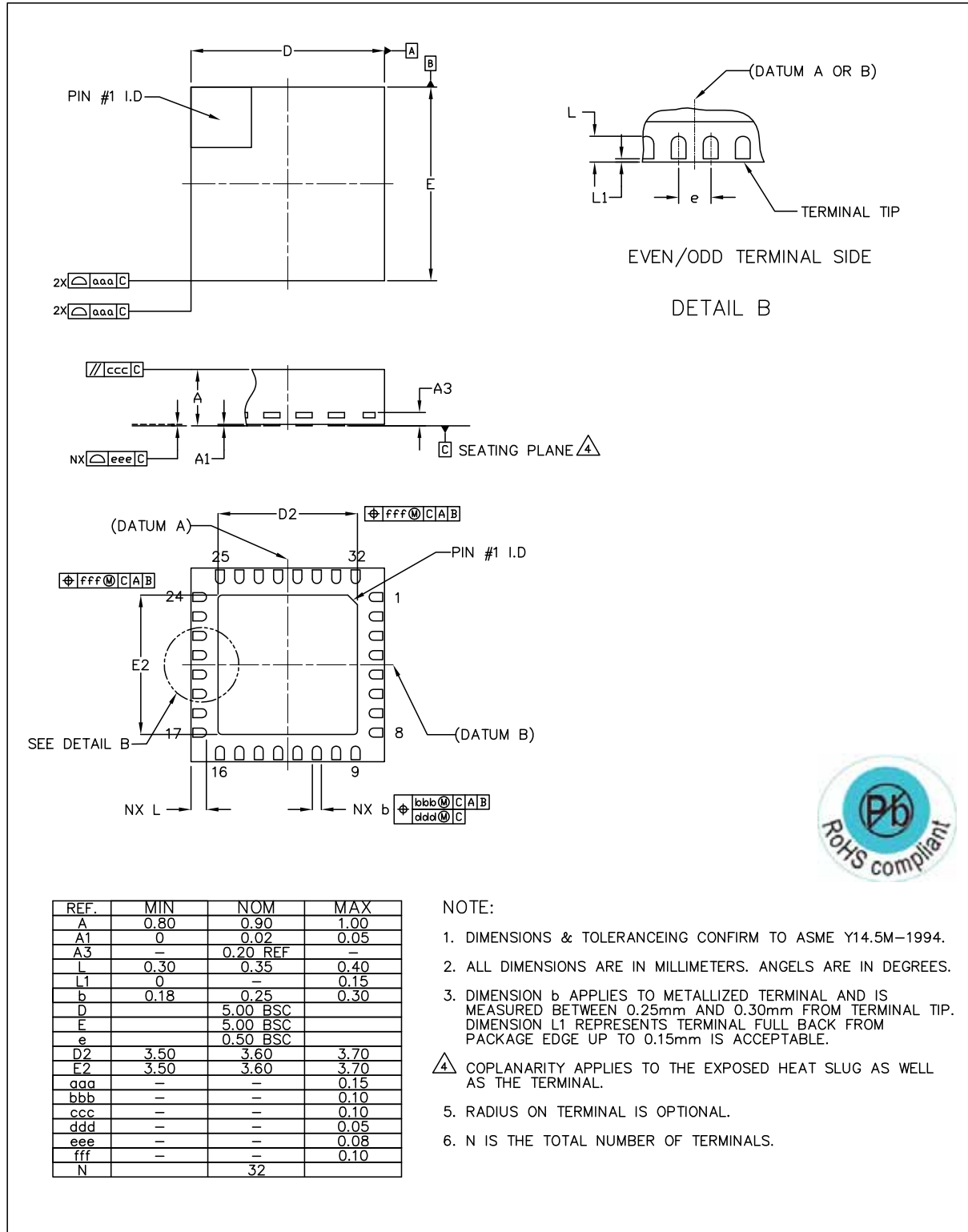


Figure 13. Packaging Code YYWWIZZ

| YY | WW | I | ZZ |
|-------------------------------------|--------------------|------------------|---------------------------------|
| last two digits of the current year | manufacturing week | plant identifier | free choice / traceability code |

Figure 14. 32-pin TQFN 5x5 mm Package



| | | | | | |
|------------------------|--|--------------------|---|--|---|
| | | | ASSEMBLY ENGINEERING | | |
| a leap ahead in analog | | | TITLE SAWN QFN, PULL BACK, 5x5x0.9mm 32 LEAD, 3.60mm SQ. ePAD | | |
| DRAWN RHB | | DATE 2010.10.29 | REV. N/C | | REFERENCE DOCUMENT JEDEC MO - 220 LATEST REVISION |
| CHECKED GBO | | DATE 2010.10.29 | DRAWING NO. QRK | | UNIT |
| APPROVED MKR | | DATE 2010.10.29 | SHEET 1 OF 1 | | SCALE NOT IN SCALE |

9 Ordering Information

The device is available as the standard products shown in [Table 8](#).

Table 8. Ordering Information

| Ordering Code | Marking | Description | Delivery Form | Package |
|---------------|---------|--|---------------|--------------------|
| AS1121-BQFT | AS1121 | 16-Channel LED Driver with Dot Correction and Greyscale PWM | Tape and Reel | 32-pin TQFN 5x5 mm |
| AS1121B-BQFT* | AS1121B | 16-Channel LED Driver with Dot Correction and Greyscale PWM without Output Delay | Tape and Reel | 32-pin TQFN 5x5 mm |

*) on request

Note: All products are RoHS compliant.

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