ADNS-5020
Optical Mouse Sensor

Data Sheet

Description

The Avago Technologies ADNS-5020 is an entry-level, small form factor optical mouse sensor. It comes with many built-in features and optimized for LED-based corded products.

The ADNS-5020 is capable of high-speed motion detection – up to 14 ips and 2G. In addition, it has an on-chip oscillator and built-in LED driver to minimize external components. Frame rate is also adjusted internally.

The ADNS-5020 along with the ADNS-5100/ADNS-5100-00 lens, ADNS-5200 clip and HLMP-ED80 LED form a complete and compact mouse tracking system. There are no moving parts, which means high reliability and less maintenance for the end user. In addition, precision optical alignment is not required, facilitating high volume assembly.

The sensor is programmed via registers through a three-wire SPI interface. It is housed in an 8-pin staggered dual in-line package (DIP).

Theory of Operation

The ADNS-5020 is based on Optical Navigation Technology, which measures changes in position by optically acquiring sequential surface images (frames) and mathematically determining the direction and magnitude of movement.

The ADNS-5020 contains an Image Acquisition System (IAS), a Digital Signal Processor (DSP), and a three wire serial port.

The IAS acquires microscopic surface images via the lens and illumination system. These images are processed by the DSP to determine the direction and distance of motion. The DSP calculates the Δx and Δy relative displacement values.

An external microcontroller reads the Δx and Δy information from the sensor serial port. The microcontroller then translates the data into PS2 or USB signals before sending them to the host PC.

Features

- Small form factor
- Built-in LED driver for simpler circuitry
- High speed motion detection up to 14 ips and 2G
- Self-adjusting frame rate for optimum performance
- Internal oscillator – no clock input needed
- Selectable 500 and 1000 cpi resolution
- Operating voltage: 5 V nominal
- Three-wire serial interface
- Minimal number of passive components

Applications

- Optical mice
- Optical trackballs
- Integrated input devices

Pinout of ADNS-5020 Optical Mouse Sensor

Pin	Name	Description
1	SDIO	Serial Port Data Input and Output
2	XY_LED	LED Control
3	NRESET	Reset Pin (active low input)
4	NCS	Chip Select (active low input)
5	VDD5	Supply Voltage
6	GND	Ground
7	REGO	Regulator Output
8	SCLK	Serial Clock Input

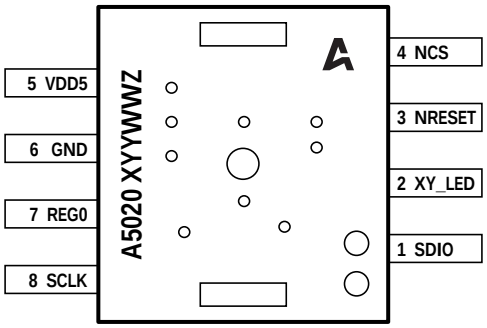
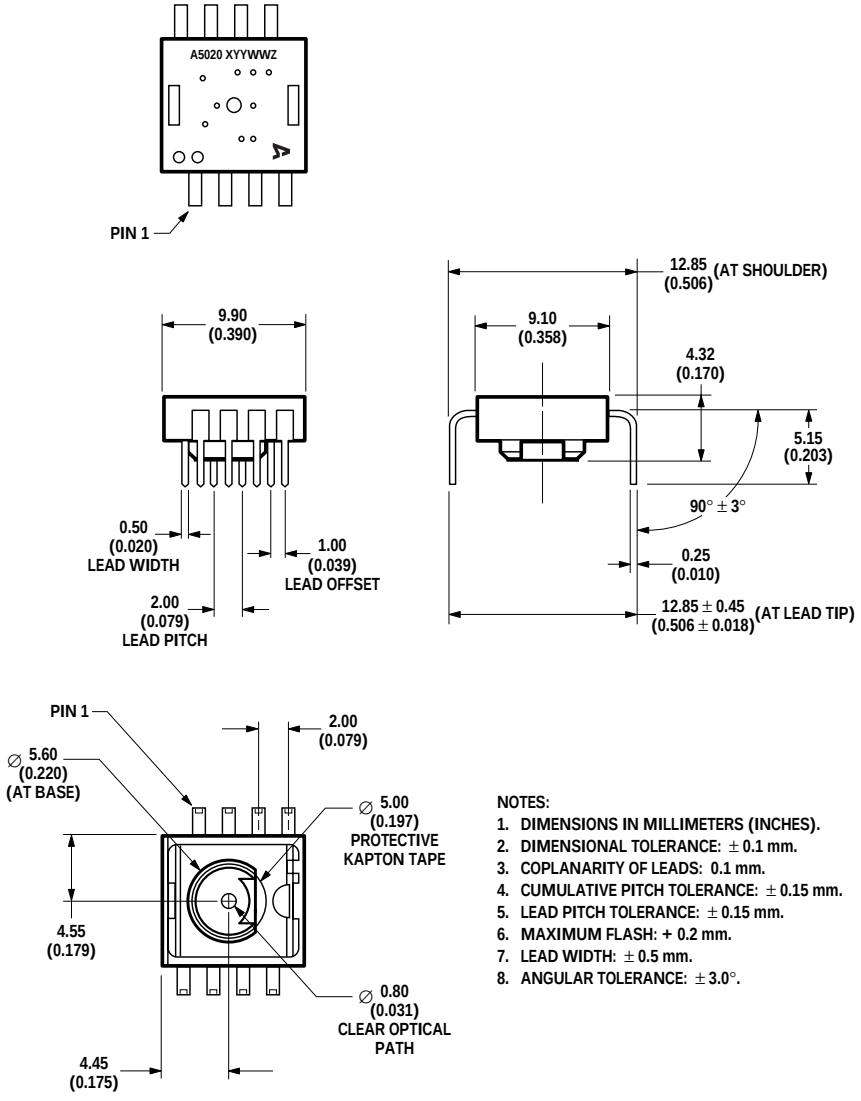


Figure 1. Package outline drawing (top view).



NOTES:
1. DIMENSIONS IN MILLIMETERS (INCHES).
2. DIMENSIONAL TOLERANCE: ± 0.1 mm.
3. COPLANARITY OF LEADS: 0.1 mm.
4. CUMULATIVE PITCH TOLERANCE: ± 0.15 mm.
5. LEAD PITCH TOLERANCE: ± 0.15 mm.
6. MAXIMUM FLASH: + 0.2 mm.
7. LEAD WIDTH: ± 0.5 mm.
8. ANGULAR TOLERANCE: ± 3.0°.

Figure 2. Package outline drawing.

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Overview of Optical Mouse Sensor Assembly

Avago Technologies provides an IGES file drawing describing the base plate molding features for lens and PCB alignment.

The ADNS-5020 sensor is designed for mounting on a through-hole PCB, looking down. There is an aperture stop and features on the package that align to the lens.

The ADNS-5100/5100-001 lens provides optics for the imaging of the surface as well as illumination of the surface at the optimum angle. Features on the lens align it to the sensor, base plate, and clip with the LED.

The ADNS-5200 clip holds the LED in relation to the lens. The LED must be inserted into the clip and the LED's leads formed prior to loading on the PCB.

The HLMP-ED80 LED is recommended for illumination.

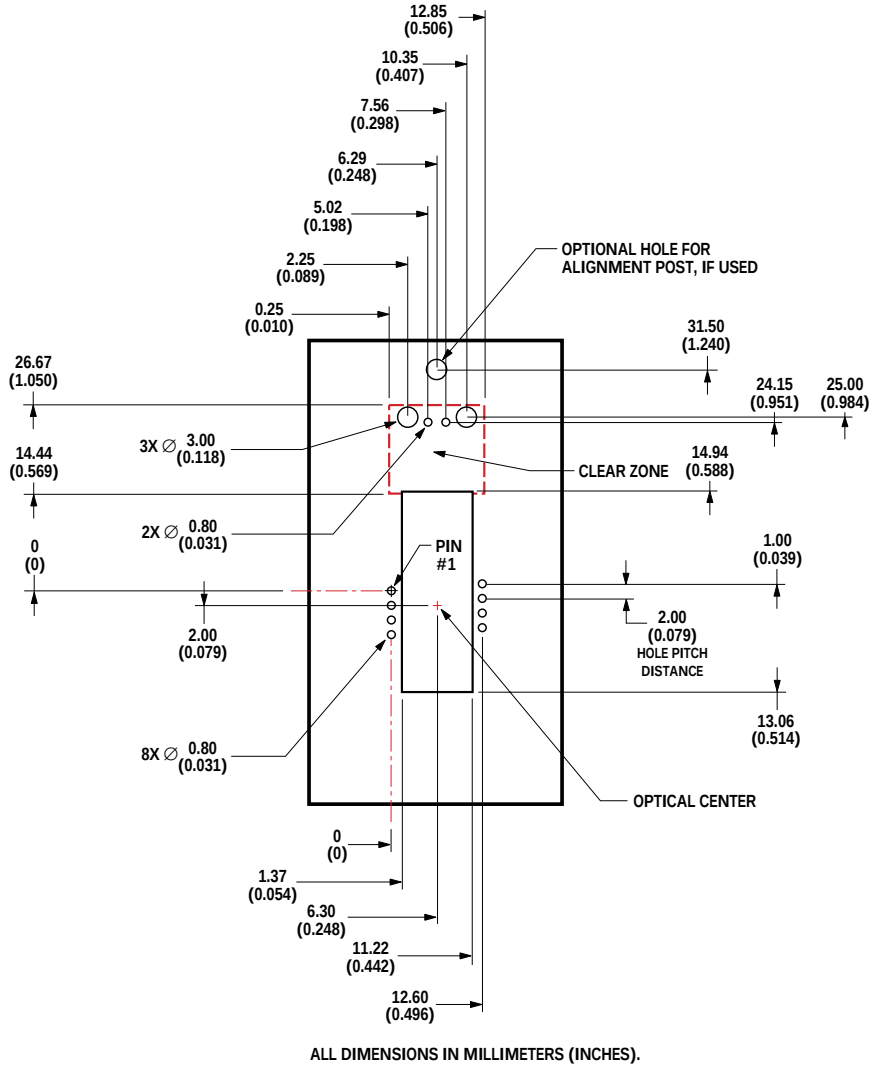


Figure 3. Recommended PCB mechanical cutouts and spacing.

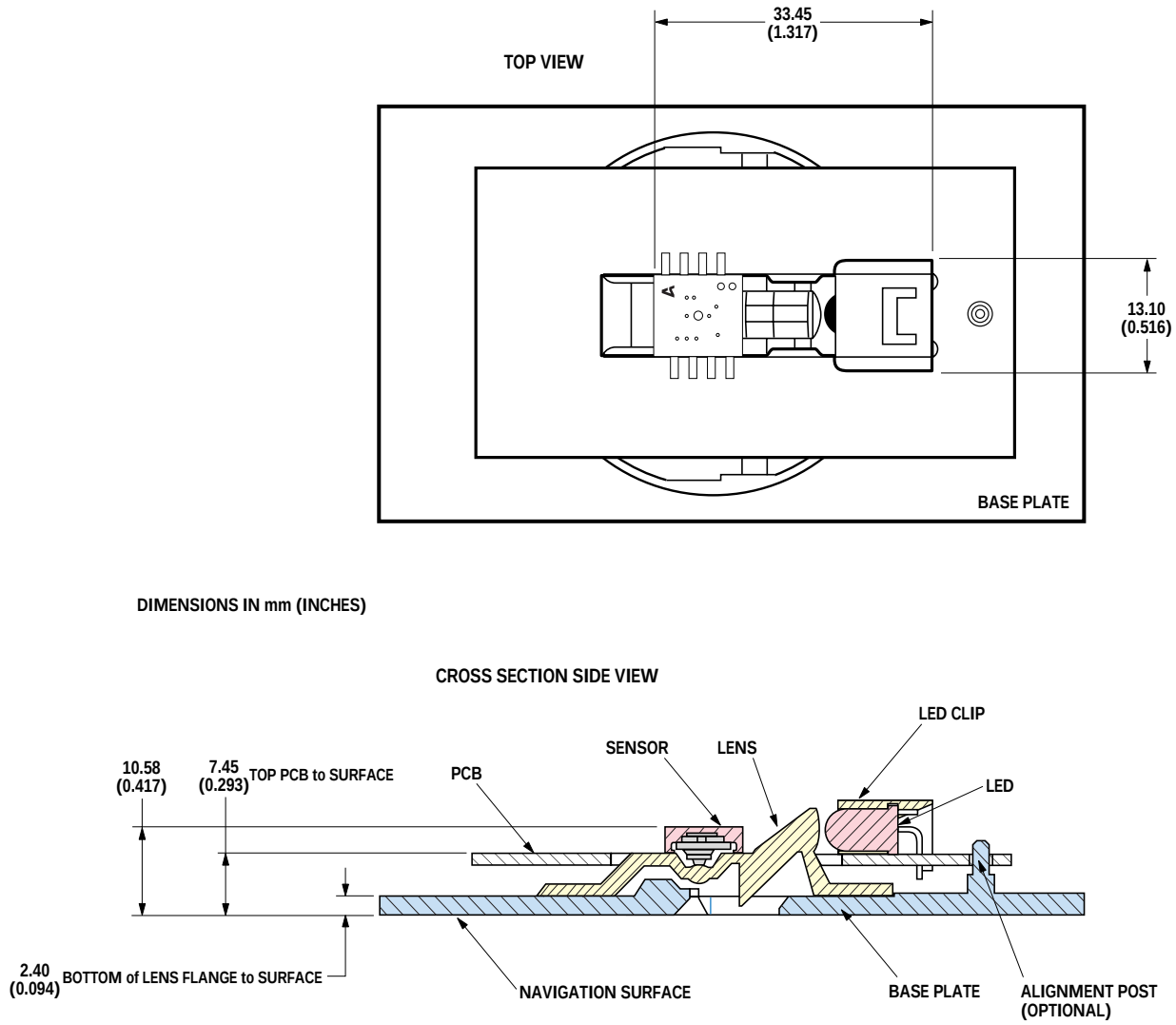


Figure 4. 2D Assembly drawing of ADNS-5020 (top and side views).

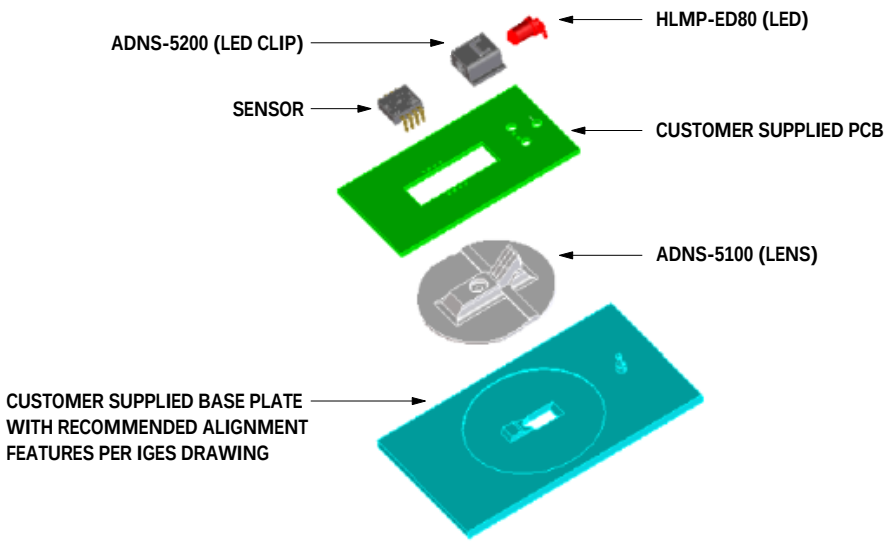


Figure 5. Exploded view drawing.

PCB Assembly Considerations

1. Insert the sensor and all other electrical components into PCB.
2. Insert the LED into the assembly clip and bend the leads 90 degrees.
3. Insert the LED clip assembly into PCB.
4. Wave solder the entire assembly in a no-wash solder process utilizing solder fixture. The solder fixture is needed to protect the sensor during the solder process. It also sets the correct sensor-to-PCB distance as the lead shoulders do not normally rest on the PCB surface. The fixture should be designed to expose the sensor leads to solder while shielding the optical aperture from direct solder contact.
5. Place the lens onto the base plate.
6. Remove the protective kapton tape from optical aperture of the sensor. Care must be taken to keep contaminants from entering the aperture. Recommend not to place the PCB facing up during the entire mouse assembly process. Recommend to hold the PCB first vertically for the kapton removal process.
7. Insert PCB assembly over the lens onto the base plate aligning post to retain PCB assembly. The sensor aperture ring should self-align to the lens.
8. The optical position reference for the PCB is set by the base plate and lens. Note that the PCB motion due to button presses must be minimized to maintain optical alignment.
9. Install mouse top case. There MUST be a feature in the top case to press down onto the PCB assembly to ensure all components are interlocked to the correct vertical height.

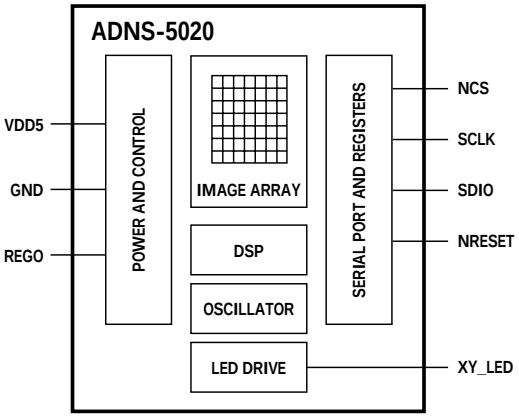


Figure 6. Block diagram of ADNS-5020 optical mouse sensor.

Design Considerations for Improved ESD Performance

For improved electrostatic discharge performance, typical creepage and clearance distance are shown in the table below. Assumption: base plate construction as per the Avago Technologies supplied IGES file and ADNS-5100/5100-001 lens.

Typical Distance	Millimeters
Creepage	16.0
Clearance	2.1

Note that the lens material is polycarbonate and therefore, cyanoacrylate based adhesives or other adhesives that may damage the lens should **NOT** be used.

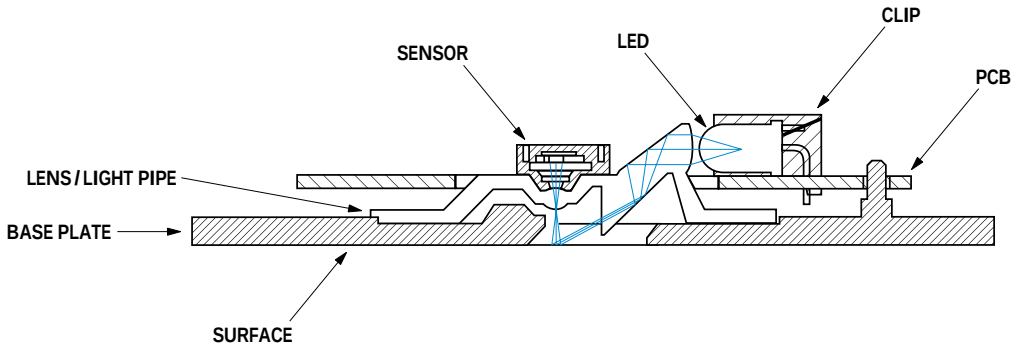


Figure 7. Sectional view of PCB assembly highlighting optical mouse components.

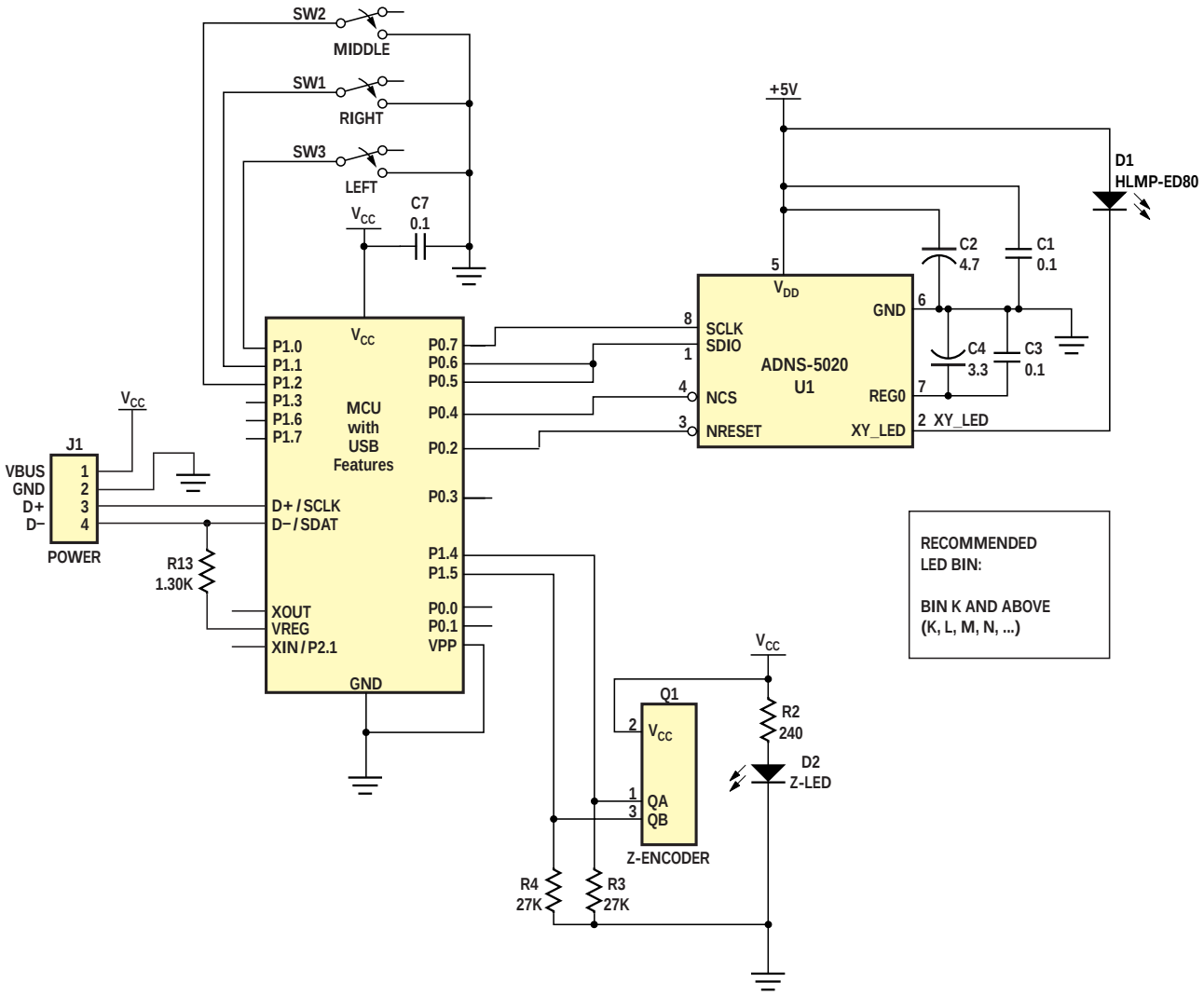


Figure 8. Schematic diagram for interface between ADNS-5020 and microcontroller.

Regulatory Requirements

- Passes FCC B and worldwide analogous emission limits when assembled into a mouse with shielded cable and following Avago Technologies recommendations.
- Passes IEC-1000-4-3 radiated susceptibility level when assembled into a mouse with shielded cable and following Avago Technologies recommendations.
- Passes EN61000-4-4/IEC801-4 EFT tests when assembled into a mouse with shielded cable and following Avago Technologies recommendations.
- UL flammability level UL94 V-0.
- Provides sufficient ESD creepage/clearance distance to avoid discharge up to 15 kV when assembled into a mouse using ADNS-5100 round lens according to usage instructions above.

Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units	Notes
Storage Temperature	T_S	-40	85	℃	
Lead Solder Temp			260	℃	
Supply Voltage	V_{DD}	-0.5	5.5	V	
ESD			2	kV	All pins, human body model MIL 883 Method 3015
Input Voltage	V_{IN}	-0.5	V_{DD}+0.5	V	All I/O pins
Output Current	Iout		7	mA	SDIO pin

Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Operating Temperature	T_A	0		40	℃	
Power Supply	V_{DD}	4.0	5.0	5.25	V	
Power Supply Rise Time	V_{RT}	0.005		100	ms	0 to V_{DD}
Supply Noise (Sinusoidal)	V_{NA}			100	mV p-p	10 kHz-50 MHz
Serial Port Clock Frequency	f_{SCLK}			1	MHz	50% duty cycle.
Distance from Lens Reference Plane to Tracking Surface (Z)	Z	2.3	2.4	2.5	mm	
Speed	S			14	ips	
Acceleration	a			2	G	
Load Capacitance	C_{out}			100	pF	SDIO

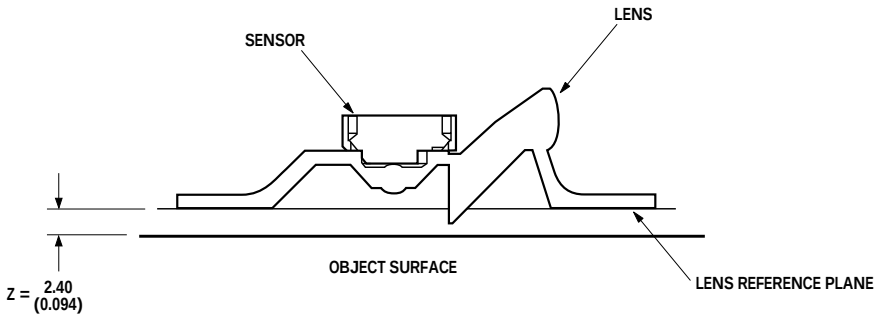


Figure 9. Distance from lens reference plane to tracking surface (Z).

AC Electrical Specifications

Electrical Characteristics over recommended operating conditions. Typical values at 25 °C, V_{DD} = 5.0 V.

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Reset Pulse Width	t_{RESET}	250			ns	Active low.
Motion Delay after Reset	$t_{MOT-RST}$			50	ms	From NRESET pull high to valid motion, assuming V_{DD} and motion is present.
SDIO Rise Time	t_{r-SDIO}		150	300	ns	C_L = 100pF
SDIO Fall Time	t_{f-SDIO}		150	300	ns	C_L = 100pF
SDIO delay after SCLK	$t_{DLY-SDIO}$			120	ns	From SCLK falling edge to SDIO data valid, no load conditions.
SDIO Hold Time	$t_{hold-SDIO}$	0.5		$1/f_{SCLK}$	us	Data held until next falling SCLK edge.
SDIO Setup Time	$t_{setup-SDIO}$	120			ns	From data valid to SCLK rising edge.
SPI Time between Write Commands	t_{SWW}	30			µs	From rising SCLK for last bit of the first data byte, to rising SCLK for last bit of the second data byte.
SPI Time between Write and Read Commands	t_{SWR}	20			µs	From rising SCLK for last bit of the first data byte, to rising SCLK for last bit of the second address byte.
SPI Time between Read and Subsequent Commands	t_{SRW} t_{SRR}	500			ns	From rising SCLK for last bit of the first data byte, to falling SCLK for the first bit of the next address.
SPI Read Address-Data Delay	t_{SRAD}	4			µs	From rising SCLK for last bit of the address byte, to falling SCLK for first bit of data being read.
NCS Inactive after Motion Burst	t_{BEXIT}	250			ns	Minimum NCS inactive time after motion burst before next SPI usage.
NCS to SCLK Active	$t_{NCS-SCLK}$	120			ns	From NCS falling edge to first SCLK rising edge.
SCLK to NCS Inactive (for read operation)	$t_{SCLK-NCS}$	120			ns	From last SCLK rising edge to NCS rising edge, for valid SDIO data transfer.
SCLK to NCS Inactive (for write operation)	$t_{SCLK-NCS}$	20			us	From last SCLK rising edge to NCS rising edge, for valid SDIO data transfer.
NCS to SDIO High-Z	$t_{NCS-SDIO}$			500	ns	From NCS rising edge to SDIO high-Z state.
Transient Supply Current	I_{DDT}			60	mA	Max supply current during a V_{DD} ramp from 0 to V_{DD}.

DC Electrical Specifications

Electrical Characteristics over recommended operating conditions. Typical values at 25 °C, V_{DD} = 5.0 V.

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
DC Supply Current	I_{DD_AVG}		3.6	6	mA	Average sensor current, at max frame rate. No load on SDIO.
Idle Supply Current			2		mA	
Input Low Voltage	V_{IL}			0.5	V	SCLK, SDIO, NCS, NRESET
Input High Voltage	V_{IH}	V_{DD} – 0.5			V	SCLK, SDIO, NCS, NRESET
Input Hysteresis	V_{I_HYS}		200		mV	SCLK, SDIO, NCS, NRESET
Input Leakage Current	I_{leak}		±1	±10	µA	Vin = VDD-0.6 V, SCLK, SDIO, NCS, NRESET
XY_LED Current	I_{XY_LED}		29		mA	XY_LED pin voltage range should be greater than 0.8 V.
Output Low Voltage	V_{OL}			0.7	V	I_{out} = 1 mA, SDIO
Output High Voltage	V_{OH}	VDD-0.7			V	I_{out} = -1 mA, SDIO
Input Capacitance	C_{in}		50		pF	NCS, SCLK, SDIO, NRESET

Typical Performance Characteristics

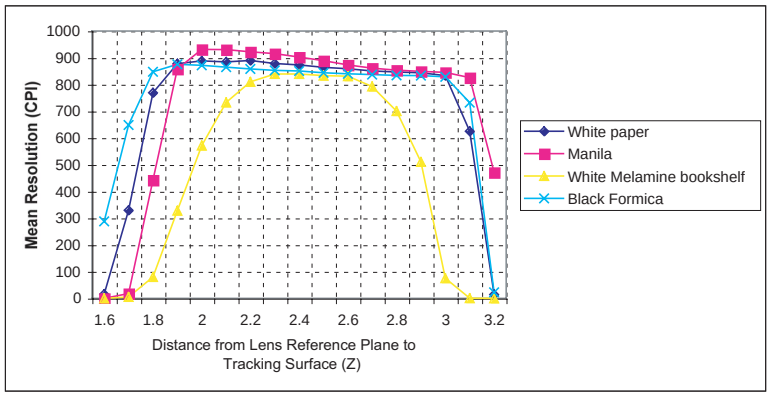


Figure 10. Mean resolution vs. distance from lens reference plane to surface.

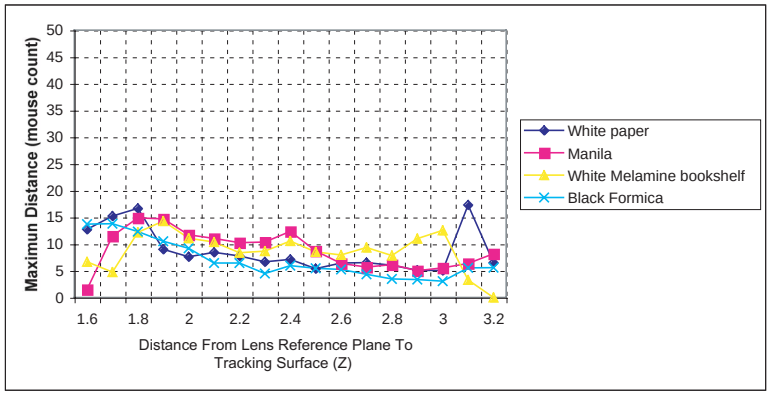


Figure 11. Average error vs. distance (mm).

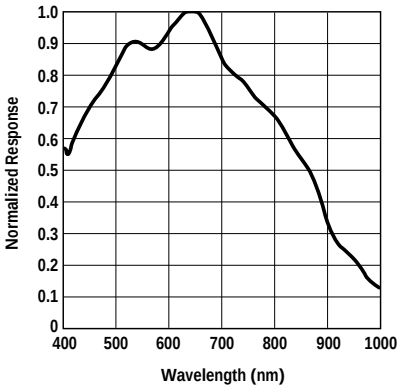


Figure 12. Relative wavelength responsivity.

LED Mode

For power savings, the LED will not be continuously on. ADNS-5020 will pulse the LED only when needed.

Synchronous Serial Port

The synchronous serial port is used to set and read parameters in the ADNS-5020, and to read out the motion information.

The port is a three wire serial port. The host micro-controller always initiates communication; the ADNS-5020 never initiates data transfers. SCLK, SDIO, and NCS may be driven directly by a micro-controller. The port pins may be shared with other SPI slave devices. When the NCS pin is high, the inputs are ignored and the output is tri-stated.

The lines that comprise the SPI port:

SCLK: Clock input. It is always generated by the master (the micro-controller).

SDIO: Input and Output data.

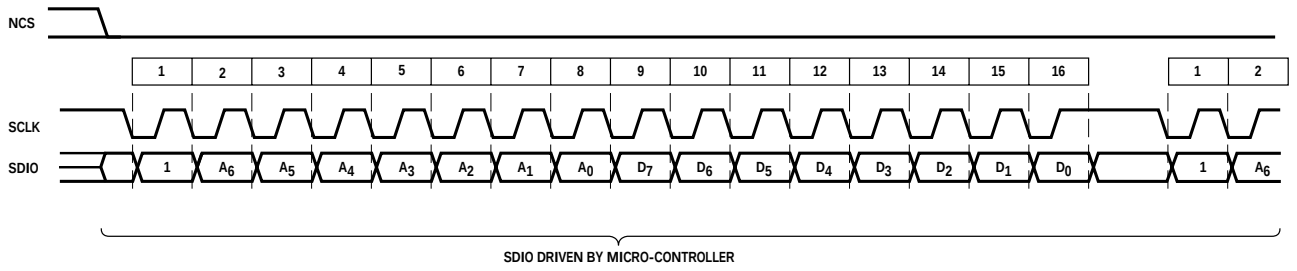
NCS: Chip select input (active low). NCS needs to be low to activate the serial port; otherwise, SDIO will be high Z, and SDIO & SCLK will be ignored. NCS can also be used to reset the serial port in case of an error.

Chip Select Operation

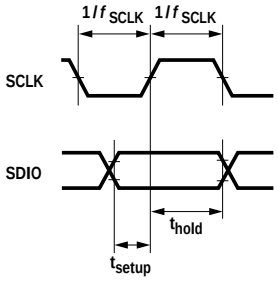
The serial port is activated after NCS goes low. If NCS is raised during a transaction, the entire transaction is aborted and the serial port will be reset. This is true for all transactions. After a transaction is aborted, the normal address-to-data or transaction-to-transaction delay is still required before beginning the next transaction. To improve communication reliability, all serial transactions should be framed by NCS. In other words, the port should not remain enabled during periods of non-use because ESD and EFT/B events could be interpreted as serial communication and put the chip into an unknown state. In addition, NCS must be raised after each burst-mode transaction is complete to terminate burst-mode. The port is not available for further use until burst-mode is terminated.

Write Operation

Write operation, defined as data going from the micro-controller to the ADNS-5020, is always initiated by the micro-controller and consists of two bytes. The first byte contains the address (seven bits) and has a “1” as its MSB to indicate data direction. The second byte contains the data. The ADNS-5020 reads SDIO on rising edges of SCLK.



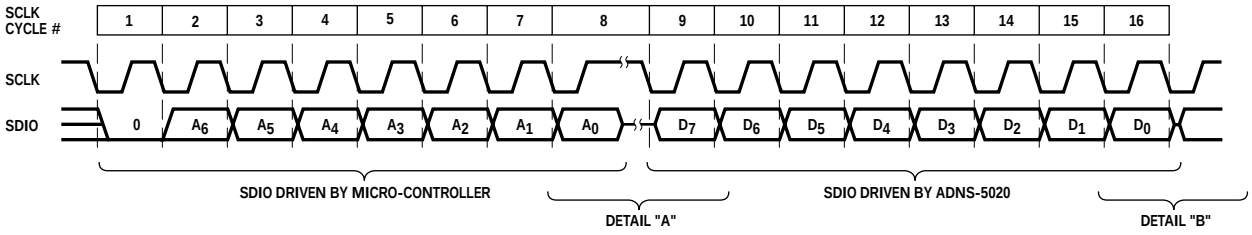
Write Operation



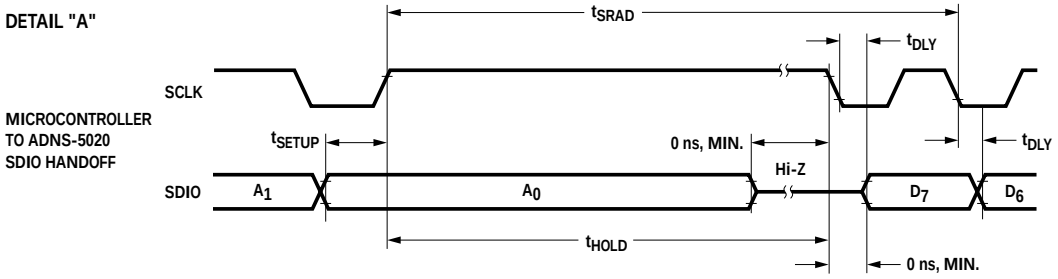
SDIO Setup and Hold Time

Read Operation

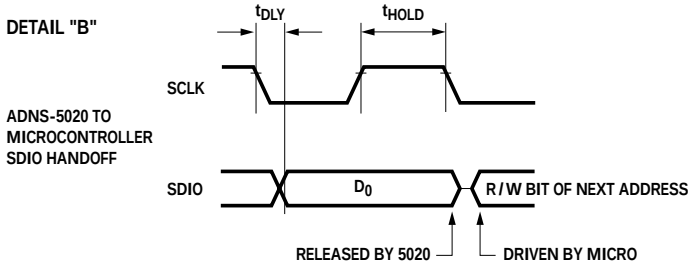
A read operation, defined as data going from the ADNS-5020 to the micro-controller, is always initiated by the micro-controller and consists of two bytes. The first byte contains the address, is sent by the micro-controller over SDIO, and has a “0” as its MSB to indicate data direction. The second byte contains the data and is driven by the ADNS-5020 over SDIO. The sensor outputs SDIO bits on falling edges of SCLK and samples SDIO bits on every rising edge of SCLK.



Read Operation



Microcontroller to ADNS-5020 Handoff

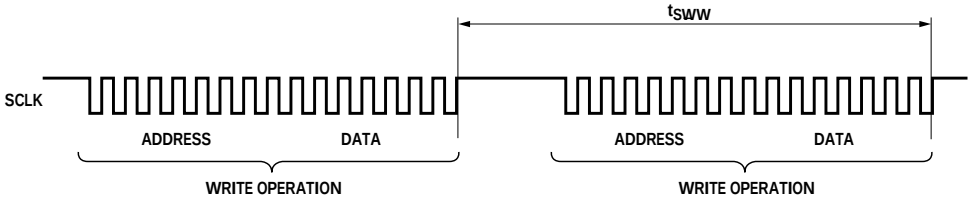


ADNS-5020 to Microcontroller Handoff

NOTE: The $0.5/f_{SCLK}$ minimum high state of SCLK is also the minimum SDIO data hold time of the ADNS-5020. Since the falling edge of SCLK is actually the start of the next read or write command, the ADNS-5020 will hold the state of data on SDIO until the falling edge of SCLK.

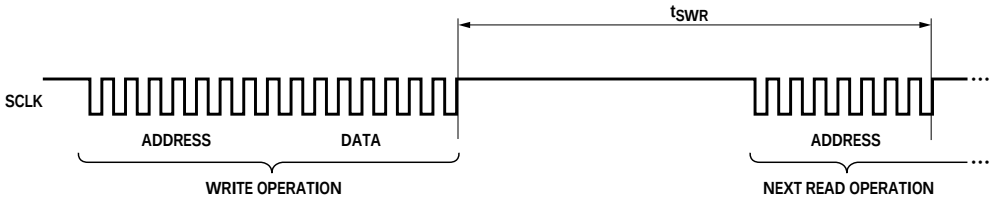
Required Timing between Read and Write Commands

There are minimum timing requirements between read and write commands on the serial port.



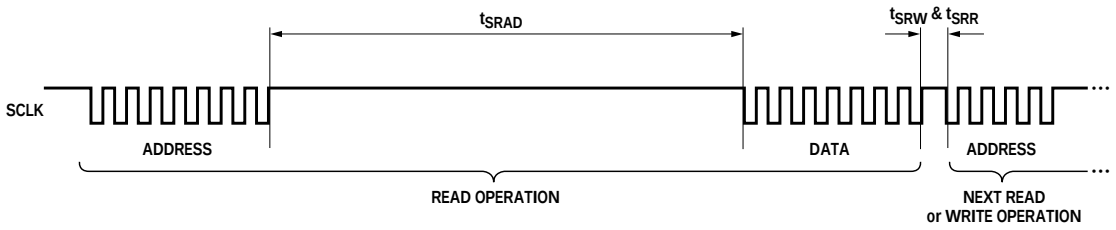
Timing between Two Write Commands

If the rising edge of the SCLK for the last data bit of the second write command occurs before the required delay (t_{SWW}), then the first write command may not complete correctly.



Timing between Write and Read Commands

If the rising edge of SCLK for the last address bit of the read command occurs before the required delay (t_{SWR}), the write command may not complete correctly.



Timing between Read and Either Write or Subsequent Read Commands

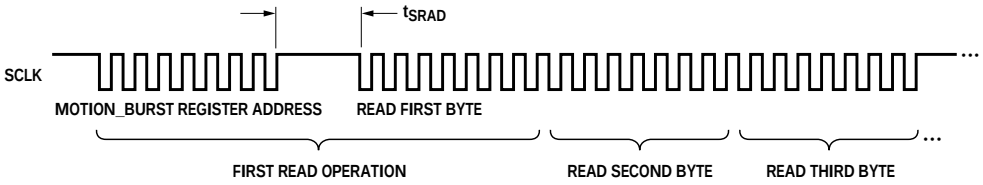
During a read operation SCLK should be delayed at least t_{SRAD} after the last address data bit to ensure that the ADNS-5020 has time to prepare the requested data. The falling edge of SCLK for the first address bit of either the read or write command must be at least t_{SRR} or t_{SRW} after the last SCLK rising edge of the last data bit of the previous read operation.

Burst Mode Operation

Burst mode is a special serial port operation mode that may be used to reduce the serial transaction time for a motion read. The speed improvement is achieved by continuous data clocking to or from multiple registers without the need to specify the register address, and by not requiring the normal delay period between data bytes.

Burst mode is activated by reading the Motion_Burst register. The ADNS-5020 will respond with the contents of the Delta_X, Delta_Y, SQUAL, Shutter_Upper, Shutter_Lower, Maximum_Pixel and Pixel_Sum registers in that order. The burst transaction can be terminated anywhere in the sequence after the Delta_X value by bringing the NCS pin high. After sending the register address, the micro-controller must wait t_{SRAD} and then begin reading data. All data bits can be read with no delay between bytes by driving SCLK at the normal rate. The data are latched into the output buffer after the last address bit is received. After the burst transmission is complete, the micro-controller must raise the NCS line for at least t_{BEXIT} to terminate burst mode. The serial port is not available for use until it is reset with NCS, even for a second burst transmission.

Avago Technologies highly recommends the usage of burst mode operation in optical mouse sensor design applications.



Motion Burst Timing

Notes on Power-up and Reset

The ADNS-5020 does not perform an internal power up self-reset; the NRESET pin must be asserted low every time power is applied. There are two ways to reset the chip, either assert low NRSET pin or by writing 0x5a to register 0x3a. A full reset will thus be executed. Any register settings must then be reloaded.

During power-up there will be a period of time after the power supply is high but before any clocks are available. The table below shows the state of the various pins during power-up and reset.

State of Signal Pins After VDD is Valid

Pin	During Reset	After Reset
NCS	Ignored	Functional
SDIO	Ignored	Depends on NCS
SCLK	Ignored	Depends on NCS
XY_LED	Hi-Z	Functional

Registers

The ADNS-5020 registers are accessible via the serial port. The registers are used to read motion data and status as well as to set the device configuration.

Address	Register	Read/Write	Default Value
0x00	Product_ID	R	0x12
0x01	Revision_ID	R	0x00
0x02	Motion	R	0x00
0x03	Delta_X	R	Any
0x04	Delta_Y	R	Any
0x05	SQUAL	R	Any
0x06	Shutter_Upper	R	Any
0x07	Shutter_Lower	R	Any
0x08	Maximum_Pixel	R	Any
0x09	Pixel_Sum	R	Any
0x0a	Minimum_Pixel	R	Any
0x0b	Pixel_Grab	R/W	Any
0x0c	Reserved		
0x0d	Mouse Control	R/W	0x00
0x0e – 0x39	Reserved		
0x3a	Chip_Reset	W	N/A
0x3b – 0x3e	Reserved		
0x3f	Inv_Rev_ID	R	0xff
0x40 – 0x62	Reserved		
0x63	Motion_Burst	R	0x00

Product_ID Address: 0x00

Access: Read Reset Value: 0x12

Bit	7	6	5	4	3	2	1	0
Field	PID_7	PID_6	PID_5	PID_4	PID_3	PID_2	PID_1	PID_0

Data Type: 8-Bit unsigned integer

USAGE: This register contains a unique identification assigned to the ADNS-5020. The value in this register does not change; it can be used to verify that the serial communications link is functional.

Revision_ID Address: 0x01

Access: Read Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	RID_7	RID_6	RID_5	RID_4	RID_3	RID_2	RID_1	RID_0

Data Type: 8-Bit unsigned integer

USAGE: This register contains the IC revision. It is subject to change when new IC versions are released.

Motion Address: 0x02

Access: Read/Write Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	MOT	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Data Type: Bit field.

USAGE: Register 0x02 allows the user to determine if motion has occurred since the last time it was read. If the MOT bit is set, then the user should read registers 0x03 and 0x04 to get the accumulated motion. Read this register before reading the Delta_X and Delta_Y registers.

Writing anything to this register clears the MOT bit, Delta_X and Delta_Y registers. The written data byte is not saved.

Field Name	**Description**
MOT	Motion since last report **0 = No motion** 1 = Motion occurred, data ready for reading in Delta_X and Delta_Y registers
Reserved	Reserved

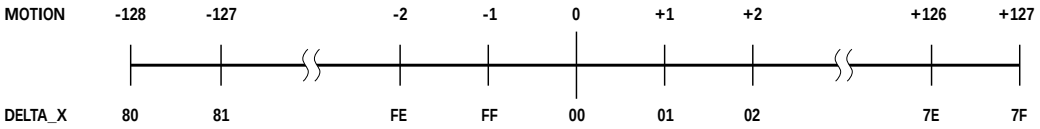
Delta_X Address: 0x03

Access: Read Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0

Data Type: Eight bit 2's complement number.

USAGE: X movement is counts since last report. Absolute value is determined by resolution. Reading clears the register.



NOTE: Avago Technologies RECOMMENDS that registers 0x03 and 0x04 be read sequentially.

Delta_Y Address: 0x04

Access: Read Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0

Data Type: Eight bit 2's complement number.

USAGE: Y movement is counts since last report. Absolute value is determined by resolution. Reading clears the register.

NOTE: Avago Technologies RECOMMENDS that registers 0x03 and 0x04 be read sequentially.

SQUAL Address: 0x05

Access: Read Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	SQ_7	SQ_6	SQ_5	SQ_4	SQ_3	SQ_2	SQ_1	SQ_0

Data Type: Upper 8 bits of a 9-bit unsigned integer.

USAGE: SQUAL (Surface Quality) is a measure of the number of valid features visible by the sensor in the current frame.
The maximum SQUAL register value is 144. Since small changes in the current frame can result in changes in SQUAL, variations in SQUAL when looking at a surface are expected. The graph below shows 250 sequentially acquired SQUAL values, while a sensor was moved slowly over white paper. SQUAL is nearly equal to zero, if there is no surface below the sensor. SQUAL is typically maximized when the navigation surface is at the optimum distance from the imaging lens (the nominal Z-height).

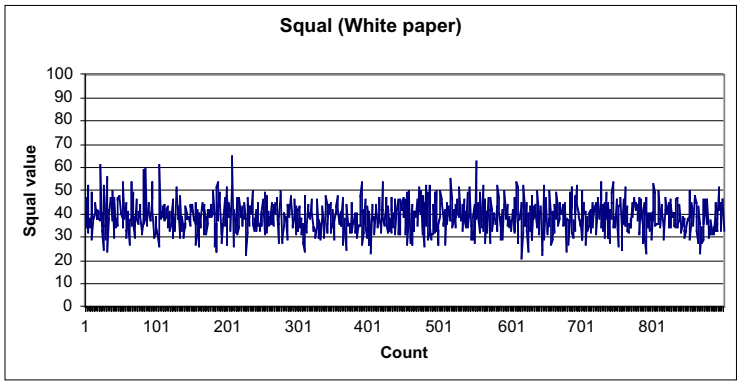


Figure 13. Squal values (white paper).

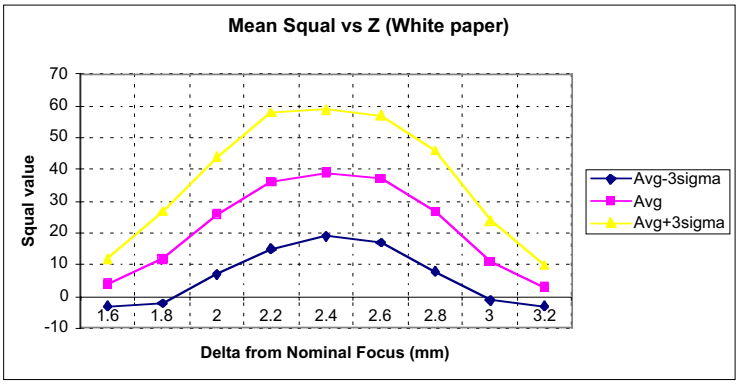


Figure 14. Mean squal vs. Z (white paper).

Shutter_Upper Address: 0x06

Access: Read Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	S_{15}	S_{14}	S_{13}	S_{12}	S_{11}	S_{10}	S_9	S_8

Shutter_Lower Address: 0x07

Access: Read Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	S_7	S_6	S_5	S_4	S_3	S_2	S_1	S_0

Data Type: Sixteen bit unsigned integer.

USAGE: Units are clock cycles. Read Shutter_Upper first, then Shutter_Lower. They should be read consecutively. The shutter is adjusted to keep the average and maximum pixel values within normal operating ranges. The shutter value is automatically adjusted.

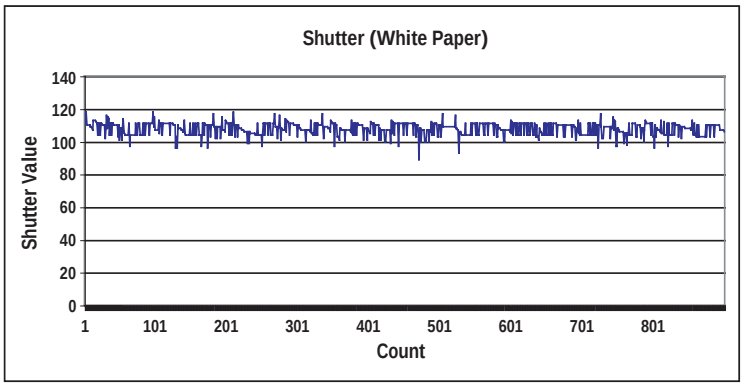


Figure 15. Shutter (white paper).

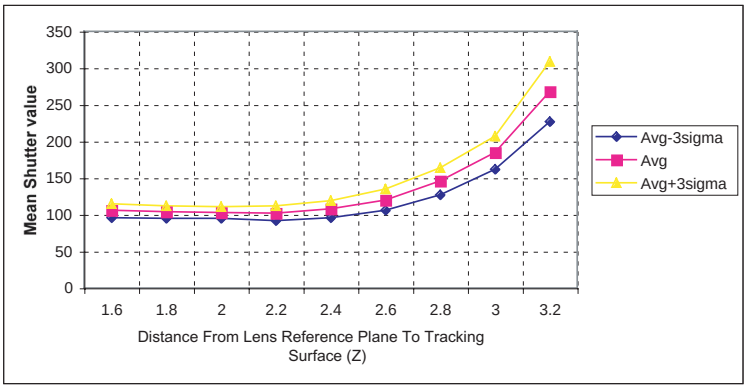


Figure 16. Mean shutter vs. Z (white paper).

Maximum_Pixel Address: 0x08

Access: Read Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	MP_0	MP_6	MP_5	MP_4	MP_3	MP_2	MP_1	MP_0

Data Type: Eight-bit number.

USAGE: Maximum Pixel value in current frame. Minimum value = 0, maximum value = 127. The maximum pixel value can vary with every frame.

Pixel_Sum Address: 0x09

Access: Read Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	AP_7	AP_6	AP_5	AP_4	AP_3	AP_2	AP_1	AP_0

Data Type: High 8 bits of an unsigned 15-bit integer.

USAGE: This register is the accumulated pixel value from the last image taken. The maximum accumulator value is 28,575, but only bits [14:7] are reported. It may be described as the full sum divided by 1.76.

The maximum register value is 223. The minimum is 0. The pixel sum value can change on every frame.

Minimum_Pixel Address: 0x0a

Access: Read Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	MP_0	MP_6	MP_5	MP_4	MP_3	MP_2	MP_1	MP_0

Data Type: Eight-bit number.

USAGE: Minimum Pixel value in current frame. Minimum value = 0, maximum value = 127. The minimum pixel value can vary with every frame.

Pixel_Grab Address: 0x0b

Access: Read/Write Reset Value: 0x00

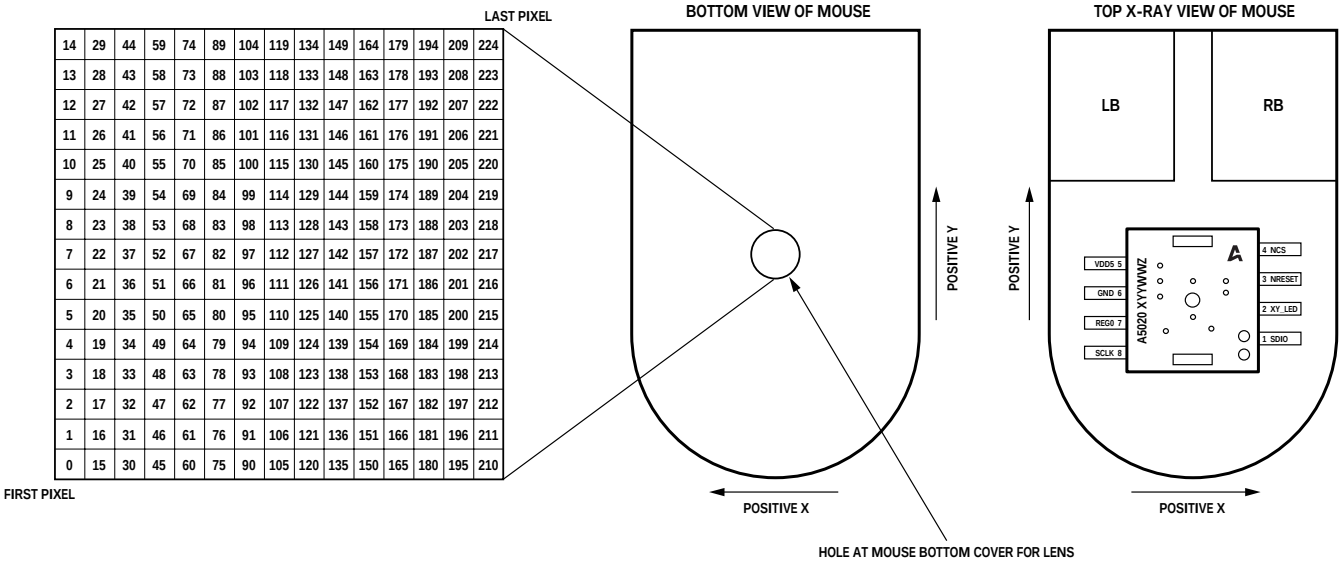
Bit	7	6	5	4	3	2	1	0
Field	Valid	PD_6	PD_5	PD_4	PD_3	PD_2	PD_1	PD_0

Data Type: Eight-bit word.

USAGE: The pixel grabber captures 1 pixel per frame. If there is a valid pixel in the grabber when this register is read, the MSB will be set, an internal counter will incremented to capture the next pixel and the grabber will be armed to capture the next pixel. It will take 225 reads to upload the complete image. Any write to this register will reset and arm the grabber to grab pixel 0 on the next image.

Physical Pixel Address Map – readout order of the array

(looking through the sensor aperture at the bottom of the package)



14	29	44	59	74	89	104	119	134	149	164	179	194	209	224
13	28	43	58	73	88	103	118	133	148	163	178	193	208	223
12	27	42	57	72	87	102	117	132	147	162	177	192	207	222
11	26	41	56	71	86	101	116	131	146	161	176	191	206	221
10	25	40	55	70	85	100	115	130	145	160	175	190	205	220
9	24	39	54	69	84	99	114	129	144	159	174	189	204	219
8	23	38	53	68	83	98	113	128	143	158	173	188	203	218
7	22	37	52	67	82	97	112	127	142	157	172	187	202	217
6	21	36	51	66	81	96	111	126	141	156	171	186	201	216
5	20	35	50	65	80	95	110	125	140	155	170	185	200	215
4	19	34	49	64	79	94	109	124	139	154	169	184	199	214
3	18	33	48	63	78	93	108	123	138	153	168	183	198	213
2	17	32	47	62	77	92	107	122	137	152	167	182	197	212
1	16	31	46	61	76	91	106	121	136	151	166	181	196	211
0	15	30	45	60	75	90	105	120	135	150	165	180	195	210

Reserved Address: 0x0c

Mouse_control Address: 0x0d

Access: Read/Write Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RES

Data Type: Eight bit number

USAGE: Resolution and chip reset information can be accessed or to be edited by this register.

Field Name	Description
RES	Set resolution **0 = 500 cpi** 1 = 1000 cpi
Reserved	Reserved

Reserved Address: 0x0e-0x39

Chip_Reset Address: 0x3a

Access: Write Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	CR_7	CR_6	CR_5	CR_4	CR_3	CR_2	CR_1	CR_0

Data Type: 8-Bit unsigned integer

USAGE: Write 0x5a to initiate chip RESET.

Reserved Address: 0x3b – 0x3e

Inv_Rev_ID Address: 0x3f

Access: Read Reset Value: 0xff

Bit	7	6	5	4	3	2	1	0
Field	$RRID_7$	$RRID_6$	$RRID_5$	$RRID_4$	$RRID_3$	$RRID_2$	$RRID_1$	$RRID_0$

Data Type: 8-Bit unsigned integer

USAGE: This register contains the inverse of the revision ID which is located at register 0x01.

Reserved Address: 0x40-0x62

Motion_Burst Address: 0x63

Access: Read Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	MB_7	MB_6	MB_5	MB_4	MB_3	MB_2	MB_1	MB_0

Data Type: Various.

USAGE: Read from this register to activate burst mode. The sensor will return the data in the Delta_X, Delta_Y, Squal, Shutter_Upper, Shutter_Lower, Maximum_Pixel and Pixel_Sum. If the burst is not terminated at this point, the internal address counter stops incrementing and Pixel Sum register's value will be continuously returned. Bursts are terminated when NCS is raised.

AV02-0114EN January 25, 2007