CV110-3A

Cellular-band High Linearity Downconverter

TriQuint SEMICONDUCTOR

Product Features

- High dynamic range downconverter with integrated LO, IF, & RF amps
- RF: 800 – 960 MHz
- IF: 200 – 350 MHz
- +37 dBm Output IP3
- +20 dBm Output P1dB
- 5 dB Noise Figure
- +5V Single supply operation
- Pb-free 6mm 28-pin QFN package
- High-side LO configuration
- Common footprint with other PCS/UMTS versions

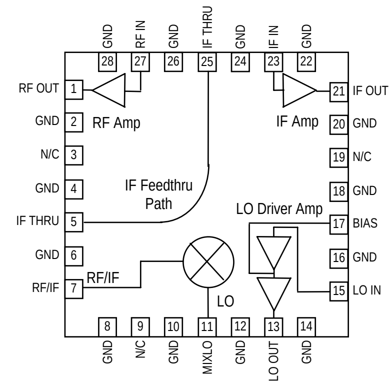
Product Description

The CV110-3A is a high linearity downconverter designed to meet the demanding issues for performance, functionality, and cost goals of current and next generation mobile infrastructure. It provides high dynamic range performance in a low profile surface-mount leadless package that measures 6 x 6 mm square.

Functionality includes RF amplification, frequency conversion and IF amplification, while an integrated LO driver amplifier powers the passive mixer. The MCM is implemented with reliable and mature GaAs MESFET and InGaP HBT technology.

Typical applications include frequency downconversion used in CDMA/GSM/TDMA, CDMA2000, W-CDMA, and EDGE 2.5G and 3G mobile base transceiver stations for cellular frequency bands.

Functional Diagram



Specifications [(1)]

Parameters	Units	Min	Typ	Max	Comments
RF Frequency Range	MHz		800 – 960		
LO Frequency Range	MHz		1000 – 1310		
IF Center Frequency Range	MHz		200 – 350		See note 2
% Bandwidth around IF center frequency	%		±7.5		See note 3
IF Test Frequency	MHz		240		
SSB Conversion Gain	dB		22.5		Temp = 25 °C
Gain Drift over Temp (-40 to 85 °C)	dB		±1.5		Referenced to +25 °C
Output IP3	dBm		+37		See note 4
Output IP2	dBm		+45		See note 4
Output 1dB Compression Point	dBm		+20		
Noise Figure	dB		5		See note 5
LO Input Drive Level	dBm	-2.5	0	+2.5	
LO-RF Isolation	dB		60		See note 6
LO-IF Isolation	dB		40		P_{LO} = 0 dBm
Return Loss: RF Port	dB		15		
Return Loss: LO Port	dB		10		
Return Loss: IF Port	dB		15		
Operating Supply Voltage	V	+4.9	+5	+5.1	
Supply Current	mA	290	360	480	
FIT Rating	failures/1E9 hrs			72.1	@ 70° C ambient, 90% confidence
Thermal Resistance	°C / W			27	
Junction Temperature	°C			160	See note 7

1. Specifications when using the application specific circuit (shown on page 3) with a low side LO = 0 dBm in a downconverting application over the operating case temperature range.
2. IF matching components affect the center IF frequency. Proper component values for other IF center frequencies than shown can be provided by emailing to applications.engineering@wj.com.
3. The IF bandwidth of the converter is defined as 15% around any center frequency in its operating IF frequency range. The bandwidth is determined with external components. Specifications are valid around the total ±7.5% bandwidth. ie. with a center frequency of 240 MHz, the specifications are valid from 240 ± 18 MHz.
4. Assumes the supply voltage = +5 V. OIP3 is measured with Δf = 1 MHz with IF_{out} = 5 dBm / tone.
5. Assumes LO injection noise is filtered at the thermal noise floor, -174 dBm/Hz, at the RF, IF, and Image frequencies.
6. L-R Isolation is referenced to an LO injection of 0 dBm. The L-R performance shown also includes the isolation due to an external SAW filter between the RF amplifier and mixer.
7. The maximum junction temperature ensures a minimum MTTF rating of 1 million hours of usage.

Absolute Maximum Rating

Parameter	Rating
Operating Case Temperature	-40 to +85 °C
Storage Temperature	-55 to +125 °C
DC Voltage	+6 V
Junction Temperature	+220 °C
RF Input (continuous)	+2 dBm

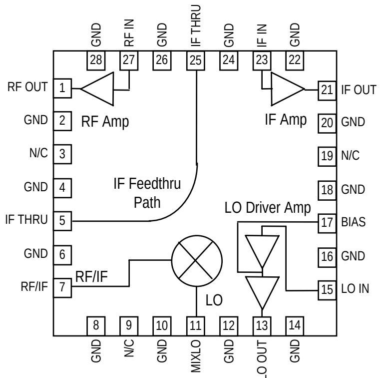
Operation of this device above any of these parameters may cause permanent damage.

Ordering Information

Part No.	Description
CV110-3AF	Cellular-band High Linearity Downconverter (lead-free/RoHS-compliant 6x6mm QFN package)
CV110-3APCB240	Fully Assembled Eval. Board, IF = 240MHz

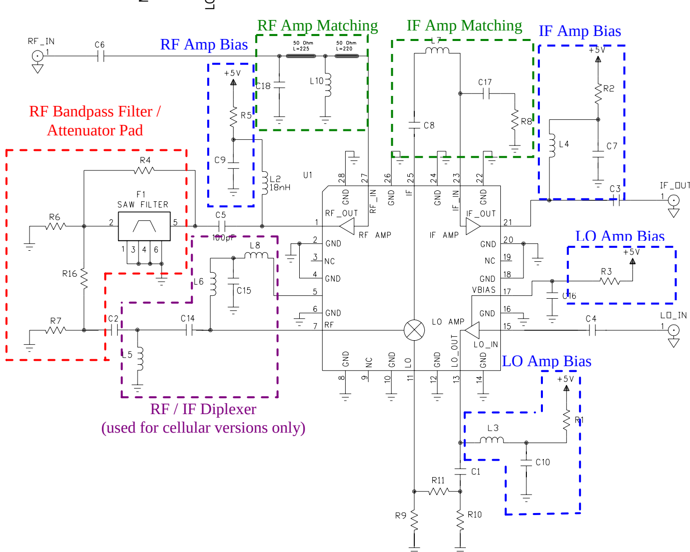
Specifications and information are subject to change without notice

Device Architecture / Application Circuit Information

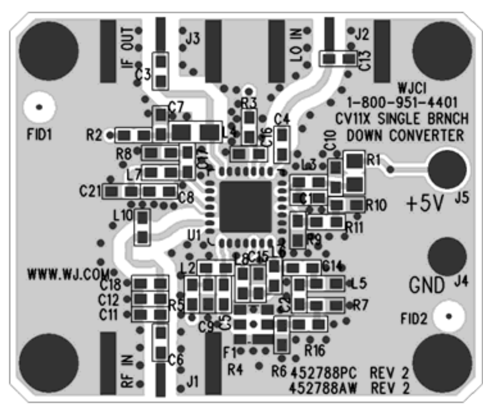


Typical Downconverter Performance Chain Analysis

Stage	Gain (dB)	Output P1dB (dBm)	Output IP3 (dBm)	NF (dB)	Current (mA)	Cumulative Performance			
						Gain (dB)	Output P1dB (dBm)	Output IP3 (dBm)	NF (dB)
RF Amplifier	13.5	21	40.0	3.5	150	13.5	21.0	40.0	3.5
RF Filter	-1.5	---	---	1.5	---	12.0	19.5	38.5	3.5
MMIC Mixer	-9.0	8	23.0	9.8	60	3.0	6.1	22.1	4.5
IF Amplifier	19.0	22	39.1	2.5	150	22.0	20.3	37.0	5.0
CV110-3A	**Cumulative Performance**				**360**	**22.0**	**20.3**	**37.0**	**5.0**



Printed Circuit Board Material:
.014" FR-4, 4 layers, .062" total thickness



CV110-3A: The application circuit can be broken up into four main functions as denoted in the colored dotted areas above: RF/IF diplexing (purple), amplifier matching (green), filtering (red), and dc biasing (blue). There are various placeholders for chip components in the circuit schematic so that a common PCB can be used for all WJ single-branch converters. Additional placeholders for other optional functions such as filtering are also included.

RF / IF Amplifier Matching: The RF amplifier requires a shunt matching element for optimal gain and input return loss performance. The IF amplifier requires matching elements to optimize the performance of the amplifier to the desired IF center frequency. Since IF bandwidths are typically on the order of 5 to 10%, a simple two element matching network, in the form of either a high-pass or low-pass filter structure, is sufficient to match the MMIC IF amplifier over these narrow bandwidths. Proper component values for other IF center frequencies can be found in the IF Amplifier Matching Table or by e-mailing to sjcapplication.engineering@tqs.com.

RF Bandpass Filtering: Bandpass filtering is recommended to reject the image frequencies and achieve the best noise figure performance with the downconverter. The bandpass filter, implemented with a SAW filter on the application circuit, allows for the suppression of noise from the image frequency. It is permissible to not use a filter and use a 2 dB pad with R6, R7, and R16 instead with slightly degraded noise figure performance. Standard WJ evaluation boards will have the 2 dB pad in place.

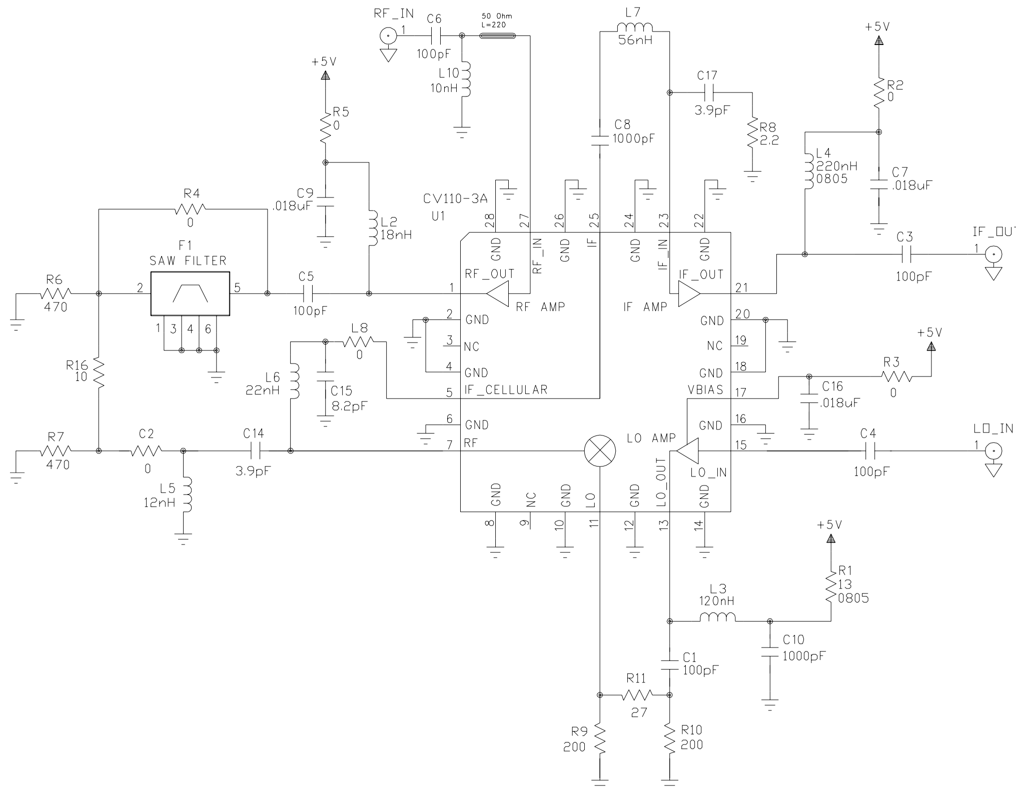
External Diplexer: In a downconversion application, the incoming RF signal impinges on the switching elements of the mixer; the interaction with these switches produces a signal at the IF frequency. The two signals (RF and IF) are directed to the appropriate ports by the external diplexer. Pin 5 contains the IF signal and allows the signal to be transferred to pin 25 for the convenience of PCB layouts.

DC biasing: DC bias must be provided for the RF, LO and IF amplifiers in the converter. R1 sets the operating current for the last stage of the LO amplifier and is chosen to optimize the mixer LO drive level. Proper RF chokes and bypass capacitors are chosen for proper amplifier biasing at the intended frequency of operation. The "+5 V" dc bias should be supplied directly from a voltage regulator.

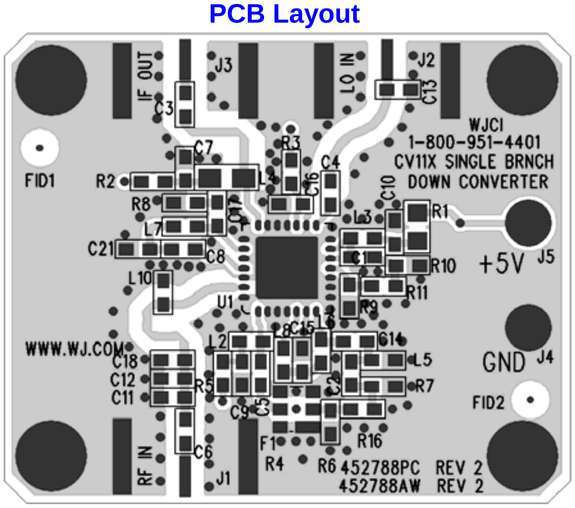
IF Amplifier Matching

Frequency (MHz)	40	50	75	100	125	130	155	169	180	210	240
L7 (nH)	470	430	150	150	120	120	100	82	82	82	56
C17 (pF)	24	15	22	10	8.2	6.8	5.6	5.0	4.7	3.3	3.9
R8 (ohms)	4.7	4.7	3.3	2.2	2.2	2.2	2.2	2.2	2.2	2.2	2.2
L4 (nH)	470	240	330	330	330	330	330	330	330	220	220

Downconverting Application Circuit: CV110-3APCB240
RF = 800 – 960 MHz, IF = 240 MHz



PCB Layout



Circuit Board Material: .014” FR-4, 4 layers, .062” total thickness

Bill of Materials

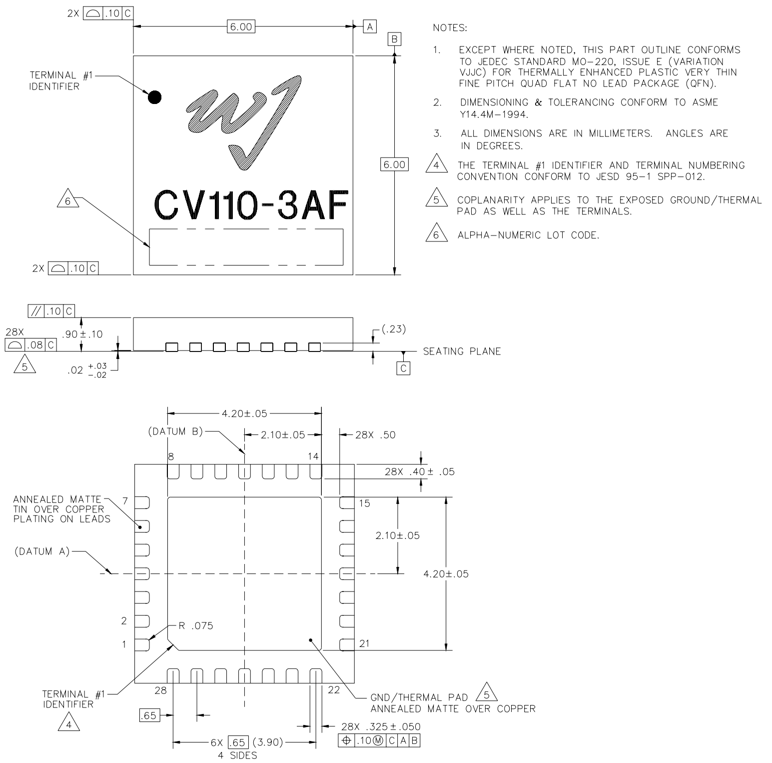
Ref. Desig.	Component
R1	13 Ω chip resistor, size 0805
R2, R3, R4, R5, C2, L8	0 Ω chip resistor
R6, R7	470 Ω chip resistor
R8	2.2 Ω chip resistor
R9, R10	200 Ω chip resistor
R11	27 Ω chip resistor
R16	10 Ω chip resistor
C1, C3, C4, C5, C6	100 pF chip capacitor
C7, C9, C16	0.018 µF chip capacitor
C8, C10	1000 pF chip capacitor
C11, C12, C13, C18, C21, F1	Shown in silkscreen, but not used in actual circuit.
C15	8.2 pF chip capacitor
C14, C17	3.9 pF chip capacitor
C18	1.5 pF chip capacitor
L2	18 nH chip inductor
L3	120 nH chip inductor
L4	220 nH chip inductor, size 0805
L5	12 nH chip inductor
L6	22 nH chip inductor
L7	56 nH chip inductor
L10	10 nH chip inductor
U1	CV110-3A WJ Converter

All components are of size 0603 unless otherwise specified.

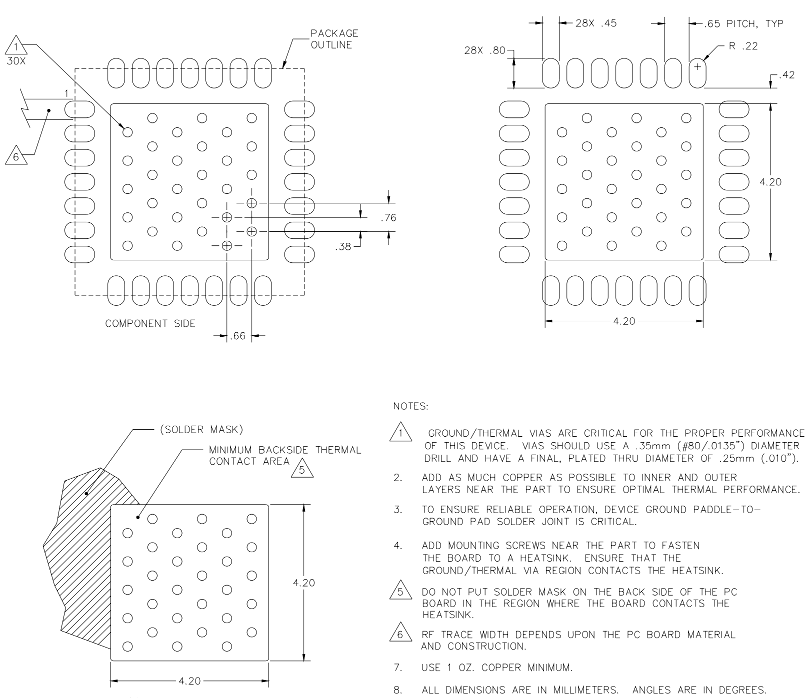
Mechanical Information

This package is lead-free/RoHS-compliant. The plating material on the pins is annealed matte tin over copper. It is compatible with both lead-free (maximum 260 °C reflow temperature) and leaded (maximum 245 °C reflow temperature) soldering processes.

Outline Drawing



Mounting Configuration / Land Pattern



Product Marking

The component will be lasermarked with a "CV110-3AF" product label with an alphanumeric lot code on the top surface of the package.

Tape and reel specifications for this part will be located on the website in the "Application Notes" section.

ESD / MSL Information

Caution! ESD sensitive device.

ESD Rating: Class 1B
Value: Passes ≥500V to <1000V
Test: Human Body Model (HBM)
Standard: JEDEC Standard JESD22-A114

ESD Rating: Class III
Value: Passes ≥500V to <1000V
Test: Charged Device Model (CDM)
Standard: JEDEC Standard JESD22-C101

MSL Rating: Level 2 at +260 °C convection reflow
Standard: JEDEC Standard J-STD-020

Functional Pin Layout

Pin	FUNCTION	Pin	FUNCTION
1	RF Amp Output	15	LO Amp Input
2	GND	16	GND
3	N/C	17	LO Amp Bias
4	GND	18	GND
5	IF Feedthru Port	19	N/C or GND
6	GND	20	GND
7	Mixer RF / IF Port	21	IF Amp Output/Bias
8	GND	22	GND
9	N/C or GND	23	IF Amp Input
10	GND	24	GND
11	Mixer LO Input	25	IF Feedthru Port
12	GND	26	GND
13	LO Amp Output	27	RF Amp Input
14	GND	28	GND