ProASIC3/E Starter Kit

User's Guide and Tutorial

Actel
POWER MATTERS

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Introduction

Thank you for purchasing the Actel ProASIC3/E Starter Kit.

This guide provides the information required to easily evaluate the ProASIC3/E devices.

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Chapter 1 – "Contents and System Requirements" describes the contents of the ProASIC3/E Starter Kit.

Chapter 2 – "Hardware Components" describes the components of the ProASIC3/E Evaluation Board.

Chapter 3 – "Setup and Self Test" describes how to setup the ProASIC3/E Evaluation Board and how to perform a self test.

Chapter 4 – "Description of Test Design" describes the existing design on the ProASIC3/E Evaluation Board.

Chapter 5 – "LVDS Signal Evaluation" explains test setup and design, reports the measurements performed on the board, and makes recommendations to increase the LVDS signal quality in order to meet the performance criteria.

Chapter 6 – "Actel VHDL ProASIC3/E Design Flow" introduces the design flow for VHDL using the Actel Libero® Integrated Design Environment (IDE) suite.

Chapter 7 – "Quick Start Tutorial" illustrates a VHDL design for a ProASIC3/E starter kit board.

Chapter 8– "Test Procedures for Board Testing" details the test procedure to be carried out at the Actel designated manufacturer's testing facility on the ProASIC3/E Evaluation Board with silkscreen labeling A3PE-A3P-EVAL-BRD-1 REV3.

Appendix A – **"PQ208 Package Connections for A3PE600 and A3P250 Devices" provides a table listing the board connections.**

Appendix B – **"Board Schematics" provides illustrations of the ProASIC3/E Evaluation Board.**

Appendix C – "Signal Layers" provides illustrations for the six signal layers of the Evaluation Board.

Appendix D– **"Product Support"** describes Actel support services.

Document Assumptions

This user's guide assumes:

- You intend to use Actel Libero IDE software.
- You have installed and are familiar with Actel Libero IDE v6.2 SP1 or later software.
- You are familiar with VHDL.
- You are familiar with PCs and Windows operating systems.

1 Contents and System Requirements

This chapter details the contents of the ProASIC3/E Starter Kit and lists the power supply and software system requirements.

Starter Kit Contents

The starter kit includes the following:

- ProsASIC3/E Evaluation Board
- Libero IDE Gold
- FlashPro3
- The *ProASIC3/E Starter Kit User's Guide & Tutorial*
- CD with design examples
- Switching brick power supply (rated from 110 V to 240 V AC) from 50 Hz to 60 Hz input, providing 9 V DC output at up to 2 A, part number DTS090220U-P5P-SZ from CUI INC

For the CD contents, review the *ReadMe.doc* file at the top level of the CD.

2 Hardware Components

This chapter describes the hardware components of the ProASIC3/E Evaluation Board.

ProASIC3/E Evaluation Board

Figure 2-1 on page 10 illustrates a top-level view of the ProASIC3/E Evaluation Board.

The ProASIC3/E Evaluation Board consists of the following:

- Wall mount power supply connector, with switch and LED indicator
- Switches to select from among 1.5 V, 1.8 V, 2.5 V, and 3.3 V – I/O voltages on banks 4 and 5 (southern side)
- 10-pin 0.1 inch pitch programming connector compatible with Altera connections
- 40 MHz oscillator and two independent manual clock options for global reset and pulse
- Eight LEDs (driven by outputs from the device)
- Jumpers (allow disconnection of all external circuitry from the FPGA)
- Two monostable pulse generator switches ("global" and "reset")
- Four switches (provide input to the device)
- Two hex switches to provide four inputs each to the FPGA, and which are set to a user-switchable hexadecimal input value
- Large LCD alphanumeric display to facilitate detailed message outputs from the FPGA application

For further information, refer to the following appendices:

Appendix A – "PQ208 Package Connections for A3PE600 and A3P250 Devices" on page 71.

Appendix B – "Board Schematics" on page 81.

Detailed Board Description and Usage

The ProASIC3 Starter kit board has various advanced features that are covered in later sections of this chapter. It will be noted that the Advanced Prototyping Starter Kit has a socket on the board into which an end user may place any ProASIC3 device, as all devices in both the ProASIC3 and ProASIC3E families are available in the PQ208 package. The EVAL kit version can be identified as the one that has the FPGA soldered directly to the board.

A block diagram of the ProASIC3 Starter kit board is shown in Figure 2-1 on page 10 and will facilitate understanding of the more detailed schematics shown in this tutorial in the appendix, "Board Schematics" on page 81.

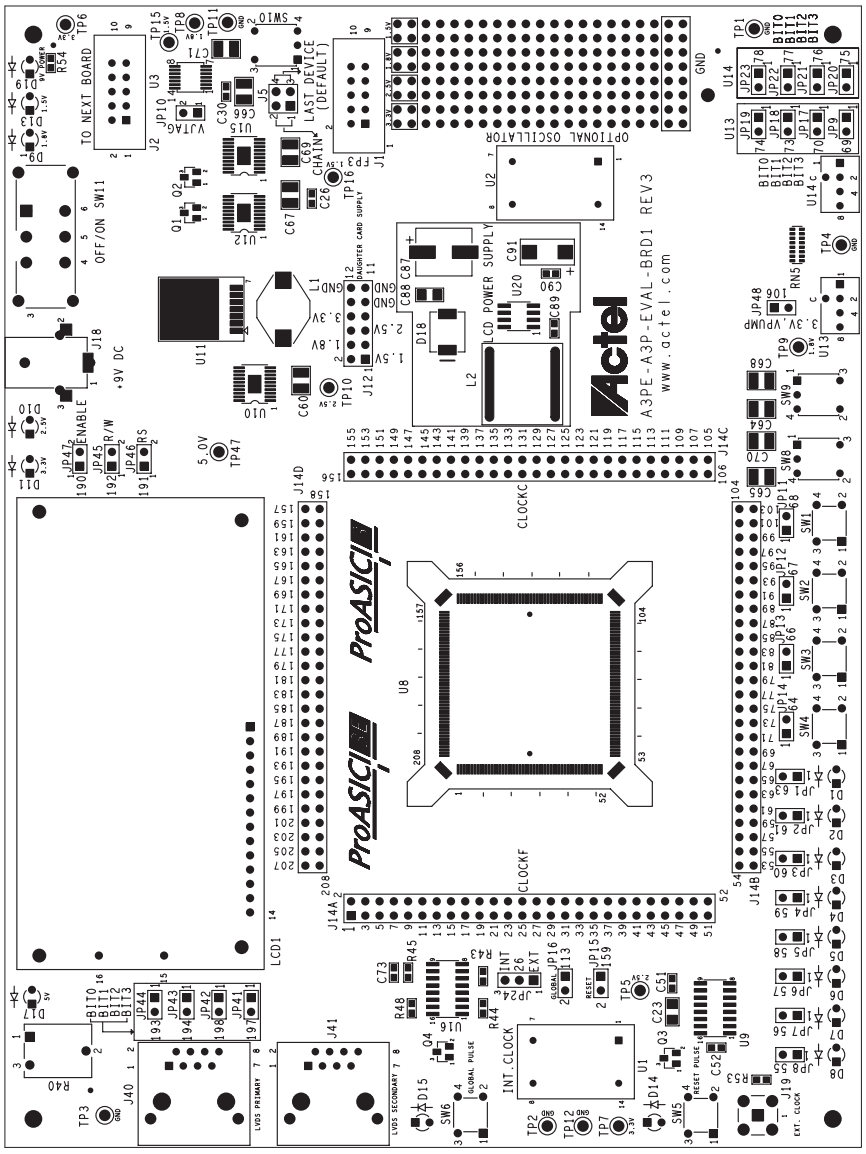

Figure 2-1. ProASIC3/E Evaluation Board: Top-Level View

Full schematics are available on the Starter Kit Tutorial CD that is supplied with the Starter Kit. The schematics are also available for download from the Actel website. The electronic versions of the dedicated schematics can naturally be enlarged to a far greater degree than can be shown in the printed version of this manual or even in the electronic version of this manual, hence the interested reader is referred to the dedicated schematics to see the appropriate level of detail.

PLL Parts/Usage on ProASIC3

Instructions for PLL Activation on ProASIC3 Starter Kit Board

In order to use the PLLs on the ProASIC3 starter kit board, power must be applied to their respective analog supply rails. For the west side PLL, known as PLF, the V_{CCPLF} line must be connected to V_{CC}, which is held at 1.5 V. The same is true for V_{CCPLC} of the PLL on the east side, known as PLC. In addition, the V_{COMPLF} and V_{COMPLC} lines must be connected to ground. We do not connect these voltages by default on the board for three reasons:

1. The PLC analog voltage rails are not available on A3P devices, only on A3PE in the PQ208 package. Only the west side PLL, namely PLF, is available on A3P devices in PQ208. In A3P devices, the pins are used as general I/Os. The same board is used for A3PE and A3P devices.
2. We want to demonstrate the lowest possible power consumption for the part. Perpetually powering the PLL lines would not achieve that.
3. It is easy to connect the appropriate pins together when desired. That is why we make the pins available on the headers.

A variety of valid connections are possible. Two examples are as follows:

1. For PLF, connect pin 27 (V_{CCPLF}) to pin 36 (V_{CC}), and pin 25 (V_{COMPLF}) to pin 17 (GND).
2. For PLC, (*A3PE only*) connect pin 131 (V_{CCPLC}) to pin 142 (V_{CC}), and pin 133 (V_{COMPLC}) to pin 141 (GND).

To facilitate end users, we will be supplying jumper wires with selected production versions of the kit to allow end users to quickly connect and disconnect these voltage supply rails. If a user has lost the jumper wires or has a production kit without jumper wires, it is a simple matter of soldering short insulated connecting wire to the appropriate header pins on the J14A and J14C headers.

Power Supplies

A 9 V power supply is provided with the kit (Figure 2-2). There are many power supply components in the starter kit board to illustrate the many ways that differing voltage banks may be supported with ProASIC3 and ProASIC3E

technology. These voltage banks are not all required for general use of ProASIC3 silicon. They are provided purely for illustrative purposes.

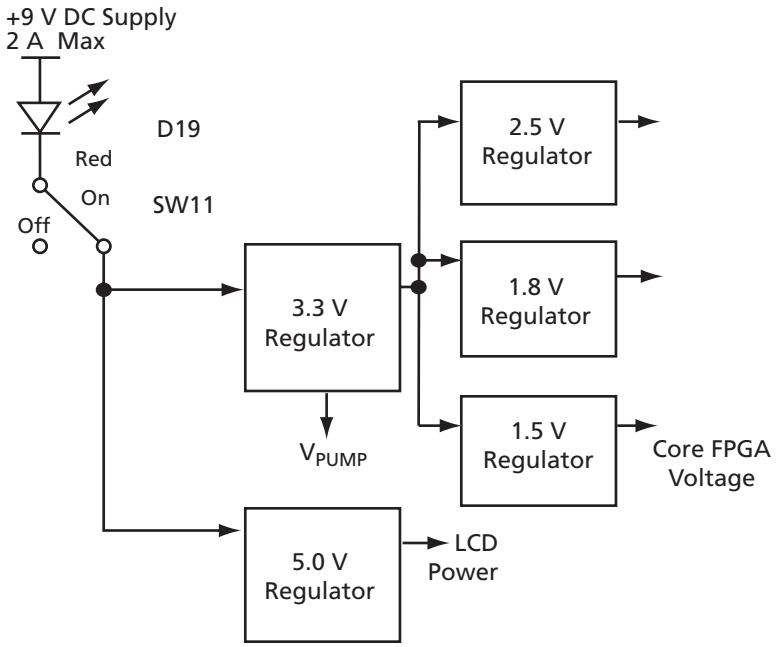

Figure 2-2. Power Supply Block Diagram

To use the ProASIC3/E Evaluation board with a wall mount power supply, use the switching brick power supply that is provided with the kit.

The external +9 V positive center power supply provided to the board via connector J16 goes to a voltage regulator chip U11 on the evaluation board. As soon as the external voltage is connected to the board, the red power applied LED (the only red LED on the board) D19 illuminates to indicate that an external supply has been connected to the board. As soon as switch SW11 is moved to the ON position (to the right, as labeled on the board "OFF/ON"), the disabling ground signal is removed from pin 7 of U11 and the regulator begins to provide power at its output.

The U11 switching voltage regulator provides a dedicated 3.3 V supply at its output. The board's 3.3 V supply is used for feeding separate regulators that deliver 1.5 V (via U15), 1.8 V (via U12) and 2.5 V (via U15). The 1.5 V is required for the core voltage of the ProASIC3 family, and the 2.5 V is required for demonstrating LVDS extended I/O bank capability.

The presence of these voltages is indicated by four green LEDs (D13, D9, D10, and D11 respectively) illuminating at the top right of the board. Each LED is labeled with the voltage it represents and its component identifier. All four voltages are selectable on the I/O banks 4 and 5 (the two southernmost banks on a ProASIC3E device).

Note: Only ProASIC3E devices have 8 I/O banks. ProASIC3 devices have four I/O banks—one per side of the PQ208 package.]

The 3.3 V supply is also used for optionally providing the V_{PUMP} programming voltage. This V_{PUMP} voltage may be provided to the chip during programming by applying a FlashPro3 programmer to the J1 interface and selecting V_{PUMP} from the FlashPro v3.3 (or later) programming software. V_{PUMP} voltage may also be provided directly to the chip from the board.

Simply leave the JP48 jumper in place to apply the 3.3 V supply to the V_{PUMP} pin (106 of the PQ208 packaged FPGA). Note that if both FlashPro3 and the board are selected to provide V_{PUMP}, then it is the connection on the board that will override, as FlashPro3 will detect that a voltage is available, issue an information message in the programming software, and then move the V_{PUMP} output pin to a tristate value, allowing the board to provide all the power.

The board must be powered-up during programming because the chip needs its core voltages to be provided and VJTAG must be detected by the FlashPro3 programmer in order for it to set its JTAG signal voltages to the right level.

The LCD has its own dedicated 5 V power supply, all components of which (including the regulator U20) are marked on the circuit board in a boxed area so that you may know which components on the PCB are associated with which tasks. An LED (D17) representing the 5 V supply availability is positioned at the top left of the board.

The external +9 V power supply is rated at 2 A maximum. On the first of the full-page dedicated schematics shown in the appendix "Board Schematics" on page 81, it will be noted that the 3.3 V supply is rated at 5 A maximum. The derived power supplies of 1.5 V, 1.8 V, and 2.5 V are rated at 2 A max each, and the LCD 5 V power supply is rated at 500 mA, as shown in Figure B-11 on page 92. Clearly, not all these derived supplies can be working at their respective maximum current outputs simultaneously. The maximum ratings are for the individual regulator ICs and cannot be numerically added together.

Both the U11 (LM2678S-3.3) and U20 (LM2674M-5.0) components are rated for an input voltage range of +8 V to +40 V, so a wide range of power supplies may be used with the board with no concern about over-voltage conditions occurring from inadvertent accidental usage of the wrong power supply. However, the user should take care to ensure that the voltage provided is positive at the center pin of the J16 connector and grounded on the outside. Greater heating of the regulator chips will be observed with higher voltages. It is therefore recommended that only the included power supply or an equivalent substitute be used with the evaluation kit. The included power supply has been rated for this board, including Actel daughter cards that may be attached to the board.

Daughter Card Power Supply Connections

Limited power to a daughter card may be supplied by the board. The connector for the daughter card is shown in Figure B-7 on page 88 and is the J12 header. All the FPGA voltages of 1.5 V, 1.8 V, 2.5 V, and 3.3 V are provided to the daughter card via a 12-pin 0.1 inch pitch connector. The voltages are arranged with a no-connection pin interspersing the voltage pins. This prevents accidental use of a jumper to short a supply rail to ground, which could connect differing supply rails together. The purpose is not to protect the power supply regulators, as these will go high-impedance when an over-voltage condition is detected. It is to protect the FGPA from unintentional application of a higher voltage to the 1.5 V core. Three of the twelve pins are ground pins, which will provide more than sufficient current return capability for future Actel daughter cards that will work with this board.

Power Supplies and Chaining Boards Together

There is a special note on "V_{PUMP} Connections When Chaining Boards Together" on page 14.

Instructions are detailed here but the novice reader is advised to return to this section after reading the section on standard JTAG programming connections via FlashPro3.

When joining multiple ProASIC3 starter kit boards together via the chain programming connection, bear in mind that the J2 connector is used to connect to the J1 connector of the next board in the chain by attaching a standard 0.100-inch pitch 10-pin programming cable. The length of the cable does need to be kept as short as possible, because multiple boards connected to form a JTAG chain of ProASIC3/E devices will provide much greater noise pick-up and may degrade the TCK clock for devices remote from the FlashPro3 programmer. Set VJTAG at an absolute minimum of 1.8 V to help with signal integrity when chaining boards together. Higher voltages will give better noise and impedance mismatch immunity.

Disconnect the jumper at JP10 on all boards. This jumper can be used to provide VJTAG to a downstream board or to some element in the design that you wish to supply with the VJTAG voltage used by the ProASIC3/E component. The shunt that is normally in this location can be safely stored across pins 11 and 12, or 9 and 10 of the J12 daughter card power supply connector. For particularly long chains, the value of TCK used during programming should be reduced.

During its development, various revisions of the ProASIC3 Starter Kit board have been produced. This documentation contains additional text that documents some of these earlier versions, as well as the newest Rev3 version of the board. Schematics for Rev3 and Rev2 boards are the same when viewed as PDF files, but there is a short in the board layers on the Rev2 that has been corrected for Rev3. The rare Rev1 prototype boards had different schematics and are not discussed in this document.

Procedure for Rev3 Boards

To determine if the board is a Rev3 board:

A Rev3 Board is recognized by examining the front of the board and looking for the part number just beneath the large Actel corporate logo on the board top silk-screen. The part number will be A3PE-**A3P-EVAL-BRD1** followed by **REV3**.

To chain Rev3 boards together:

All boards from the board nearest the FlashPro3 programmer should have the shunt that is placed by default on pins 3 and 4 of the J5 header moved to connect pins 1 and 2. On the board and schematic this is labeled quite clearly as **CHAIN** (pins 1 and 2) and **LAST DEVICE (DEFAULT)** (pins 3 and 4). Only the very last board in the chain should have the shunt remaining across pins 3 and 4 of the J5 connector.

Note that if there is only one board in the chain then it, by definition, is the last board and should have the shunt at J5 connecting pins 3 and 4. This is why this position is labeled as the DEFAULT position for a typical customer with a single starter kit board.

Procedure for Rev2 Boards, With and Without Rework

To determine if the board is a Rev2 board:

A Rev2 board is indicated by a red power LED in the upper right corner of the board and a part number underneath the Actel corporate logo on the board top silk-screen. The part number will be "A3PE-A3P-EVAL-BRD1". No additional text will follow the board number. If the board has been reworked to force it to become equivalent to a Rev3 board, it will contain a green wire on the top side of the board. If it does not contain green wire, it is an original Rev2.

To chain Rev2 boards together:

If reworked, treat it as Rev3 in the previous section. If not reworked, then chaining of the boards cannot be done. The shunt on J5 must be removed for any programming to take place.

Procedure for Rev1 Boards

To determine if the board is a Rev1 board:

A Rev1 Board is indicated by no red power LED in the upper right corner of the board. The part number on the board top silk-screen is **A3PE-EVAL-BRD600**.

Note: Rev1 boards should not be used with this tutorial guide or with design files included with this Starter Kit as the schematics are incompatible with current commercial boards.

V_{PUMP} Connections When Chaining Boards Together

When these boards are connected via a connection from J2 of one board to J1 of another board, V_{PUMP} will be connected from one board to another. When powering on one board with a connector in place, notice that the 1.5 V, 1.8 V, 2.5 V, and 3.3 V LEDs will light on the board to which no power has been applied. The FPGA on that board, if it is programmed, will start operating. This is clearly an inappropriate situation for a large chain of boards. This is caused by having the JP48 connector for supplying V_{PUMP} from the board connected on other boards in the chain, as V_{PUMP} is itself connected to the 3.3 V supply output that is used to generate the other FPGA voltages on a board. To prevent V_{PUMP} from being used as the source of a 3.3 V supply, you should remove the shunt that is in place on the JP48 connector to force JP48 to be open-circuit. To prevent loss of the shunt, it may be safely stored on the J12 header for the daughter card power supply as it is impossible to cause a short by joining any adjacent pins.

Programming the A3PE-A3P-EVAL-BRD1 with a FlashPro3

The base board used for all ProASIC3/E starter kits is the A3PE-A3P-EVAL-BRD1.

In an A3PE-PROTO-KIT, the particular board is an A3PE-EVAL-BRD600-SKT. In an A3PE-EVAL-KIT, the board is an A3PE-EVAL-BRD600-SA. The only difference between these two is that the –SKT indicates that the board is fitted with an A3PE600-PQ208 part, which is mounted in a PQ208 screw-down socket.

In an A3P-PROTO-KIT, the particular board is an A3P-EVAL-BRD250-SKT. In an A3P-EVAL-KIT, the board is an A3P-EVAL-BRD250-SA. The only difference between these two is that the –SKT indicates that the board is fitted with an A3P250-PQ208 part, which is mounted in a PQ208 screw-down socket.

In a kit with a socket on the board, a reasonable number of insertions may be made if the user exercises great care in inserting components into the socket. Note that screw-down sockets are not clam shell sockets, and do have a lifetime of about 20 insertions, although far greater may be achieved with careful placement and use of a torque-limiting screwdriver. Placement of the FPGA in the socket is critical, to ensure all pins are correctly connected.

Connecting the FlashPro3 Programmer to the Board

Connect the FlashPro3 programmer to your computer via the USB cable. Follow the instructions in the User's Guide with FlashPro v3.3 (or later) software for installing the software and connecting to FlashPro3. The amber (yellow) power LED on the FlashPro3 should be illuminated at this stage. If it is not, recheck the procedure in the FlashPro User's Guide until you obtain a steady amber (yellow) power LED illumination.

Make sure the board power switch SW11 is in the OFF position and only the red board external power LED is illuminated on the board.

Connect the FlashPro3 programmer to the board via the 10-pin programming cable supplied with the FlashPro3 programmer hardware. The connector to use on the board is labeled FP3 and is the lower J1 shrouded and keyed header. The pin 1 location on the cable indicated by the red ribbon running along the side of the cable will be on the left side as it enters into the board. After connecting the FlashPro3 programmer, select Analyze Chain from the File menu in the FlashPro software. If all is well, the appropriate device ID for the ProASIC3 or ProASIC3E part will show in the software display on the PC. If you suspect a JTAG communication issue, try changing the VJTAG voltage. For overcoming noise, higher values usually work better, but all values should work with the supplied programming cable (6 inches in length) with connection to just one board.

Programming or Re-Programming the Example Design

On the Starter Kit CD you will find a Designer directory containing a STAPL file for programming the target design. Select the *TOP_A3PE.STP* file (for A3PE600 parts) or the *TOP_A3P.STP* file (for A3P250 parts) from the CD and use that as the STAPL file in the FlashPro software. Selecting the **PROGRAM** action will erase, program, and verify the part (note that **Verify** is disabled with A3PE600 RevC silicon). With RevC silicon the overall programming time for an A3PE600-PQ208 will be 2 minutes, 4 seconds. With RevD silicon, the time will be approximately 30 seconds.

Jumpers for Isolating Switches and LEDs from FPGA

Many jumpers are provided on the board to allow the user to disconnect various switch combinations or LEDs from the FPGA I/O banks. All such jumpers are shown in the schematic in Figure B-1 on page 82 and are labeled on the top-layer silkscreen as JP* where * is a number. All jumpers are also labeled with the FPGA I/O pin number to which they are connected; e.g., JP48 for the 3.3 V connection of V_{PUMP} to the FPGA is labeled with "106," which indicates that it is connected to pin 106. Similarly, SW4 has a jumper above it called JP14, which is labeled with "64," indicating that SW4 is connected through to pin 64 of the FPGA when this jumper is in place.

Disconnecting the jumpers JP11, JP12, JP13, and JP14 causes the momentary push button switches (SW1, SW2, SW3, and SW4 respectively) to be disconnected from the FPGA so that the I/O pins 68, 67, 66, and 64 may be used for other purposes. Disconnecting the eight jumpers, JP1 through JP8, causes the eight Light Emitting Diodes (D1 through D8) to be disconnected from the FPGA I/O pins 63, 61, 60, 59, 58, 57, 56, and 55, respectively.

The momentary push button switches (SW5 and SW6, for applying a reset pulse and a global pulse) are connected via jumpers JP15 and JP16 to I/Os 159 and 113 respectively. Again, all labeling is clearly shown on the silk screen.

The hex switches U13 and U14 each are connected to four I/Os on the FPGA. There are four separate jumpers for each of these hex switches, located on the bottom right of the board. They are labeled with Bit0, Bit1, Bit2, and Bit3 on the silk screen, as well as being labeled with the I/O pin on the FPGA to which each is connected. This allows you to individually control the desired effect of a switch and, by connecting directly to the FPGA side of a disconnected jumper, hold a particular pin at a chosen logic level while continuing to use the hex switch to affect other pins. This flexibility is useful for experimentation with designs of your own choosing and connecting other external equipment to the board for development purposes.

The internal and external oscillator selection via JP24 is worth a mention. JP24 is a three-pin header onto which a normal two-hole shunt is fitted. Normally the shunt is connected across pins 3 and 2 of JP24. In this position the on-board oscillator, U1, provides the internal clock to the middle pin of the jumper which in turn is connected to pin 26 of the FPGA. By moving the shunt down to connect pins 2 and 1 of JP24, the external clock at pin 1 is connected to the FPGA instead. The external clock is connected via the SMA connector J19 at the bottom left of the board.

The LCD display also has associated jumpers for the data: JP41, JP42, JP43, and JP44, located on the top left side of the board. These are connected to I/O pins 197, 198, 194, and 193 respectively. The LCD control signals "Enable," "R/W," and "RS" are provided from I/O pins 190, 192, and 191 via jumpers JP47, JP45, and JP46 respectively.

Test Points

All test points on the board are fitted with small test loops. These test points are labeled on the silkscreen as TP1, TP2, etc. All such test points are also labeled on the silk screen with the voltage expected to be observed at that test point. Voltages will be one of 3.3 V, 2.5 V, 1.8 V, 1.5 V or GND. When measuring the voltage at a test point with a DVM (digital voltage multimeter), the ground lead should be connected to a test point labeled GND and the voltage lead should be connected to the voltage to be tested. All voltage labels on the board are relative to a 0 V ground reference or GND.

Prototyping Area

The prototyping area to the right of the board has the bottom two rows of pins connected to ground, labeled as GND on the silk screen and enclosed in a box, giving 16 holes connected to 0 V. The top two rows of pins are connected to various power supply rails internally in the board. They are grouped into squares of four pins from left to right as follows: 3.3 V, 2.5 V, 1.8 V, and 1.5 V, giving four holes for each voltage level. All other holes in the prototyping area are unconnected and may be used to hold various discrete components as necessary for experimentation.

Next to the prototyping area is U2, which is a space for an optional oscillator. This space may be used for fitting a second oscillator to the board, similar to the one used at U1, so as to provide two different frequency clocks to the FPGA.

On the reverse side of the board, there is an area labeled U5, which is a TQ100 pattern with some surrounding pads. This area may be used to solder a TQ100 part, and then connect that part by adding discrete wires to the pads and connecting it to desired pins on the board. The main purpose of this is to allow a previously programmed TQ100 packaged device to be used to provide a more interesting system application.

Layering on Board

The complete board design and manufacturing files are included on the Starter Kit CD. The board file is in Allegro format, which will allow an end user to create the appropriate Gerbers and other board views as needed. Pictures of the layers of the board are also attached in Appendix C of this User's Guide. For your convenience, high-resolution PDFs of these layers are also provided on the Starter Kit CD.

The board is fabricated with 6 layers of copper. The layers are arranged as follows from the top of the board down to the bottom:

Layer 1 – Top signal layer

Layer 2 – Ground Plane

Layer 3 – Signal layer 3, used for LVDS receive and other signals

Layer 4 – Signal layer 4, used for LVDS transmit and other signals

Layer 5 – Power Plane

Layer 6 – Bottom signal layer

Note: It will be noted for signal integrity that the two LVDS layers are sandwiched between ground and power planes to isolate them as best as possible from external influences.

Refer to the diagrams in "Signal Layers" on page 93.

Clock Circuits

The ProASIC3/E Evaluation Board has two clock circuits: a 40 MHz oscillator and a manual clock.

40 MHz Oscillator

The 40 MHz oscillator on the board is a 10 ppm stability crystal module which will give good LVDS performance. Should better stability be required, an external oscillator may be provided via the SMA connector. Typically a TCXO will give 1 ppm stability and an OCXO will give 0.1 ppm stability. Both the default on-board oscillator and the SMA are connected to the CLK F input of the West bank of the FPGA. Position is also provided on the board for mounting a second crystal oscillator module connected to the CLK C input of the FPGA on the East bank.

LED Device Connections

Eight LEDs are connected to the device via jumpers. If the jumpers are in place, the device I/O can drive the LEDs. The LEDs change based on the following output:

- A '1' on the output of the device lights the LED.
- A '0' on the output of the device switches off the LED.
- An unprogrammed or tristated output may show a faintly lit LED.

Note: If the I/O voltage of Bank 5 (on A3PE, set by SW8) or Bank 2 (A3P, set by SW8 and SW7 being at the same level) is not at least 2.5 V, the LEDs will not illuminate. A setting of 1.8 V on the voltage bank will cause extremely faint illumination.

Table 2-1 on page 18 lists the LED/device connections.

To use the device I/O for other purposes, remove the jumpers.

Table 2-1 · LED Device Connections

LED	Device Connection
D1	U8 Pin 63
D2	U8 Pin 61
D3	U8 Pin 60
D4	U8 Pin 59
D5	U8 Pin 58
D6	U8 Pin 57
D7	U8 Pin 56
D8	U8 Pin 55

Switches Device Connections

Four switches are connected to the device via jumpers. If the jumpers are in place, the device I/O can be driven by the switches listed in Table 2-2.

- Pressing a switch drives a '1' into the device. The '1' continues to drive while the switch is in place.
- Releasing a switch drives a zero into the device.

Table 2-2 lists the switch/device connections.

To use the device I/O for other purposes, remove the jumpers.

Table 2-2 · Switch Device Connections

Switch	Device Connections
SW1	U8 Pin 68
SW2	U8 Pin 67
SW3	U8 Pin 66
SW4	U8 Pin 64

FPGA – LCD Interface

An 8 × 1 LCD module is provided on the ProASIC3 Evaluation board for demonstrating the board's functionality. Table 2-3 provides detailed information about the LCD module.

Table 2-3 · LCD Module Details

Part Number	MDLS-81809-SS-LV-G-LED-04-G
Manufacturer Name	VARIRONIX
Display Type	STN - Super-Twisted Nematic
Display Mode	Transflective
Display Format	8 × 1
Character Format	5 × 8 Dots
Character Size	6.45 mm × 10.75 mm
Backlight	LED Backlighting - Green
Viewing Area	61mm × 15.8mm
Operating Temperature	-5°C to +50°C
Voltage-Supply	5 V

Description

The LCD module MDLS-81809-SS-LV-G-LED-04-G can be operated in either 4-bit data mode or 8-bit data mode. In this PA3 evaluation board, the above LCD module is being operated in 4-bit data mode to minimize the number of FPGA lines committed to the interface. The 4-bit data lines (DB4, DB5, DB6, and DB7) and the required control signals for this LCD module, specifically RS (Register Select), R/~W (Read/~Write), and E (Enable) lines, are driven from BANK0 I/O lines of FPGA. These BANK0 I/O lines of FPGA are configured as LVTTL outputs for driving the LCD.

Both V_{CCI} and VMV power points of Bank0 are from a fixed 3.3 volts source, thereby enabling BANK0 to function in LVTTL mode.

The interconnection details between the FPGA and the LCD module are listed in Table 2-4 on page 19.

Table 2-4 · FPGA – LCD Interconnections

FPGA Pin No.	LCD Pin No.	LCD Pin Name
197	14	DB7
198	13	DB6
194	12	DB5
193	11	DB4
192	5	R / ~W (Read / ~Write)
191	4	RS (Register Select)
190	6	E (Enable)

When the user of the evaluation board is in need of these BANK0 I/O lines of FPGA for his application, the shorting links inserted on the 2-pin headers JP41, JP42, JP43, JP44, JP45, JP46, and JP47 are to be removed. Refer to Figure B-6 on page 87. These BANK0 I/O lines of FPGA are also available on J14, J15, J16, and J17 for user evaluation.

Caution

Both the removal and insertion of shorting links on the JP41, JP42, JP43, JP44, JP45, JP46, and JP47 must be carried out only when the entire PA3 evaluation board is in powered OFF condition.

Note: Using an R40 potentiometer, the contrast of letters displayed on the LCD can be varied.

LCD Power Supply Circuit

Power to the LCD module power supply is sourced from the LM2674M-5.0 switching regulator, which can provide up to 500 mA.

Description

The MDLS-81809-SS-LV-G-LED-04-G LCD module requires a 5 V power supply. This is derived from VIN (DC power jack J18). From VIN, which is at most 24 volts DC, the 5 volts required for the LCD module is derived using the LM2674M-5.0 high efficiency 500 mA switching regulator U20.

The ON/OFF control required for the U20 is controlled by SW11.

Note: SW11 also controls U11 and hence all the board regulator power supplies.

The presence of the LCD power supply (5 V) from U20 is indicated by the LED D17. The glowing of D17 indicates the presence of a 5 V power supply.

When the user of the PA3 evaluation board does not need the LCD at all, the shorting links on JP41, JP42, JP43, JP44, JP45, JP46, and JP47 headers are to be removed. Follow the procedure listed in "Caution" note on page 20.

Refer to Figure B-11 on page 92 for the LCD power supply circuit details.

LVDS Channels

Four LVDS channels with up to a maximum signaling rate of 350 MHz are supported on the evaluation board. These LVDS signals are brought out to a pair of RJ-45 (CAT-5E) sockets (J40 and J41). Refer to the PA3 Evaluation board PCB layout, Figure 2-1 on page 10, for the position of these connectors.

The LVDS signals are driven using 8 differential pairs (consisting of 16 I/O pins) from the west side (Bank6 and Bank7) of the FPGA device A3PE600-PQ208. These 16 signals are terminated on the J40 and J41 connectors. The FPGA Pins used for LVDS signaling are listed in Table 2-4 on page 19.

The LVDS signals are terminated on J40 and J41 connectors so that a standard patch cable can be used for doing loop-back testing. Refer to Figure 2-1 on page 10 of the PA3 evaluation board schematics for schematic representation of connector signal details.

The 4 differential pairs (consisting of 8 I/O pins) are terminated as shown in Table 2-5 using the color convention on the first RJ45 connector (which we'll call "CAT 5E Primary" for the purposes of differentiating it).

Table 2-5 · Color Convention on CAT 5E Primary

White/Orange	p1	TX1+
Orange	p2	TX1–
White/Green	p3	RX1+
Blue	p4	TX2–
White/Blue	p5	TX2+
Green	p6	RX1–
White/Brown	p7	RX2+
Brown	p8	RX2–

Notes:

1. *TXn+ refers to positive signal of the transmit side of balanced signal Transmission.*
2. *TXn– refers to negative signal of the transmit side of balanced signal Transmission.*
3. *RXn+ refers to positive signal of the receive side of balanced signal Transmission.*
4. *RXn– refers to negative signal of the receive side of balanced signal Transmission.*

The 4 differential pairs (consisting of 8 I/O pins) are terminated as shown in Table 2-6 using the following color convention on the second LVDS connector (which we'll call "CAT 5E SECONDARY" for the purposes of differentiating it).

Table 2-6 · Color Convention on CAT 5E Secondary

White/Orange	p1	RX3+
Orange	p2	RX3–
White/Green	p3	TX3+
Blue	p4	RX4–
White/Blue	p5	RX4+
Green	p6	TX3–
White/Brown	p7	TX4+
Brown	p8	TX4–

Note: The colors refer to the colors that will appear on the CAT 5E cable. The pin numbers correspond to the pin numbers of an RJ-45 connector. Note that the CAT-5E PRIMARY connections are labeled for the purposes of what is regarded as standard connections for CAT-5E on Ethernet-type connectors. The connections on the CAT-5E SECONDARY are reversed so as to allow a standard patch cable to check loopback on these LVDS signals.

A 1-foot CAT5 standard patch cable supplied with the PA3 evaluation kit can be used for LVDS signals loopback.

Also note that the V_{CCI} and VMV voltages of Bank6 and Bank7 (west side) are connected to a fixed 2.5 volts, which is required in ProASIC3 (LVDS only available in A3P250 and larger) and ProASIC3E (LVDS available in all devices) for LVDS signaling.

Table 2-7 · FPGA – LVDS I/O Pin Details

FPGA Pin No.	FPGA I/O Pin Name[1]	Signal Name	CAT5E Connector Pin No.
7	GAC2/IO132PDB7V1	TX1+	CAT 5E – PRI –1
8	IO132NDB7V1	TX1–	CAT 5E – PRI –2
9	IO130PDB7V1	TX2+	CAT 5E – PRI – 5
10	IO130NDB7V1	TX2–	CAT 5E – PRI – 4
11	IO127PDB7V1	RX1+	CAT 5E – PRI –3
12	IO127NDB7V1	RX1–	CAT 5E – PRI – 6
13	IO126PDB7V0	RX2+	CAT 5E – PRI – 7
14	IO126NDB7V0	RX2–	CAT 5E – PRI – 8
30	GFA2/IO117PDB6V1	TX3+	CAT 5E – SEC –3
31	IO117NDB6V1	TX3–	CAT 5E – SEC –6
37	IO112PDB6V1	TX4+	CAT 5E – SEC – 7
38	IO112NDB6V1	TX4–	CAT 5E – SEC – 8
42	IO106PDB6VO	RX3+	CAT 5E – SEC –1
43	IO106NDB6V0	RX3–	CAT 5E – SEC – 2
44	GEC1/IO104PDB6V0	RX4+	CAT 5E – SEC – 5
45	GEC0/IO104NDB6VO	RX4–	CAT 5E – SEC – 4

Notes:

1. *Pin names are valid only for the A3PE600-PQ208 part. They are not correct for use with an A3P250.*
2. *J40 – RJ45 connector is referred as CAT 5E PRIMARY connector.*
3. *J41 – RJ45 connector is referred as CAT 5E SECONDARY connector*

Refer to the PCB layout, Figure 2-1 on page 10, for the location of J40 and J41 connectors on the PA3 Evaluation board.

3 Setup and Self Test

This chapter outlines how to set up and test the ProASIC3/E Evaluation Board.

Software Installation

The ProASIC3/E Starter Kit includes the Libero® Integrated Design Environment (IDE) software (version 2.3 SP2). For Libero IDE software installation instructions, refer to the *Actel Libero IDE / Designer Installation and Licensing Guide:* http://www.actel.com/documents/install_ug.pdf.

Hardware Installation

FlashPro3 is required to use the ProASIC3/E Starter Kit. For software and hardware installation instructions, refer to the *FlashPro User's Guide*: http://www.actel.com/documents/flashpro_ug.pdf

Testing the Evaluation Board

Refer to "Test Procedures for Board Testing" on page 67.

Programming the Test File

To retest the evaluation board at any time, use the test program to reprogram the board. Use the TOP_A3PE.stp file with an A3PE600-PQ208 fitted on the board. Use TOP_A3P.stp with an A3P250-PQ208 fitted on the board.

This design is currently implemented for the A3PE600 die size. For a device of a different size, it is possible to recompile the design into other device sizes. For information about retargeting the device, refer to the *Designer User's Guide* at http://www.actel.com/documents/designer_ug.pdf. The design files are available under *actelprj/eval* in the Starter Kit CD.

For instructions on programming the device using FlashPro3, refer to the FlashPro User's Guide.

4 Description of Test Design

This description of the test design is provided with the Starter Kit. This design contains a data generator block for LEDs, clock divider, and an LCD display block. A block diagram of the design is shown in Figure 4-1.

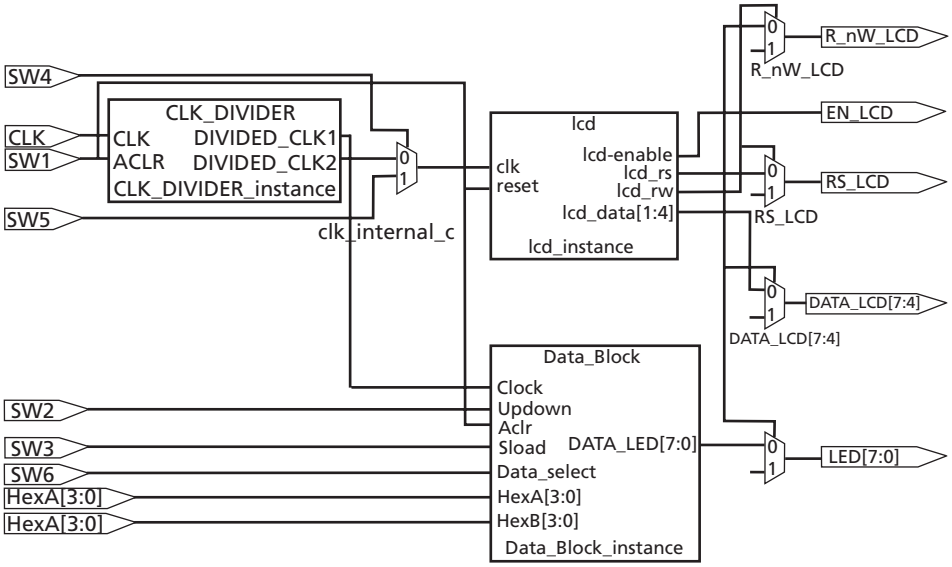

Figure 4-1. Design Block Diagram

The clock divider divides the 40 MHz oscillator clock and sends the divided clock to the LCD module and the counter. The data generator (Data_Block) generates an eight-bit up-down counter and eight-bit flashing signal. The data generator output is displayed on the ProASIC3E demo board LEDs. You can switch between the data using the SW6 signal. The counter has a synchronous load and an asynchronous clear.

A block diagram of the Data_Block is shown in Figure 4-2.

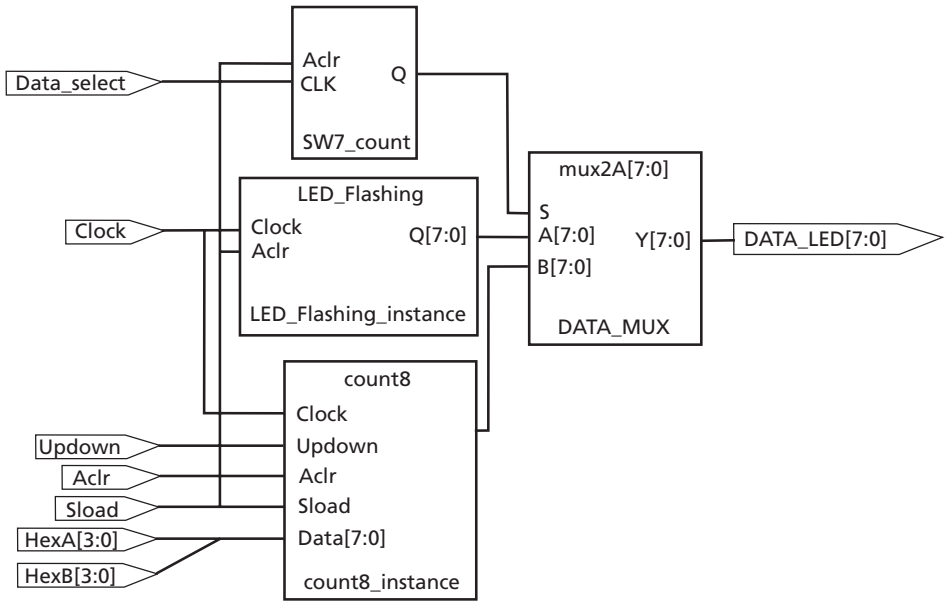

Figure 4-2. Data Block Diagram

A message is generated and displayed on the demo board LCD display. A state machine controls the LDC module.

Table 4-1 · Switches

Action	Results
Press SW1	Asynchronous clear for the whole design
Press SW2	Up-Down Control for the 8-bit counter. Press and hold SW2 for down count.
Press SW3	Synchronous load for the 8-bit counter. Press SW3 for loading from the Hex switches.
Press SW4	Switching between manual clock(SW5) and 40 Mhz Oscillator Clock.
Press SW5	Manual clock (very useful for simulation)
Press SW6	Select for DATA_BLOCK. It allows switching LED output between the counter and Flashing data.
Change Hex Switch setting (U13 and U14)	Changes the loaded data for the eight-bit counter.

The state diagram is shown in Figure 4-3.

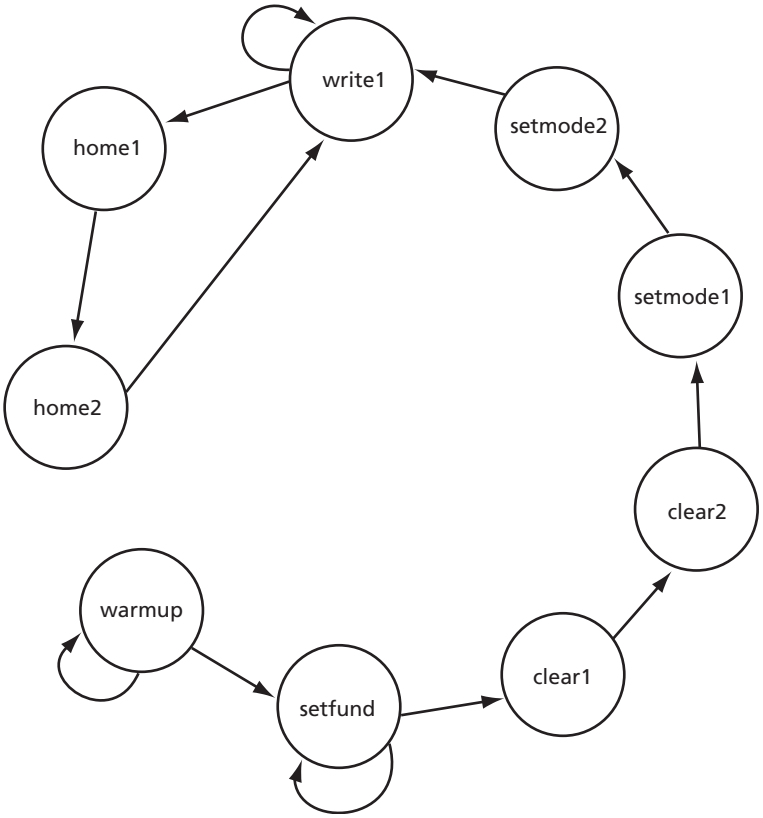

Figure 4-3. LCD State Diagram

5 LVDS Signal Evaluation

Introduction

Due to concerns about the Proasic3 Dev-Kit board layout with respect to the LVDS signaling, the Applications Consulting group took initiative to evaluate the LVDS signaling on the board. The performance criteria of the board with respect to LVDS signaling is set to 300 Mb/s per product marketing.

This document explains the test setup and design. It reports the measurements performed on the board, and at the end, makes recommendations to increase the LVDS signal quality in order to meet the performance criteria.

Test Setup

Hardware

The test setup uses a ProASIC3 Dev-Kit containing an A3PE600-PQ208 engineering sample. LVDS loopback is closed using various lengths of CAT-5E cables (1-, 3-, and 6-foot). The measurements are taken using a 1159A-1GHz Agilent differential probe.

Design

Figure 5-1 on page 29 shows the block diagram of the transmitter section of the test design programmed inside the Proasic3 FPGA. As shown in Figure 5-1 on page 29, the design contains two similar channels of data. One channel (channel A) is driven by PLL to achieve high data rates, and the other (channel B) uses an external clock in case slow data rates are needed for test or debugging purposes.

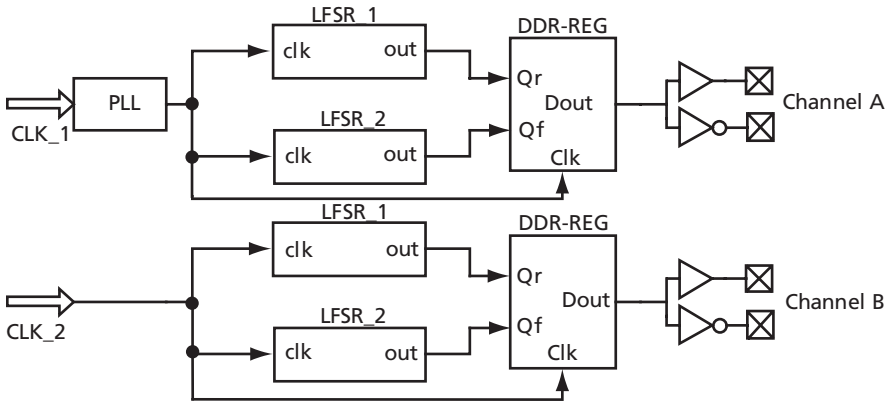

Figure 5-1. TX Portion of Test Design

Each channel uses an LFSR to generate a pseudo-random data stream. The data stream is entered in DDR registers to achieve higher data rates from relatively slower clocks (e.g., 300 Mb/s data rate from 150 MHz clock). The output of the DDR registers is sent out using the LVDS I/O standard. The output data is looped back and received by the FPGA using LVDS receivers.

Measurement Results

Figure 5-2 shows the LVDS signal across the 100 Ohm termination resistor at 300 Mb/s. Figure 5-2 shows that the eye height across the termination is about 275 mV which is well within the LVDS spec.

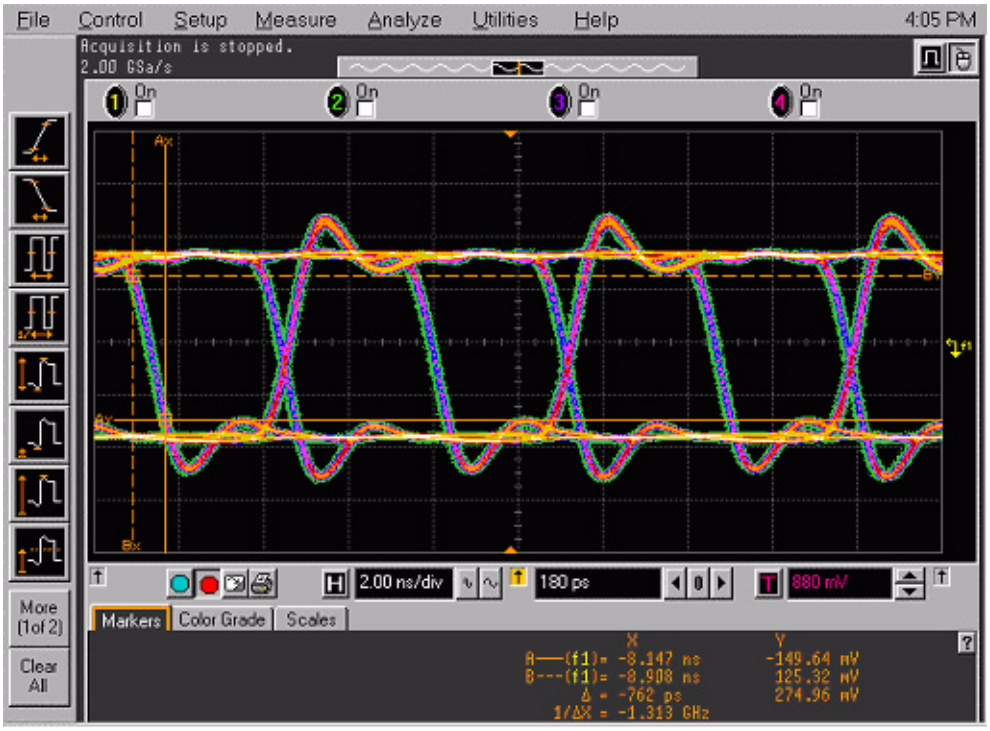

Figure 5-2. LVDS Signal across RX Termination at 300Mb/s

6

Actel VHDL ProASIC3/E Design Flow

This chapter introduces the design flow for VHDL using the Actel Libero IDE software suite. This chapter also briefly describes how to use the software tools and provides information about the sample design. Figure 6-1 shows the VHDL-based design flow.

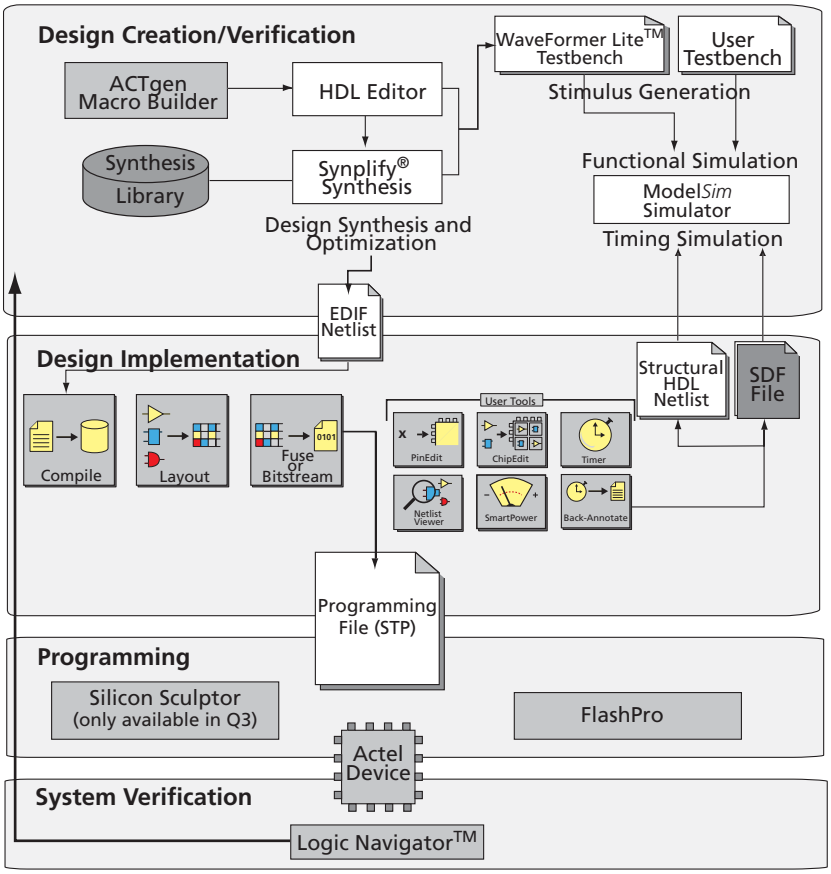

Figure 6-1. VHDL-Based Design Flow

The Libero IDE design flow has four main components:

- Design Entry
- Design Implementation
- Programming
- System Verification

Design Entry

Design entry consists of capturing a schematic representation of the design and performing functional simulations with a test bench.

Design Capture

For schematic capture, Libero uses ViewDraw® for Actel, which includes a schematic editor. The schematic editor provides a graphical entry method to capture designs. ViewDraw for Actel is the Libero IDE integrated schematic entry vehicle, supporting mixed mode entry in which HDL blocks and schematic symbols can be mixed.

The ViewDraw *wir* file is automatically created after using the **Save + Check** command in ViewDraw. This file is used to create the structural HDL netlist.

For more information on using ViewDraw for Actel, refer to the Libero User's Guide.

Adding ACTgen Macros

Use the ACTgen Macro Builder to instantly create customized macros and then use ViewDraw to add these macros to a schematic. Alternatively, add the ACTgen Macros in the HDL file.

Creating and Adding Symbols for HDL Files

Schematic users can encapsulate a HDL block into a block symbol.

To create a symbol:

1. Right-click the block in the **Design Hierarchy** window of Libero IDE.
2. Click **Create Symbol**. Libero IDE generates a symbol for the selected HDL block.

   The macro is accessible from the components list in ViewDraw for Actel.

Test Bench Generation

It is necessary to create a test bench and associate it with a project in order to run a simulation. WaveFormer Lite™ from SynaptiCAD™ is the Libero IDE integrated test bench generator. WaveFormer Lite fits perfectly into the Libero IDE, automatically extracting signal information from HDL design files, and producing HDL test bench code that can be used with any standard VHDL or Verilog simulator.

WaveFormer Lite generates VHDL and Verilog test benches from drawn waveforms.

Pre-Synthesis Simulation

Functional simulation verifies that the logic of a design is functionally correct. Simulation is performed using the Libero IDE integrated simulator, Model*Sim* for Actel, which is a custom edition of Model*Sim* PE that is integrated into the Libero IDE. Model*Sim* for Actel is an OEM edition of Model Technology Incorporated (MTI) tools. Model*Sim* for Actel supports VHDL or Verilog, but it can only simulate one language at a time. It only works with Actel libraries and is supported by Actel.

Synthesis & Netlist Generation

After entering the design source, synthesize it to generate a netlist. Synthesis transforms the behavioral HDL source into a gate-level netlist and optimizes the design for a target technology.

For more detailed information on the above topics, refer to the Libero User's Guide.

Design Implementation

During design implementation, Actel Designer places-and-routes the design.

Place-and-Route

Start Designer from Libero IDE to place-and-route the design.

Timing Simulation

Perform timing simulation on the design after place-and-route in Designer. Timing simulation requires information extracted and back-annotated from Designer.

Optional Tools

The tools listed in Table 6-1 provide optional functions that are not required in a basic design. Use these tools to perform static timing analysis, power analysis, customize I/O placements and attributes, and view the netlist. After place-and-route, perform the post-layout (timing) simulation.

Table 6-1 · Designer User Tools

Designer User Tools	User Tool Function
Timer	Static timing analysis
SmartPower	Power analysis
ChipEdit	Customize I/O and logic macro placements
PinEdit	Customize I/O placements and attributes
Netlist Viewer	View your netlist and trace paths

For more information on the tools described in the above section, refer to the Designer User's Guide.

Programming

Program the device with programming software and hardware from Actel or a supported third party programming system. Refer to the Designer User's Guide, Silicon Sculptor User's Guide, and FlashPro User's Guide for information about programming an Actel device. These guides can be found at http://www.actel.com/techdocs/manuals/default.aspx.

System Verification

Use the Logic Navigator tool to perform system verification on a programmed device.

7 Quick Start Tutorial

This tutorial illustrates a VHDL design for a ProASIC3/E starter kit board. The design is created in Actel Libero IDE v6.2. The steps involved are as follows:

Step 1 – Create a New Project

This step uses the Libero IDE HDL Editor to enter an Actel VHDL design.

To create the VHDL project:

1. Double-click the **Libero IDE** icon on your desktop to start the program.
2. From the **File** menu, select **New Project**. This displays the New Project Wizard, as shown in Figure 7-1.

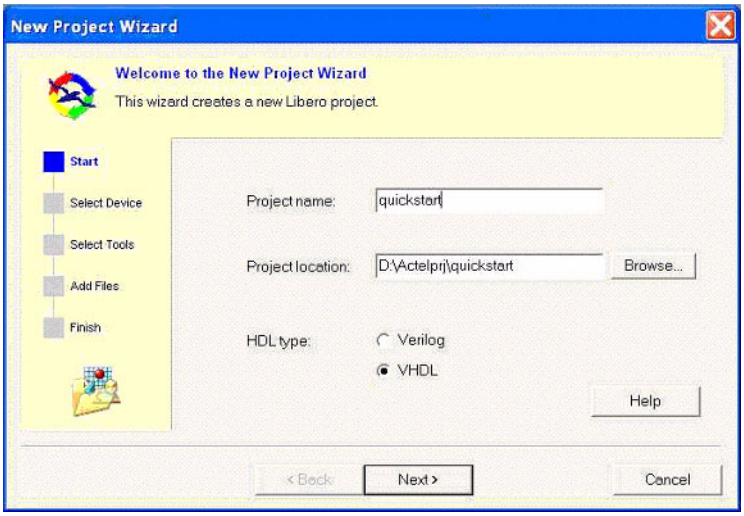

Figure 7-1. New Project Wizard in Libero IDE

3. Enter your **Project name**. For this tutorial, name your project **quickstart**.
4. Select your HDL type.
5. If necessary, in the Project location field, click **Browse** to navigate to *C:\Actelprj*. Click **Next** to continue.

6. Select your project **Family**, **Die**, and **Package**. For this tutorial, you can select **ProASIC3E**, the **A3PE600** die, and **208 PQFP** for the package (Figure 7-2), or select **ProASIC3**, the **A3P250** die, and **208 PQFP** for the package (Figure 7-3).

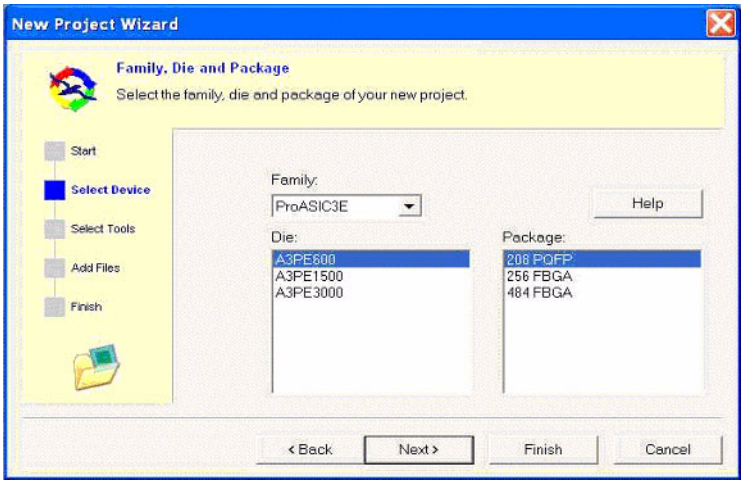

Figure 7-2. Select A3PE600-PQ208

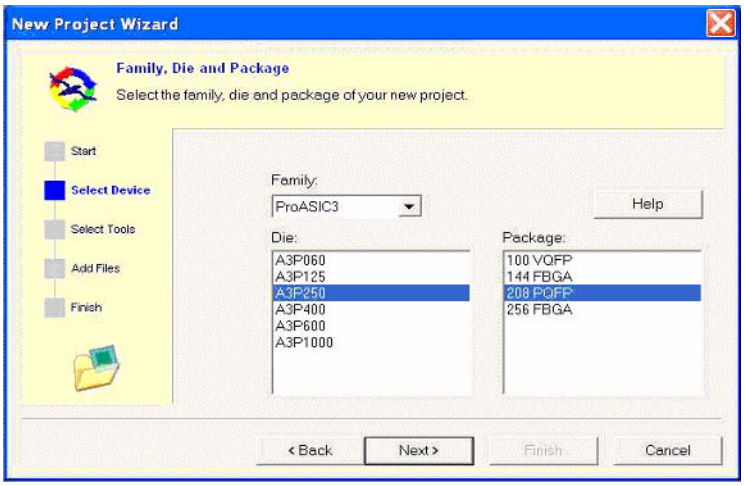

Figure 7-3. Select A3P250-PQ208

7. Click **Next** to select **Integrated Tools** in the **New Project Wizard** (Figure 7-4).

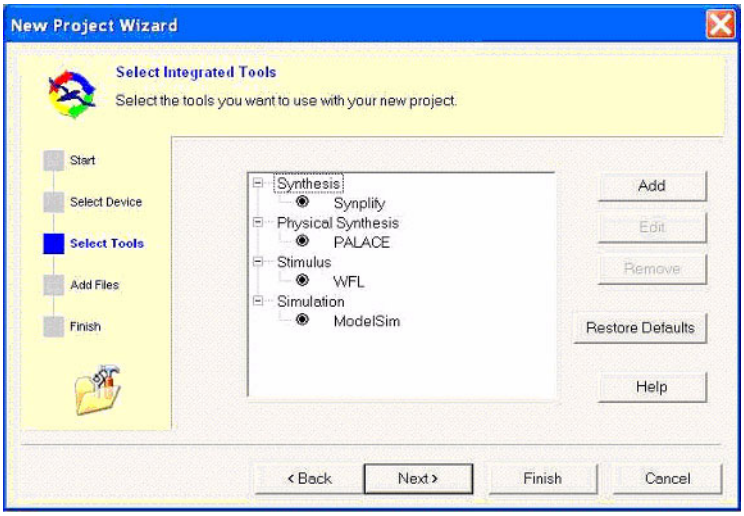

Figure 7-4. Selected Integrated Tools in New Project Wizard (Libero IDE)

8. Click the **Restore Defaults** button to use the default tools included with Libero IDE.
9. Click the **Add** button to add a different Synthesis, Simulation, or Stimulus tool. If you wish to add a tool, Libero IDE opens the **Add Profile** dialog box (Figure 7-5).

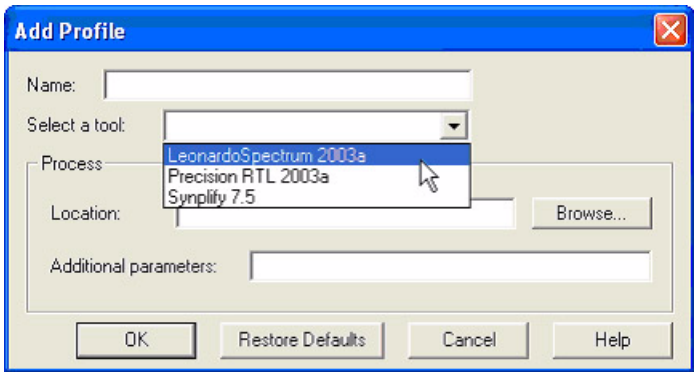

Figure 7-5. Add Profile Dialog Box in Libero IDE

10. Name your profile, select a tool from the list of Libero IDE supported tools, and **Browse** to the **Location** of your tool. Click **OK** to return to the New Project Wizard.
11. After you have selected your tools, click **Next** to continue.

12. Click **Add Files** in the New Project Wizard to add existing project design files. Include any ACTgen cores, Block Symbol Files, Schematic Files, VHDL Packages, HDL Source Files, Implementation files, and Stimulus Files (Figure 7-6).

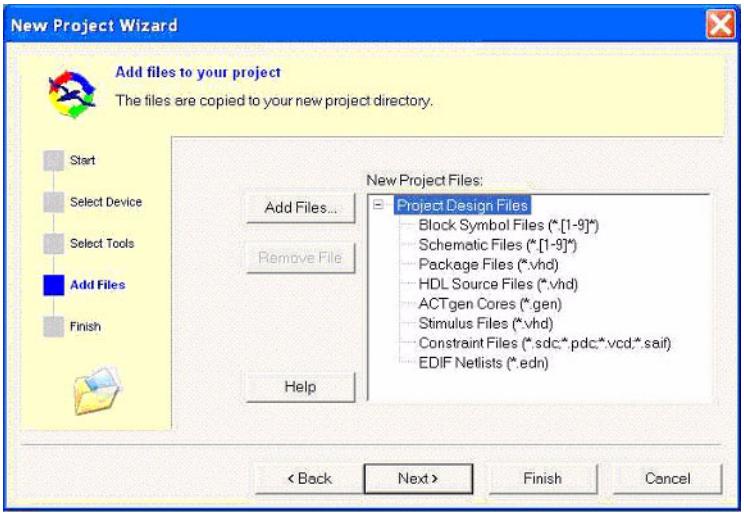

Figure 7-6. Add Files in the New Project Wizard (Libero IDE)

13. Select the file type and click **Add Files**. Browse to your file, and click **Add**. Add as many files as you wish in this way. Click **Next** to continue.
14. Review your project information. Click **Finish** to close the Wizard and create your new project (Figure 7-7). Click **Back** to return to any step of the Wizard and correct information in your project.

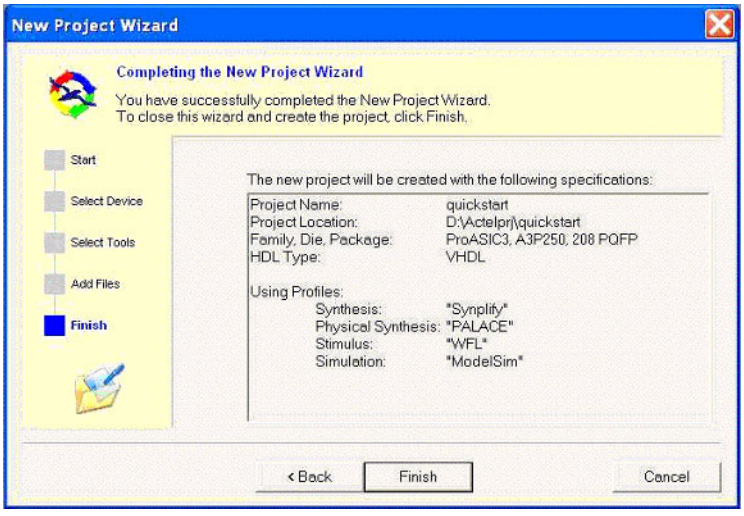

Figure 7-7. Summary in New Project Wizard

Your Libero IDE project exists, but you must add code or source to the project, such as a schematic, an ACTgen core, or a VHDL entity or package file, before you can run synthesis.

To add HDL to your project:

1. From the **File** menu, click **New**. This opens the New dialog box, as shown in Figure 7-8.

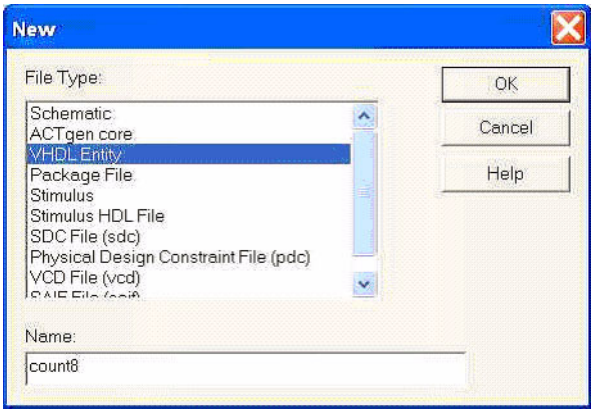

Figure 7-8. New File Dialog Box

2. Select **VHDL Entity** in the File Type field, enter **count8** in the **Name** field, and click **OK**. The HDL Editor opens. Enter the following VHDL file, or if this document is open in an electronic form, copy and paste it from here.

```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_arith.all;
use IEEE.std_logic_unsigned.all;

entity count8 is
  port(Clock : in std_logic;
       Q : out std_logic_vector(7 downto 0);
       Updown : in std_logic;
       Aclr : in std_logic;
       Sload : in std_logic;
       Data : in std_logic_vector(7 downto 0));
end count8;

architecture behavioral of count8 is

  signal Qaux : UNSIGNED(7 downto 0);

begin

  process(Clock, Aclr)
  begin

    if (Aclr = '1') then
      Qaux <= (others => '0');
```

```
    elsif (Sload = '1') then
      Qaux <= UNSIGNED(Data);
    elsif (Clock'event and Clock = '1') then
      if (Updown = '0') then
        Qaux <= Qaux + 1;
      else
        Qaux <= Qaux - 1;
      end if;
    end if;

  end process;

  Q <= std_logic_vector(Qaux);

end behavioral;
```

3. From the **File** menu, click **Save**. The design file counter appears in the Design Hierarchy. Libero IDE lists **count8.vhd** under HDL files in the File Manager, as shown in Figure 7-9.

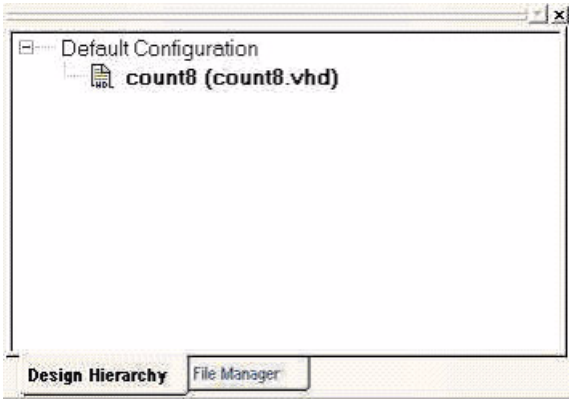

Figure 7-9. Design Hierarchy

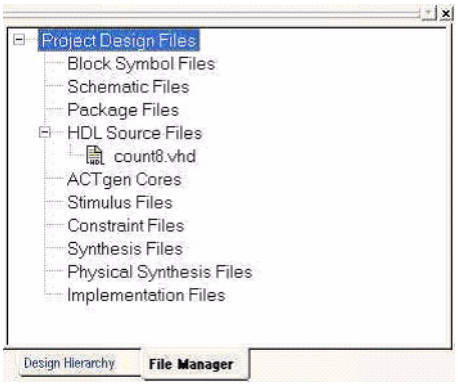

Figure 7-10. Design Hierarchy and File Manager Tabs

4. Check the HDL in the file before you continue. In the Design Hierarchy or File Manager tab (Figure 7-10), right-click **count8.vhd** and select **Check HDL** file. This checks the syntax of the *count8.vhd* file. Before moving to the next section, modify the code if you find any errors.

   The rest of the source code is in the */src* folder. Right-click *Top.vhd* in the design hierarchy and select **Set As Root** so that *Top.vhd* is represented as the top-level file for the project. You can import all the files from the Libero IDE menu, using **File** > **Import Files** (Figure 7-11).

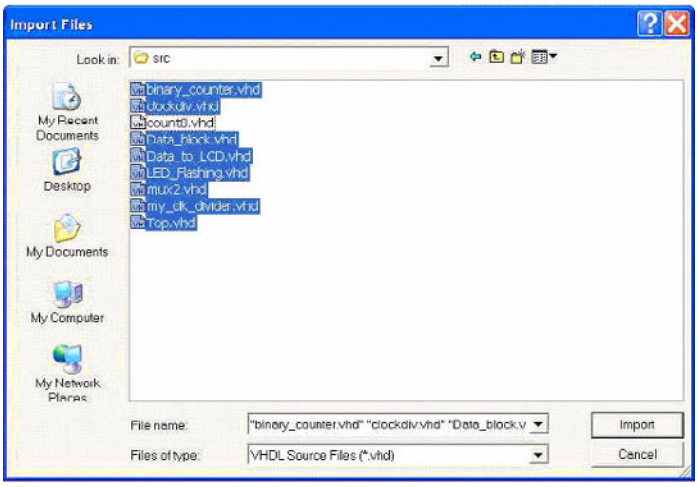

Figure 7-11. Import Source Files

Step 2 – Perform Pre-Synthesis Simulation

The next step is simulating the RTL description of the design. First, use WaveFormer Lite to create a stimulus for the design and then generate a testbench for the design.

Create Stimulus Using WaveFormer Lite

WaveFormer Lite generates VHDL testbenches from drawn waveforms. There are three basic steps for creating testbenches using WaveFormer Lite and the Actel Libero IDE software:

1. Import Signal Information

2. Draw Waveforms
3. Export the Testbench

Import Signal Information

To launch WaveFormer Lite and import signal information:

Right-click the **Top.vhd** file in the Design Hierarchy tab and select **Create Stimulus** > **HDL Source files (source files)**. WaveFormer Lite launches with the port signals in the **Diagram** window, as shown in Figure 7-12.

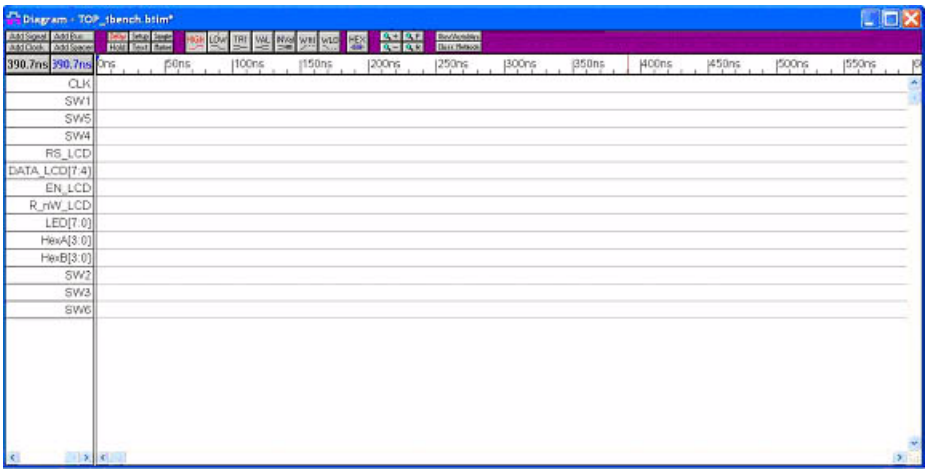

Figure 7-12. WaveFormer Lite Timing Diagram Window

Draw Waveforms

The state buttons are the buttons with the waveforms drawn on their face: HIGH, LOW, TRIstate, VALid, INValid, WHI weak high, and WLO weak low, as shown in Figure 7-13.

Figure 7-13. State Buttons

When a state button is activated, it is pushed in and colored red. The active state is the type of waveform that is drawn next. Click a state button to activate it.

The state buttons automatically toggle between the two most recently activated states. The state with the small red "T" above the name will be the toggle state. The initial activated state is HIGH and the initial toggle state is LOW.

Signal edges are automatically aligned to the closest edge grid when signals are drawn using the mouse. Control the edge grid from the **Options** > **Grid Settings** menu item.

To draw a waveform:

1. Select the **High** state and place the mouse cursor inside the Diagram window at the same vertical row as the signal name.
2. Click the mouse button. This draws a waveform from the end of the signal to the mouse cursor. The red state button on the button bar determines the type of waveform drawn. The cursor shape also mirrors the red state button.
3. Move the mouse to the right and click again to draw another segment.

Copy Waveforms

It is possible to copy and paste sections of waveforms onto (overwrite) or into (insert) any signal in the diagram.

To copy and paste waveform sections:

1. Select the names of the required signals. If no signals are selected, the Block Copy command selects all the signals in the diagram.
2. Select the **Edit** > **Block Copy Waveforms** menu option (choose to select all waveforms, if necessary). This opens the Block Copy Waveforms dialog box (Figure 7-14 on page 43) with the selected signals displayed in the Change Waveform Destination list box.

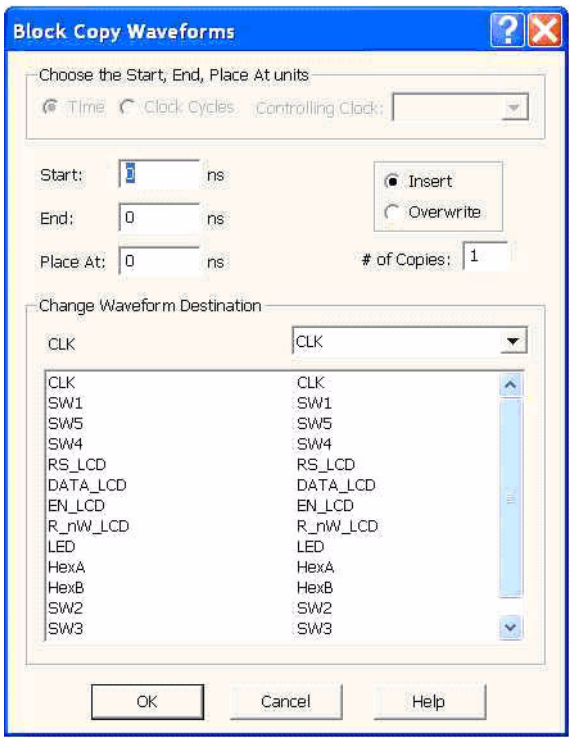

Figure 7-14. Block Copy Waveforms Dialog Box

3. Enter the values that define the copy and paste.
4. Select either **Time** or **Clock** cycle for the base units of the dialog.

   Remember the following:

   When copying only signals (no clocks), time is the default base unit of the dialog.

   When copying part of a clock, it is best to choose a clock cycles base unit and choose the copied clock as the reference clock.

   If you select time when copying clocks, the end_time minus the start_time must equal an integral number of clock periods, and the place_at time must be at the same clock period offset as the start_time.

   Start and **End** define the times of the block copy.

   Place At is the time at which the block will be pasted.

   The **Insert** and **Overwrite** radio buttons determine whether the paste block is inserted into the existing waveforms or overwrites those waveforms.

The list box at the bottom of the dialog determines which signal the copied waveforms will be pasted into.

To change this mapping:

1. Select a line in the list box. This places the destination signal in the drop-down list box on top of the list box.
2. Select another signal from the drop-down list box. Each destination signal can be used only once per copy.
3. Click **OK** to complete the copy and paste operation.

Export the Testbench

In this step you create a stimulus file for the design and generate a testbench using WaveFormer Lite. After exporting the testbench, perform a pre-synthesis simulation using Model*Sim*.

To create a stimulus file and generate a VHDL testbench:

In this step, a design stimulus file is created using WaveFormer Lite. Follow the instructions in the previous sections and define a 20 MHz value for the Clock.

1. Right-click the Clock signal to select it. Select **Signal(s) <-> Clock(s)** to create the clock signal (Figure 7-15).

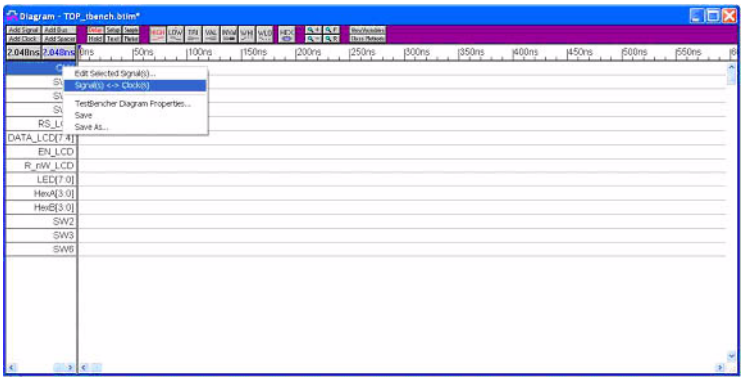

Figure 7-15. Create Clock Signal in Waveformer Lite

2. Double-click any clock segment to edit the clock parameters (Figure 7-16). Set a frequency of 40 MHz.

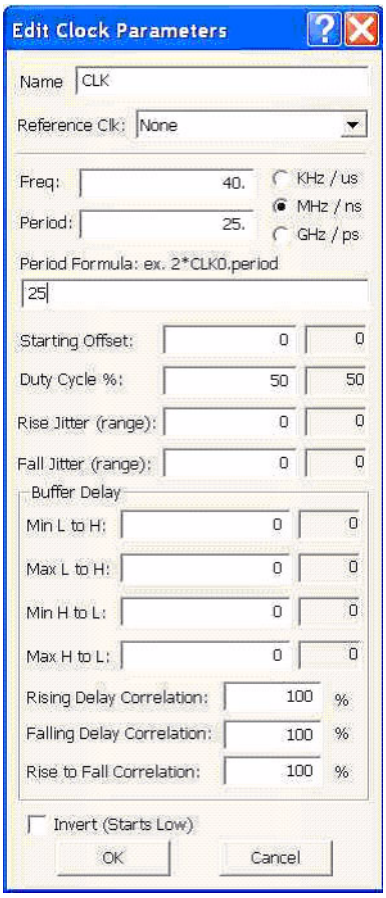

Figure 7-16. Edit Clock Parameters in WaveFormer Lite

This creates the waveform shown in Figure 7-17.

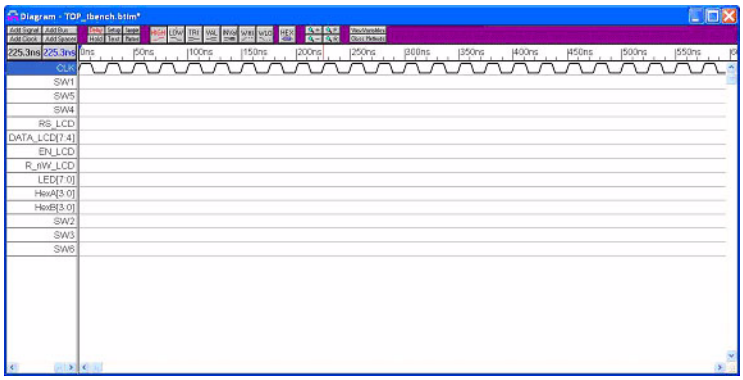

Figure 7-17. WaveForm Timing Diagram

3. Click the **HIGH** state button before you start to draw the SW4 waveform. If you have not selected any other state buttons since you drew the clock waveform, you may continue.

4. Click and drag in the SW4 signal to draw a high segment from 0 to 5 µs. When you release the mouse button, WaveFormer Lite switches your state to LOW.
5. Click and drag in the SW4 signal to draw a low segment from 5 us to 6.8 µs.
6. Follow similar procedure to enter the rest of the input signals. You will get a waveform similar to the one shown in Figure 7-18.

   A waveform was pre-drawn for you and you can find it in the *stimulus* folder.

Figure 7-18. Testbench Waveform for the Tutorial Design

7. After creating the waveforms, select **Save As** from the **File** menu. In the **Save As** dialog box, enter **test_tbench.btim** as the file name and click **Save**.
8. After saving the timing diagram file, select **Export Timing Diagram As** from the **Export** menu.
9. Select **VHDL w/ Top Level Testbench** in **Files of Type** and enter **test_tbench.vhd** for the file name, as shown in Figure 7-19.

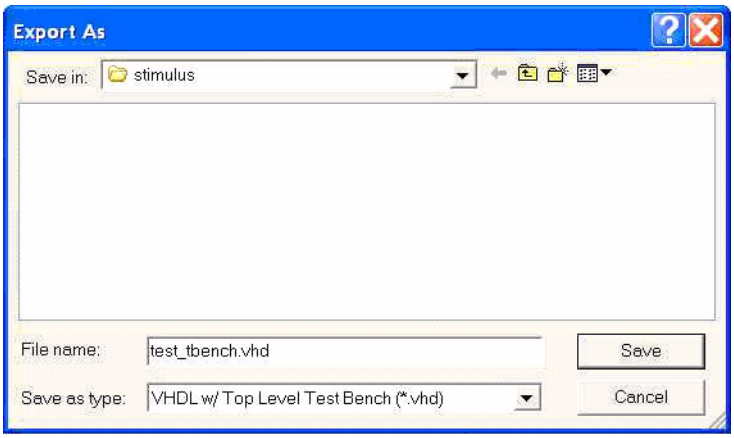

Figure 7-19. Export VHDL Testbench Save As Dialog Box

   The WaveFormer Lite Report window displays the VHDL testbench with a component declaration and instantiation inside.

10. Exit WaveFormer Lite (**File** > **Exit**). The File Manager displays the stimulus files. The design is ready to simulate under Model*Sim*.

Alternatively, you can create a testbench using the HDL editor.

To create a testbench using the HDL editor:

1. From the **File** menu, select **New**. This opens the New File dialog box.

2. Select **Stimulus HDL file** from the **File Type** list, enter **test_tbench** for the name, and click **OK**. The file opens in the HDL Editor.
3. Create the VHDL testbench and save it.

Pre-Synthesis Simulation

Once you generate a testbench, use Model*Sim* to perform a pre-synthesis simulation.

To perform a pre-synthesis simulation:

Right-click **Top.vhd** in the **Design Hierarchy** tab and choose **Organize Stimulus**, as shown in Figure 7-20.

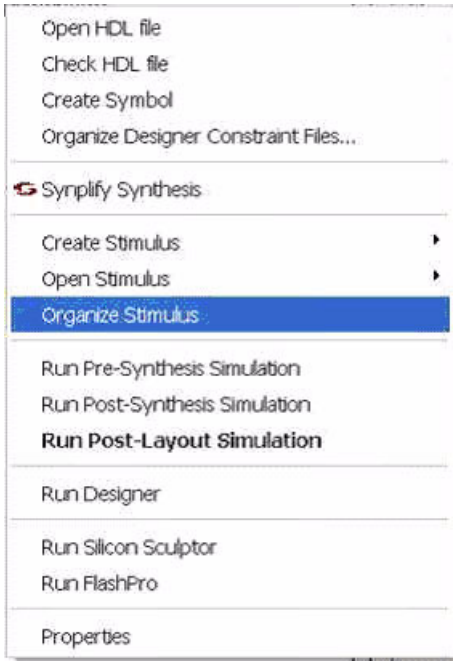

Figure 7-20. Organize Stimulus Files

The Organize Stimulus dialog box appears (Figure 7-21).

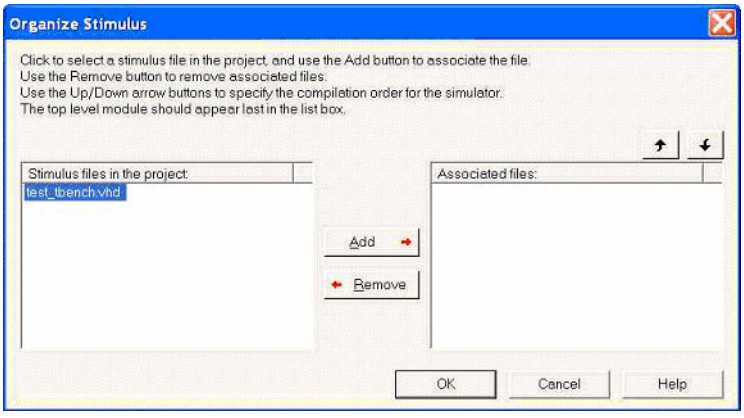

Figure 7-21. Organize Stimulus Dialog Box

4. Select **test_tbench.vhd** in the Stimulus files in the project list box and click **Add** to add the file to the Associated Files list.
5. Click **OK**. Stimulus icons in the Design flow window turn green to notify you that there is a testbench file associated with them.
6. Click the **Simulation** icon in the Design Flow window, or right-click **Top** in the **Design Hierarchy** tab and select **Run Pre-Synthesis Simulation**, as shown in Figure 7-22.

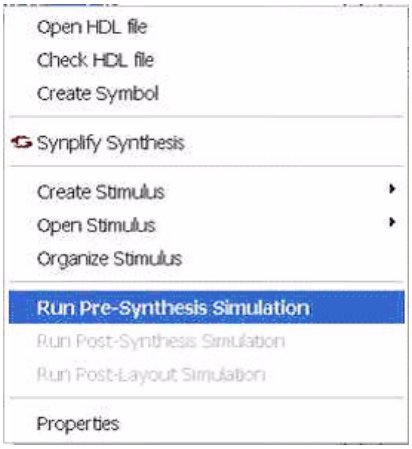

Figure 7-22. Run Pre-Synthesis Simulation

The Model*Sim* VHDL simulator opens and compiles the source files, as shown in Figure 7-23.

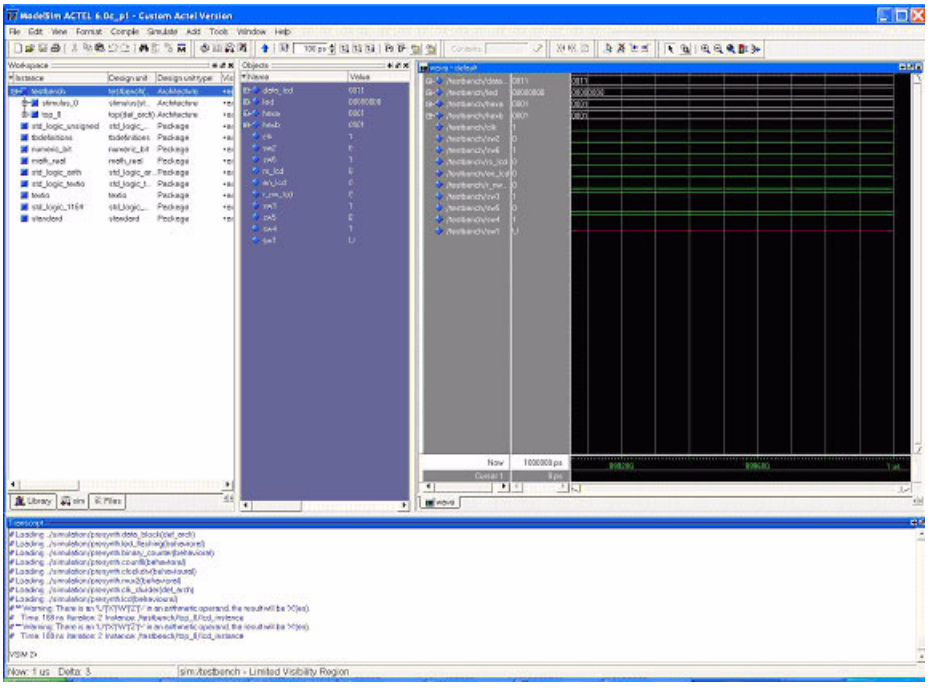

Figure 7-23. ModelSim Main Window

Once the compilation completes, the simulator simulates for the default time period of 1000 ns and a Wave window, shown in Figure 7-24 on page 49, opens to display the simulation results.

7. From the Model*Sim* menu, select **Simulate** > **Run** > **Run All** to execute the full simulation time defined in the testbench. Scroll in the Wave window to verify that the design functions properly.

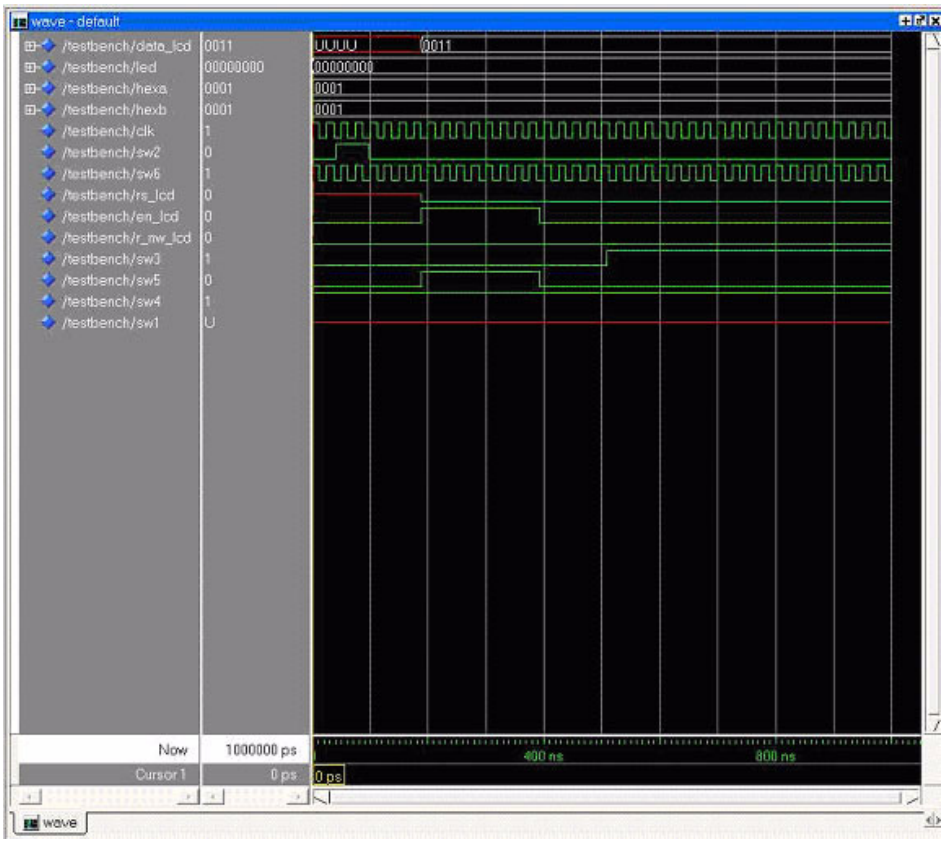

Figure 7-24. Model*Sim* Wave Window

8. In the Model*Sim* window, select **File** > **Quit** to close the window.

Step 3 – Synthesize the Design in Synplify

The next step is to generate an EDIF netlist by synthesizing the design in Synplify. For HDL designs, Libero IDE launches and loads Synplicity Synplify synthesizer with the appropriate design files.

To create an EDIF netlist for the design using Synplify:

1. In the Libero IDE, double-click the Synplify **Synthesis** icon in the Libero IDE process window, or right-click the **Top.vhd** file in the Design Hierarchy and select **Synthesize**. This launches the Synplify synthesis tool with the appropriate design files, as shown in Figure 7-25.

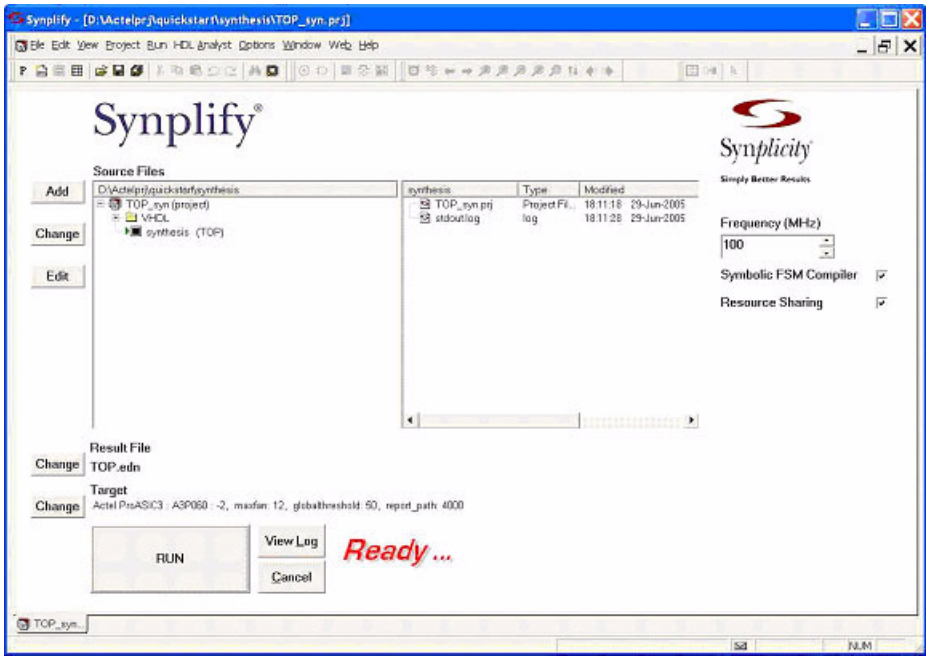

Figure 7-25. Synplify Main Window

2. From the **Project** menu, select **Implementation Options**. This displays the Options for the Implementation dialog box, as shown in Figure 7-26 for A3PE600 and Figure 7-27 for A3P250.

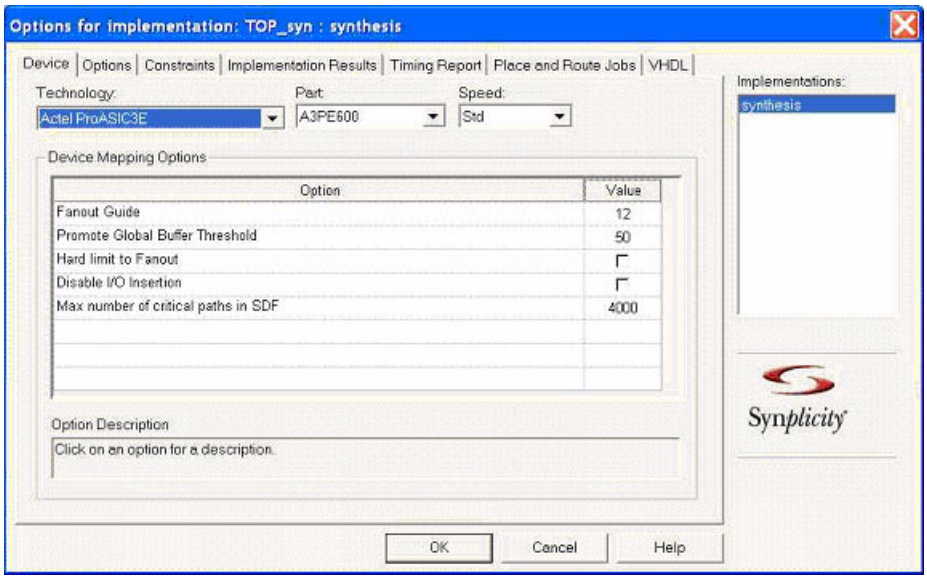

Figure 7-26. Options for Implementation Dialog Box-A3PE600

Set the following in the dialog box:

Technology: Actel ProASIC3E (set by Libero IDE)

Part: A3PE600

Fan-out Guide: 12 (default)

Hard Limit to Fan-out: Off (default). This refers to the fan-out limit.

Accept the default values for each of the other tabs in the Options for Implementation dialog box and click **OK**.

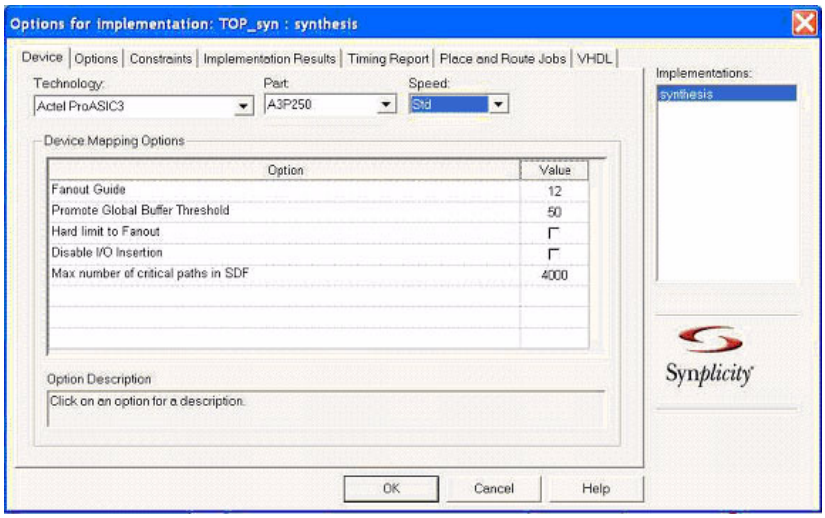

Figure 7-27. Options for Implementation Dialog Box-A3P250

Set the following in the dialog box:

Technology: Actel ProASIC3 (set by Libero IDE)

Part: A3P250

Fan-out Guide: 12 (default)

Hard Limit to Fan-out: Off (default). This refers to the fan-out limit.

Accept the default values for each of the other tabs in the Options for Implementation dialog box and click **OK**.

3. In the Synplify main window, click **Run**. Synplify compiles and synthesizes the design into a netlist called *Top.edn*. The resulting *Top.edn* file is then automatically translated by Libero IDE into a VHDL netlist called *Top.vhd*.

   The resulting EDIF and VHDL files are displayed under Implementation Files in the File Manager.

4. If any errors appear after you click the **Run** button, edit the file using the Synplify editor. To edit the file, double-click the file name in the Synplify window. Any changes made here are saved to the original design file in Libero IDE.

5. Save and close Synplify. From the **File** menu, click **Exit** to close Synplify. Click **Yes** to save any settings made to the *Top_syn.prj* in Synplify.

Step 4 – Perform Post-Synthesis Simulation

The next step is simulating the VHDL netlist of the design using the VHDL testbench created in the section, "To create a stimulus file and generate a VHDL testbench:" on page 44.

1. Click the **Simulation** icon in the Libero IDE Design Flow window, or right-click the **Top.vhd** file in the Design Hierarchy tab and select **Run Post-Synthesis Simulation**. This launches the Model*Sim* Simulator that compiles the source file and testbench.

Once the compilation completes, the simulator runs for 1000 ns and a Wave window opens to display the simulation results.

2. From the Model*Sim* menu, **Simulate** > **Run** > **Run All** to execute the full simulation time defined in the testbench.
3. Scroll in the Wave window to verify that the counter works correctly. Use the zoom buttons to zoom in and out as necessary.

Step 5 – Implement the Design with Designer

After creating and testing the design, the next phase is implementing the Design using the Actel Designer software.

1. Click Designer **Place-and-Route** in the Libero IDE Design Flow window, or right-click **Top.vhd** in the **Design Hierarchy** tab and select **Run Designer**. Designer (Figure 7-28) reads in the design file and opens the Device Selection Wizard (Figure 7-29 on page 53 for A3PE600 and Figure 7-30 on page 53 for A3P250).

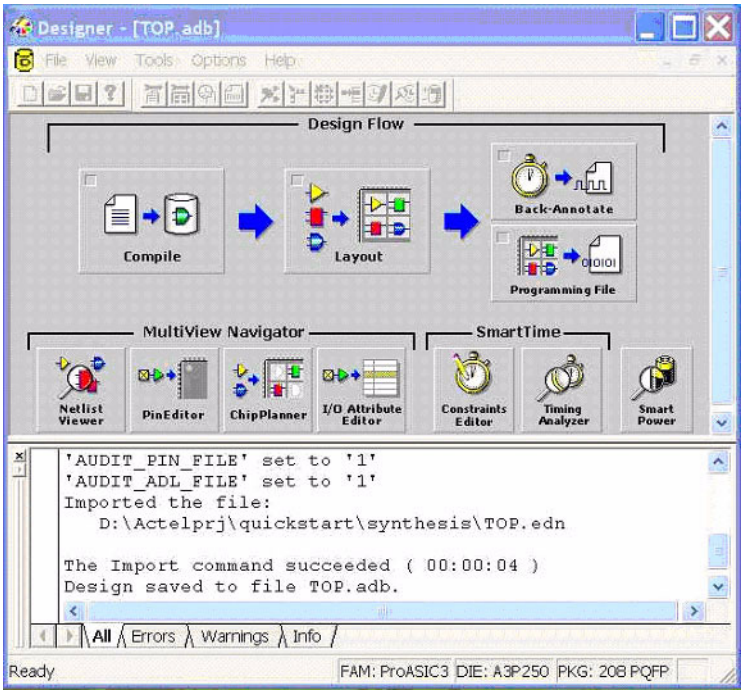

Figure 7-28. Designer GUI

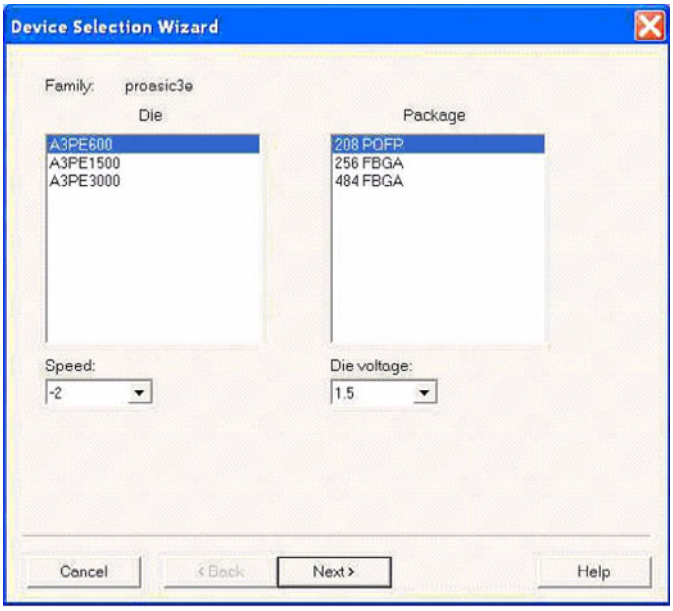

Figure 7-29. Device Selection Wizard-A3PE600

2. Select **A3P250** in the Die field and select **208 PQFP** in the Package field. Accept the default Speed grade and Die Voltage and click **Next**.
3. Use the default I/O settings and click **Next**.
4. Use the default Junction Temperature and Voltage setup and click **Finish**.

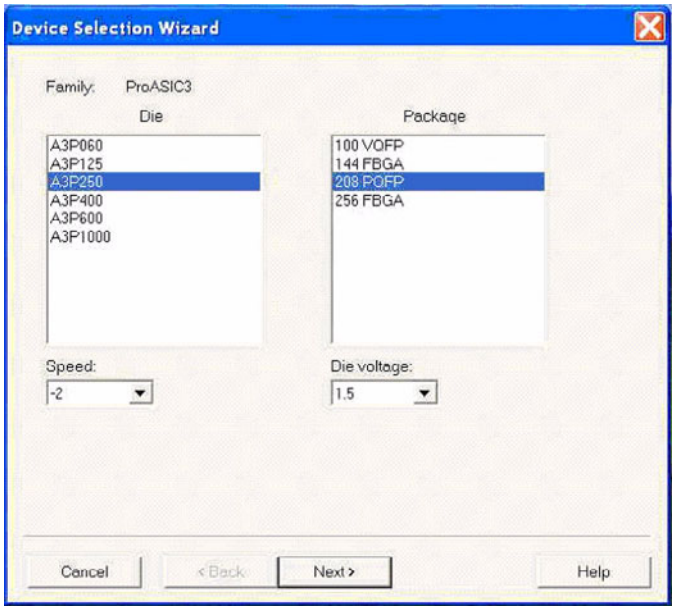

Figure 7-30. Device Selection Wizard—A3P250

5. Click the **Compile** icon. Leave the default Compile settings (Figure 7-31) and click **OK**.

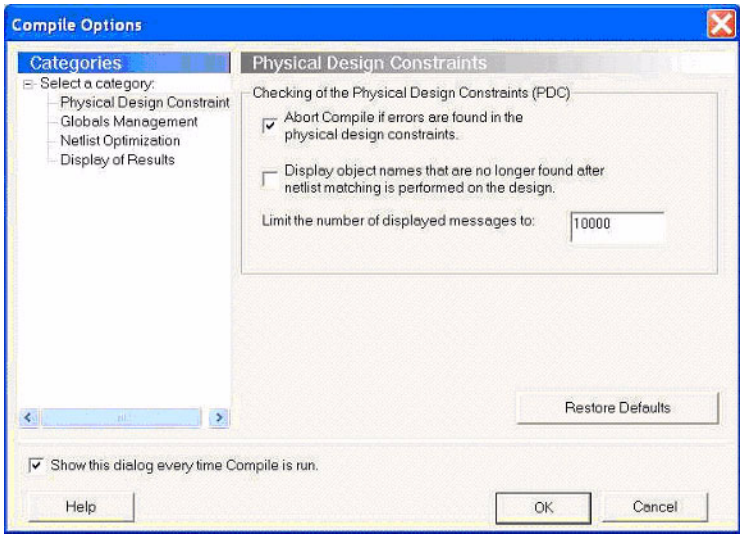

Figure 7-31. Compile Options Window

Designer compiles the design and shows the utilization of the selected device. Also, note that the Compile icon in Designer turns green, indicating that the compile has successfully completed.

6. Once the design compiles successfully, use the **I/O Attribute Editor** tool to assign the pin for subsequent place-and-route runs. Click the **I/O Attribute Editor** to open the tool. It opens in the MultiView Navigator user interface, as in Figure 7-32 on page 54.
7. See the Libero IDE or Designer online help for more information on the I/O Attribute Editor or MultiView Navigator.

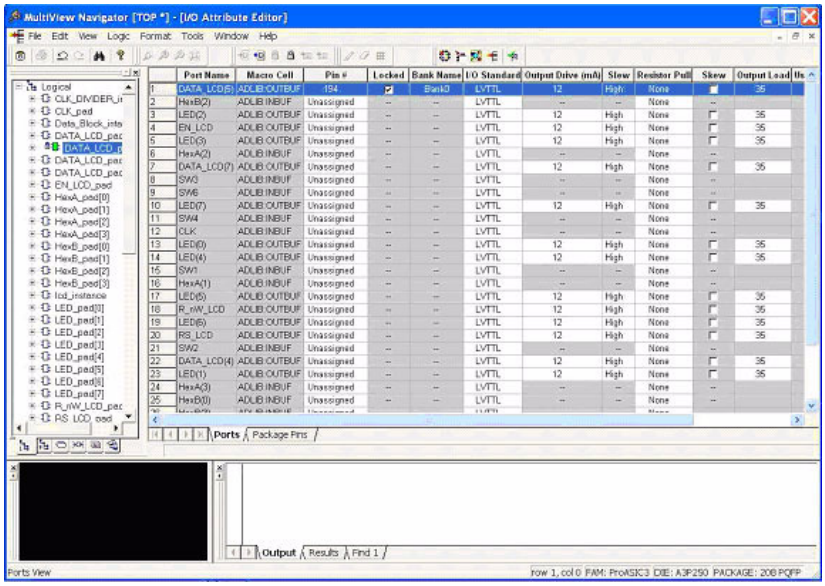

Figure 7-32. I/O Attribute Editor in MultiView Navigator

8. Assign a pin number to all of the signals, then select **Commit** from the **File** menu and close the I/O Attribute Editor.

9. Another way to assign pin location is to import the Physical Design Constraint (PDC) file as a source file for Compilation. From the Designer menu, select **File** > **Import Source File** (Figure 7-33) .

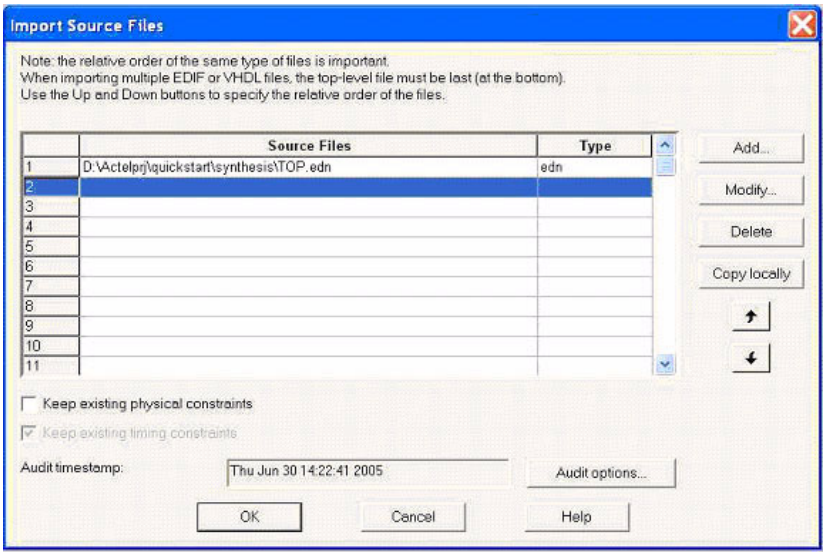

Figure 7-33. Import Designer Source Files

10. Select row 2, then click **Add**. Browse to the pre-defined **Top.pdc** file (you can find it in the */src* folder). Choose *.pdc for **Files of type**, click **Top.pdc** and **Import**.

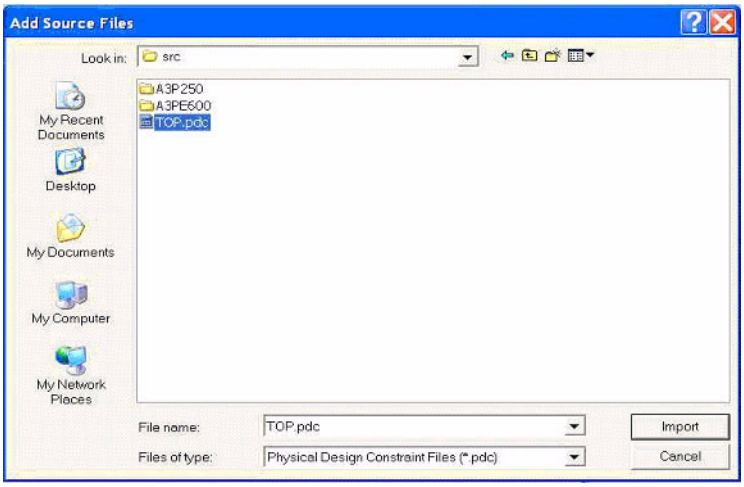

Figure 7-34. Import PDC File

11. Click **OK** in the Import Source Files window. You need to re-Compile the design once a new PDC file is imported.

    (Optional) After successfully compiling the design, use the Designer Tools to view the pre-layout static timing analysis with Timer, set the timing constraints in Timer, analyze the static and dynamic power with SmartPower, and use the ChipPlanner to assign modules. Click the appropriate icon to access these tools.

    For more information on these functions, refer to the Designer or Libero online help.

12. In Designer, click Layout. This opens the Layout Options dialog box shown in Figure 7-35.

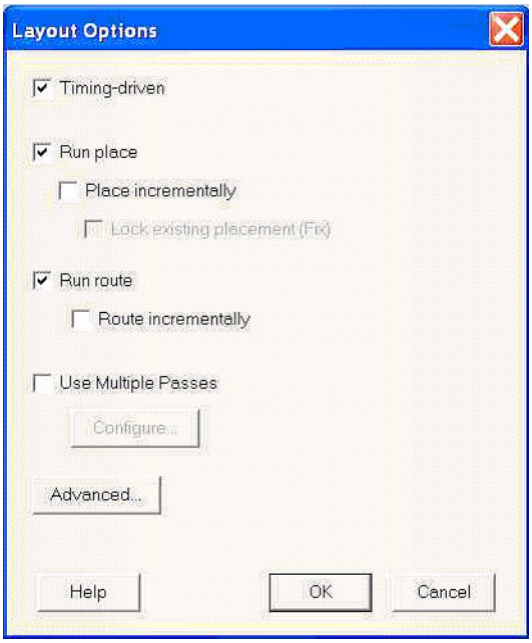

Figure 7-35. Layout Options Dialog Box

13. Click **OK** to accept the default layout options. This runs place-and-route on the design. The Layout icon turns green to indicate that the layout has successfully completed.

14. From Designer, click **Back-Annotate** in the Design Flow window. This opens the Back-Annotate dialog box, shown in Figure 7-36.

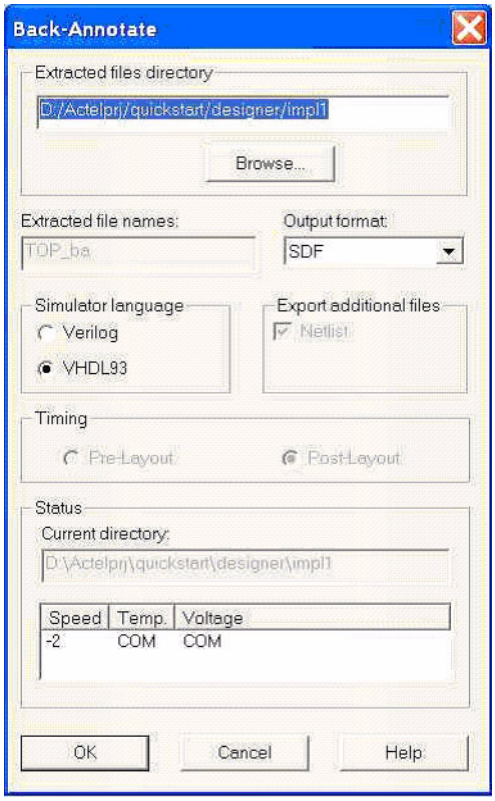

Figure 7-36. Back-Annotate Dialog Box

15. Accept the default settings and click **OK**. The Back-Annotate icon turns green.
16. Save and close Designer. From the **File** menu, click **Exit**. Click **Yes** to save the design before closing Designer. Designer saves all the design information in an *.adb file.

    The file *Top.adb* appears under the Designer Files of the File Manager. To reopen the file, right-click the file and select **Open** in Designer.

Step 6 – Perform Timing Simulation with Back-Annotated Timing

After completing the place-and-route and back annotation of the design, perform a timing simulation with the Model*Sim* HDL simulator.

To perform a timing simulation:

1. Click the **Simulation** icon in the Libero IDE Design Flow window, or right-click the **Top.vhd** file in the Design Hierarchy tab and select **Run Post-Layout Simulation**.
2. This launches the Model*Sim* Simulator that compiles the back annotated VHDL netlist file and testbench. Once the compilation completes, the simulator runs for 1000 ns and a Wave window opens to display the simulation results. From the Model*Sim* menu, select **Simulate** > **Run** > **Run All** to execute the full simulation time defined in the testbench.
3. Scroll in the Wave window to verify that the counter works correctly. Use the zoom buttons to zoom in and out as necessary.

Step 7 – Generate the Programming File

1. Open the **Top.adb** file in Designer and click the **Programming File** icon in the Design Flow window, which opens the Flash Point window (Figure 7-37).

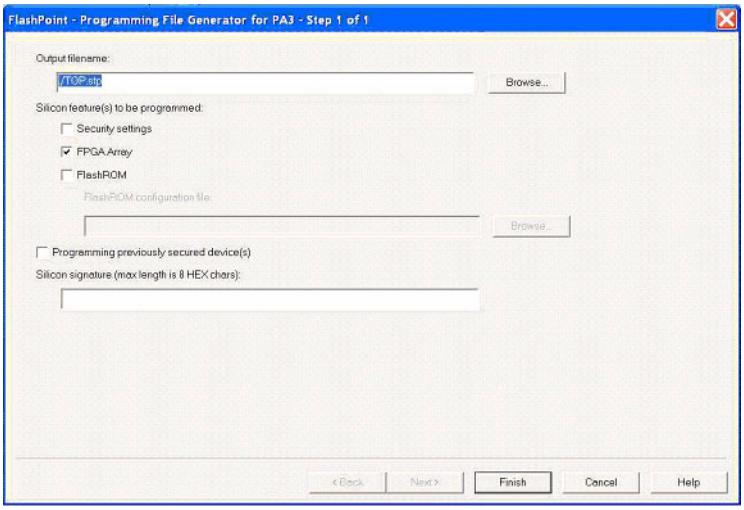

Figure 7-37. Flash Point Dialog Box

2. Click **Finish**, and then the programming file is generated and saved in the *\designer\impl1* folder.

Step 8 – Program the Device

After generating the programming file, program the device using an Actel FlashPro3 programmer.

Initial Setup

Before performing any action with the FlashPro3 programmer, it must be properly set up. Connect the FlashPro3 USB cable to your PC USB slot, connect the ribbon cable to the programming header on the target board, and turn on the power switch on the board.

To set up FlashPro3:

1. From the Actel FlashPro software File menu, click **Connect**. The FlashPro Connect to Programmer dialog box displays, as shown in Figure 7-38.

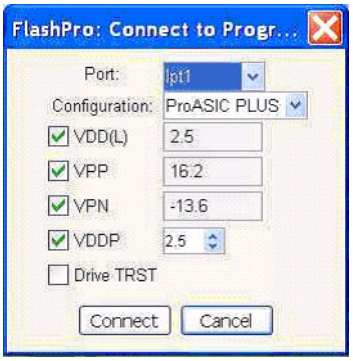

Figure 7-38. FlashPro3:Connect to Programmer Dialog Box

2. In the Port list, select the USB port. The FlashPro3 programmer is connected as shown in Figure 7-39.

Figure 7-39. Connect to Programmer Dialog Box for ProASIC3/E Devices

3. In the Configuration list, select **ProASIC3/E**.
4. Click **Connect**. A successful connection, or any error, appears in the Log window, as shown in Figure 7-40.

Figure 7-40. FlashPro3 Successful Connection

Analyze Chain and Device Selection

To analyze the chain and select the device:

1. From the File menu, click **Analyze Chain**. Chain details appear in the Log window, as shown in Figure 7-41.
2. If any failures appear, refer to the error and troubleshooting section of the FlashPro User's Guide.

If you have an A3PE600 device on board, you will see the message shown in Figure 7-41.

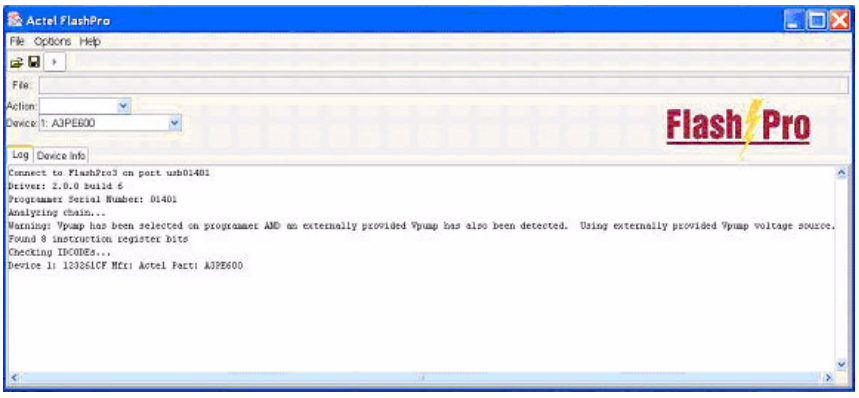

Figure 7-41. FlashPro3: Analyzing Chain—A3PE600

If you have an A3P250 device on board, you will see the message shown in Figure 7-42.

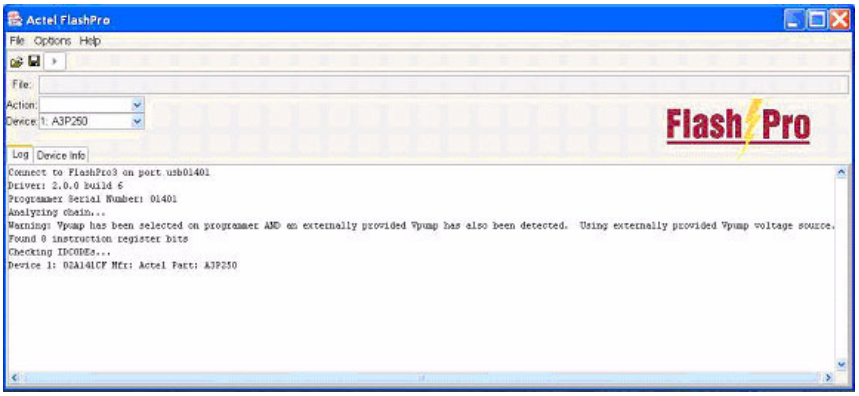

Figure 7-42. FlashPro3: Analyzing Chain—A3PE250

3. Select the **A3PE600** or the **A3P250** from the Device list. If only one device is present in the chain, performing Analyze Chain will select that device automatically from the Device list.

Loading the STAPL File

The FlashPro3 programmer uses a STAPL (*.stp) file to program the device.

To load the STAPL file:

1. Click the **Open File** button in the toolbar; or from the **File** menu, click **Open STAPL file**. The Open dialog box will appear, as shown in Figure 7-43.

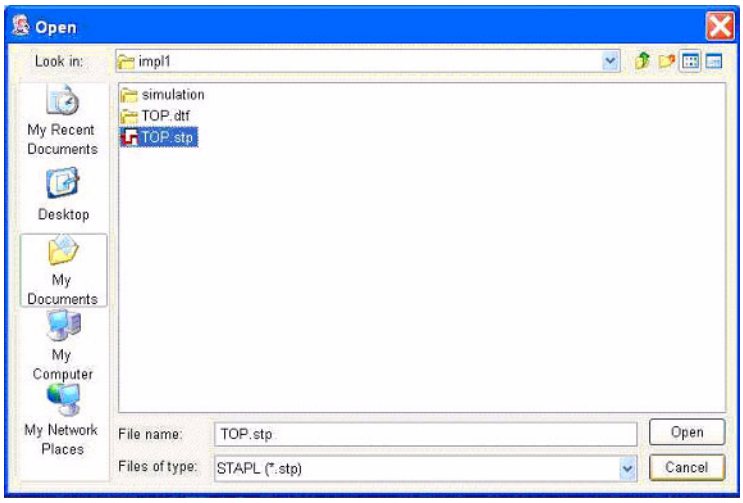

Figure 7-43. Open STAPL File Dialog Box

2. Browse to your Libero IDE *project /designer/impl1* folder, select the **STAPL** file, and click **Open**. The FlashPro software loads the file.

   Note: You can also find a copy of the *Top.stp* file in the */src/A3PE600* or */src/A3P250* folder.

The FlashPro Log window will display a message indicating that the software has successfully loaded, as shown in Figure 7-44.

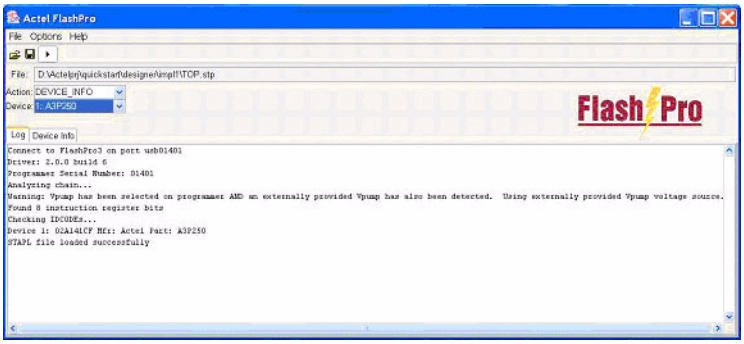

Figure 7-44. STAPL File Load Successfully

Note: If your board has an A3PE600 device, you will see A3PE600 in the Device list.

Selecting an Action

After loading the *STAPL* file, select an action from the Action list. See Table 7-1 for a definition of each action.

Table 7-1 · Action Options

Option	Action
QUERY_SECURITY	Checks the security status of the device. If the device is programmed with the security key, then this command returns with Read inhibit:1, Write inhibit:1. If the security key is not present, the values are Read inhibit:0, Write inhibit:0.
ERASE	Erases the device.
READ_IDCODE	Reads the device ID code.
VERIFY	Verifies if the device is programmed with the loaded STAPL file. Can be used to ensure that the bitstream programmed in the device is the same as the original STAPL file. If the wrong STAPL file is loaded, Exit 11 appears in the log window. A successful operation results in Exit 0.
PROGRAM	Programs the device.
DEVICE_INFO	Displays the serial number of the device, the Design Name that is programmed into the device, and the checksum that is programmed into the device.
ERASE_FROM	Erases FlashROM only.
PROGRAM_FROM	Programs FlashROM only.
VERIFY_FROM	Verifies FlashROM only.
PROGRAM_ARRAY	Programs the FPGA Array only.
ERASE_ARRAY	Erases the FPGA Array only.
VERIFY_ARRAY	Verifies the FPGA Array only.
PROGRAM	Programs FPGA Array, FlashROM and/or security settings of the device.
ERASE_ALL	Erases FPGA Array, FlashROM and/or security settings of the device.
ACTION_VERIFY	Verifies FPGA Array, FlashROM and/or security settings of the device.
READ_IDCODE	Reads the device ID code.
ENC_DATA_AUTHENTICATION	Authenticates the encrypted data against the security settings you previously programmed into the device. This is a preventative measure that stops the program from corrupting data into the device.
PROGRAM_SECURITY	Programs security settings into the device.
DEVICE_INFO	Displays the Device IDCODE, security settings, design name, checksum, and FlashROM content that is programmed into the device.

Programming the Device

To program the device:

1. In the Action list, select **PROGRAM**.

2. In the Device list, select the **A3P250** device (or **A3PE600** if your board has an A3PE600 device).
3. Click the **Execute** button in the toolbar.
4. The Execute Action dialog box appears, as shown in Figure 7-45.

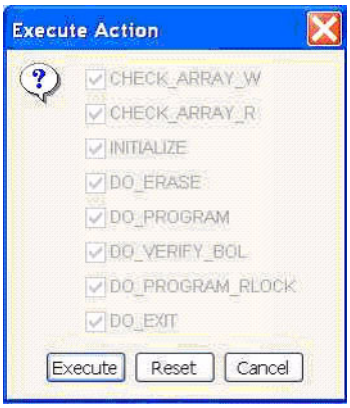

Figure 7-45. Execute Action Dialog Box—Program

All the steps of the programming sequence are listed. Grayed out options are required for programming and cannot be changed. All of these steps, as shown in Figure 7-45, are grayed out because they are required for programming and cannot be changed.

5. Click **Execute** to start programming. The progress of the programming action displays in the Log window. The message 'Exit 0' indicates that the device has successfully been programmed, as shown in Figure 7-46.

Note: Do not interrupt the programming sequence, it may damage the device or programmer. If you encounter any failures, refer to the troubleshooting section of the FlashPro User's Guide.

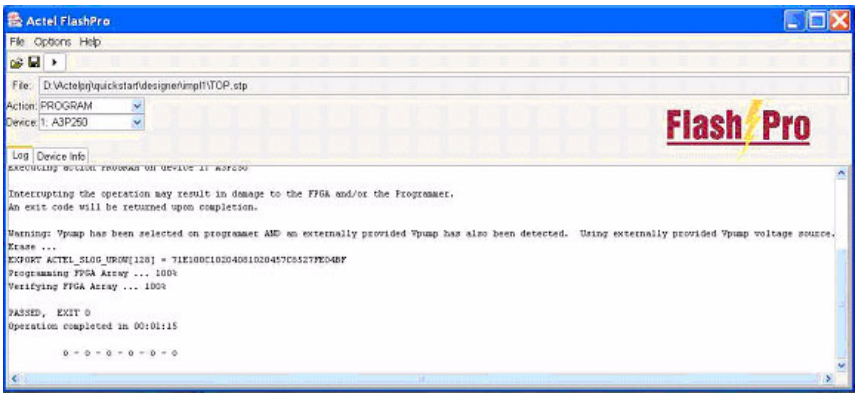

Figure 7-46. Successfully Programmed Device

Note: If you have an A3PE600 device on board, you will see A3PE600 in the Device list.

Verifying the Correct Programming

To verify the device is programmed with the correct STAPL file:

1. Load the *STAPL* file.
2. In the Action list, click **Verify**.

3. Click the **Execute** button in the toolbar. The Execute Action dialog box will appear, as shown in Figure 7-47.

Figure 7-47. Execute Action Dialog Box--Verify

The default settings appear in the Execute Action dialog box.

4. Click **Execute** to start the verification process. A successful verification will result in Exit 0, as shown in Figure 7-48 on page 64. If the *STAPL* file is different from the file used for programming, Exit 11 will appear in the Log window.

Note: Do not interrupt the verifying sequence, it may damage the device.

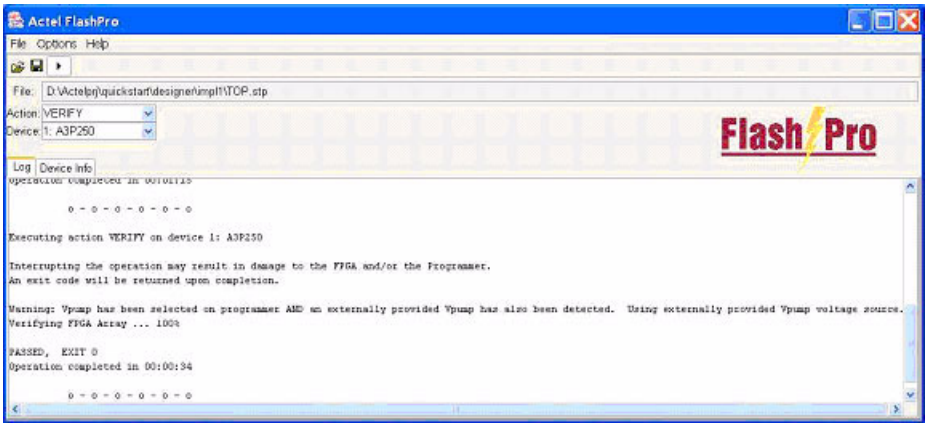

Figure 7-48. Successful Verification

Note: If you have an A3PE600 device on board, you will see A3PE600 in the Device list.

Saving Your Log File

All FlashPro3 results are displayed in the Log window. Save these results into a file.

To save the log file:

1. From the File menu, click **Save Log**. The Save dialog box will appear, as shown in Figure 7-49.

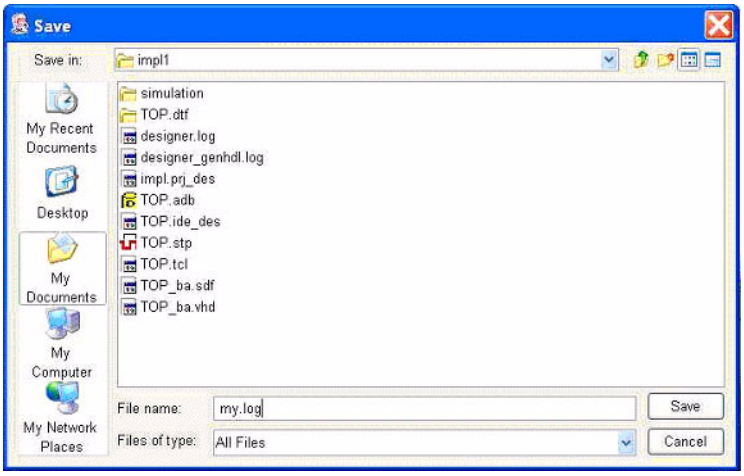

Figure 7-49. Save Log File Dialog Box

2. Select a directory, type in the file name, and click **Save**. The FlashPro software saves the file.

Check Functionality of Tutorial Design

After programming the device, you will see "ACTEL A3PE STARTER KIT" display on the LCD panel as well as flashing LEDs. There are 6 switches (SW) equipped with special functions.

Press **SW1** to Asyn_Clear on the flashing LEDs and the LCD panel.

Press **SW6** to change the LEDs from flashing to counting.

Press **SW3** to Asyn_Load the counter.

Press **SW2** to change the up counter to down counter.

Press **SW4** for LEDs manual clock.

Press **SW5** for LCD manual clock.

8 Test Procedures for Board Testing

Overview

This document defines the test procedure required to be carried out by the Actel designated manufacturer's testing facility on the ProASIC3/E Evaluation Board with silkscreen labeling A3PE-A3P-EVAL-BRD-1. This testing is specific to the socketed version of the board. All steps in the following enumerated test procedure should be followed in sequence for testing the board. Deviations in the sequence are explained in the text.

Equipment Required

Actel Equipment Provided by Actel to Testing Facility

Actel will provide the following:

- This test procedure document.
- FlashPro v3.4 software on a CD-ROM.
- FlashPro3 programmer and programming cable for connecting to the A3PE-A3P-EVAL-BRD1.
- Pre-programmed A3PE600-PQ208 or A3P250-PQ208 silicon. Ten devices will be provided for ten boards. The initial silicon will not be labeled as having been programmed. (This is just for the testing associated with the first manufacturing build.) Additional devices will be provided for testing further boards and this change will be detailed in an update to the procedure.
- Power supply (+9 V, 2 A CUI) for the ProASIC3 Starter Kit board plus a mains cable for the power supply.

Testing Facility Equipment to be Available for Testing

The manufacturer's testing facility will provide the following equipment for testing of the board:

- Digital Multimeter to measure voltages on the circuit board at the known test points.

Test Procedure for the A3PE-A3P-EVAL-BRD1

In this section, full test procedure for the boards is outlined. This procedure applies to socketed boards. For boards fitted with directly soldered parts, the procedure is the same except for fitting of the FPGA. In such cases, the reader should adjust the procedure accordingly and ignore references to fitting parts to sockets.

Initial Power-On Procedure

This part of the procedure may be carried out independently and ahead of the other parts of the test procedure. Boards passing this procedure may be transferred to a passing set of boards.

To perform the initial power-on procedure:

1. Record the time of the test and the board serial number (written by the bar code on the back of the board) into a test log.
2. Plug the +9 V power supply into the wall.
3. Take an A3PE-A3P-EVAL-BRD1 that has an empty socket. Make sure the switch SW11 is in the OFF position, (the switch should be moved to the left). This corresponds with the labeling of the silkscreen on the board.
4. Connect +9 V DC output of the CUI power supply to the J18 connector on the board. You should observe the red LED at the top right of the board, i.e. LED D19 should light indicating +9 V DC has been applied to the board.
5. Move the SW11 switch to the ON position, i.e., move the switch to the right. Observe that LEDs, D13, D9, D10, D11, and D17 light up green on the board. All LEDs are on the top edge of the board (same edge as red D19 power connector LED, which should remain lit).

6. Using a DVM, measure DC voltages using TP11 as ground:

   TP6 and TP7 – should be 3.3 V (values ±0.2 V are acceptable). Values outside this range are a failure.

   TP15 – should be 1.5 V (values ±0.1 V are acceptable).

   TP8 – should be 1.8 V (values ±0.1 V are acceptable).

   TP10 – should be 2.5 V (values ±0.2 V are acceptable).

   TP47 – should be 5.0 V (values ±0.2 V are acceptable).

   J14C pin 106 – should be 3.3 V (values ±0.2 V are acceptable). Note that jumper JP48 must be in place for this measurement, otherwise zero will be recorded.
7. That completes the initial power-on check. The board should now be switched off by moving SW11 to the OFF position (to the left).

Testing Board Functionality with A3PE600-PQ208 or A3P250-PQ208 Silicon

To test board functionality:

1. Record the time of the test and the board serial number (written by the bar code on the back of the board) into a test log.
2. Make sure the switch SW11 is in the OFF position (i.e., to the left.)
3. Apply power to the board by attaching the +9 V DC supply to J18. Only the red LED should be illuminated.
4. Undo the four screws holding the socket of U8 in place. Remove the lid of the socket.
5. Place a pre-programmed A3PE600-PQ208 or A3P250-PQ208 FPGA part into the socket using the appropriate vacuum pen while observing anti-static precautions. Make sure that pin 1 of the FPGA is oriented correctly. (The Actel logo on the part should match the orientation of the Actel logo on the board just above the A3PE-A3P-BRD1 part number.) Take great care to make sure all pins are in correct alignment so that the FPGA is on a level plane parallel to the board.
6. Carefully replace the socket cover and screw down all four corners to appropriate tightness. It is recommended to do opposite corners first so as to lessen rotational torque on the part.
7. Switch on SW11 to the ON position (slide it to the right).
8. Validate that all 5 LEDs at the top of the board including the red one turn on. D17, D11, D10, D9, D13, and D19.
9. Validate that the 8 LEDS: D8, D7, …, and D2, D1 all pulsate in either a counting pattern or a “center to outside swinging” pattern.
10. If no LEDs are visible, stop and switch off SW11. Rotate SW8 and SW9 clockwise to the 3.3 V selection. This is best described with the thicker arrow bar pointing upward. Switch the board back on. The LEDs should be visible. If very dim, stop, switch off the board and rotate the switches one quarter turn clockwise before switching board back on. Continue if the LEDs are glowing. If unable to get a display on the LEDs, the board must be tagged as bad.
11. If it is a bad board, carefully remove the A3PE600-PQ208 or A3P250-PQ208 silicon from the socket and set it aside in an electrostatic-safe area. Using another piece of pre-programmed silicon, repeat steps 4 to 8 above.

    If still no response, mark the board as defective and re-use the silicon for other testing.

    If there is a good response, then place the previous silicon in a “bad” tray to prevent it from being retested.
12. Validate that the patterns can be switched by pressing SW6 (Global pulse) on the left side of board. When the switch is pressed, the LED D15 should momentarily light. The pattern on the 8 LEDs D8 through D1 will change.
13. Validate that the message “Actel A3PE Starter Kit” continually cycles on the LCD display. You may need to turn R40 clockwise to adjust contrast on the display until the message is dark enough to see.

    If no message is observed, press buttons SW4 and SW3 simultaneously. This will usually reset the system after a few cycles of the counter.
14. Connect a FlashPro3 programmer to a PC USB port and observe the power light illuminating. Ensure that the FlashPro v3.3 software is installed on the PC being used.

15. Connect the programming cable of the FlashPro3 programmer to the J1 shrouded and keyed header labeled FP3. The red line labeling pin 1 should be close to pin 1 on the header – no other orientation is possible.
16. On the PC, run the FlashPro v3.3 software and connect to the programmer. Select ProASIC3E as the device family. Once the software has shown a connection, select **Analyze Chain** from the **File** menu.

    If an error message of incorrect VJTAG is reported, then remove the jumper placed at J5 and place it instead at J12 across pins 11 and 12. It may safely be left there. Repeat the **Analyze Chain** command.

    If a message appears indicating that an A3PE600 or A3P250 part (depending on the device fitted to the board) has been detected, then the board has passed this test. Leave the silicon in place in the socket and move to the next step.

    If a message of **11** or some other numeric indication appears, then record the message in a test log and fail the board. Remove the silicon from the socket and place it in the safe silicon holding area.
17. This concludes the testing of the board. Switch SW11 to the OFF position and remove the power connector from J18.

A

PQ208 Package Connections for A3PE600 and A3P250 Devices

Due to the comprehensive and flexible nature of ProASIC3 device user I/Os, a naming scheme is used to show the details of the I/O. The name identifies to which I/O bank it belongs, as well as the pairing and pin polarity for differential I/Os.

I/O Nomenclature = Gmn/IOuxwBy

Gmn is only used for I/Os that also have CCC access – i.e., global pins.

G = Global

m = Global pin location associated with each CCC on the device: A (northwest corner), B (northeast corner), C (east middle), D (southeast corner), E (southwest corner), and F (west middle)

n = Global input MUX and pin number of the associated Global location m, either A0, A1,A2, B0, B1, B2, C0, C1, or C2

u = I/O pair number in the bank, starting at 00 from the northwest I/O bank in a clockwise direction

x = P (Positive) or N (Negative) for differential pairs, or S (Single-Ended) for the I/O that support single-ended and voltage-referenced I/O standards only

w = D (Differential Pair) or P (Pair) or S (Single-Ended). D (Differential Pair) if both members of the pair are bonded out to adjacent pins or are separated only by one GND or NC pin; P (Pair) if both members of the pair are bonded out but do not meet the adjacency requirement; or S (Single-Ended) if the I/O pair is not bonded out. For Differential (D) pairs, adjacency for ball grid packages means only vertical or horizontal. Diagonal adjacency does not meet the requirements for a true differential pair.

B = Bank

y = Bank number [0..3] for ProASIC3 and [0..7] for ProASIC3E. Bank number starting at 0 from the northwest I/O bank in a clockwise direction

Figure A-1 on page 72 and Table A-1 on page 72 are extracted from the ProASIC3 and ProASIC3E datasheets and provide package connections for the A3P250 and A3E600 devices. Pinouts for other devices in the PQ208 family may be found on the Actel website:

ProASIC3 Flash Family FPGAs datasheet at www.actel.com/documents/PA3_DS.pdf

ProASIC3E Flash Family FPGAs datasheet at www.actel.com/documents/PA3E_DS.pdf

These datasheets are included on the ProASIC3 and ProASIC3E Starter Kit CD. However, the website should always be referenced for access to the most recent datasheet.

208-Pin PQFP

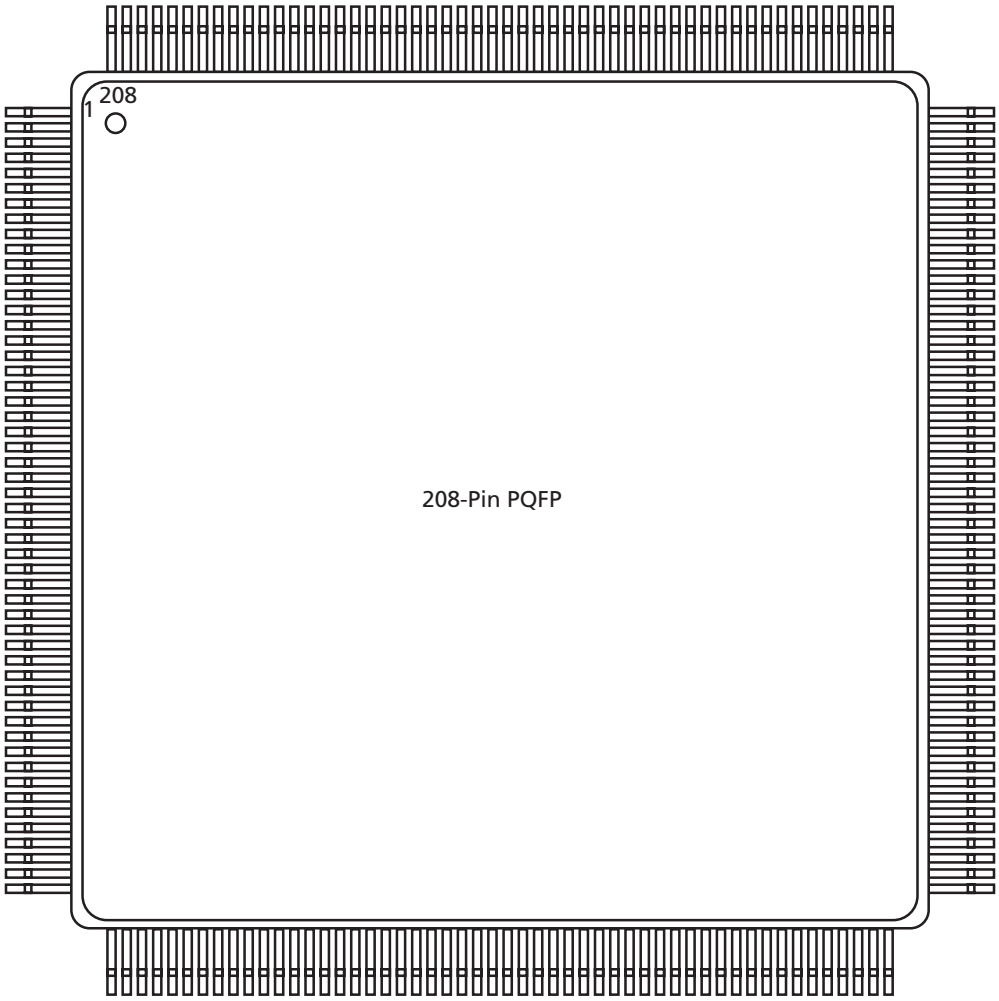

Figure A-1. 208-Pin PQFP

Table A-1 · Device Connections for 208-Pin PQFP

208-Pin PQFP		
Pin Number	**A3PE600 Function**	**A3P250 Function**
1	GND	GND
2	GNDQ_	GAA2/IO118PDB3
3	VMV7	IO118NDB3
4	GAB2/IO133PSB7V1	GAB2/IO117PDB3
5	GAA2/IO134PDB7V1	IO117NDB3

Table A-1 · Device Connections for 208-Pin PQFP (Continued)

208-Pin PQFP		
Pin Number	**A3PE600 Function**	**A3P250 Function**
6	IO134NDB7V1	GAC2/IO116PDB3
7	GAC2/IO132PDB7V1	IO116NDB3
8	IO132NDB7V1	IO115PDB3
9	IO130PDB7V1	IO115NDB3
10	IO130NDB7V1	IO114PDB3
11	IO127PDB7V1	IO114NDB3
12	IO127NDB7V1	IO113PDB3
13	IO126PDB7V0	IO113NDB3
14	IO126NDB7V0	IO112PDB3
15	IO124PSB7V0	IO112NDB3
16	V_{CC}	V_{CC}
17	GND	GND
18	V_{CCI}B7	V_{CCI}B3
19	IO122PPB7V0	IO111PDB3
20	IO121PSB7V0	IO111NDB3
21	IO122NPB7V0	GFC1/IO110PDB3
22	GFC1/IO120PSB7V0	GFC0/IO110NDB3
23	GFB1/IO119PDB7V0	GFB1/IO109PDB3
24	GFB0/IO119NDB7V0	GFB0/IO109NDB3
25	V_{COMPLF}	V_{COMPLF}
26	GFA0/IO118NPB6V1	GFA0/IO108NPB3
27	V_{CCPLF}	V_{CCPLF}
28	GFA1/IO118PPB6V1	GFA1/IO108PPB3
29	GND	GND
30	GFA2/IO117PDB6V1	GFA2/IO107PDB3
31	IO117NDB6V1	IO107NDB3
32	GFB2/IO116PPB6V1	GFB2/IO106PDB3
33	GFC2/IO115PPB6V1	IO106NDB3
34	IO116NPB6V1	GFC2/IO105PDB3
35	IO115NPB6V1	IO105NDB3

Table A-1 · Device Connections for 208-Pin PQFP (Continued)

208-Pin PQFP		
Pin Number	**A3PE600 Function**	**A3P250 Function**
36	V_{CC}	NC
37	IO112PDB6V1	IO104PDB3
38	IO112NDB6V1	IO104NDB3
39	IO108PSB6V0	IO103PSB3
40	V_{CCI}B6	V_{CCI}B3
41	GND	GND
42	IO106PDB6V0	IO101PDB3
43	IO106NDB6V0	IO101NDB3
44	GEC1/IO104PDB6V0	GEC1/IO100PDB3
45	GEC0/IO104NDB6V0	GEC0/IO100NDB3
46	GEB1/IO103PPB6V0	GEB1/IO99PDB3
47	GEA1/IO102PPB6V0	GEB0/IO99NDB3
48	GEB0/IO103NPB6V0	GEA1/IO98PDB3
49	GEA0/IO102NPB6V0	GEA0/IO98NDB3
50	VMV6	VMV3
51	GNDQ	GNDQ
52	GND	GND
53	VMV5	NC
54	GNDQ	NC
55	IO101NDB5V2	GEA2/IO97RSB2
56	GEA2/IO101PDB5V2	GEB2/IO96RSB2
57	IO100NDB5V2	GEC2/IO95RSB2
58	GEB2/IO100PDB5V2	IO94RSB2
59	IO99NDB5V2	IO93RSB2
60	GEC2/IO99PDB5V2	IO92RSB2
61	IO98PSB5V2	IO91RSB2
62	V_{CCI}B5	V_{CCI}B2
63	IO96PSB5V2	IO90RSB2
64	IO94NDB5V1	IO89RSB2
65	GND	GND

Table A-1 · Device Connections for 208-Pin PQFP (Continued)

208-Pin PQFP		
Pin Number	**A3PE600 Function**	**A3P250 Function**
66	IO94PDB5V1	IO88RSB2
67	IO92NDB5V1	IO87RSB2
68	IO92PDB5V1	IO86RSB2
69	IO88NDB5V0	IO85RSB2
70	IO88PDB5V0	IO84RSB2
71	V_{CC}	V_{CC}
72	V_{CCI}B5	V_{CCI}B2
73	IO85NPB5V0	IO83RSB2
74	IO84NPB5V0	IO82RSB2
75	IO85PPB5V0	IO81RSB2
76	IO84PPB5V0	IO80RSB2
77	IO83NPB5V0	IO79RSB2
78	IO82NPB5V0	IO78RSB2
79	IO83PPB5V0	IO77RSB2
80	IO82PPB5V0	IO76RSB2
81	GND	GND
82	IO80NDB4V1	IO75RSB2
83	IO80PDB4V1	IO74RSB2
84	IO79NPB4V1	IO73RSB2
85	IO78NPB4V1	IO72RSB2
86	IO79PPB4V1	IO71RSB2
87	IO78PPB4V1	IO70RSB2
88	V_{CC}	V_{CC}
89	V_{CCI}B4	V_{CCI}B2
90	IO76NDB4V1	IO69RSB2
91	IO76PDB4V1	IO68RSB2
92	IO72NDB4V0	IO67RSB2
93	IO72PDB4V0	IO66RSB2
94	IO70NDB4V0	IO65RSB2
95	GDC2/IO70PDB4V0	IO64RSB2

Table A-1 · Device Connections for 208-Pin PQFP (Continued)

208-Pin PQFP		
Pin Number	**A3PE600 Function**	**A3P250 Function**
96	IO68NDB4V0	GDC2/IO63RSB2
97	GND	GND
98	GDA2/IO68PDB4V0	GDB2/IO62RSB2
99	GDB2/IO69PSB4V0	GDA2/IO61RSB2
100	GNDQ	GNDQ
101	TCK	TCK
102	TDI	TDI
103	TMS	TMS
104	VMV4	VMV2
105	GND	GND
106	V_{PUMP}	V_{PUMP}
107	GNDQ	NC
108	TDO	TDO
109	TRST	TRST
110	V_{JTAG}	V_{JTAG}
111	VMV3	GDA0/IO60NDB1
112	GDA0/IO67NPB3V1	GDA1/IO60PDB1
113	GDB0/IO66NPB3V1	GDB0/IO59NDB1
114	GDA1/IO67PPB3V1	GDB1/IO59PDB1
115	GDB1/IO66PPB3V1	GDC0/IO58NDB1
116	GDC0/IO65NDB3V1	GDC1/IO58PDB1
117	GDC1/IO65PDB3V1	IO57NDB1
118	IO62NDB3V1	IO57PDB1
119	IO62PDB3V1	IO56NDB1
120	IO58NDB3V0	IO56PDB1
121	IO58PDB3V0	IO55RSB1
122	GND	GND
123	V_{CCI}B3	V_{CCI}B1
124	GCC2/IO55PSB3V0	NC
125	GCB2/IO54PSB3V0	NC

Table A-1 · Device Connections for 208-Pin PQFP (Continued)

208-Pin PQFP		
Pin Number	**A3PE600 Function**	**A3P250 Function**
126	NC	V_{CC}
127	IO53NDB3V0	IO53NDB1
128	GCA2/IO53PDB3V0	GCC2/IO53PDB1
129	GCA1/IO52PPB3V0	GCB2/IO52PSB1
130	GND	GND
131	V_{CCPLC}	GCA2/IO51PSB1
132	GCA0/IO52NPB3V0	GCA1/IO50PDB1
133	V_{COMPLC}	GCA0/IO50NDB1
134	GCB0/IO51NDB2V1	GCB0/IO49NDB1
135	GCB1/IO51PDB2V1	GCB1/IO49PDB1
136	GCC1/IO50PSB2V1	GCC0/IO48NDB1
137	IO49NDB2V1	GCC1/IO48PDB1
138	IO49PDB2V1	IO47NDB1
139	IO48PSB2V1	IO47PDB1
140	V_{CCI}B2	V_{CCI}B1
141	GND	GND
142	V_{CC}	V_{CC}
143	IO47NDB2V1	IO46RSB1
144	IO47PDB2V1	IO45NDB1
145	IO44NDB2V1	IO45PDB1
146	IO44PDB2V1	IO44NDB1
147	IO43NDB2V0	IO44PDB1
148	IO43PDB2V0	IO43NDB1
149	IO40NDB2V0	GBC2/IO43PDB1
150	IO40PDB2V0	IO42NDB1
151	GBC2/IO38PSB2V0	GBB2/IO42PDB1
152	GBA2/IO36PSB2V0	IO41NDB1
153	GBB2/IO37PSB2V0	GBA2/IO41PDB1
154	VMV2	VMV1
155	GNDQ	GNDQ

Table A-1 · Device Connections for 208-Pin PQFP (Continued)

208-Pin PQFP		
Pin Number	**A3PE600 Function**	**A3P250 Function**
156	GND	GND
157	VMV1	NC
158	GNDQ_	GBA1/IO40RSB0
159	GBA1/IO35PDB1V1	GBA0/IO39RSB0
160	GBA0/IO35NDB1V1	GBB1/IO38RSB0
161	GBB1/IO34PDB1V1	GBB0/IO37RSB0
162	GND	GND
163	GBB0/IO34NDB1V1	GBC1/IO36RSB0
164	GBC1/IO33PDB1V1	GBC0/IO35RSB0
165	GBC0/IO33NDB1V1	IO34RSB0
166	IO31PDB1V1	IO33RSB0
167	IO31NDB1V1	IO32RSB0
168	IO27PDB1V0	IO31RSB0
169	IO27NDB1V0	IO30RSB0
170	V_{CCI}B1	V_{CCI}B0
171	V_{CC}	V_{CC}
172	IO23PPB1V0	IO29RSB0
173	IO22PSB1V0	IO28RSB0
174	IO23NPB1V0	IO27RSB0
175	IO21PDB1V0	IO26RSB0
176	IO21NDB1V0	IO25RSB0
177	IO19PPB0V2	IO24RSB0
178	GND	GND
179	IO18PPB0V2	IO23RSB0
180	IO19NPB0V2	IO22RSB0
181	IO18NPB0V2	IO21RSB0
182	IO17PPB0V2	IO20RSB0
183	IO16PPB0V2	IO19RSB0
184	IO17NPB0V2	IO18RSB0
185	IO16NPB0V2	IO17RSB0

Table A-1 · Device Connections for 208-Pin PQFP (Continued)

208-Pin PQFP		
Pin Number	**A3PE600 Function**	**A3P250 Function**
186	V_{CCI}B0	V_{CCI}B0
187	V_{CC}	V_{CC}
188	IO15PDB0V2	IO16RSB0
189	IO15NDB0V2	IO15RSB0
190	IO13PDB0V2	IO14RSB0
191	IO13NDB0V2	IO13RSB0
192	IO11PSB0V1	IO12RSB0
193	IO09PDB0V1	IO11RSB0
194	IO09NDB0V1	IO10RSB0
195	GND	GND
196	IO07PDB0V1	IO09RSB0
197	IO07NDB0V1	IO08RSB0
198	IO05PDB0V0	IO07RSB0
199	IO05NDB0V0	IO06RSB0
200	V_{CCI}B0	V_{CCI}B0
201	GAC1/IO02PDB0V0	GAC1/IO05RSB0
202	GAC0/IO02NDB0V0	GAC0/IO04RSB0
203	GAB1/IO01PDB0V0	GAB1/IO03RSB0
204	GAB0/IO01NDB0V0	GAB0/IO02RSB0
205	GAA1/IO00PDB0V0	GAA1/IO01RSB0
206	GAA0/IO00NDB0V0	GAA0/IO00RSB0
207	GNDQ	GNDQ
208	VMV0	VMV0

B

Board Schematics

This appendix provides illustrations of the ProASIC3/E Evaluation Board.

Note: The following figures are in low resolution. If you would like to see the figures in high resolution, refer to the *ProASIC3 Starter Kit Board Schematics*, available at www.actel.com/products/hardware/devkits_boards/proasic3_starter.aspx#docs.

Top-Level View

Figure B-1 on page 82 illustrates a top-level view of the ProASIC3/E Evaluation Board. Figure B-2 on page 83 illustrates a bottom-level view of the ProASIC3/E Evaluation Board.

ProASIC3 Schematics

The last pages of this appendix show the following illustrations of the ProASIC3/E Starter Kit Board in order.

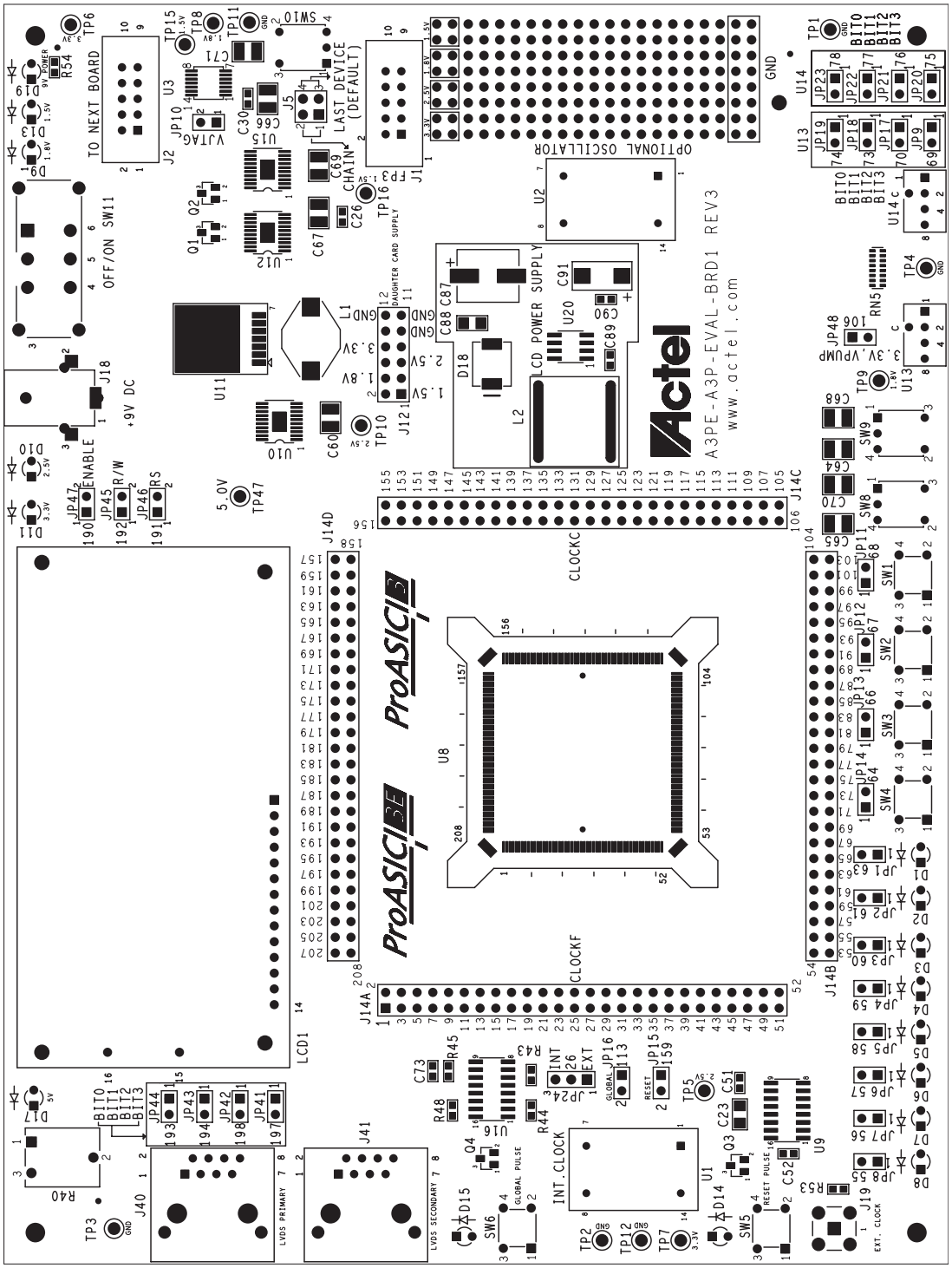

Figure B-1. Top-Level View of ProASIC3/E Evaluation Board

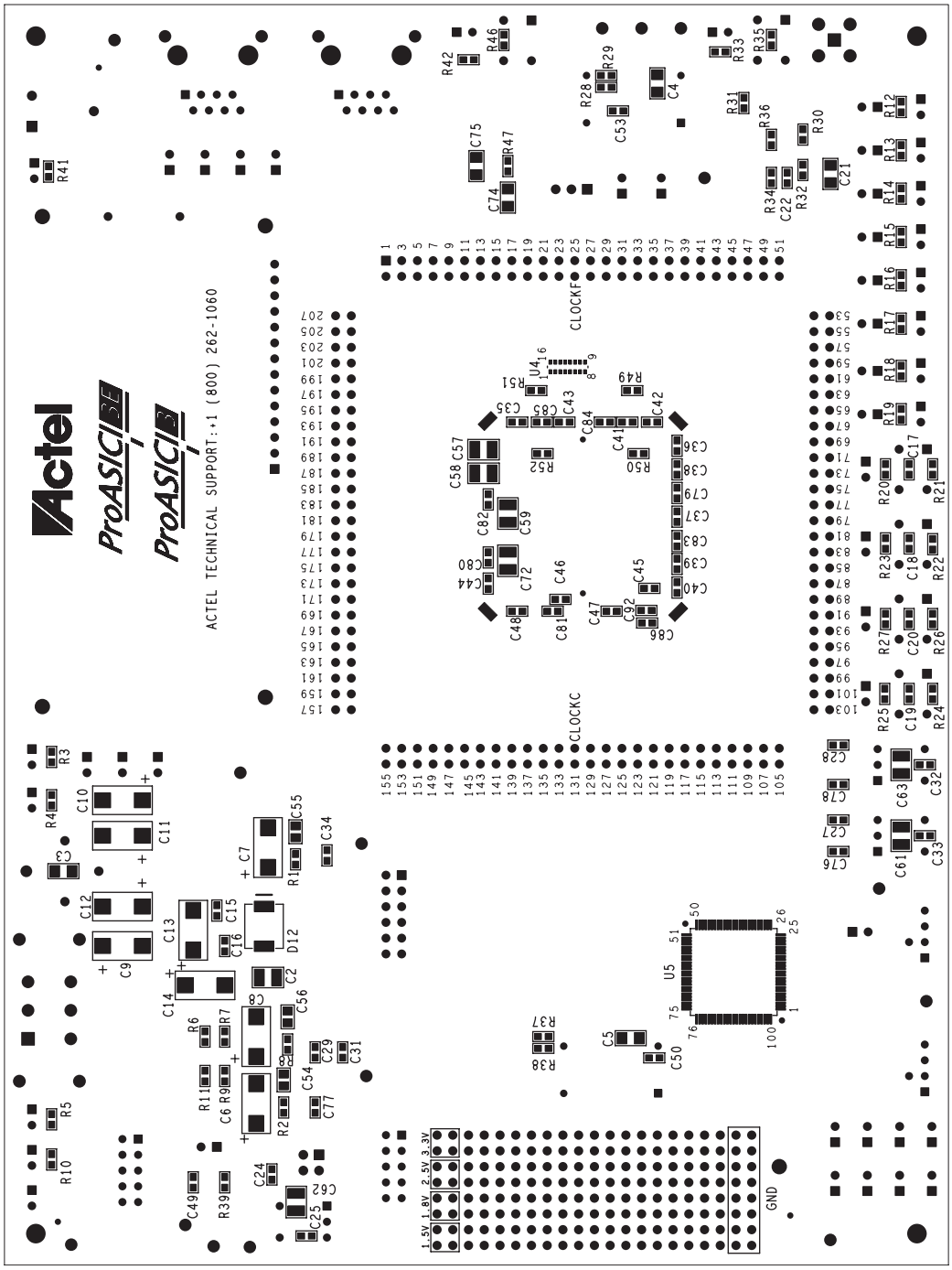

Figure B-2. Bottom-Level View of ProASIC3/E Evaluation Board

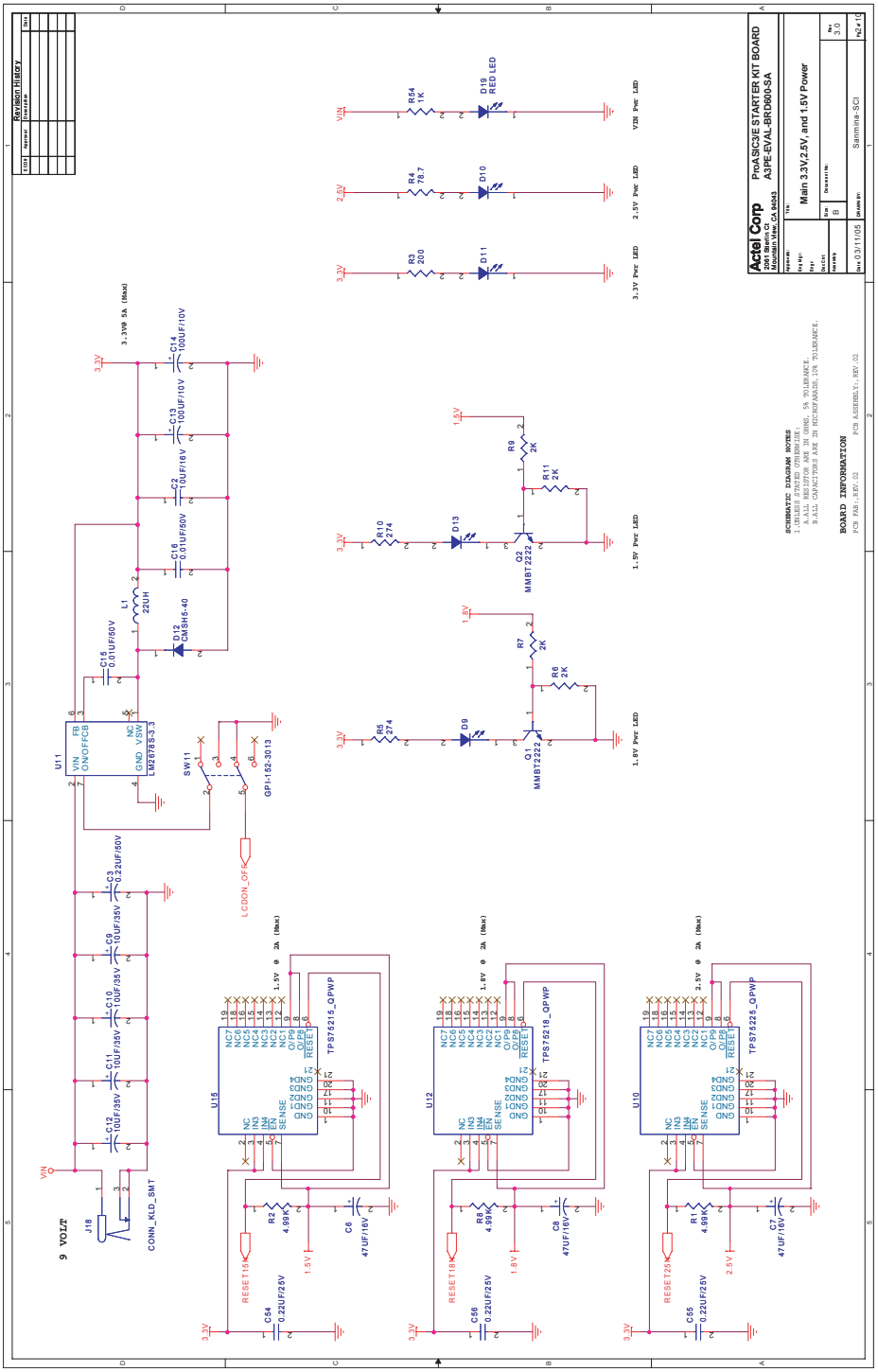

Figure B-3. Main 3.3 V, 2.5 V and 1.5 V Power

Figure B-4. ProASIC3 FPGA

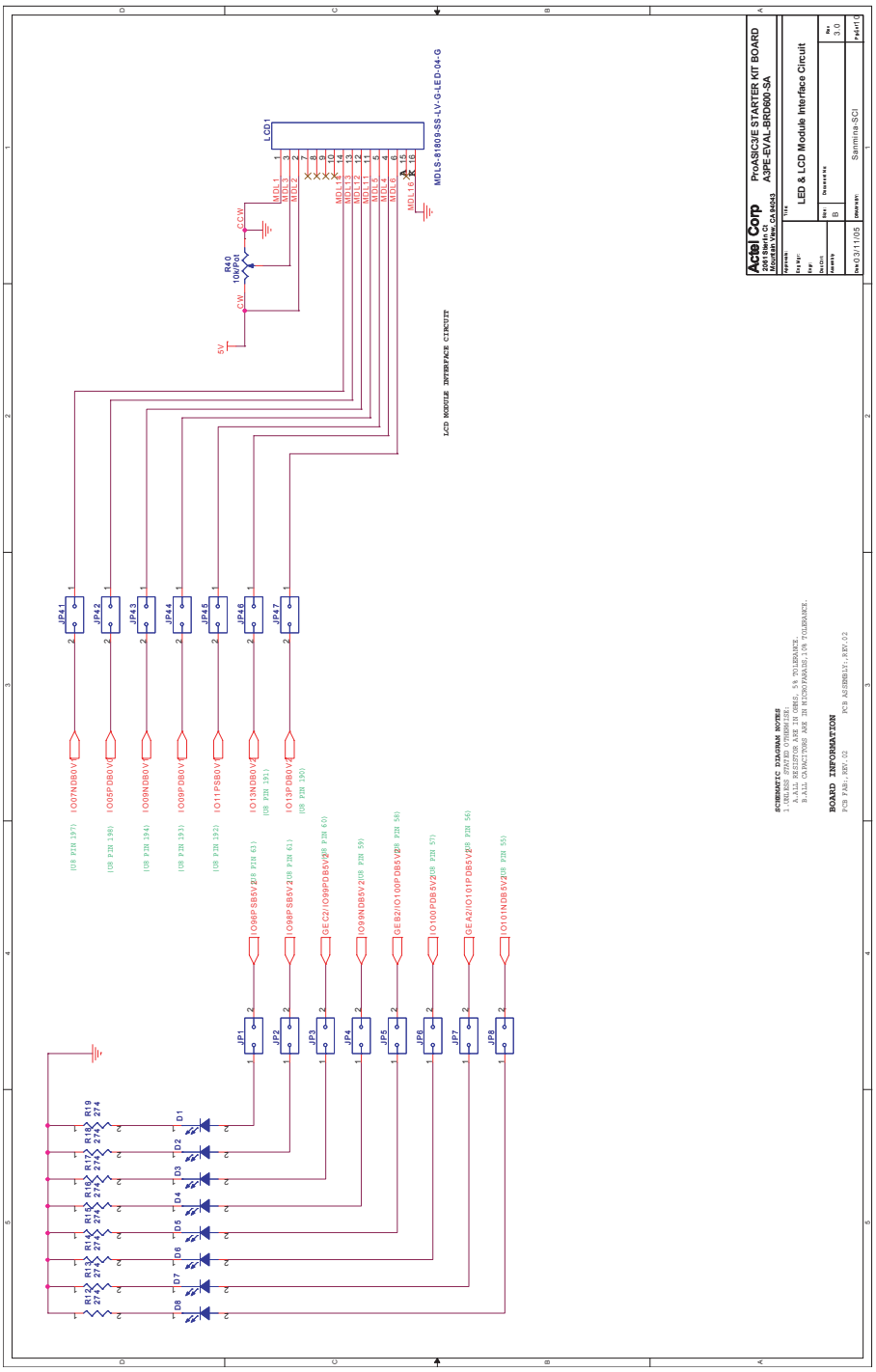

Figure B-5. LED and LCD Module Interface Circuit

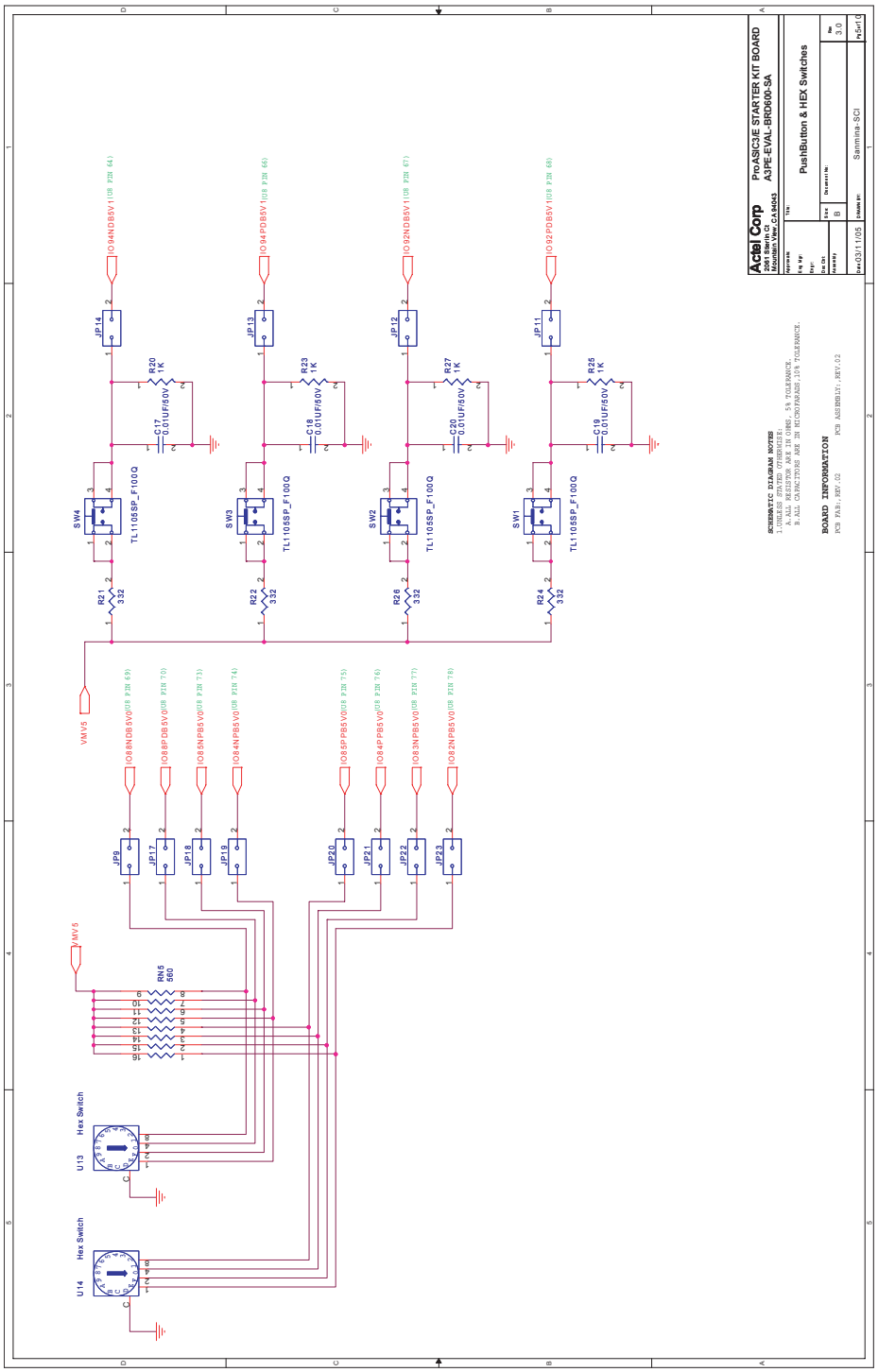

Figure B-6. PushButton and Hex Switches

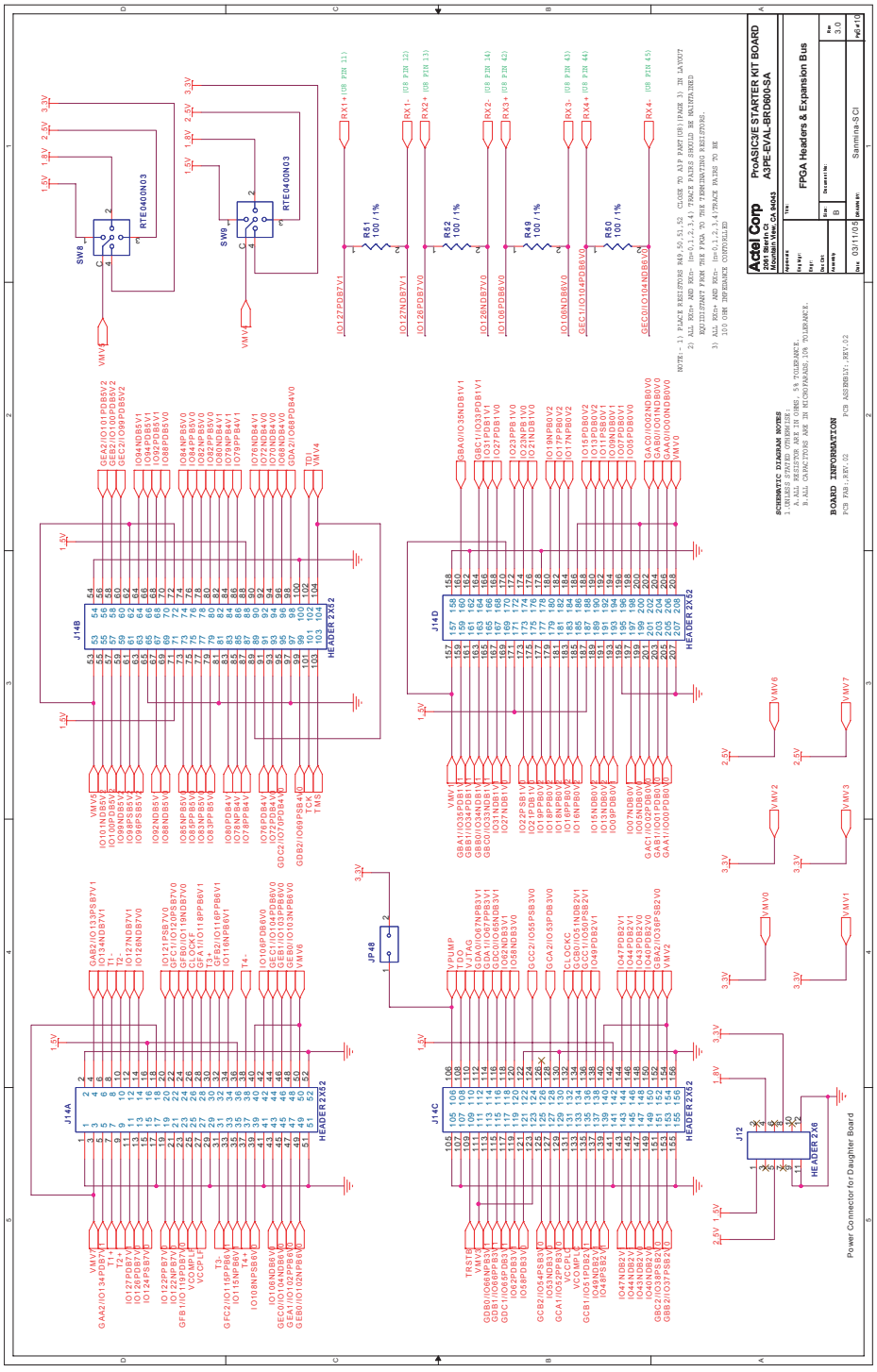

Figure B-7. FPGA Headers and Expansion Bus

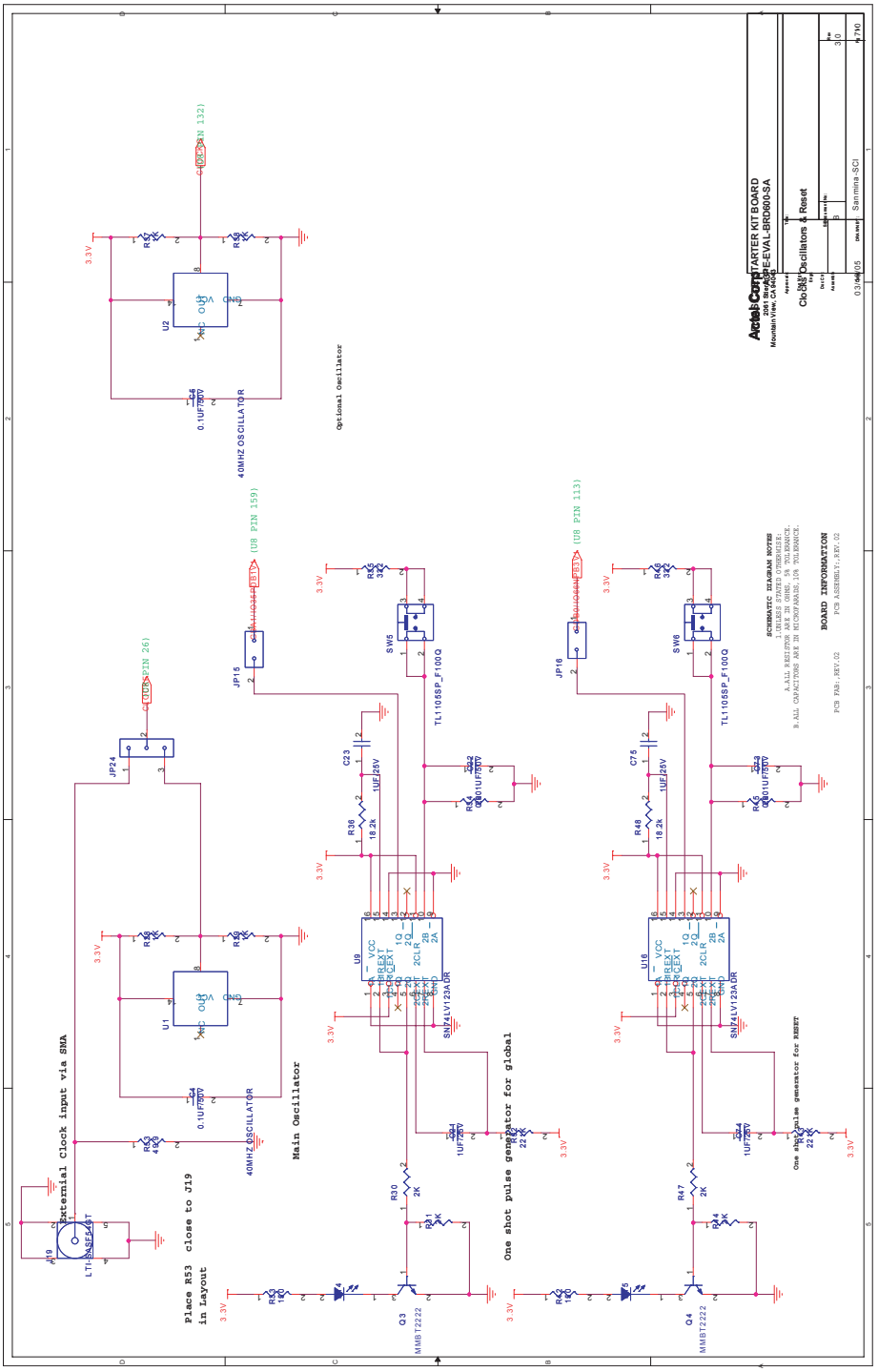

Figure B-8. Clocks Oscillators and Reset

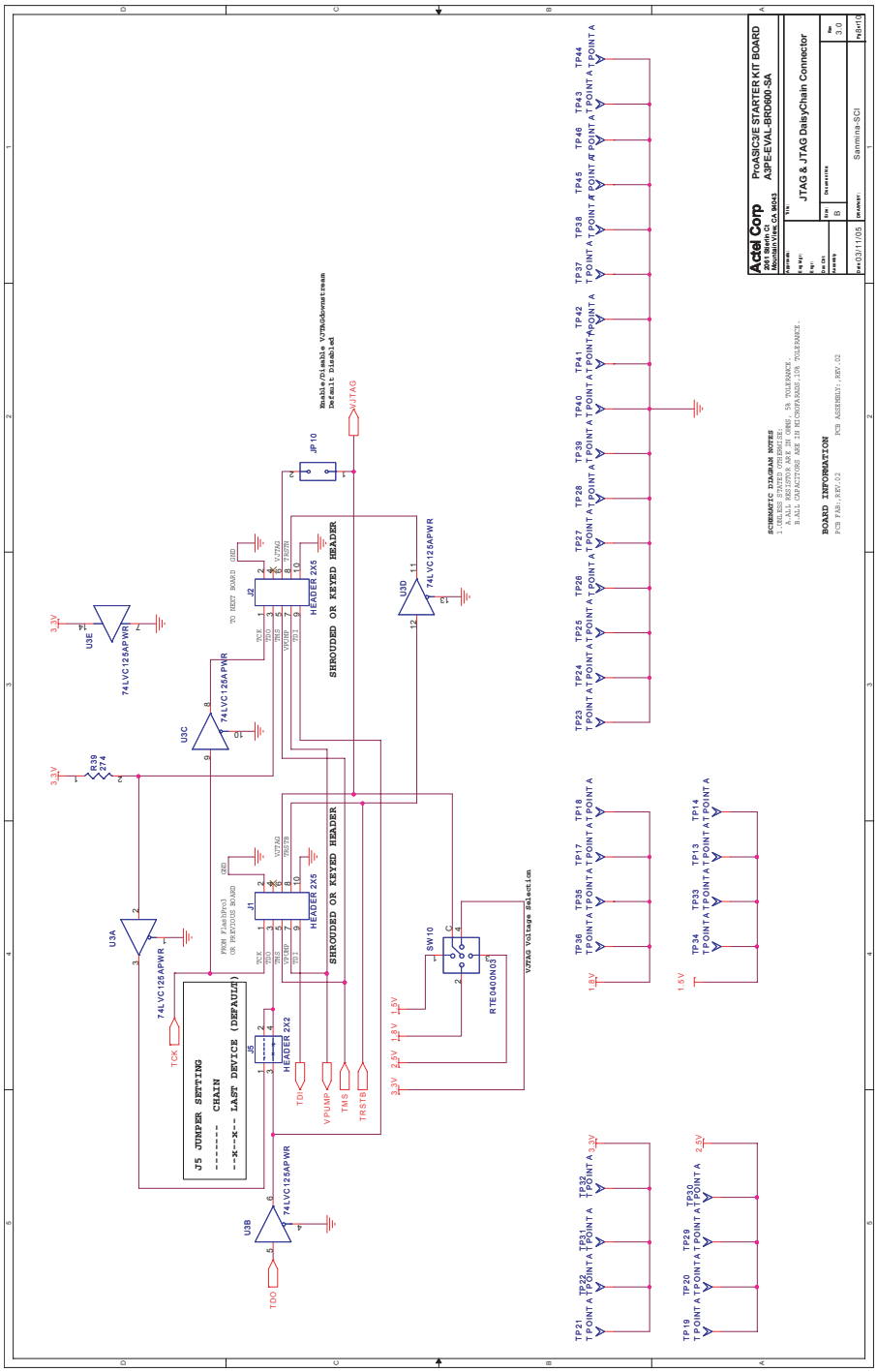

Figure B-9. JTAG and JTAG DaisyChain Connector

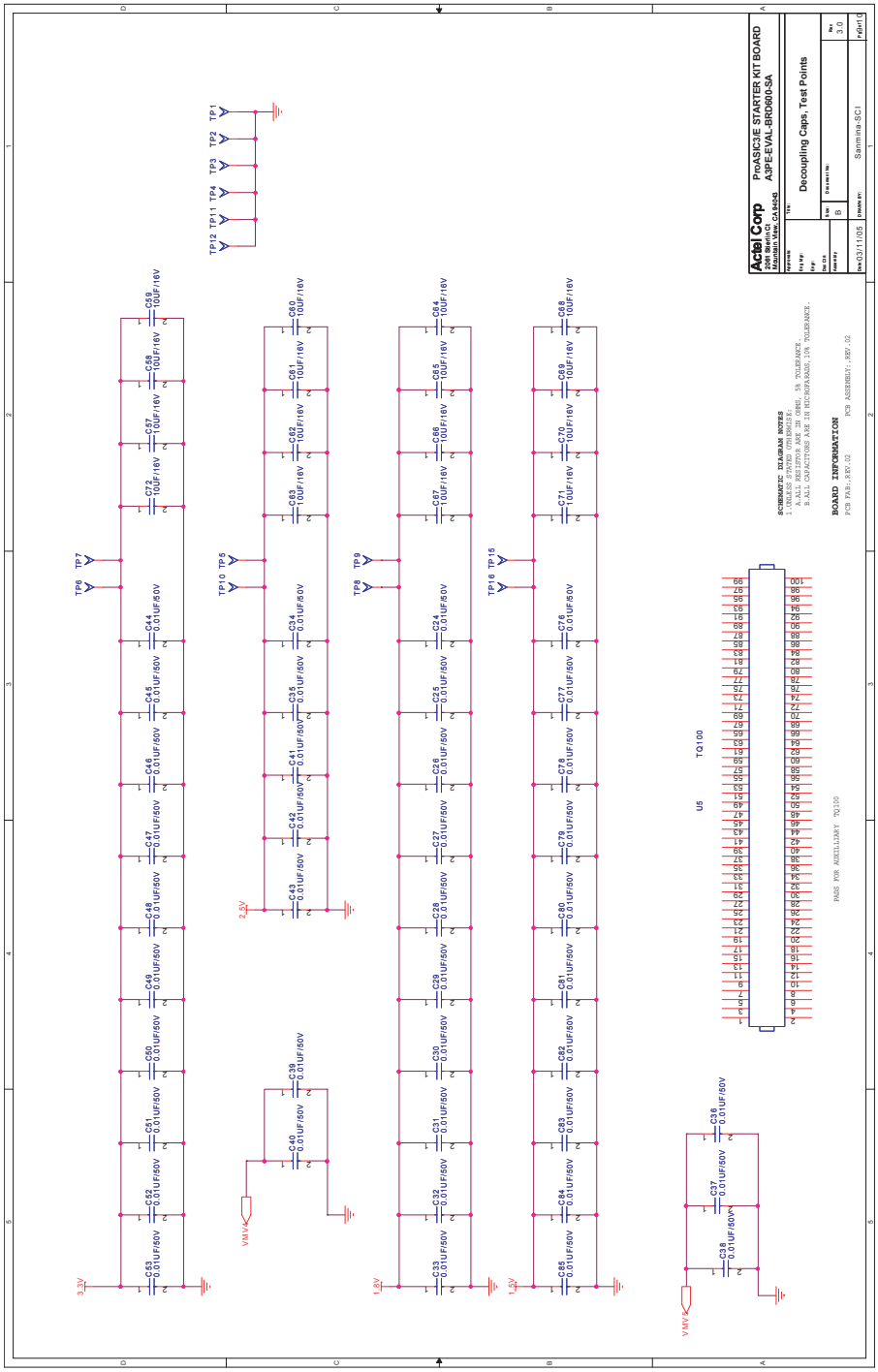

Figure B-10. Decoupling Caps, Test Points

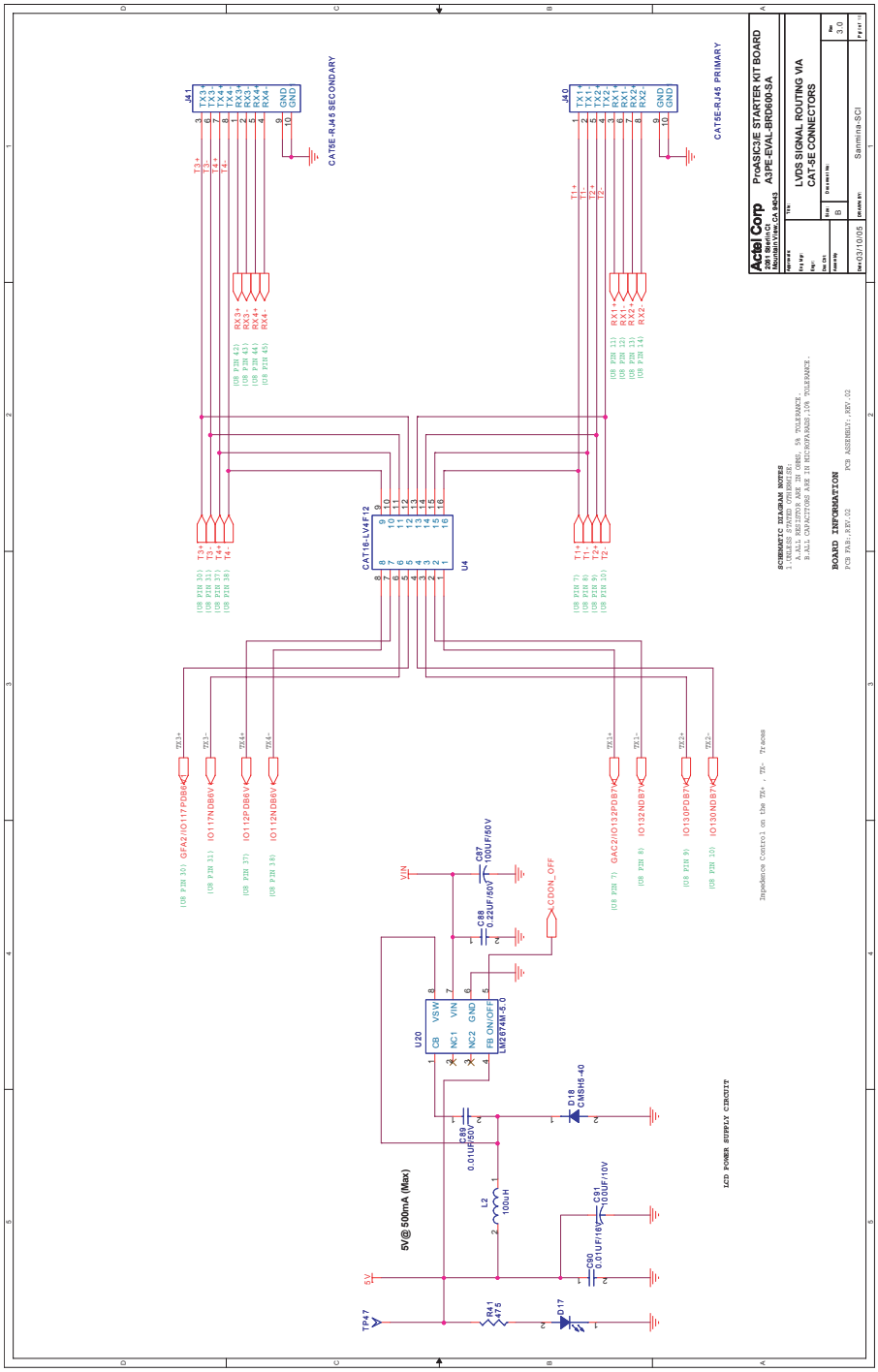

Figure B-11. LVDS Signal Routing Via CAT-5E Connectors

Signal Layers

This is a six-layer board. The board has the following layers of copper:

- Layer 1 – Top signal layer
- Layer 2 – Ground plane
- Layer 3 – Signal layer 3, used for LVDS receive and other signals
- Layer 4 – Signal layer 4, used for LVDS transmit and other signals
- Layer 5 – Power plane
- Layer 6 – Bottom signal layer

Refer to Figure C-1 on page 94 through Figure C-7 on page 100.

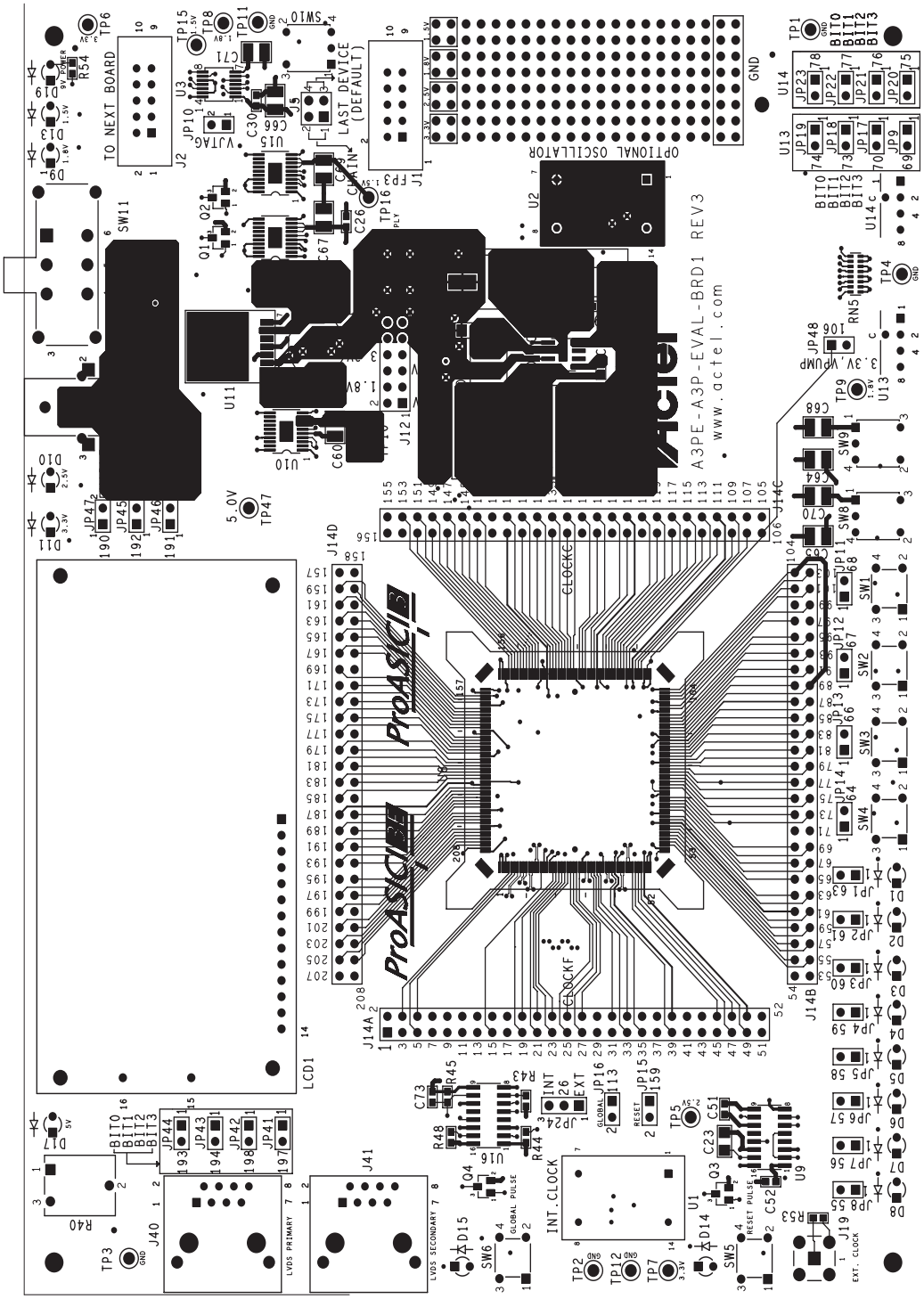

Figure C-1. Layer 1 – Top Signal Layer

Figure C-2. Layer 2 – Ground Plane (Blank)

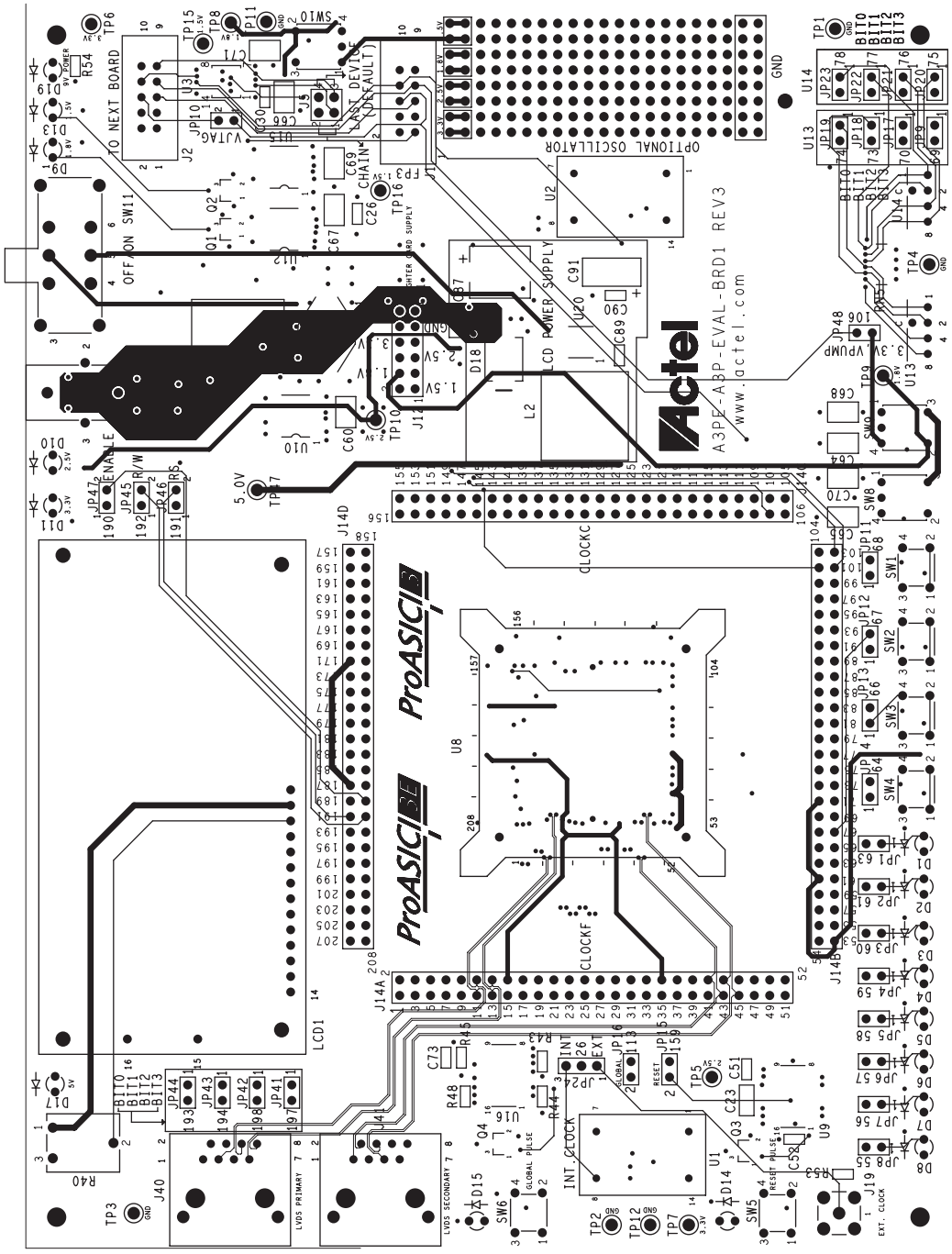

Figure C-3. Layer 3 – Signal 3 (LVDS Receive Layer)

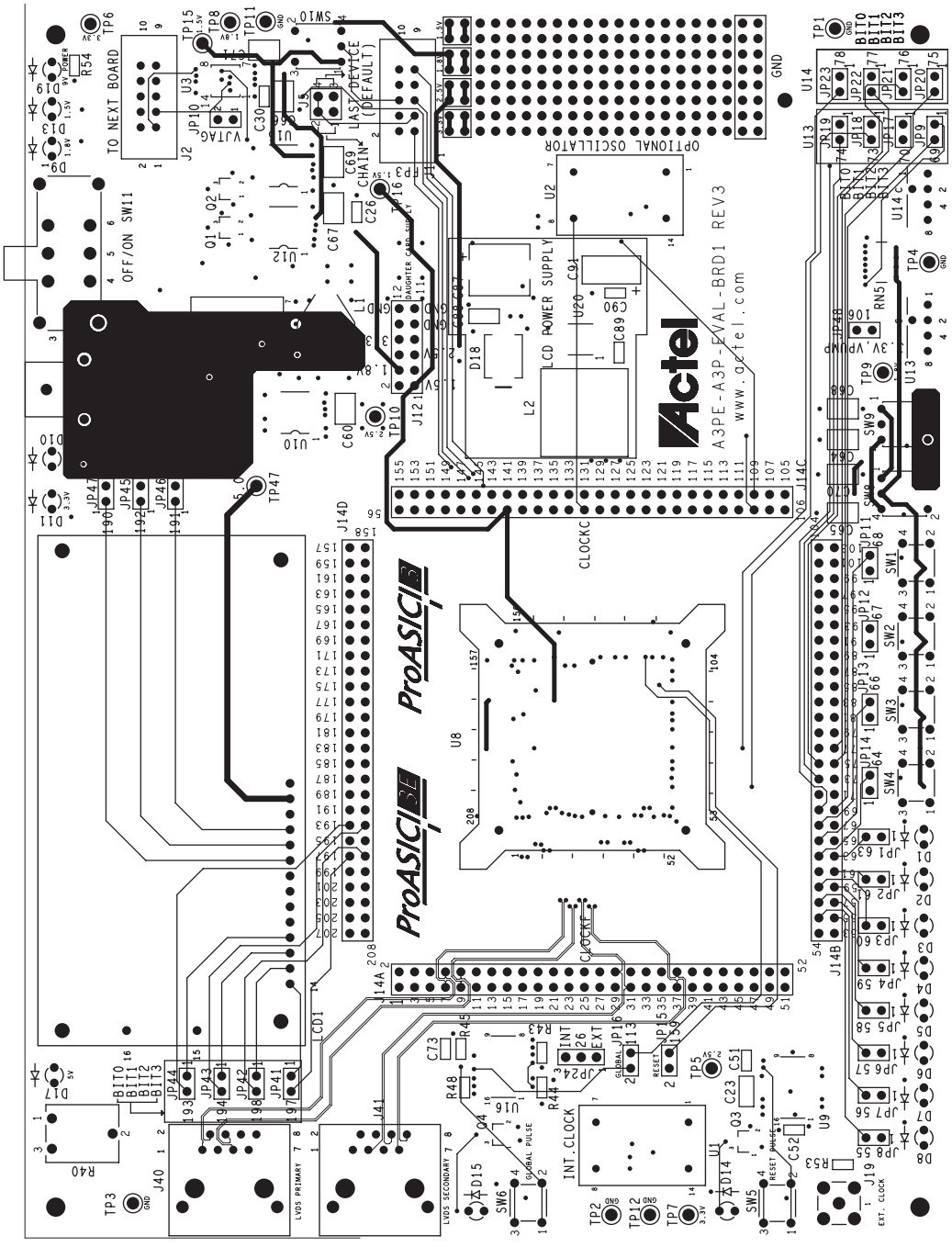

Figure C-4. Layer 4 – (LVDS Transmit Layer)

Figure C-5. Layer 5 – Power Plane (Blank)

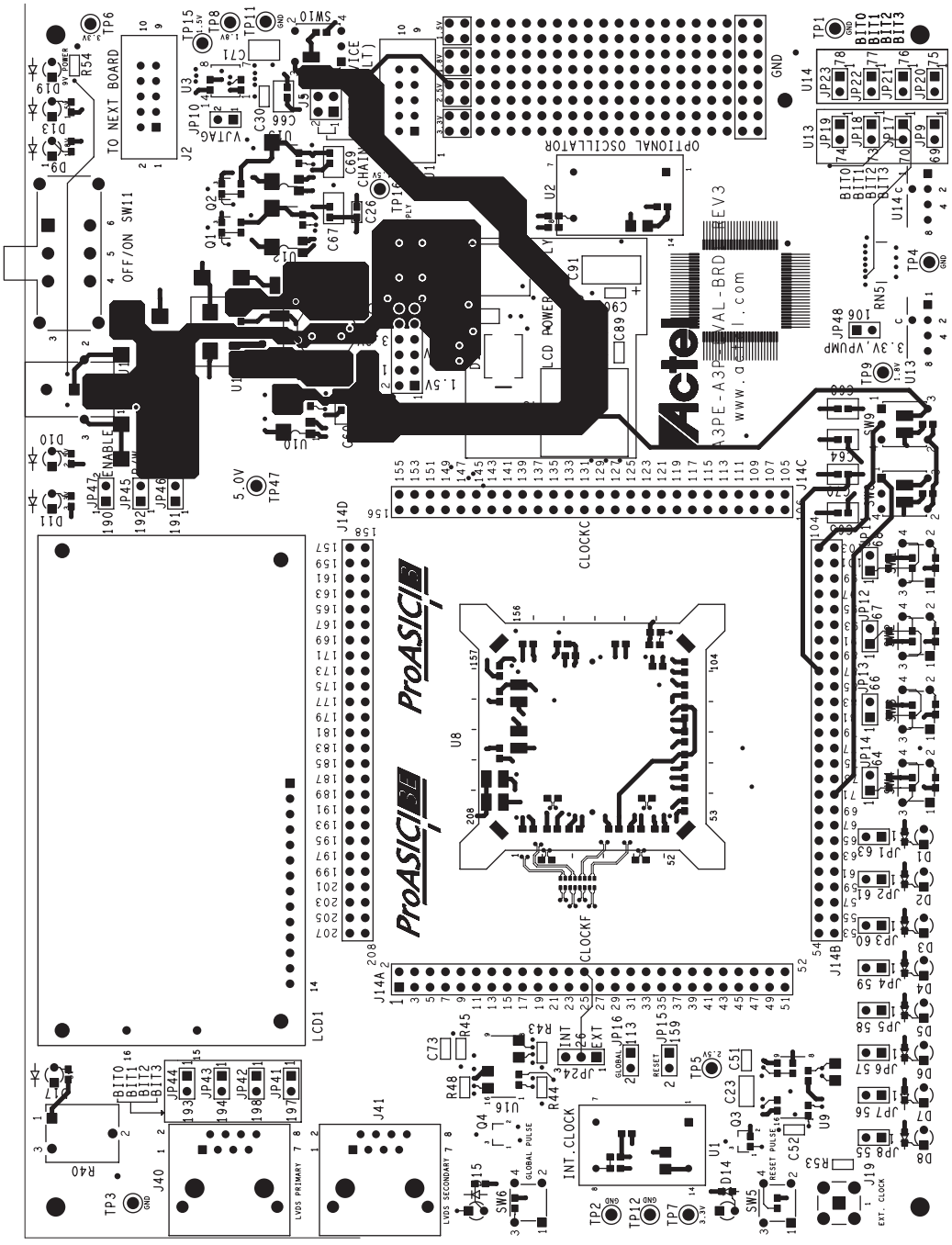

Figure C-6. Layer 6 – Bottom

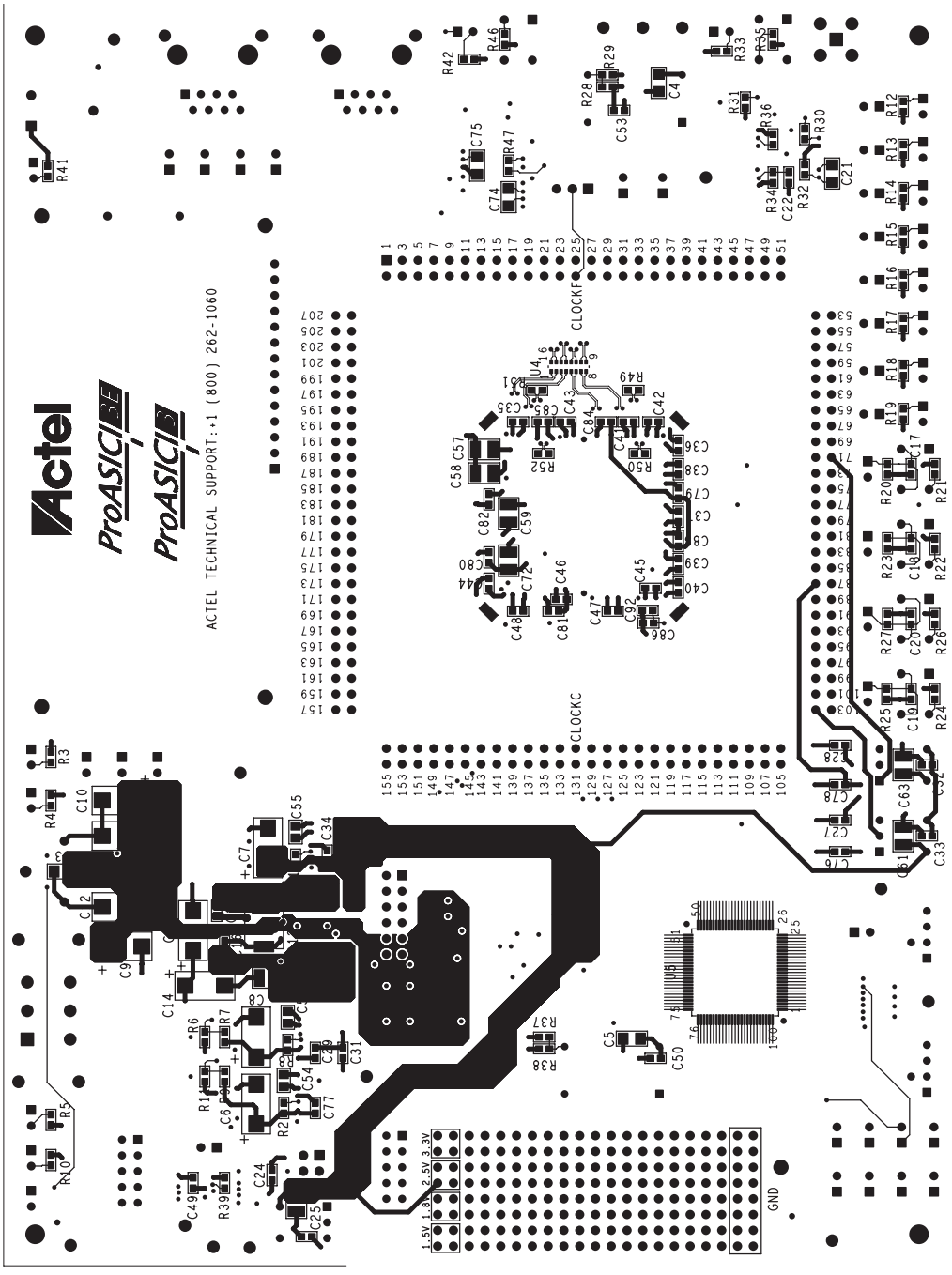

Figure C-7. Layer 6 – Bottom (Viewed from Bottom)

D

Product Support

Actel backs its products with various support services including Customer Service, a Customer Technical Support Center, a web site, an FTP site, electronic mail, and worldwide sales offices. This appendix contains information about contacting Actel and using these support services.

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Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

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From Southeast and Southwest U.S.A., call **650. 318.4480**
From South Central U.S.A., call **650.318.4434**
From Northwest U.S.A., call **650.318.4434**
From Canada, call **650.318.4480**
From Europe, call **650.318.4252** or **+44 (0) 1276 401 500**
From Japan, call **650.318.4743**
From the rest of the world, call **650.318.4743**
Fax, from anywhere in the world **650.318.8044**

Actel Customer Technical Support Center

Actel staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions. The Customer Technical Support Center spends a great deal of time creating application notes and answers to FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

Actel Technical Support

Visit the Actel Customer Support website (www.actel.com/custsup/search.html) for more information and support. Many answers available on the searchable web resource include diagrams, illustrations, and links to other resources on the Actel web site.

Website

You can browse a variety of technical and non-technical information on Actel's home page, at www.actel.com.

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Highly skilled engineers staff the Technical Support Center from 7:00 A.M. to 6:00 P.M., Pacific Time, Monday through Friday. Several ways of contacting the Center follow:

Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is tech@actel.com.

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Our Technical Support Center answers all calls. The center retrieves information, such as your name, company name, phone number and your question, and then issues a case number. The Center then forwards the information to a queue where the first available application engineer receives the data and returns your call. The phone hours are from 7:00 A.M. to 6:00 P.M., Pacific Time, Monday through Friday. The Technical Support numbers are:

650.318.4460
800.262.1060

Customers needing assistance outside the US time zones can either contact technical support via email (tech@actel.com) or contact a local sales office. Sales office listings can be found at www.actel.com/contact/offices/index.html.

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