ispPAC®10 Evaluation Board

For Configuration and Evaluation of ispPAC10 Devices

Features

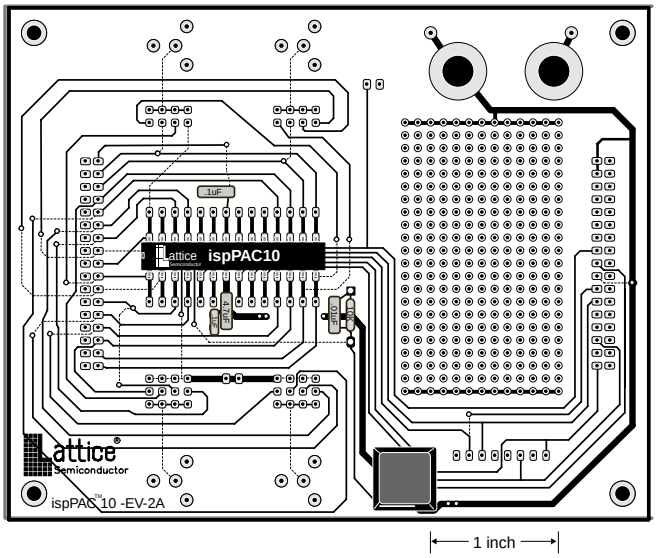
- **QUICKLY CONFIGURE & EVALUATE ispPAC10 DEVICES**
- **FULLY POPULATED DEVICE EVALUATION BOARD**
  - **VS and Ground Connectors**
  - **Decoupling and Bypass Capacitors**
  - **BNCs for Input and Output Pins**
  - **Jumpers Connect Inputs and Outputs to the BNCs**
  - **8-Pin Header Connector JTAG Programming**
  - **Interfaces with Lattice's ispDOWNLOAD® Cable Through PC Parallel Port DB-25 Connector**
  - **User Prototype Array for Custom Circuits**
- **TWO ispPAC10-P DIP DEVICE SAMPLES**

Description

The Lattice Semiconductor ispPAC10 In-System-Programmable (ISP™) Analog Circuit allows designers to build analog circuits, such as gain stages and active filters, without the use of external feedback resistors or capacitors. A standard JTAG IEEE 1149.1 interface allows the user to reconfigure the ispPAC10 while in-system using on-chip non-volatile E^2CMOS® technology.

The ispPAC10 Evaluation Board allows the user to quickly configure and evaluate the ispPAC10 on a fully assembled PC board. The double-sided board supports a 28-pin DIP package sample (included in the package), connectors for Input and Output signals, a JTAG programming cable interconnect and a prototype array section for additional circuitry to be added by the user. Each input and output is accessible to the user through BNC connectors and jumpers. The four JTAG programming signals have dedicated pins that are tied directly to the ispDOWNLOAD programming header J5. The board contains an array of 286 prototype holes that can be used for experimental evaluation and project interfacing. As an expansion feature, the programming interface signals, as well as all analog signals, are connected to dual row headers, with 34 pads, for ribbon cable or board-to-board pins. Additional jumpers allow the user to tie any input to the internal $VREF_{OUT}$ common reference circuit. The board contains a momentary push-button switch that can be used to initiate calibration. The calibration adjusts output offset and nulls the offset errors to a fraction of a millivolt. Decoupling and bypass capacitors are located on the board near the ispPAC10 device. Two banana plug receptacles are available for Vs and GND connections. A third pin is used when the optional CMV_{IN} reference voltage is externally supplied.

Figure 1. ispPAC10 Evaluation Board EV-2A



Ordering Information

Ordering Number	Description
PAC10-EV	ispPAC10 Evaluation Board

Technical Support Assistance

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