IGLOO nano Starter Kit

User's Guide

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Introduction

IGLOO nano Starter Kit Description

The IGLOO® nano starter kit is a complete package that enables you to quickly evaluate Actel's IGLOO nano family and prototype your design. The kit allows you to develop simple designs using switches and LEDs; or by removing the jumpers to the switches and LEDs you can then use the board to integrate the nano device into a full system, with all user I/Os available. In both modes you can then measure power to the device and to each I/O bank to evaluate the power consumption of your design. When using the board in conjunction with Actel's Libero® Integrated Design Environment (IDE) power analysis tools, you will have a clear picture of application power consumption at each stage in your design. In addition, the tool suite now includes power-driven layout (PDL), which can reduce the power consumption of designs up to 30 percent. Since IGLOO nano devices are footprint-compatible with ProASIC®3 nano devices, this kit can also be used to prototype designs for ProASIC3 nano FPGAs.

Key Features

- Powered by USB cable or by external power (not supplied)
- Test points for measuring current consumption of the AGLN250V2-VQG100
- USB-to-UART interface for HyperTerminal on PC connected to board
- All components used on the board are low power components (i.e., LEDs (2 mA), resets (A range), and oscillator (2-3 mA))

Board Description

The IGLOO nano evaluation board (Figure 1) enables you to measure power consumption (dynamic, static, and Flash*Freeze modes) with the core operating at either 1.2 V or 1.5 V. When using the board in conjunction with Actel's power analysis tools, you will have a clear picture of application power consumption at each stage in your design.

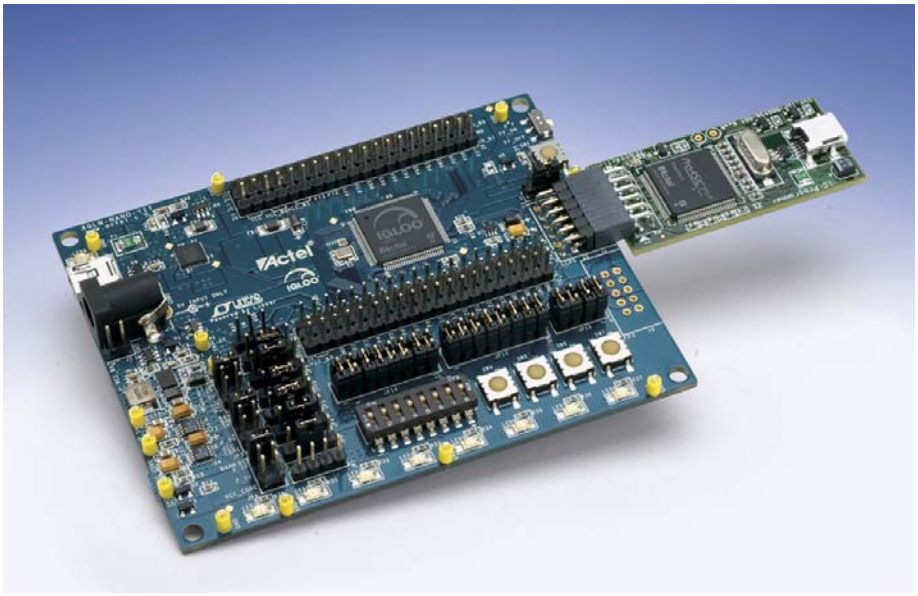


***Figure 1* • IGLOO nano Evaluation Board**

In addition, the Libero IDE tool suite now includes power-driven layout (PDL), which can reduce the power consumption of designs up to 30 percent.

The evaluation board has a small form factor, measuring 3.2 inches by 4 inches, and supports an AGLN250 IGLOO nano device in the 14 x 14 mm VQ100 package. The evaluation board consumes less than 150 mW. All components used on the board, such as LEDs, reset (µA range), and oscillator, are low-power components. Also included on the evaluation board is a USB-to-UART interface to allow for HyperTerminal on a PC to communicate with the IGLOO nano device on the board.

The right hand side of the board has a programming connector that enables the low-cost programming stick (LCPS) to be attached to the board to program the IGLOO nano AGLN250V2-VQG100 device. I/Os from the FPGA have been wired to pads on the board for debug purposes.

Kit Contents

Table 1 lists the contents of the IGLOO nano Starter Kit.

Table 1 • **IGLOO nano Starter Kit Contents**

Quantity	Description
1	IGLOO nano Evaluation Board with AGLN250V2-VQG100
1	FlashPro3-compatible low-cost programming stick (LCPS)
2	USB 2.0 high-speed cables
5	Jumpers in small packet
1	Libero IDE DVD (check web for the latest version before installing)
1	Quickstart card

Web-Based Resources

Listed below are the documents currently published on the Actel website. Additional documents and design examples may be added to the website in the future.

Users Guides and Tutorials

IGLOO nano Starter Kit User's Guide

www.actel.com/documents/IGLOO_nano_StarterKit_UG.pdf

IGLOO nano Starter Kit Quickstart Guide

www.actel.com/documents/IGLOO_nano_StarterKit_QS.pdf

IGLOO nano Starter Kit Quickstart Card

www.actel.com/documents/AGLN_NANO_KIT_QS.pdf

Libero IDE Quick Start Guide

www.actel.com/documents/gettingstarted_ug.pdf

Libero IDE User's Guide

www.actel.com/documents/libero_ug.pdf

FlashPro User's Guide

www.actel.com/documents/flashpro_ug.pdf

Libero IDE Quickstart Tutorial Design Files

IGLOO nano VHDL Design Files
www.actel.com/documents/IGLOO_nanoz_tutorial_VHDL_Libero84sp2_revB.zip
IGLOO Icicle Verilog Design Files
www.actel.com/documents/IGLOO_Icicle_tutorial_verilog_Libero84sp2_revA.zip
IGLOO Icicle VHDL Design Files
www.actel.com/documents/IGLOO_Icicle_tutorial_VHDL_Libero84sp2_revA.zip

Board References

IGLOO nano Starter Kit Board – Allegro PCB file
www.actel.com/documents/IGLOO_nano_StarterKit_PCB.zip
IGLOO nano Starter Kit Board – OrCAD Schematics (DSN)
www.actel.com/documents/IGLOO_nano_StarterKit_DSN.zip
IGLOO nano Starter Kit Board – PDF Schematics
www.actel.com/documents/IGLOO_nano_StarterKit_SS.pdf

1 – Board Components and Settings

This chapter describes the components and settings for the IGLOO nano Evaluation Board.

Block Diagram

The IGLOO nano board Evaluation Board is shown in Figure 1-1.

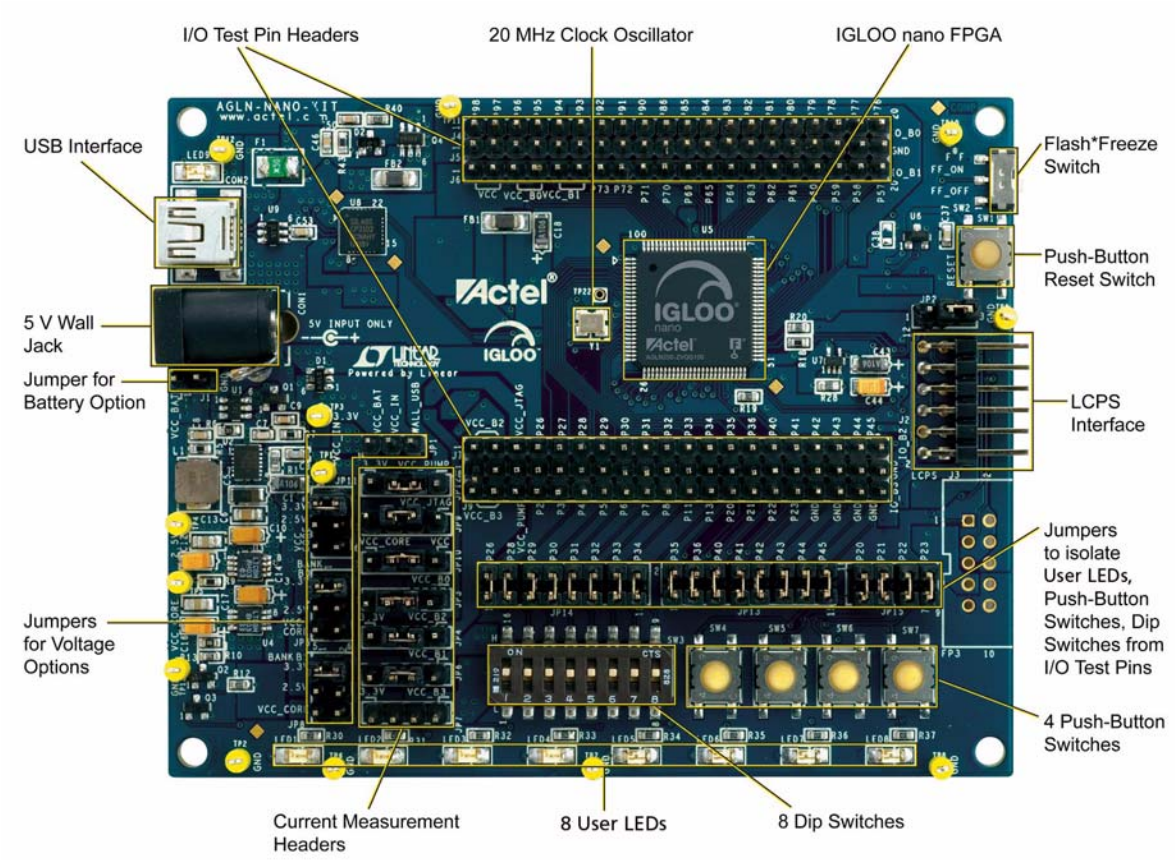


***Figure 1-1* • IGLOO nano Evaluation Board**

IGLOO nano Board Stackup

The IGLOO nano board is built on a four-layer printed circuit board (PCB):

1. Top Signal (Figure 1-2)
2. Power
3. GND
4. Bottom Signal (Figure 1-3 on page 11)

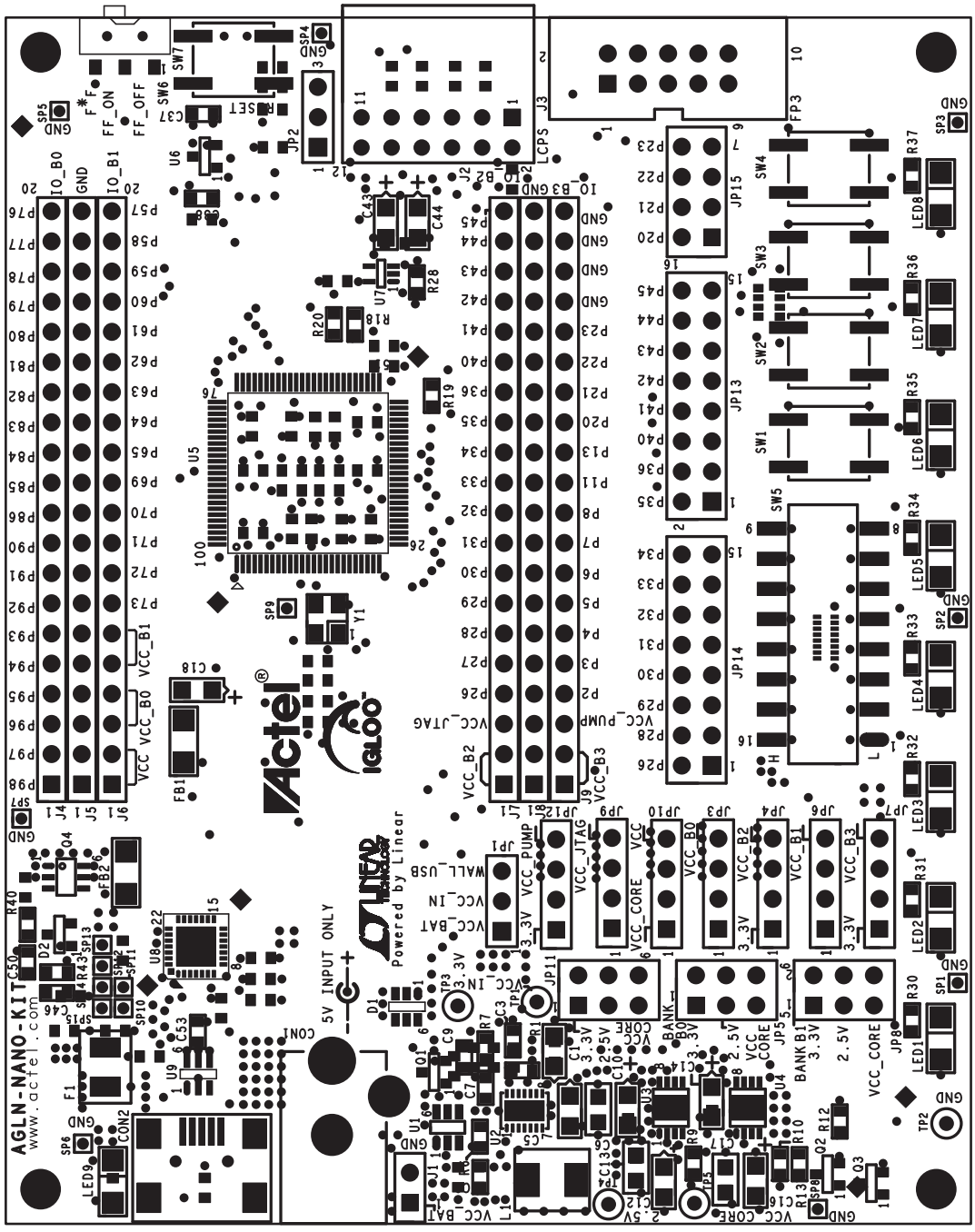


***Figure 1-2* • Top Silkscreen**

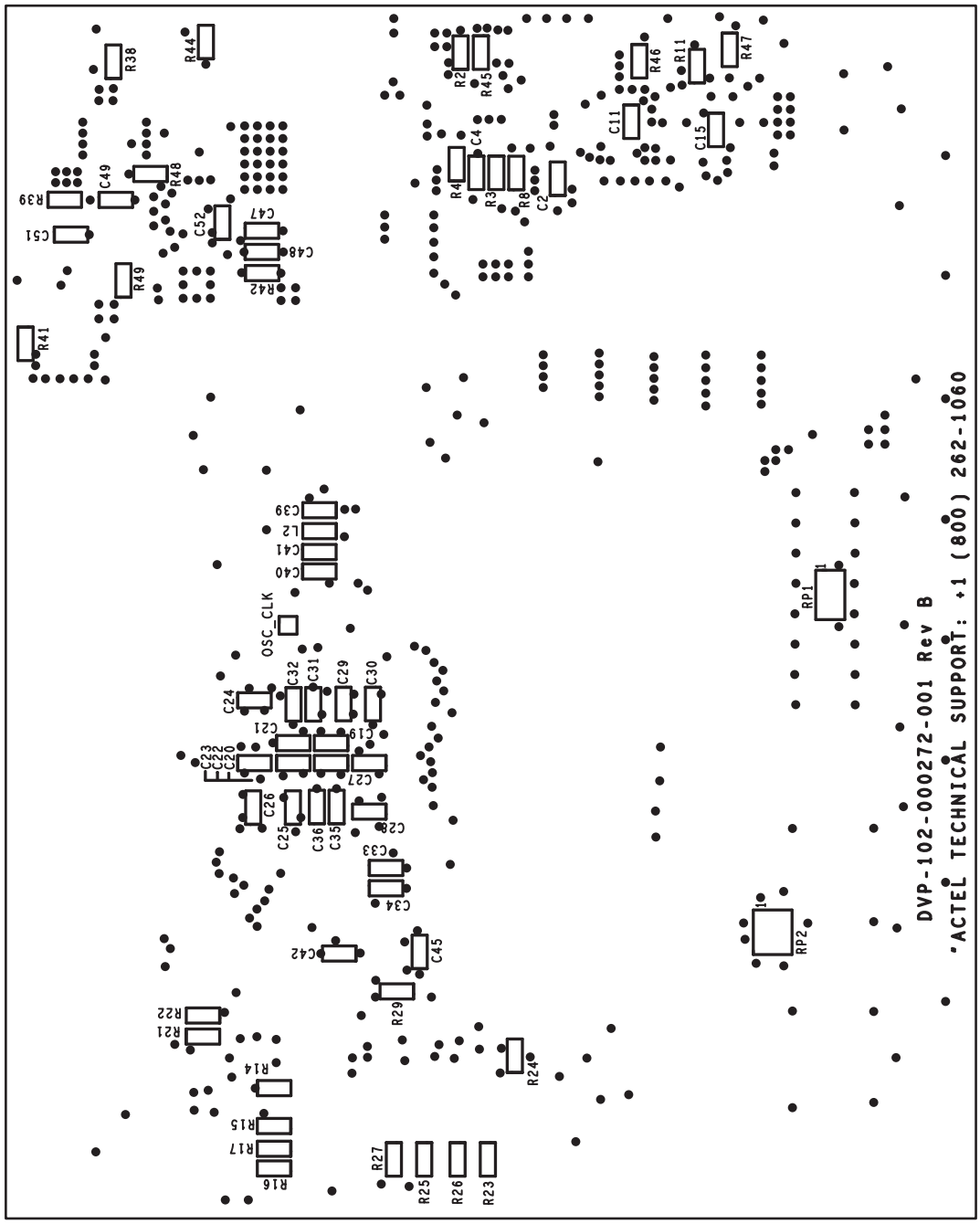


Figure 1-3 • **Bottom Silkscreen**

Jumper and Switch Settings

Recommended default jumper settings are defined in Table 1-1. The voltage selection jumpers are highlighted in grey. Connect jumpers in the default settings described in Table 1-1 to enable the pre-programmed demo design to function correctly.

***Table 1-1* • Jumper Settings for Demo Design**

Jumper	Default Setting	Comment
JP1	Pin 2-3	Main power supply. Connect Wall/USB input to VCC_IN.
JP2	Pin 2-3	VCC CORE voltage (1.2 / 1.5 V) Pin 2-3 selects 1.2 V. Pin 1-2 selects 1.5 V. Jumper is on upper right area of board.
JP3	Pin 2-3	Current measurement header for Bank 0
JP4	Pin 2-3	Current measurement header for VCC_B2 (Bank 2)
JP5	Pin 1-2	Voltage selection for VCC B0 (Bank 0) Pin 1-2 selects 3.3 V. Pin 3-4 selects 2.5 V. Pin 5-6 selects VCC_CORE.
JP6	Pin 2-3	Current measurement header for Bank 1
JP7	Pin 2-3	Current measurement header for VCC_B3 (Bank 3)
JP8	Pin 1-2	Voltage selection for VCC B1 (Bank 1) Pin 1-2 selects 3.3 V. Pin 3-4 selects 2.5 V. Pin 5-6 selects VCC_CORE.
JP9	Pin 2-3	Current measurement header for JTAG supply.
JP10	Pin 2-3	Current measurement header for VCC (FPGA core supply).
JP11	Pin 1-2	Voltage selection for VCC JTAG (JTAG supply. Pin 1-2 selects 3.3 V. Pin 3-4 selects 2.5V. Pin 5-6 selects VCC_CORE.
JP12	Pin 2-3	Current measurement header for VCC_PUMP (FPGA charge pump supply)
JP13	Pin 1-2	Remove each short default jumper to disconnect any of the 8 LEDs from the FPGA.
JP14	Pin 1-2	Remove each short default jumper to disconnect any of the 8 DIP switches SW3.1 through SW3.8 from the FPGA. By default, SW3.1 through SW3.8 should all be closed (set to the ON settings). The 8 DIP switches are connected to the 8 LEDs (LED1, LED2, … LED8).
JP15	Pin 1-2	Remove each short default jumper to disconnect any of the four push-button switches, SW4 through SW7, from the FPGA.
SW1	OFF	**Flash*Freeze**: To enable Flash*Freeze mode, slide SW1 toward FF_ON. In Flash*Freeze mode, current consumption of the FPGA goes below 50 µA. Current can be measured by placing a current meter between [pin1 or pin 2] and [pin 3 or pin 4] of JP10 (VCC_CORE).

FPGA Description: AGLN250V2-VQG100

This IGLOO nano board is populated with an IGLOO nano AGLN250V2-VQG100 FPGA. An IGLOO nano AGLN250 FPGA supports the enhanced nano features of Schmitt Trigger input, bus hold (holds previous I/O state in Flash*Freeze mode), cold-sparing, hot-swap I/O capability, and 1.2 V programming.

In Designer, users can target their design to use either IGLOO AGL250 or IGLOO nano AGLN250. Some features are listed in the "Key Features" section and Table 1-2. Refer to the *IGLOO nano Datasheet* for additional features.

Key Features

- Ultra-low power in Flash*Freeze mode
- Enhanced commercial temperature
- Reprogrammable flash technology
- 1.2 V to 1.5 V single voltage operation
- Enhanced I/O features
- Selectable Schmitt trigger Inputs
- Clock conditioning circuits (CCCs) and integrated PLLs
- Embedded SRAM and nonvolatile memory (NVM)
- In-system programming (ISP) and security

***Table 1-2* • Features of AGLN250V2-VQG100**

Component	Specification
System Gates	250,000
Typical Equivalent Macrocells	2,048
VersaTiles (D-flip-flops)	6,144
Flash*Freeze Mode (Typical, µW)	24
RAM kbits (1,024 bits)	36
4,608-Bit Blocks	8
FlashROM (bits)	1,024
Secure (AES) ISP	Yes
Integrated PLLs in CCCs	1
VersaNet Globals	18
I/O Standards	Std. or Hot-Swap
I/O Banks	4
Speed Grades	Std.
Temperature Grade	C, I
Single-Ended I/Os	68

For further information, refer to the IGLOO nano datasheet:

http://www.actel.com/documents/IGLOO_nano_DS.pdf.

AGLN250V2-VQG100 I/O Banks and Pins

Figure 1-4 shows the I/O banks for AGLN250V2-VQG100.

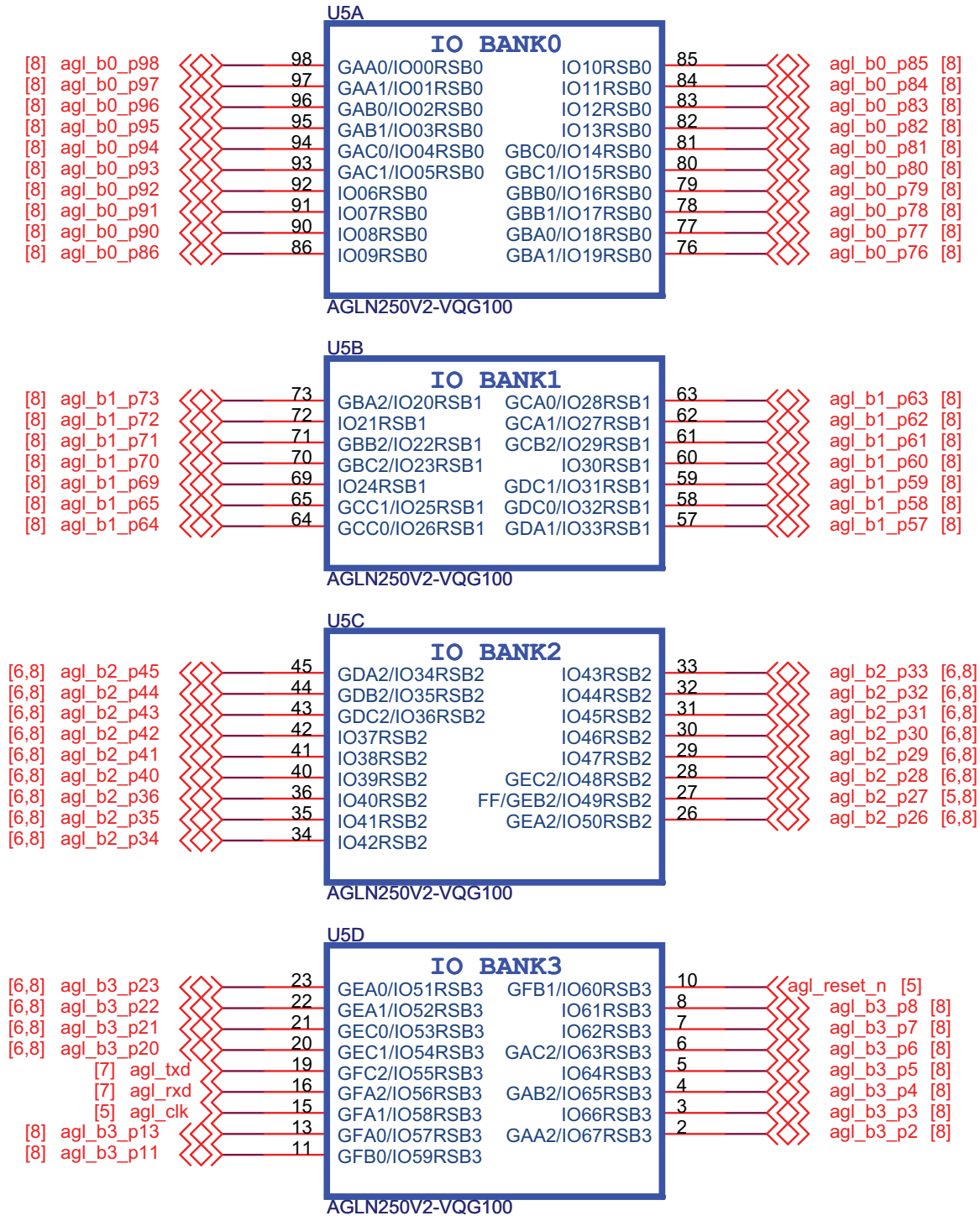


Figure 1-4 • **AGLN250V2-VQG100 Banks 0–3 Schematic**

This FPGA has advanced I/O features such as JTAG pins for the IEEE 1149.1 JTAG Boundary Scan Test (Figure 1-5).

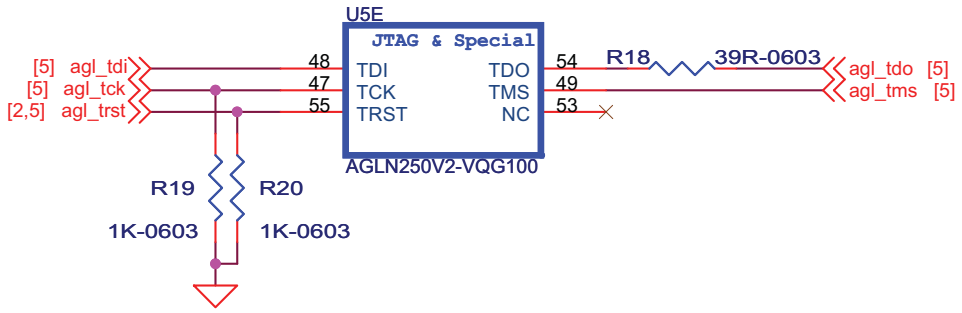


***Figure 1-5* • AGLN250V2-VQG100 JTAG Pins**

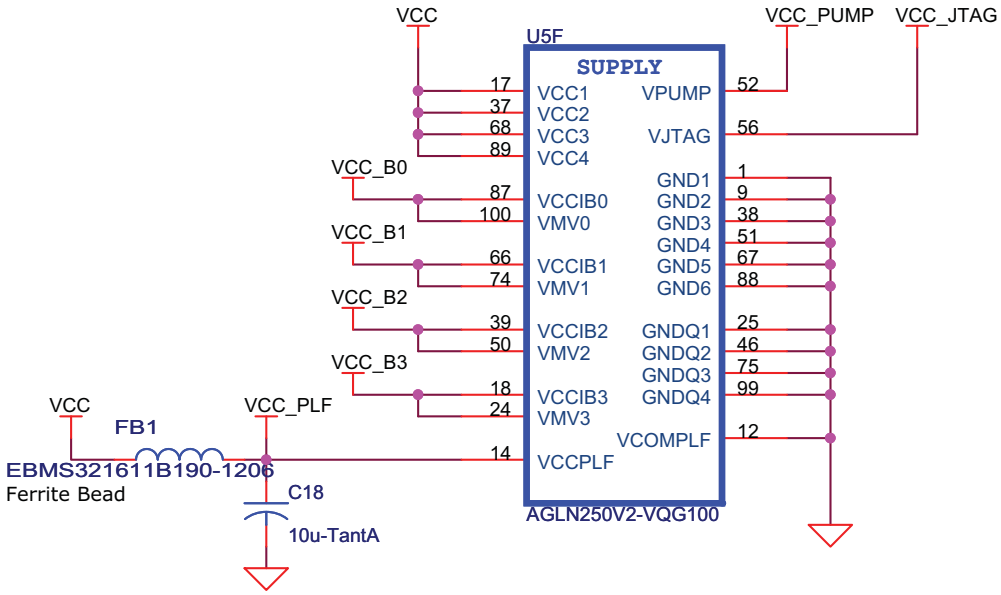


***Figure 1-6* • AGLN250V2-VQG100 Power and GND pins**

FPGA decoupling capacitors are placed close to the power pins (Figure 1-7).

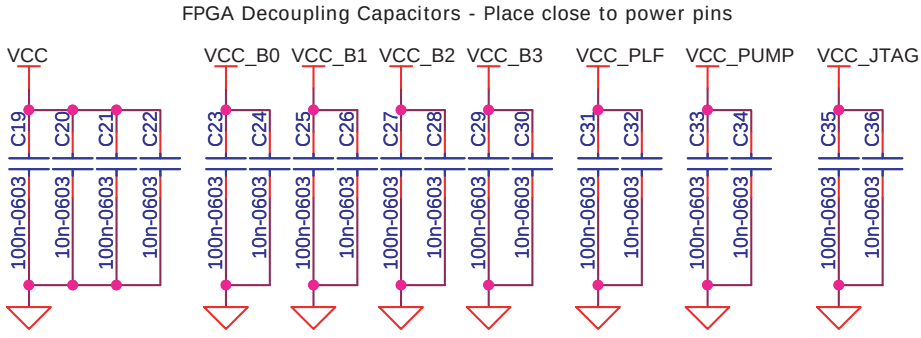


***Figure 1-7* • Decoupling Capacitors**

2 – Power

The IGLOO nano development board is powered through an external voltage power brick or USB. If both the power brick and USB are plugged in, the development board will power through the power brick. If the power brick is unplugged, the board will seamlessly switch to power through the USB. In the USB option, in-rush current meets USB specifications. The power brick option is provided in cases when 100% of total I/Os are utilized.

The development board has an input of a 5 V supply from the power brick. Protection diodes are used to protect against negative voltage. Three voltage rails (3.3 V, 2.5 V, and 1.5 V) are provided.

The regulator can be switched between the 1.5 V and 1.2 V rail because the FPGA core functions at 1.2 V, but is programmed at 1.5 V. A green LED will glow whenever the USB power is connected. Table 2-1 gives the current ratings for each voltage rail.

***Table 2-1* • Power Regulator Current Ratings**

Regulator	Current Rating
3.3 V	2A
2.5 V	1A
1.5 V	1A

Figure 2-1 shows the schematic for the power LED9.

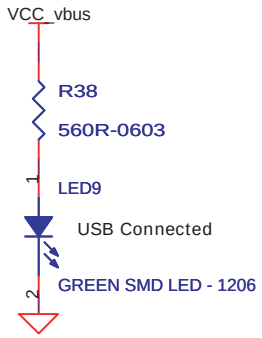


***Figure 2-1* • Power LED Schematic**

Power Modes

In addition to the board, the IGLOO nano FPGA offers power advantages. Some key power advantages of the IGLOO nano FPGAs are as follows:

- Flash*Freeze technology enables easy entry and exit from the static low power mode, whereas IGLOO consumes as little as 5 µW while retaining the contents of the system memory and data registers.
- Sleep and shutdown modes enable the IGLOO nano FPGA core power supply (or all power supplies) to be powered down when functionality is not required, while the rest of the system remains powered.
- The user low static ICC macro (ULSICC) reduces IGLOO nano FPGA dynamic and static power consumption. The ULSICC macro, when enabled, disables the FlashROM, reducing the overall power of the device.

Table 2-2 gives a summary of the power modes available with IGLOO nano devices in general and is extracted from the “Actel’s Flash*Freeze Technology and Low Power Modes” chapter of the *IGLOO nano FPGA Fabric User’s Guide*.

***Table 2-2* • Power Modes**

Mode		VCC	VCCI	Core	Clocks	ULSICC Macro	To Enter Mode	To Resume Operation	Trigger
Active		On	On	On	On	N/A	Initiate clock	None	–
Static	Idle	On	On	On	Off	N/A	Stop clock	Initiate clock	External
	Flash*Freeze Type 1	On	On	On	On*	N/A	Assert FF pin	Deassert FF pin	External
	Flash*Freeze Type 2	On	On	On	On*	Used to enter Flash*Freeze mode	Assert FF pin and LSICC	Deassert FF pin	External
Sleep		On	Off	Off	Off	N/A	Shut down VCC	Turn on VCC	External
Shutdown		Off	Off	Off	Off	N/A	Shut down VCC and VCCI supplies	Turn on VCC and VCCI supplies	External

*Note: *External clocks can be left toggling while the device is in Flash*Freeze mode. Clocks generated by the embedded PLL will be turned off automatically.*

Battery

The VIN (minimum output voltage) for the battery is 3 V. Potentially two Alkaline cells or button cells, such as LIR2450, can be used to power the board. In order to power through the higher voltage from the power brick or lower voltage from the battery, special regulators are used to meet the voltage requirements. The 3.3 V regulator used is a buck-boost type instead of a regular LDO type.

No battery casing is provided on the board. A 2-pin jumper for VBAT and GND must be provided to the input of the main regulator; you have the option of powering through a wall/USB or powering through external batteries.

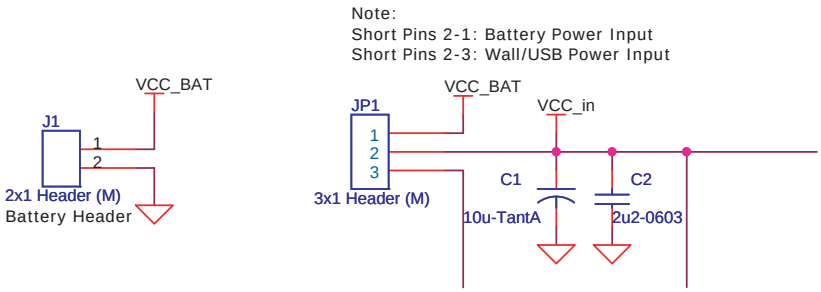
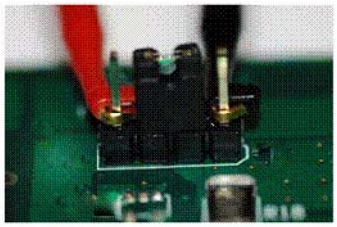


***Figure 2-2* • Battery Header and Power Input Schematics**

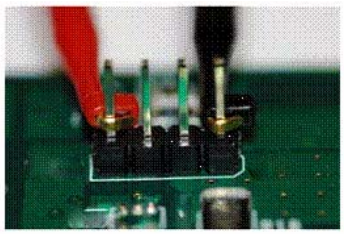
Current Measurement

Once the IGLOO nano evaluation board is powered up, you can evaluate power usage by current consumption, using the current measurement pins on the board. All banks are separated and two of the banks have the option of powering through 3.3 V or 2.5 V.

Once the IGLOO nano evaluation board is powered up, you can evaluate power consumption using the current measurement 4-pin headers on the board (Figure 2-3). Current measurement can be made without powering down the board.



Set the multimeter to measure current and attach the probes to pins 1 and 4 when the board is in normal operation.



Remove jumper from pins 2-3 for current measurement without powering down.

***Figure 2-3* • Current Measurement 4-Pin Headers**

Figure 2-4 shows the schematic for the current measurement headers.

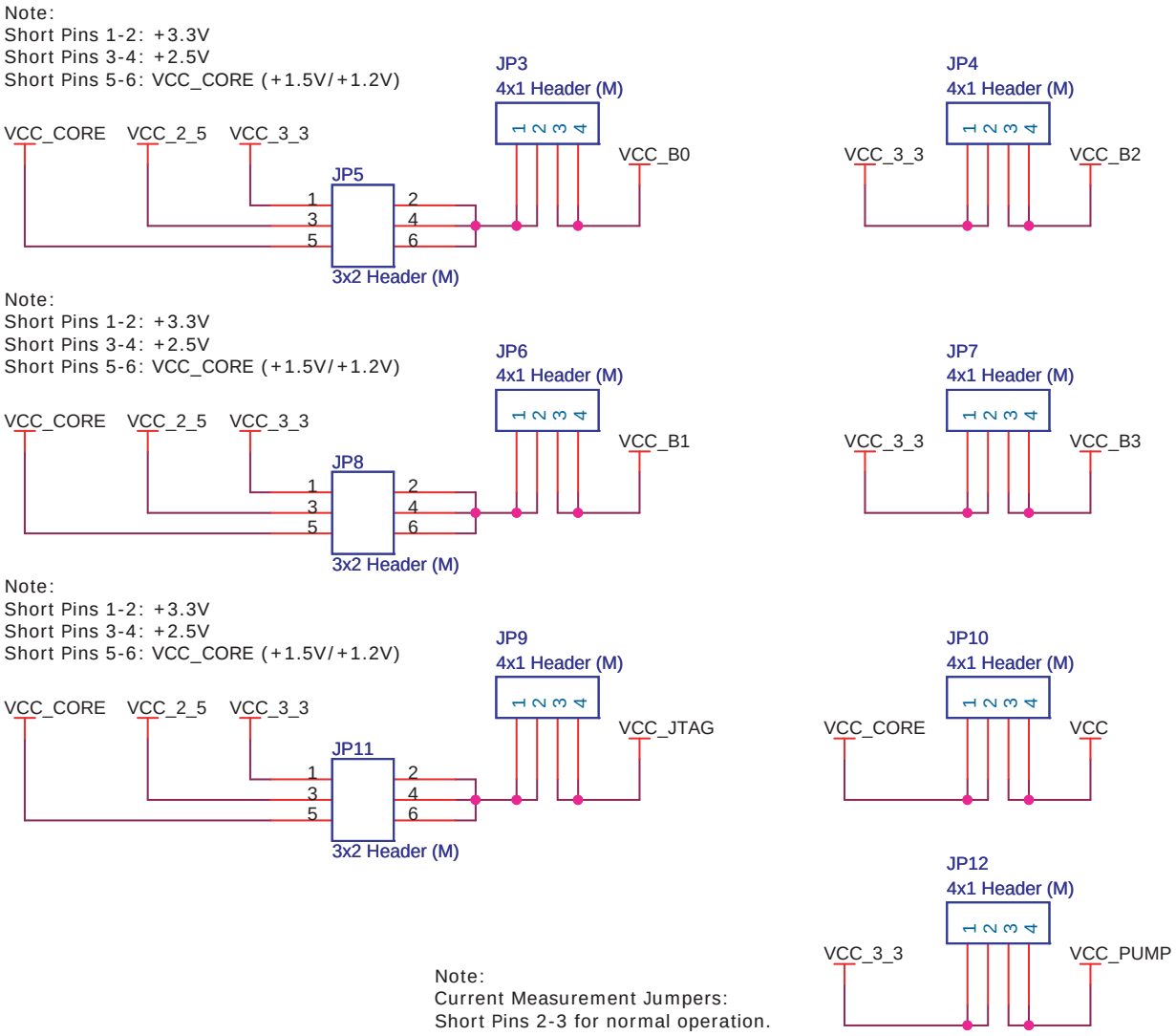


***Figure 2-4* • Current Measurement Header Schematic**

3 – Operation of Board Components

This chapter describes operation of the IGLOO nano Evaluation Board.

Clock Oscillator

One 20 MHz clock oscillator is provided on the board. The specifications are shown in Table 3-1. When combined with the on-chip CCC/PLL block, a wide range of clock frequencies can be created to support various design requirements.

***Table 3-1* • Clock Specifications**

Feature	Specification
Frequency	20 MHz
Package/Case	SMD 3.2 mm x 2.5 mm
Supply Voltage	3.3 V
Current Supply	5 mA
Operating Temperature	–20°C to 70°C
Frequency Stability	±100 ppm
RoHS Status	RoHS compliant
Duty – CMOS level (1/2 VDD)	40–60%
Rise and Fall Time (0.2 VDD and 0.8 VDD)	10 ns (maximum)
Start-up Time	10 ms (maximum)

Reference

Additional information on this clock oscillator is available at Actel's IGLOO nano Starter Kit website:

www.actel.com/products/hardware/devkits_boards/igloonano_starter.aspx.

Schematic

Figure 3-1 shows the schematic for the clock oscillator.

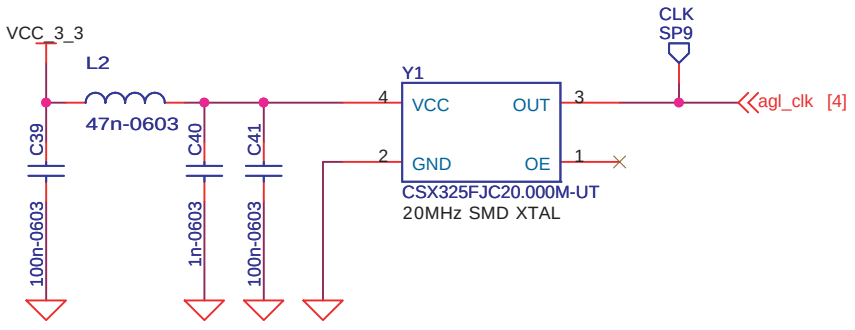


***Figure 3-1* • Clock Oscillator Schematic**

Reset

A push-button reset switch with a Schmitt-triggered device (DS1818) is provided for the IGLOO nano AGLN250 FPGA populated on the board. This Schmitt trigger device can be bypassed because an AGLN250 FPGA supports additional I/O advanced features such as Schmitt trigger.

The DS1818 uses a precision temperature-compensated reference and comparator circuit to monitor the status of the power supply (VCC). When an out-of-tolerance condition is detected, an internal power-fail signal is generated which forces reset to the active state. When VCC returns to an in-tolerance condition, the reset signal is kept in the active state for approximately 150 ms to allow the power supply and processor to stabilize.

Reference

Additional information on this push-button reset switch is available at Actel's IGLOO nano Starter Kit website:

www.actel.com/products/hardware/devkits_boards/igloonano_starter.aspx.

Schematic

Figure 3-2 shows the schematic for reset.

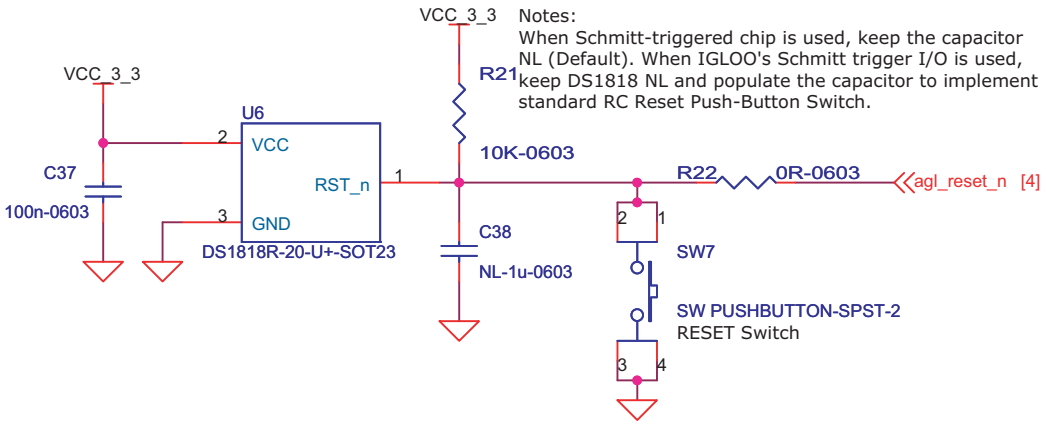


***Figure 3-2* • Reset Schematic**

Flash*Freeze Switch

Flash*Freeze technology enables the user to quickly (within 1 µs) enter and exit Flash*Freeze mode by activating the Flash*Freeze pin while all power supplies are kept at their original values. I/Os, global I/Os, and clocks can still be driven and can be toggling without impact on power consumption, and the device retains all core registers, SRAM information, and I/O states. I/Os can be individually configured to either hold their previous states or can be tristated during Flash*Freeze mode.

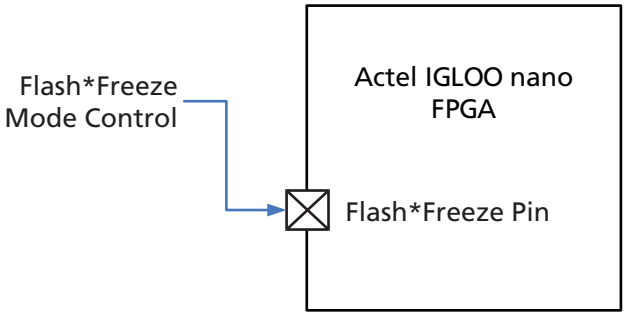


***Figure 3-3* • Flash*Freeze Mode Control**

An F*F switch is provided on the board for designs that utilize the Flash*Freeze technology. Setting the F*F switch to FF_ON will enable the Flash*Freeze mode of the IGLOO nano device. In the Flash*Freeze schematic shown in Figure 3-4, the Schmitt device is use to reduce noise on the F*F input of the IGLOO nano FPGA. This Schmitt device can be bypassed with a resistor because an AGLN250 FPGA supports additional I/O advanced features such as Schmitt trigger.

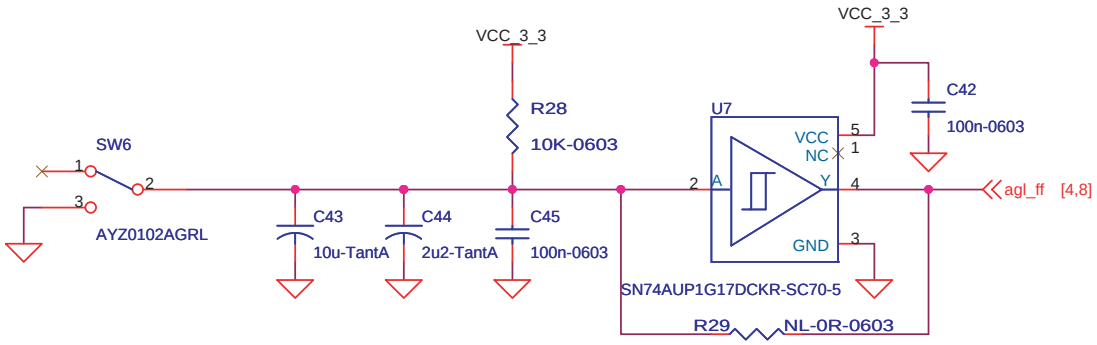


***Figure 3-4* • Flash*Freeze Schematic**

Push-Button Switches

Four active low push-button switches are provided on the board for user debug. You can remove the corresponding jumpers from the 4 x 2 Header to detach any of the four push-button switches from the FPGA I/O. Schematics are shown in Figure 3-5 and Figure 3-6.

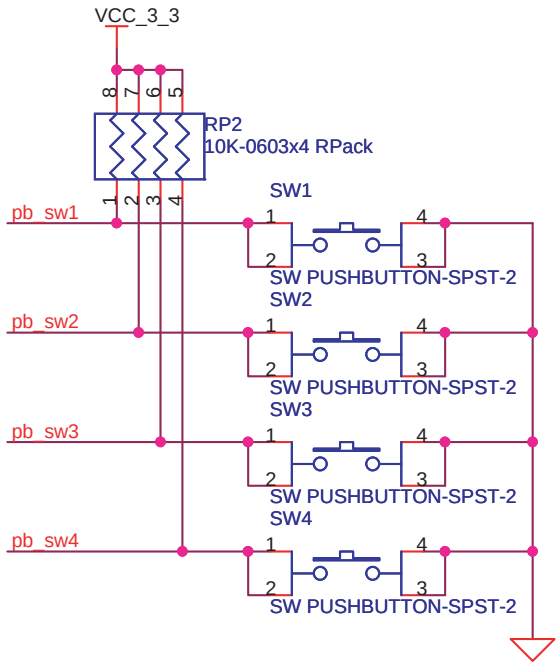


***Figure 3-5* • Push-Button Switches Schematic**

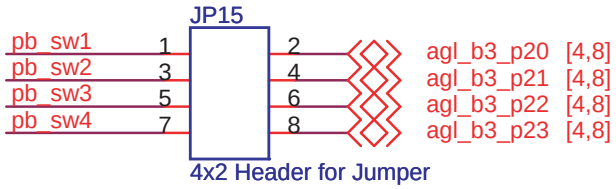


***Figure 3-6* • Jumper Header Schematic for Push-Button Switches**

DIP Switches

A DIP switch pack (8 switches) is provided on the board. You can remove the corresponding jumpers from the 8 x 2 header to detach any of the eight DIP Switches from the FPGA I/O.

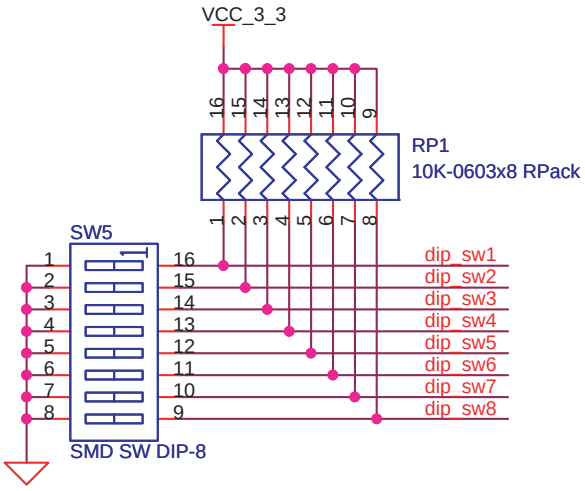


***Figure 3-7* • DIP Switches Schematic**

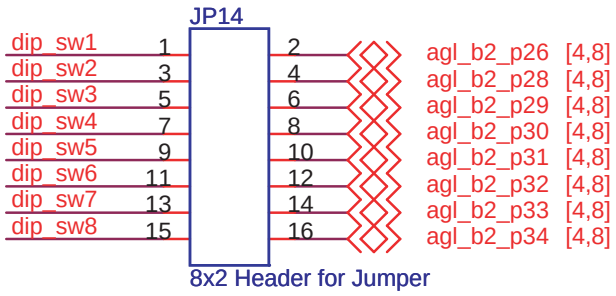


***Figure 3-8* • Jumper Header Schematic for DIP Switches**

User LEDs

Eight active low debug LEDs are provided on the board. You can remove the corresponding jumpers from the 8 x 2 headers to detach any of the eight LEDs from the FPGA I/O.

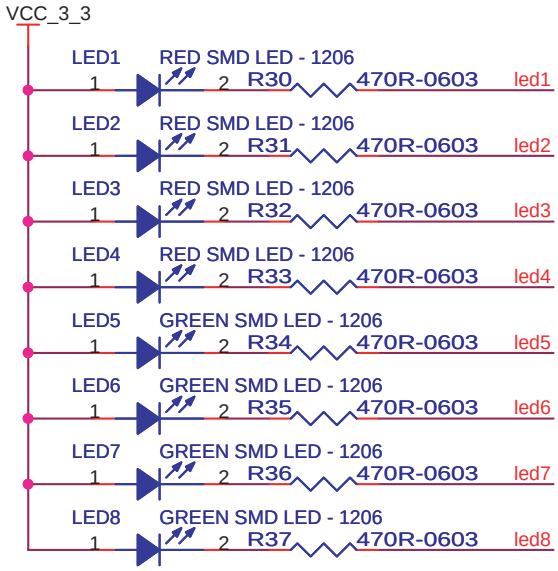


***Figure 3-9* • User LEDs Schematic**

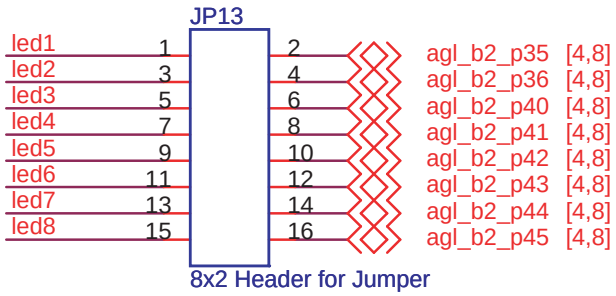


***Figure 3-10* • Jumper Header Schematic for User LEDs**

I/O Test Pins

All IGLOO nano FPGA I/Os are available on headers located on the top and bottom of the device. These headers are multiples of 100 mils apart, so you can easily place an extension card on top with an off-the-shelf bread board for a low-cost integration solution. Before you can use the I/Os assigned to the LEDs,

DIP switches, and push-button switches, you must first remove the corresponding 2-pin jumper on their path.

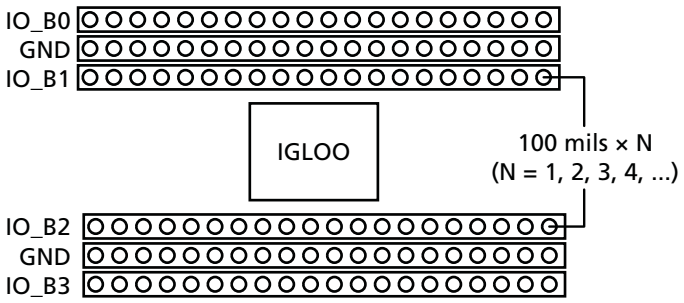


***Figure 3-11* • I/O Test Pins**

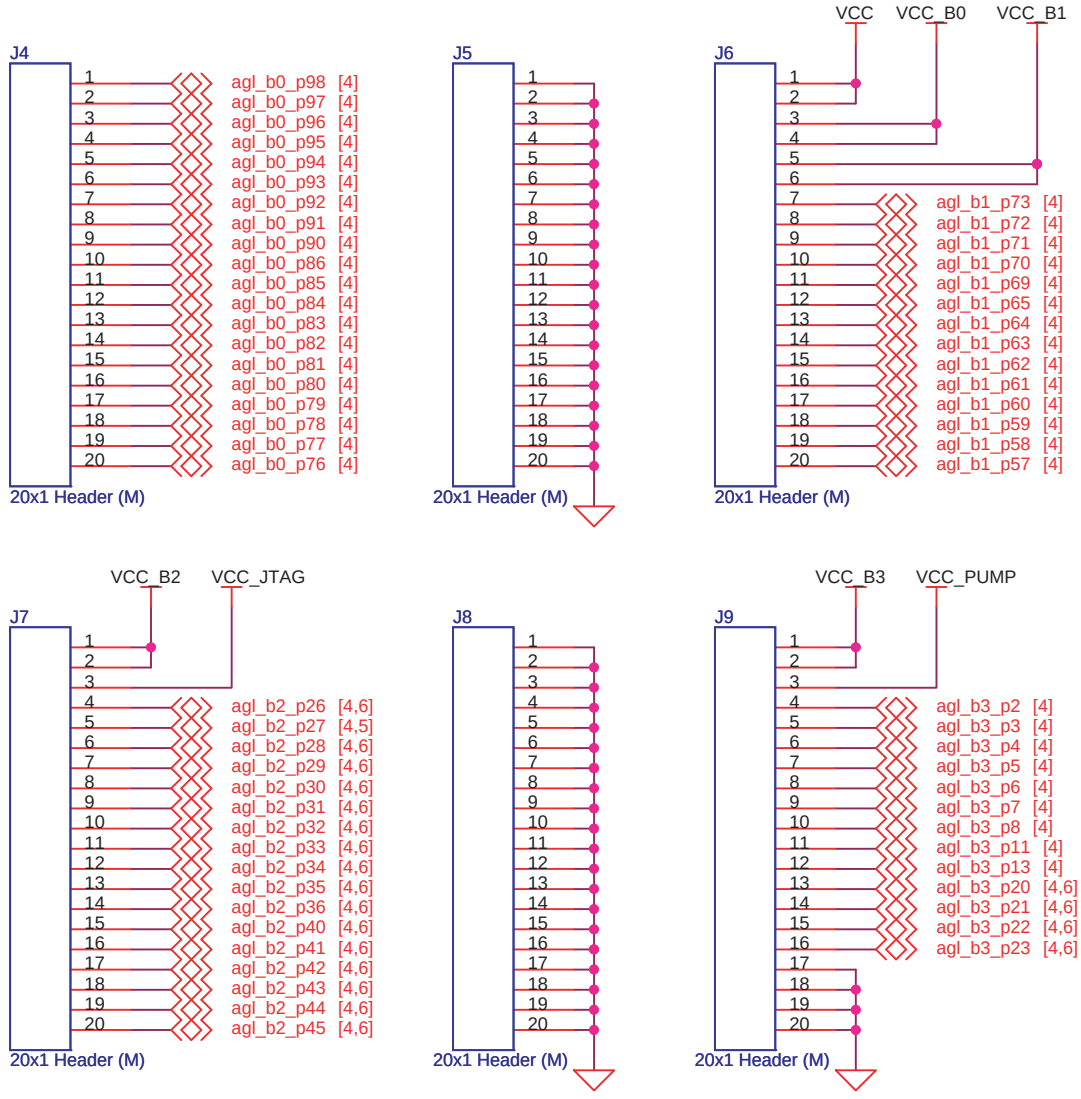


***Figure 3-12* • I/O Test Pins Schematic**

USB-to-UART Interface

Included on the starter kit board is a USB-to-UART interface with ESD protection. This interface includes an integrated USB-to-UART bridge controller (U8) to provide a standard UART connection with the IGLOO nano FPGA. Any standard UART controller can be implemented in the IGLOO nano FPGA to allow access with this interface. In addition, the Actel IP catalog includes various UART controllers, specifically CoreUART, which can be instantiated in the FPGA design with an embedded processor. CoreUART controller supports both asynchronous and synchronous modes with configurable parameters for various applications.

One application of the USB-to-UART interface is to allow HyperTerminal on a PC to communicate with the IGLOO nano FPGA. HyperTerminal is a serial communications application program that can be installed in the Windows operating system. A basic HyperTerminal program is usually distributed with Windows. With a USB driver properly installed and correct COM port and communication settings selected, you can use the HyperTerminal program to communicate with a design running in the IGLOO nano FPGA device.

Information on the USB-to-UART bridge datasheet and device drivers is available at the IGLOO nano Starter Kit website: http://www.actel.com/products/hardware/devkits_boards/igloonano_starter.aspx.

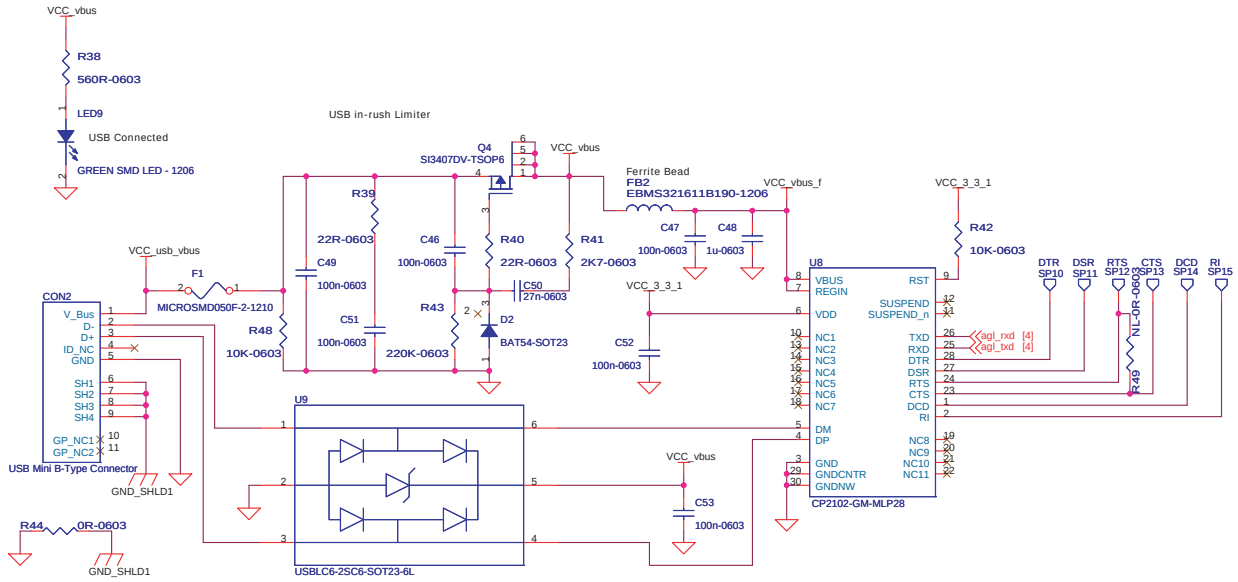


***Figure 3-13* • USB-to-UART Interface Schematic**

Low-Cost Programming Stick (LCPS)

Interface

The development board can be programmed by the low-cost programming stick or via a 10-pin FP3 header (Figure 3-14 on page 29). Regardless of the programming dongle used, IGLOO nano is programmed the same way as IGLOO PLUS, ProASIC3, and Fusion FPGA devices.

The LCPS is a special version for the FlashPro3 programming circuitry that is compatible with FlashPro3 and the generic FlashPro programming software. The LCPS, like the IGLOO nano board, is RoHS-compliant and is completely lead (Pb) free.

To use the LCPS with the FlashPro software, select FlashPro3 from the list of programmer types. The LCPS behaves exactly as if it were a regular encased FlashPro3 programmer. The LCPS shipped with this Starter Kit is designed for use with the IGLOO nano board and is not supplied as a separately orderable item from Actel Corporation. The 12-pin female connector socket is designed to interface with the 12-pin right-angle male header on the IGLOO nano kit. One of the pins is a special VJTAGENB signal that goes high when programming is taking place and returns to a low level when programming has completed. The IGLOO nano board uses this signal to effect a change in the value of VCC from 1.2 V to 1.5 V, which is required for programming all IGLOO nano devices.

You do not need to have the LCPS connected to the IGLOO nano board to operate it once the FPGA has been programmed. The Actel IGLOO nano board only needs the LCPS connected when programming the IGLOO AGLN250V2-VQG100.

Note: The LCPS supplied with this kit is intended for use with the IGLOO nano Starter Kit. An LCPS supplied for another kit, although electrically and functionally equivalent, may not connect seamlessly with the IGLOO nano Starter Kit board.

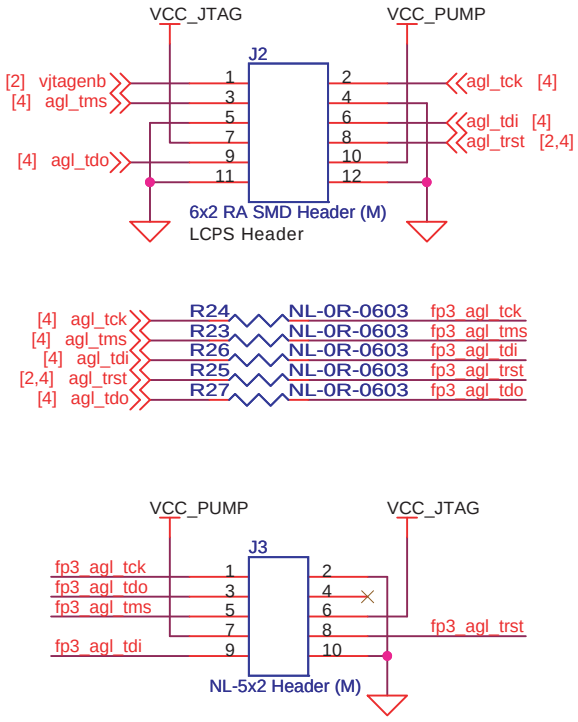


***Figure 3-14* • FPGA Programming Headers Schematic**

4 – Programming

To program a design into the IGLOO nano evaluation board:

1. Attach the LCPS board to the IGLOO nano evaluation board.
2. Attach a USB cable to the LCPS. This allows a programming data file, in programming database format (*.pdb) or STAPL format (*.stp), to be downloaded via the FlashPro software to the Actel IGLOO nano device fitted to the board.
3. A separate USB connection is required for the IGLOO nano Board if no other power source is attached to the IGLOO nano Board.
4. When using the FlashPro software, select the FlashPro3 programmer. The LCPS is functionally equivalent to a FlashPro programmer but designed specifically for use with the IGLOO nano kit.

5 – Board Demonstration

The IGLOO nano FPGA is pre-programmed with a simple demo to quickly get you started. This demo design will help give a quick overview as well as a quick check of this board. You can easily use this demo as a guide to create your own design for evaluation.

The demo design RTL code and design files are available at the IGLOO nano Starter Kit website:

http://www.actel.com/products/hardware/devkits_boards/igloonano_starter.aspx

Powering Up the Board and Running the Demo

1. Check and put the board in its default setting.
2. Plug the USB cable into a powered USB hub or a powered PC.
3. Plug the USB cable into the board to power it up.

   The board is powered from the USB connection and no external supply is required.

   A 5 V wall-jack connector is only provided on the board as an alternative if USB power is not available.
4. On power-up there should not be any activity on the LED (reset condition).
5. Refer to the table below for LEDs, push-button switch, and DIP switch functions:

***Table 5-1* • Demo Settings**

LED	Push Button Switch	Dip Switch
All 8 LEDs blinking	SW4 (User PB 1)	Don't Care
Right Shift (LED1 to LED8)	SW5 (User PB 2)	Don't Care
Left Shift (LED8 to LED1)	SW6 (User PB 3)	Don't Care
Toggles on respective DIP switch action (for example, LED1 toggles on DIP switch SW3.1 status)	SW7 (User PB 4)	DIP Switches are connected to respective LEDs
All 8 LEDs will be off	SW1 (Reset PB)	Don't Care

A – Resources

IGLOO nano Starter Kit
http://www.actel.com/products/hardware/devkits_boards/igloonano_starter.aspx

IGLOO nano Overview
http://www.actel.com/products/igloonano/default.aspx

IGLOO nano Datasheet
http://www.actel.com/documents/IGLOO_nano_DS.pdf

IGLOO nano FPGA Fabric User's Guide
http://www.actel.com/documents/IGLOO_nano_UG.pdf

Libero IDE Design Software
http://www.actel.com/products/software/libero/default.aspx

B – List Of Changes

The following table lists critical changes that were made in each revision of the chapter.

Date	Changes	Page
Revision 2 (September 2010)	The AGLN250-ZVQG100 part was replaced with AGLN250V2-VQG100 throughout the document. References to nano-Z parts were removed (SAR 27593).	5, 13, others
	The "FPGA Description: AGLN250V2-VQG100" section was revised to change "PLLs" to "integrated PLLs." The FlashROM bits value in Table 1-2 • Features of AGLN250V2-VQG100 was changed from 1,000 to 1,024 (SAR 27593).	13
	The following figures were replaced (SAR 27593): Figure 1-4 • AGLN250V2-VQG100 Banks 0–3 Schematic Figure 1-5 • AGLN250V2-VQG100 JTAG Pins Figure 1-6 • AGLN250V2-VQG100 Power and GND pins	14, 15
	The "Reset" section was revised to remove text applicable to nano-Z devices and state that the Schmitt trigger device can be bypassed because an AGLN250 FPGA supports additional I/O advanced features such as Schmitt trigger. A similar revision was made to the "Flash*Freeze Switch" section (SAR 27593).	22, 23
	The "LCPS Stackup" section was deleted.	N/A

C – Product Support

Actel backs its products with various support services including Customer Service, a Customer Technical Support Center, a web site, an FTP site, electronic mail, and worldwide sales offices. This appendix contains information about contacting Actel and using these support services.

Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

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From Southeast and Southwest U.S.A., call **650. 318.4480**
From South Central U.S.A., call **650.318.4434**
From Northwest U.S.A., call **650.318.4434**
From Canada, call **650.318.4480**
From Europe, call **650.318.4252** or **+44 (0) 1276 401 500**
From Japan, call **650.318.4743**
From the rest of the world, call **650.318.4743**
Fax, from anywhere in the world **650.318.8044**

Actel Customer Technical Support Center

Actel staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions. The Customer Technical Support Center spends a great deal of time creating application notes and answers to FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

Actel Technical Support

Visit the Actel Customer Support website (www.actel.com/support/search/default.aspx) for more information and support. Many answers available on the searchable web resource include diagrams, illustrations, and links to other resources on the Actel web site.

Website

You can browse a variety of technical and non-technical information on Actel's home page, at www.actel.com.

Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center from 7:00 a.m. to 6:00 p.m., Pacific Time, Monday through Friday. Several ways of contacting the Center follow:

Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is tech@actel.com.

Phone

Our Technical Support Center answers all calls. The center retrieves information, such as your name, company name, phone number and your question, and then issues a case number. The Center then forwards the information to a queue where the first available application engineer receives the data and returns your call. The phone hours are from 7:00 a.m. to 6:00 p.m., Pacific Time, Monday through Friday. The Technical Support numbers are:

650.318.4460
800.262.1060

Customers needing assistance outside the US time zones can either contact technical support via email (tech@actel.com) or contact a local sales office. Sales office listings can be found on the website at www.actel.com/company/contact/default.aspx.

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