AN 11.2

Current Measurements and Measurement Procedures for the LAN91C111 and LAN91C111 Evaluation Board

1 Purpose

This application note provides measurements of the current (ICC) consumed by the LAN91C111 as a stand-alone device, as well as the measurement of the current consumed by the LAN91C111 Evaluation Board. This application note also details the procedures for measuring these currents.

The ICC current consumed by LAN91C111 as a stand-alone device includes all of the digital and analog current consumed by both the MAC and PHY blocks inside the LAN91C111. Measuring this current requires measuring the total current flowing into all of the Vdd and Avdd pins of the LAN91C111. This current does not include the current consumed by the termination resistors for the Ethernet transmit and receive circuits.

The current consumed by the LAN91C111 Evaluation Board includes the current consumed by the LAN91C111 as a stand-alone device plus the supply current consumed by the passive components used in the analog front end. These passive components consist of magnetics, resistors on the Ethernet transmit circuit.

Current consumption of the LAN91C111 varies according to which state it is in. These states include the idle state, three power-down states and normal operation.

2 Measurement Details and Procedures

2.1 Set-up Used

PCB:	PartNumber PCB Assembly No 6173 Rev.B. (S/N#112) configured to schematic B1
Magnetics:	Halo TG110-S050N2 Magnetics
Passive Components:	R1, R2, R5, R6 = 24.9Ω; R3, R4 = 49.9Ω; C1 = 0.01uf;
Supply Voltage:	3.30 V;
Temperature:	Ambient (25°C)
Device:	PartNumber-NE
Date Code:	B0222-B847
Lot Code:	8G111758

2.2 Location of VDD and AVDD Pins

For the LAN91C111 TQFP package, the Vdd and AVdd pins are located as follows: Pin #1, #11, #16, #33, #44, #62, #77, #98, #110, #120.

For the LAN91C111 QFP package, the Vdd and AVdd pins are located as follows: Pin #3, #13, #18, #35, #46, #64, #79, #100, #112, #122.

All of the measurements made for this application note were made using the TQFP package.

2.3 Measurement Procedure

2.3.1 LAN91C111 Initialization Steps

Upon power-up, LAN91C111 defaults in a not complete working status. The PHY portion is in isolate mode as the MII bus disabled. The transmitter and receiver of the EPH block of the MAC portion are both not enabled. In order to set LAN91C111 in normal working status and establishing a link, all blocks of the device must be properly powered on and initialized.

A power up Auto-Negotiation enable initialization sequence is provided below for reference:

1. Power up the device; Wait for 50ms.
2. Reset the device by setting and clearing the SOFT_RST bit in the Receive Control Register (MAC Register, Bank 0 Offset 4); Write 0x8000, then write 0x0000; Wait for 50ms.
3. Set the ANEG bit to 1 in the Receive/PHY Control Register (MAC Register, Bank 0, Offset A) to enable the Auto_Negotiation mode.
4. Reset PHY by set the RST bit of PHY Register 0 (0x8000); wait for 50ms.
5. Turn off the isolation mode of the internal PHY by writing x1000 to the PHY Register 0 – Control Register. The PHY will start the Auto_Negotiation Process.
6. The PHY needs at least 1.5 second to complete the Auto_Negotiation process.
7. Read the ANEG_ACK bit and the LINK bit in the PHY Register 1 – Status Register to check whether the Auto_Negotiation Process is completed and Link is established.

Once the initialization completed, the link should be established between the local device and the remote partner node connected.

2.3.2 Procedure for Setting Idle State without Cable Connected

This idle state defined in this document is a test condition of LAN91C111 after power up initialization, and the link established, then disconnecting the connecting cable for the current measurement.

2.3.3 Procedure for Setting EPH (MAC) Power Down Mode:

1. Disable Transmitter – Clear the TXENA bit of the Transmit Control Register;
2. Remove and release all TX completion packet numbers on the TX completion FIFO;
3. Disable Receiver – Clear the RXEN bit of the Receive Control Register;
4. Remove and Release all Received packets;
5. Clear the Interrupt Status Register;
6. Write and set “0” to the “EPH Power EN” Bit located in the Configuration Register (MAC Register Bank 1 Offset 0) to set EPH (MAC) in power down mode.

2.3.4 Procedure for Setting PHY Power Down Mode:

1. Disable Transmitter – Clear the TXENA bit of the Transmit Control Register;
2. Remove and release all TX completion packet numbers on the TX completion FIFO;
3. Disable Receiver – Clear the RXEN bit of the Receive Control Register;
4. Remove and Release all Received packets;
5. Clear the Interrupt Status Register;
6. Set PDN bit in PHY MI Register 0 to “1” to set internal PHY entered in power down mode.

2.3.5 Procedure for Setting Both EPH (MAC) and PHY in Power Down Mode:

1. Disable Transmitter – Clear the TXENA bit of the Transmit Control Register;
2. Remove and release all TX completion packet numbers on the TX completion FIFO;
3. Disable Receiver – Clear the RXEN bit of the Receive Control Register;
4. Remove and Release all Received packets;
5. Clear the Interrupt Status Register;
6. Set PDN bit in PHY MI Register 0 to 1 to set internal PHY entered in power down mode;
7. Write and set “0” to the “EPH Power EN” Bit located in the Configuration Register (MAC Register, Bank 1 Offset 0) to set EPH (MAC) in power down mode.

2.3.6 Restoring Back in Normal Operation from Power Down Mode:

1. Write and set “1” to the “EPH Power EN” Bit of the Configuration Register, Bank 1 Offset 0;
2. Be sure the ANEG bit of RPCR Register is set already;
3. Clearing PDN bit of the PHY register 0 to 0x1000 from 0x1800, this will set the PHY in the isolation mode (0x1400);
4. Set one more time with 0x1000 to clear the MII_DIS bit to clear the isolation mode. Wait for at least 1500 ms for the PHY resuming back to normal operation;
5. Issue MMU Reset Command;
6. Enable Transmitter of EPH block – Set the TXENA bit of the Transmit Control Register;
7. Enable Receiver of EPH block– Set the RXEN bit of the Receive Control Register.

3 Measurement Results

3.1 LAN91C111 Stand-Alone Measurements

3.1.1 Currents Measured Under Normal Operation Modes:

a. Typical currents measured under Normal Operation Modes:

NORMAL OPERATION MODE	VOLTAGE (V)	TYPICAL CURRENT (MA)
Idle (No cable connected)	3.3	111
100MB	3.3	113
10MB	3.3	82

b. Typical current measured in Tx mode under different % wire utilization:

NORMAL OPERATION MODE	VOLTAGE	CURRENT (MA) UNDER 25 % WIRE UTILIZATION	CURRENT (MA) UNDER 50% WIRE UTILIZATION	CURRENT (MA) UNDER 75% WIRE UTILIZATION	CURRENT (MA) UNDER 100% WIRE UTILIZATION
100MB Full Duplex	3.3	113	115	116	116
100MB Half Duplex	3.3	113	115	116	116
10MB Full Duplex	3.3	84	84	84	85
10MB Half Duplex	3.3	84	84	84	85

3.1.2 Typical Currents Measured for Different Power Down Modes:

FUNCTION	VOLTAGE (V)	TYPICAL CURRENT (MA)
EPH (MAC) in power down mode (PHY is enabled)	3.3 volts	105
PHY in power down mode (MAC is enabled)	3.3 volts	15
Both EPH (MAC) and PHY in power down mode	3.3 volts	14

3.2 LAN91C111 Evaluation Board Measurements

3.2.1 Total Supply Currents Measured for the Whole EVB Board:

NORMAL OPERATION MODE	VOLTAGE (V)	TYPICAL CURRENT (MA)
Idle (No cable connected)	3.3	212
100MB	3.3	176
10MB	3.3	209

3.2.2 Typical Currents Measured for the Front End Circuit of the EVB Board:

This includes the current consumed by the R3 and R4 resistors on the transmit circuit, and the R1 / R5, R2 /R6 resistors and C1 on the receive circuit, as well as any current consumed by the magnetics and its related circuitry components.

NORMAL OPERATION MODE	VOLTAGE (V)	TYPICAL CURRENT (MA)
Idle (No cable connected)	3.3	100
100MB	3.3	52
10MB	3.3	110

4 Revision History

NAME	REVISION LEVEL AND DATE	SECTION/FIGURE/ENTRY	CORRECTION
Marcom	Rev. 1.0 (1-28-09)		Standard SMSC Formatting

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